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Impacts of Cooling Technology on Solder Fatigue for Power Modules in Electric Traction Drive Vehicles

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Impacts of Cooling Technology on Solder Fatigue for Power Modules in Electric Traction Drive Vehicles

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Abstract—This paper presents three power module cooling topologies that are being considered for use in electric traction drive vehicles such as a hybrid electric, plug-in hybrid electric, or electric vehicle. The impact on the fatigue life of solder joints for each cooling option is investigated along with the thermal performance. Considering solder joint reliability and thermal performance, topologies using indirect jet impingement look attractive.

Keywords-power electronics; reliability; jet impingement; solder joint fatigue

I. INTRODUCTION

Power electronics are a key component of the electric traction drives being used and proposed for hybrid electric vehicles, plug-in hybrid electric vehicles, fuel cell electric vehicles, and pure electric vehicles. These vehicle technologies could play a key role in the reduction of vehicle emissions, reduction in the transportation sector's contribution to global warming, and enhancement of energy security due to reduced dependence on imported petroleum for transportation.

In order to increase the market share of advanced electric traction drive vehicles, component costs must come down while acceptable volume, weight, and life are maintained. The U.S. Department of Energy is collaborating with the U.S. automotive industry under the FreedomCAR and Fuel Partnership to develop component technologies that overcome the market barriers to advanced vehicle deployment. This paper focuses on the power electronics (specifically, the power inverter) for advanced electric traction drive vehicles. Further details of the R&D program can be found in [1].

Thermal management and reliability at high temperature and under thermal cycling are major barriers for advanced automotive power electronics (see, for example, [2-4]). The electrical devices in the power inverter can experience immediate overstress failures at high temperatures. Furthermore, device reliability degrades as a result of fatigue mechanisms at higher temperatures and/or with higher magnitude or frequency of thermal cycling. Despite these challenges, the engineering community is pushing the limits of power electronics ever further. Improvements in thermal design have enabled further advances in power modules, allowing industry to meet increasingly stringent cost, weight, volume, and life targets (see, for example, [5]). This is not enough, however, as good thermal designs must also be reliable.

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Furthermore, it is increasingly important to evaluate reliability as we push the envelope into smaller, higher powered, and higher temperature systems.

This paper presents a simulation study that begins to combine thermal performance with reliability prediction. In our study, the reliability of solder joints for three different cooling topologies is compared. The cooling topologies consist of two advanced options using jet impingement cooling and a baseline option using pin-fin liquid cooling. Several major failure modes can be seen in automotive power modules. In this study, we will limit ourselves to predicting the number of temperature cycles until the onset of solder joint cracking. Delamination due to failure of the solder joint is one of the main failure modes for automotive power inverters (see, for example, [6]).

The paper begins with a literature review followed by an introduction to the model used and the simulation setup. Following that, thermal performance and reliability results are presented. Finally, concluding remarks and next steps are given.

II. REVIEW OF PRIOR WORK

There are numerous studies on solder joint reliability in the context of electronics packaging (see, for example, [7-11]). Analytical models have been proposed to estimate the thermally induced (elastic) stresses due to differences in coefficients of thermal expansion between adjacent layers in multilayered bonded materials (see, for example, [12-13]). In these studies, both experimental and analytical evidence indicates that stresses in "soft" lead-based soldered joints are highest at the edges, and cracks will tend to propagate from the edge. This is not true for "hard" solders such as 80Au/20Sn or 95Sn/5Ag (see [11]). Furthermore, the literature indicates that the joint between the substrate and the heat sink is typically the weakest (see, in particular, [14]).

In [15-16], the authors discuss power cycling procedures for both wire bond and solder joint fatigue. We use this solder joint power cycling procedure in our simulation as opposed to thermal shock procedures and/or temperature cycling procedures in which temperatures are induced via the ambient environment. Power cycling involves heating by means of the power semiconductors embedded in the inverter system under test.

Reference [4] presents a recent overview of the reliability challenges of advanced power modules for hybrid electric vehicles. The authors discuss the trend toward increased power density of next-generation power modules as well as industry's interest in operating power modules over a common coolant loop that includes the internal combustion engine (for hybrid electric vehicles). This would result in coolant temperatures up to 110°C. This is similar to the coolant target of 105°C used by the FreedomCAR and Fuel Partnership Electrical and Electronics Technical Team for the same reasons [1]. The relevant stressors on an automotive inverter are discussed, along with an overview of recent results of an analysis of wire bond cycles to failure and solder joint crack propagation due to stress/strain hysteresis. A reliability test with a temperature rise of 90°C using a 95°C coolant was briefly presented in which a mild-hybrid inverter (with output power of 8 kW) was shown to fail by wire-bond failure at 40,000 cycles.

In [17], the authors present three avenues for improving the power density of power inverters for automotive applications: better cooling, devices and packages that tolerate higher temperatures, and reduction of losses at the chip. Interconnection reliability in high-temperature-tolerant inverter packages is cited as a major requirement for the realization of inverters that tolerate higher temperatures. The failure mechanisms behind solder cracking and wire-bond lift-off are reviewed, as well as which accelerated tests correspond to which mechanisms: thermal shock tests and temperature cycling tests are commonly used for solder joint reliability, while power cycling is commonly used to determine wire-bond fatigue failure. Data for percentage delamination by number of temperature cycles are presented; unfortunately, the testing conditions are not stated.

III. SIMULATION SETUP

In this study, three topologies for a hybrid inverter are compared with each other on the basis of their heat transfer performance and the reliability of their soldered interconnects. The three topologies include a baseline system that uses a liquid-cooled pin-fin heat sink and two advanced concepts that use jet impingement cooling. The two jet impingement concepts are of interest because they have similar thermal performance but potentially very different reliability implications that reflect their different designs. In the following sections, the geometry, material properties, boundary conditions, and loading of the models will be discussed.

We used SolidWorksTM and Pro/ENGINEERTM to build the geometries and ANSYSTM version 11 to predict steady-state temperature, thermally induced stress, and solder fatigue failure results. The fatigue analysis required the ANSYSTM Fatigue Module.

A. Geometries and Material Properties

The models used in this analysis represent a small section of a larger inverter. Specifically, we modeled a single insulated gate bipolar transistor (IGBT) and diode pair. Our model is loosely based on the power semiconductor layout and sizes of the model year 2004 Toyota Prius, as shown in Fig. 1. In the photo, the gate drivers and housing have been removed to show the power semiconductors. The Prius inverter drives two electric machines: a traction motor and a generator. The yellow dashed line in Fig. 1 encircles the part of the inverter that drives the traction motor, and it is the focus of this study. More details on the Prius inverter and motor technology can be obtained from [18]. The IGBT and diode pair in our models loosely correspond to the inset of Fig. 1. Note that we are not modeling wire bonds for this study.

Three geometries are being used in our study. The first, topology 1, a baseline system, is shown in Fig. 2. The left side of the figure shows a top view, and the right side depicts the package topology from the bottom and highlights the pin-fin array design. The pin-fins have an elliptical shape. From top to bottom, the layers of this geometry are power semiconductors (one IGBT and one diode—the IGBT is the larger device) modeled with the temperature-dependent material properties of silicon, 63Sn-37Pb solder, an aluminum nitride (AIN) substrate metallized on the top and bottom with copper (this layer is called the *DBC* or *direct bond copper* layer), 63Sn-37Pb solder, an aluminum baseplate, a layer of thermal grease, and the aluminum pin-fin heat sink.

The layer thicknesses are depicted in Fig. 3. Note that pinfins are not depicted in this figure. The graph is annotated with the layers that correspond to each topology.

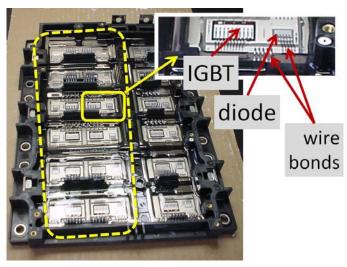


Figure 1. Example HEV Inverter (MY2004 Prius)

Topologies 2 and 3 share the same top section as topology 1 from the power semiconductors to the substrate. In topology 2, instead of having a thermal interface material and pin-fin heat exchanger, a coolant jet impinges upon the baseplate. This is depicted in Fig. 4. The dashed line in the figure indicates two jets—each jet is located directly below a power semiconductor.

Topology 3 goes one step further by removing the base plate and directly impinging upon the metalized bottom of the DBC substrate. Topology 3 is depicted graphically in Fig. 5.

The dimensions of the power semiconductors and DBC are given in Fig. 6. Further exploration of the heat transfer for these package geometries is given in [19]. The temperaturedependent properties of the materials used in this study were obtained from [20]. Temperature-dependent properties were used because of the large change in some properties across the temperature range of thermal cycling. For example, the thermal conductivity of silicon varies from over 170 W/m-K at -40°C to under 100 W/m-K at 150°C; this temperature range is commonly considered in the testing of components for automotive applications. Fatigue properties of the solder (presented later) were estimated using [21].

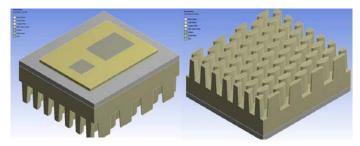


Figure 2. Topology 1: Baseline Package with Pin-Fin Cooling

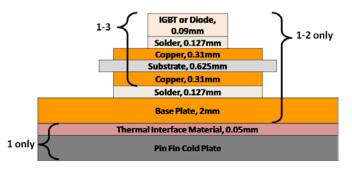


Figure 3. Layer Thicknesses and Materials in Package Topologies Modeled

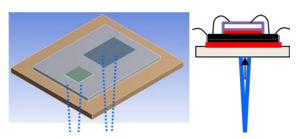


Figure 4. Topology 2: Indirect Jet Impingement on Base-Plate

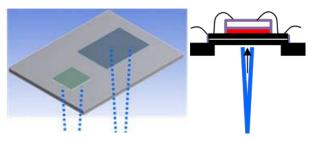


Figure 5. Topology 3: Indirect Jet Impingement on DBC Substrate

B. Heat Transfer Boundary Conditions

It is important to correctly predict the temperature distribution since the thermally induced stresses and fatigue analyses require it. Two heat transfer boundary conditions are relevant to the topologies examined in this study: pin-fin convective cooling and jet impingement cooling. Both boundary conditions are discussed below. The coolant used in this study is 50/50 by mass of water and ethylene glycol, and the fluid properties are obtained from [22]. The coolant inlet temperature is assumed to be 105°C during periods of maximum heat generation.

The pin-fin heat exchanger used in topology 1 contains pins spaced 5.08 mm apart in the transverse direction (perpendicular to the flow) and 10.16 mm apart streamwise. The pins are 7.62 mm tall and taper from top to bottom; they are 2.8 mm x 6 mm at the top and 2 mm x 5.2 mm at the bottom, and the dimensions are ellipse minor and major diameters, respectively. A total of 5 liters per minute of coolant flows through the section of the array pictured in Fig. 2 (a parallel section carries an additional 5 liters per minute for a total flow of 10 liters per minute through the inverter). Note that the actual Prius inverter uses straight fins instead of pin-fins, though pin-fin heat exchangers have appeared in other automotive inverters. The portion of the heat sink above the pins is 6.35 mm thick.

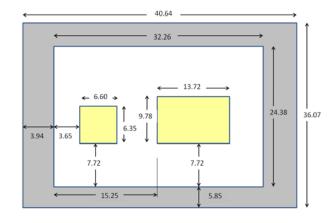


Figure 6. Dimensions of Package Topologies (mm)

Empirical relations for pin-fins from [23] were used in conjunction with CFD analysis to predict the area-averaged local heat transfer coefficient across the pin-fin surface. Fin efficiency is taken into account directly by explicitly modeling the pin-fins.

For jet impingement, the relation from [24] was used. This relation breaks the jet heat transfer coefficient into an impingement zone and a wall-jet region. For this analysis, we assume that there is no interference between adjacent jets. The heat transfer coefficients applied to the various model boundaries are summarized in Table 1. We applied an area-averaged heat transfer coefficient directly below each power semiconductor on the baseplate; this heat transfer coefficient consists of an area average of impingement zone and wall jet zone directly under each chip. The remainder of the DBC is assumed to be in the wall jet region.

The jet nozzle diameter is assumed to be approximately 1.4 mm based on a simple calculation of 1 jet per 1 power semiconductor and a total of 24 power semiconductors (i.e., a total of 12 IGBTs and 12 diodes) at a total flow rate of 10 liters per minute and target nozzle velocity of 4.5 m/s per jet.

TABLE 1. HEAT TRANSFER COEFFICIENTS USED IN SIMULATION

Location	Heat Transfer Coefficient (W/m ² .K)
Pin surface	10,437
Surface between pins	1,191
Jet impingement diode	31,534
Jet impingement igbt	20,426
Wall jet zone (under DBC ^a)	15,382
Outside the wall jet zone	1,191
a. Direct bond copper layer.	

C. Loading Conditions

A simple relationship was used to estimate the heat generation due to losses in the IGBT and diode pair. This estimate corresponds to an electric traction drive system of 55 kW, per the FreedomCar and Fuel Partnership targets [1]. A peak efficiency of ~98% was assumed for the inverter and 94% for the motor drive. Using the Prius geometry, 12 pairs of devices were assumed (i.e., 12 IGBTs and 12 diodes for a total of 24 devices or 12 pairs of devices). This results in a heat loss per IGBT and diode pair of approximately 120 W. Approximately 70% of the heat was apportioned to the IGBT and 30% to the diode, based on a rough estimate of the heat breakdown between components. This results in a heat loss per diode of 35 W and heat loss per IGBT of 85 W.

D. Structural Support

Structurally, the three topologies are assumed to be floating in space with "weak springs" as structural boundary conditions. This technique was chosen to avoid mounting-specific complexity.

E. Failure Models and Physics

Although there are several failure modes of concern for power inverters in automotive applications (see, for example, [6]), this study is focused only on solder joint fatigue due to temperature cycling. Solder joint delamination is one of the main failure modes in power inverters (see, for example, [25]). As reported in the literature, temperature cycling and thermal shock tests tend to directly stress solder joints and elicit failures. These tests are conducted in environmental chambers where the system under test is subjected to extreme changes in external temperature from ambient or even -40°C to 140°C or greater (see, for example, [26]).

Based on the discussion in [15], we are simulating a power cycling test in which the devices in the inverter create the heat necessary to raise the inverter temperatures, after which the entire inverter is allowed to cool back to ambient conditions (assumed to be 22°C). The end effect is similar to those of the temperature cycling tests discussed above, but more realistic since the temperature distribution corresponds to that of an active inverter. Note that this is different from power cycling tests conducted to elicit wire-bond fatigue failures.

In power cycling for wire-bonds, the package is never allowed to cool back to ambient conditions, and the power semiconductors are cycled on and off at a higher frequency. In contrast, the power cycling method to elicit solder joint fatigue has much higher temperature rises, which bring the inverter to a high temperature and then back to ambient, but at a much lower frequency than power cycling for wire-bond fatigue. We currently do not take viscoplastic or other dynamic effects such as creep into account with our model. Instead, our model calculates the effect of going from a stress-free state to the thermally induced stress state associated with the steady-state temperature field obtained by applying the heat loading condition. One power cycle is depicted in Fig. 7.

The solder joints can experience both elastic and plastic deformation during high temperature excursions. The model we use to account for the elastic and plastic strain conditions is called the strain-life relationship:

$$\frac{\Delta\epsilon}{2} = \frac{\sigma'_f}{E} \cdot \left(2 \cdot N_f\right)^b + \epsilon'_f \cdot \left(2 \cdot N_f\right)^c.$$
(1)

In (1), $\Delta \epsilon$ is the change in strain due to the application of our loading condition. The factor of 2 occurs because (1) is derived under the assumption of completely reversed loading i.e., a load is fully applied in one direction and then applied at the same magnitude in the opposite direction. Thus, the total change in strain for the application of a load in one direction is half the total. N_f is the number of cycles to failure (the parameter of interest). *E* is the modulus of elasticity.

The remaining four terms are fatigue strength coefficient, σ'_f , fatigue strength exponent, *b*, fatigue ductility coefficient, ϵ'_f , and fatigue ductility exponent, *c*. The first term of (1) accounts for cycles to failure under elastic deformation, while the second term accounts for cycles to failure under plastic deformations. An in-depth derivation and discussion of this relationship and the parameters that are used can be found in [27] and Chapter 2 of [21]. A discussion of the engineering behind the ANSYS fatigue module that implements the strain-life model can be found in [28].

The fatigue properties of the solder corresponding to the strain-life model from (1) are given in Table 2. These properties were estimated using material properties from [20] and guidelines from [21]. Four empirical properties are needed to use (1): σ'_f , b, ϵ'_f , and c. Two additional properties, called cyclic strength coefficient, K', and cyclic strain hardening coefficient, n', are reported as well. These can be derived by curve fitting experimental data (see [21]), and they relate to the other parameters as follows [21]:

$$K' = \frac{\sigma'_f}{\left(\epsilon'_f\right)^{n'}} \tag{2}$$

$$n' = \frac{b}{c}.$$
 (3)

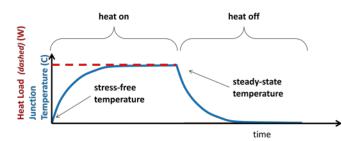


Figure 7. Equivalent Power Cycle Test

TABLE 2. FATIGUE PROPERTIES OF 63S	N-37PB SOLDER
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Fatigue Property	Value
Fatigue strength coefficient (MPa), σ'_f	93.3
Fatigue strength exponent, b	-0.085
Fatigue ductility coefficient (MPa), ϵ'_f	1.0 x 10 ⁻⁶
Fatigue ductility exponent, c	-0.6
Cyclic strength coefficient (MPa), K'	93.3
Cyclic strain hardening exponent, n'	0.15

IV. RESULTS AND DISCUSSION

The results section is broken into two parts: thermal performance and solder joint fatigue failure prediction. The motivation behind topologies 2 and 3 is based on their thermal performance, but thermal performance alone is not sufficient. As new designs push the limits of materials and devices, the reliability must be considered as well. The section on fatigue prediction begins to address greater questions of concept feasibility in terms of meeting life requirements.

A. Thermal Results

The steady-state peak temperatures at the power semiconductors under the analysis conditions presented in the simulation setup section are given in Table 3. Fig. 8 depicts the temperature profile of topology 1 and shows the location of the maximum temperature to be on the IGBT. There is nearly a 25% drop in thermal resistance from junction to fluid between topology 1 and 2. Thermally, topology 2 and 3 are similar.

The three topologies are interesting from a thermal perspective as there is a complex relationship between heat transfer coefficient, package thermal resistance, and heat spreading. Jet impingement provides an increased heat transfer coefficient but lower surface area. The pin-fins of topology 1 have a large area for heat transfer, but must contend with fin efficiencies and a lower heat transfer coefficient at the pins. This results in a few interesting "cross-over" points, as shown in Fig. 9. The same results corrected for heat transfer coefficient multiplied by the area are shown in Fig. 10. These phenomena have been reported elsewhere (see [19, 29]).

Topology	Max. Temperature at IGBT (°C)	Max. Temperature at Diode (°C)	Package Thermal Resistance (°C/kW)	
Topology 1	136.1	123.3	279	
Topology 2	130.3	126.7	211	
Topology 3	129.8	117.7	206	

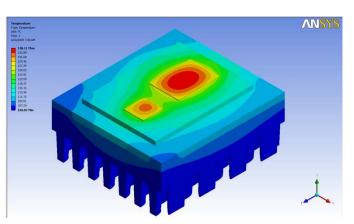


Figure 8. Temperature Distribution in Topology 1

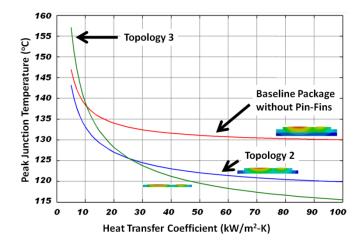


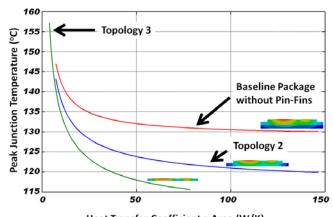
Figure 9. Thermal Performance by Heat Transfer Coefficient

B. Solder Joint Fatigue Prediction

Each topology is expected to dissipate the same amount of heat. However, the temperature rise for each topology is different on account of their different thermal performances (see Table 3). This is an important caveat since one may wish to use the enhanced thermal performance of topology 2 and 3 to dissipate more heat. One must use caution with this approach, since both topology 2 and 3 have less thermal mass than topology 1. Thus, the junction temperature of topology 2 and 3 would rise faster than topology 1 under fault conditions such as a loss of flow and/or short circuits. This matter requires further investigation.

As shown in Fig. 11, the analysis predicts that fatigue failure initiates from the edges, which is expected for lead-based solders, as discussed in the literature review.

The fatigue cycles to failure presented in Table 4 show a dramatic difference in fatigue life between the DBC solder joint and the other die attach joints. From the literature review, we expected the DBC solder joint to be the most susceptible to fatigue failure. This joint attaches the DBC to the base plate in topologies 1 and 2. Thus, we expected the model to predict the lowest number of cycles to failure for this joint based on test data from the literature (see, for example, [10]).



Heat Transfer Coefficient x Area (W/K) Figure 10. Thermal Performance by Heat Transfer Times Area

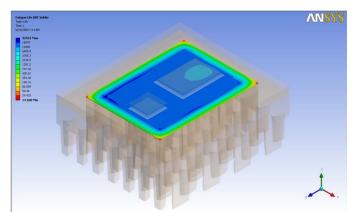


Figure 11. IGBT Solder Fatigue Life for Topology 1

TABLE 4. CYCLES TO FAILURE UNDER SIMULATED CONDITIONS

Topology	Cycles to Failure for DBC Solder	Cycles to Failure for IGBT Solder	Cycles to Failure for Diode Solder
Topology 1	17	26,261	31,032
Topology 2	163	18,031	23,558
Topology 3	NA	36,465	42,245

Based on the literature, the predicted number of cycles seems reasonable. Basaran and Chandaroy [30] state that "a few hundred cycles of -40° C to $+130^{\circ}$ C is typically enough to cause cracks and electrical failures." Our analysis technique predicts fatigue failure, which we interpret as the onset of a growing crack that will eventually lead to unacceptable delamination. As the solder delaminates, the thermal contact between the joined layers degrades, causing an increase in temperature. The device will eventually fail as a result of this excessive temperature and/or a loss of connection to the lower layer.

Reference [14] presents test results for solder joints subjected to thermal shock. Fig. 6 of [14] indicates the onset of a crack occurs in less than 50 cycles for a temperature delta of 180°C for experiments with lead and lead-free solders (the exact composition was not disclosed in the paper as it was considered proprietary). Since for this study we define failure as the onset of cracking, the number of cycles to failure should be lower. Similarly, Fig. 9 of [17] depicts the onset of delamination on the order of hundreds of cycles. Unfortunately, the temperature range and solder type are not reported in this paper, so we cannot draw stronger conclusions. Based on the limited data available, the predicted low number of cycles for DBC solder joint fatigue seems reasonable.

In terms of the die attach solders (i.e., the IGBT and diode solder joints), [15] presents information on power cycling to predict solder joint lifetimes at the die attach. The authors report a lifetime of 1.7×10^4 cycles for a 100°C temperature rise for the die attach solder. This is of similar magnitude to the predicted value of 2 to 2.5 x 10^4 for the topology 1 and 2 packages from Table 4.

In Table 4, the minimum number of cycles to failure is highlighted. Based on the analysis results under the conditions and scope of consideration for this study, we see that topology 3 offers a significantly higher cycle life due to the elimination of the weakest joint. However, more work is necessary before final conclusions can be drawn.

V. CONCLUSIONS AND NEXT STEPS

This paper presented the application of modern computeraided engineering tools to assess the thermal performance and reliability of three different power inverter topologies. Although the models have not been directly validated against experimental data, there appears to be good qualitative agreement between the numbers we predict and information in the literature, suggesting that our predicted results are reasonable. Based on the data available so far, topology 3 shows promise both from a reliability standpoint (by removing the weakest solder joint from the system) and from a thermal performance standpoint. This effort, however, is far from complete.

Future activities that could be incorporated into this effort include prediction of solder crack propagation with cycling, wire-bond flexural fatigue prediction, expanding the solder models to include viscoplastic effects such as creep, incorporating substrate reliability (brittle fracture), bringing more rigor and analysis to the structural loading boundary conditions, adding transient heat transfer effects such as fault conditions due to short circuit or loss of coolant, adding vibration loading conditions, adding jet impingement erosion studies, enhancing the thermal loading conditions similar to those in [31], and enhancing thermal-fluid models and associated predictions. To foster the analysis indicated by these future activities, dedicated testing for model validation is being pursued.

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