IEEE SCC21/P1547.1 Draft Standard Conformance Test Procedures for Equipment Interconnecting Distributed Energy Resources with Electric Power Systems and Associated Interfaces

P1547.1 Subgroup on Hardware-in-the-Loop (HIL) Testing

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- **Extended grid interactive features**
  - Constant power factor, Voltage – reactive power, Active power – reactive power, Constant reactive power
  - Voltage – active power, Frequency – Watt
  - Ride-through, Extended trip settings

- **Unintentional islanding**
  - 2 seconds (up to 5 by agreement)
  - Testing: still based on RLC-load bank but **PHIL as an option**
    - Focus on requirements, tests as written for load bank setup
  - RLC-based subgroup proposed sustained island test for validation
    - Disable UI function for initial test, RLC circuit tuning proven by >10s run-on
    - HIL subgroup using this approach for validating HIL setup but with PHIL RLC
- **Extended Installation-Commissioning-Periodic guidelines**
  - **CHIL: design evaluation (informative annex)**
    - Testing controllers that are not type-tested
- **Annex on HIL**
  - Terminology, setup examples, additional UI-requirements information

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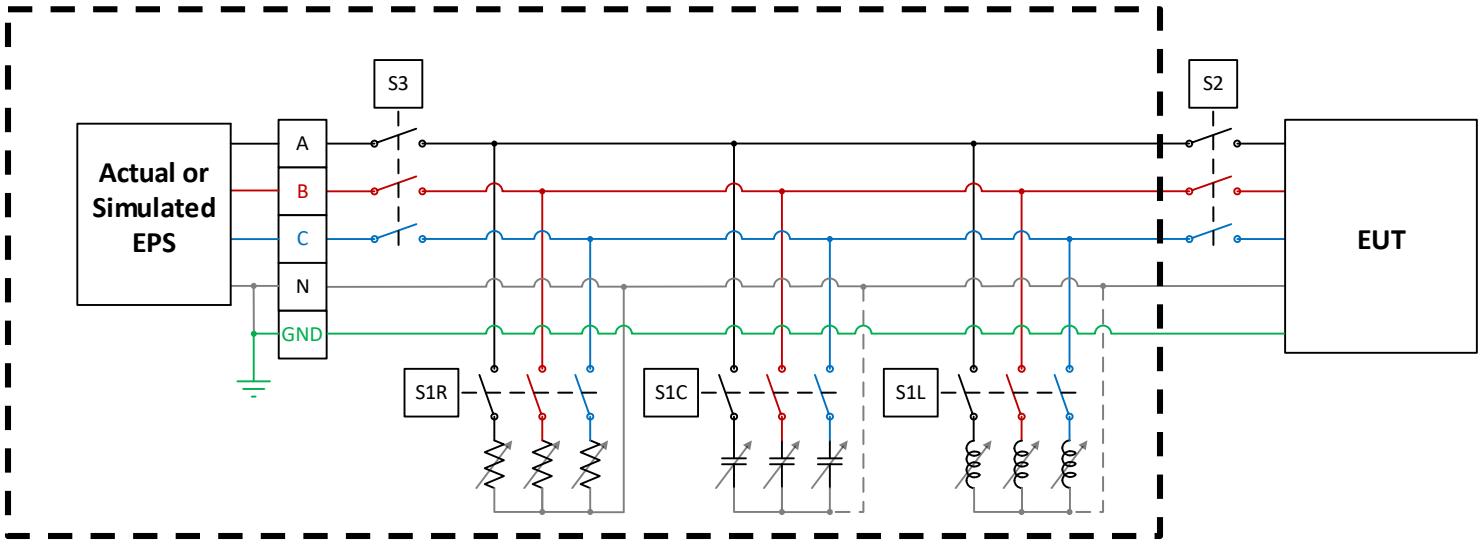
Hardware-in-the-Loop (HIL) Testing

Unintentional islanding

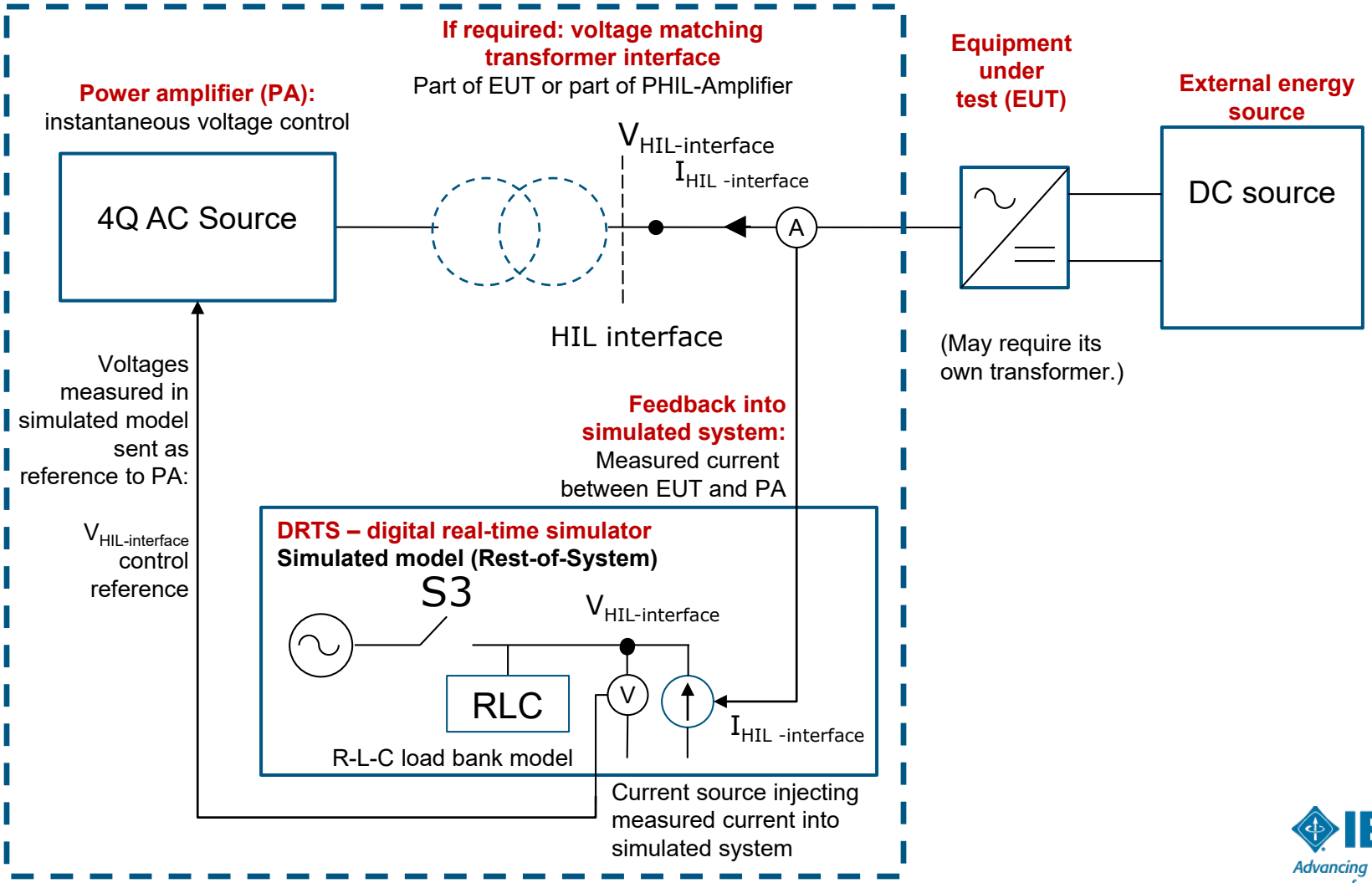
When using Power Hardware-in-the-Loop (HIL) simulation-based testing approach …

- simulated EPS (electric power system), switch S3, switch S1,
- simulated resonant load bank;
- simulated subsystem be interfaced to the EUT (equipment under test) through power amplifiers;
- requirements for PHIL test setup and simulated subsystem.



Hardware-in-the-Loop (HIL) Testing

Unintentional islanding: example PHIL-setup



Hardware-in-the-Loop (HIL) Testing

Unintentional islanding -- Requirements

… compliance with the following test equipment and setup characteristics (in addition to the general requirements and unintentional islanding testing requirements)

1. Simulated Rest-of-System and Interface Algorithm shall use **electromagnetic transient-type** approach and use **instantaneous** voltages and currents, **maximum time step of 50 µs**

2. **Validation of simulated circuit behavior**
   - Once per EUT with any means necessary to achieve the test points,
     - EUT operates at nominal power with power factor of 1
   - Start at the EUT's nominal conditions and reach four test points
     - Adjust resistance and capacitance to yield voltage and frequency changes
     - Note:
       - Magnitude guided by continuous operating region of 0.88 pu ≤ V ≤ 1.10 pu
       - Frequency is within OF1 and UF1 (default 300 s clearing time)

PHIL-setup reflecting RLC-load bank behavior at the following operating points:

1. R: 81%, C: 106% yields V: 90%, f: 97% (58.2 Hz)
2. R: 81%, C : 94% yields V: 90%, f: 103% (61.8 Hz)
3. R: 117%, C : 106% yields V: 108%, f: 97%
4. R: 117%, C : 94% yields V: 108%, f: 103%

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Hardware-in-the-Loop (HIL) Testing

Unintentional islanding -- Requirements

… continued

- PHIL simulation setup shall be capable of **voltage harmonic synthesis**
  - At least 800 Hz and up to a frequency that is twice the UI-control bandwidth of the EUT
  - Upper frequency capabilities shall be at least 3 kHz if information on the UI-control bandwidth is not available
  - Once per EUT test setup
  - Frequency test points following a logarithmic scale starting at five times the fundamental with at least five data points per decade.
  - Voltage harmonic magnitude shall be greater than 1% of the nominal voltage while operating as a standalone voltage source.

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Hardware-in-the-Loop (HIL) Testing

Unintentional islanding

Alternative to the RLC-operating points test:

Impedance measurement may be used evaluate the PHIL-simulation capabilities …

- Measured impedance characteristics shall reflect the expected RLC behavior within magnitude and angle requirements
- Frequency range: f_{LL} = 10 Hz to f_{UL} = 3 kHz or up to twice the EUT's UI-control bandwidth.
- ROS simulating the RLC load bank with nominal EUT-derived values, power factor of 1
- EUT (unintentional islanding algorithm disabled) or any other appropriately rated and controllable source
- Using a dedicated impedance measurement unit or the PHI-setup
- ROS-impedance as seen from the terminals of the EUT shall be determined. At least 5 data points per decade shall be collected with the frequency data points following a logarithmic scale. The magnitude and phase requirements (next slide)

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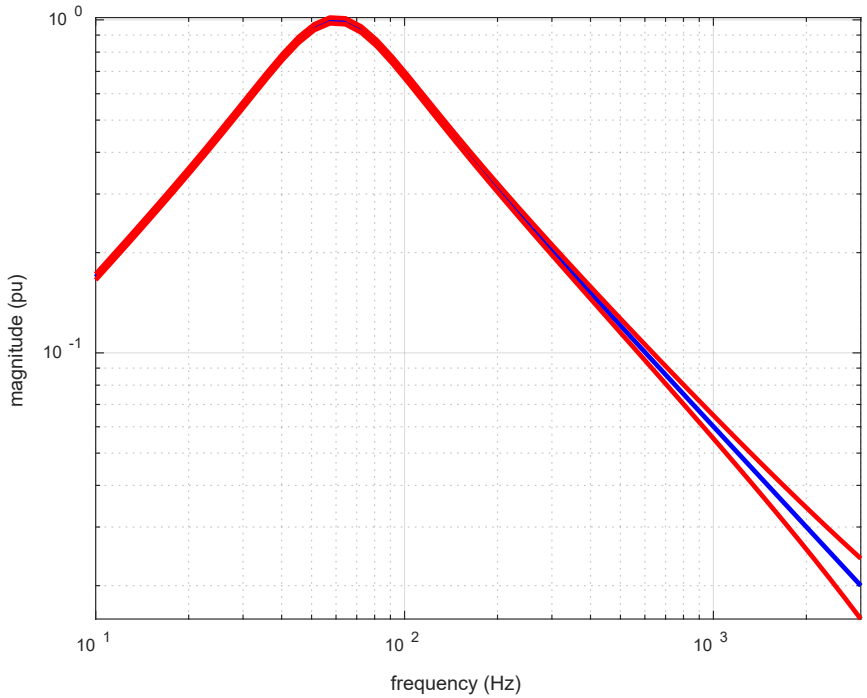
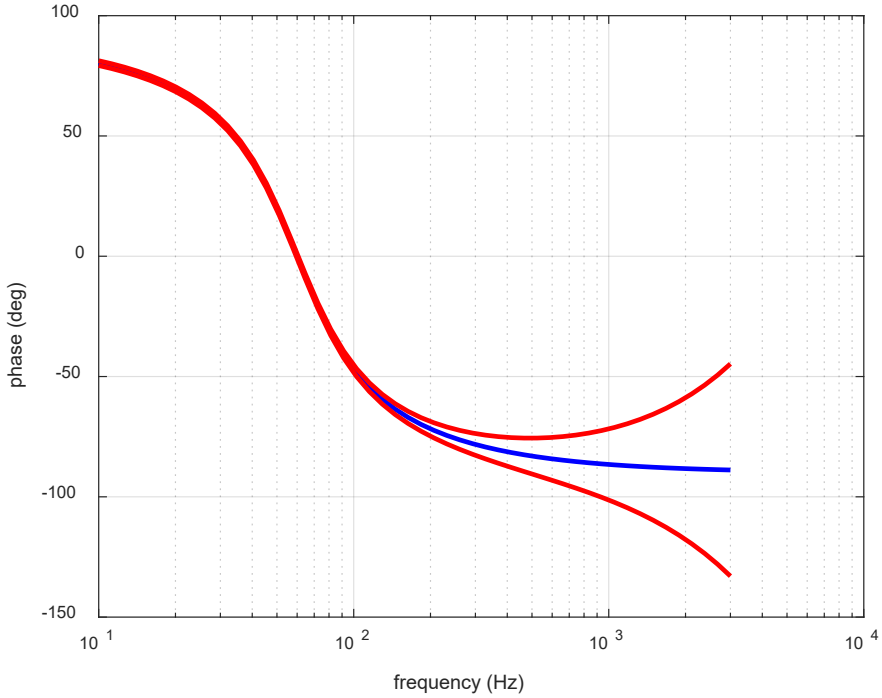
Impedance characteristics





- Magnitude requirement: for f_{LL} <= f <= f_{UL} the impedance magnitude |Z| shall be within a magnitude range $|\Delta Z|$ about the simulated RLC-load with
  $|\Delta Z| = \max(2.5\%, 2.5\% + (f - 60Hz) / f_{UL} * 30\%)$.

  Phase requirement: for f_{LL} <= f <= f_{UL} the impedance phase $\angle(Z)$ shall be within a phase range $\angle(\Delta Z)$ of the simulated RLC-load bank with
  $\angle(\Delta Z) = \max(1 \text{ deg}, 1 + (f - 60Hz) / f_{UL} * 44 \text{ deg})$.

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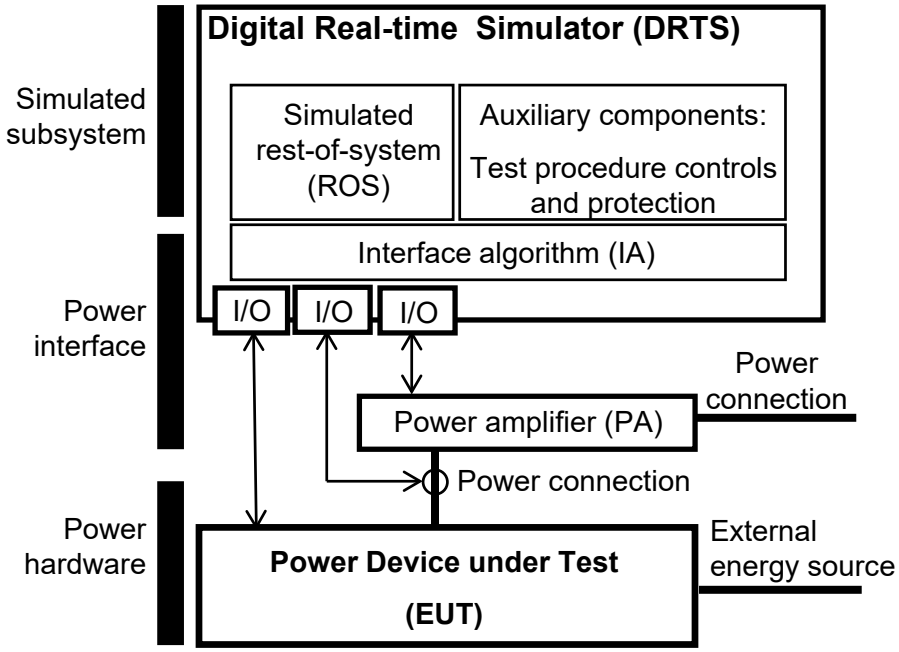
HIL Annex - Terminology

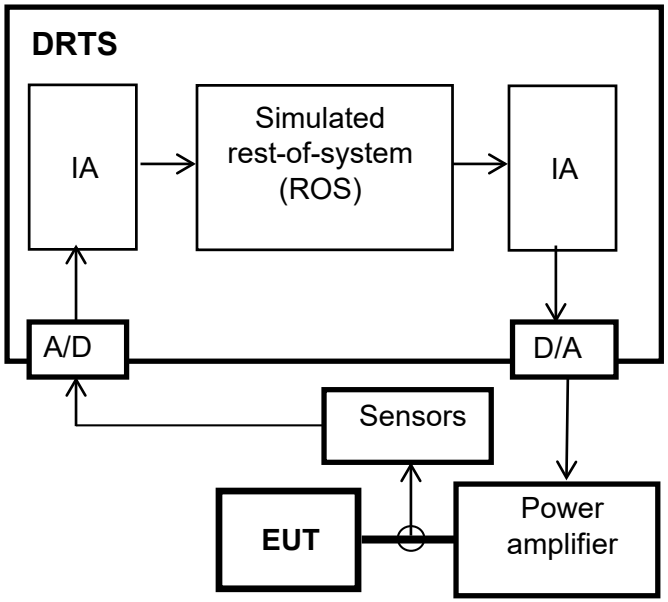
- **Digital real-time simulator (DRTS):** A digital real-time simulator (DRTS) is an integral part of HIL test setups and simulates a model (rest-of-system, ROS), provides interfaces to exchange signals between the simulated subsystem and external hardware, and controls the test conditions at the terminals of the EUT. For electric subsystems, which interface to the device under test, electromagnetic transient program (EMTP) type modeling and simulation approach shall be used.
- **Interface algorithm (IA):** An interface algorithm in the context of PHIL is a method of linking a DRTS simulated subsystem to a power device under test. For example, a power interface (amplifier) may be used as a controlled voltage source and its measured current fed back into the simulated system. Several interface algorithms are available, see for example [B18].
- **Low-power input/output interfaces:** Low power input/output (I/O) interfaces provide the means to interface signals that control power equipment or controls as part of HIL-based testing. Typically, analog I/O-signals are in the range of 0-10V and digital signals follow standards such as TTL. These interfaces may also use digital communication protocols to exchange information.
- **Power amplifier (PA):** Power amplifiers receive reference signals that reflect voltages and/or currents of simulated subsystems. The amplifier transforms the reference signals to voltages and/or currents at its power terminals to interact with the EUT.
- **Power interface:** A power interfaces links the signals of the simulated subsystem to the power equipment under test. A power amplifier enables the interface by amplifying the low-power reference signals to voltages and/or currents as provided by the DRTS.
- **Rest-of-system (ROS):** HIL tests require models to be simulated on the DRTS to close the loop between the simulated subsystem and EUT. Properties and requirements of models are specific to a HIL test. In PHIL experiments, the simulated subsystem provides the reference signals for the power amplifiers and receives voltages and/or currents as feedback. The rest-of-system (ROS) refers to the simulated subsystem that is executed on the DRTS and interfaced to the EUT.

Power HIL (PHIL) Principals



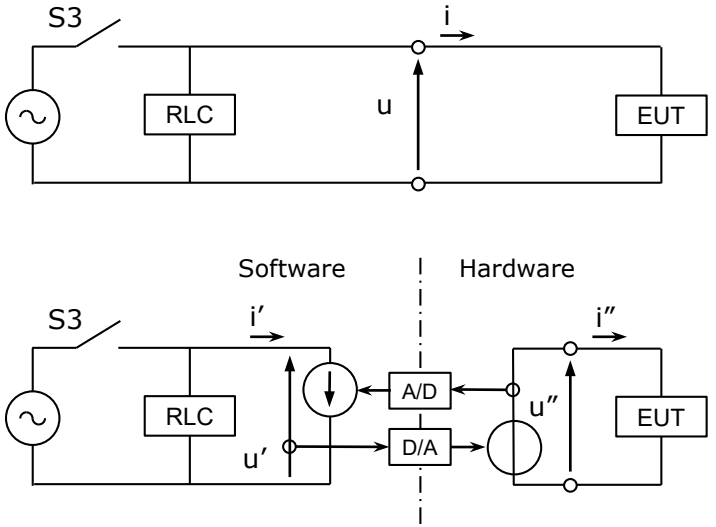
Power Hardware-in-the-Loop test setup overview

Power HIL (PHIL)



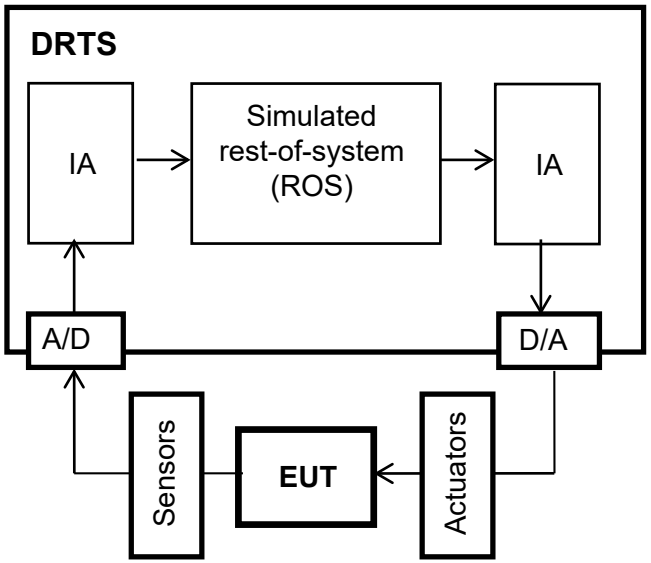
Interface algorithm linking simulated ROS with power amplifier and EUT

(1) unintentional islanding test circuit with dedicated RLC-load bank



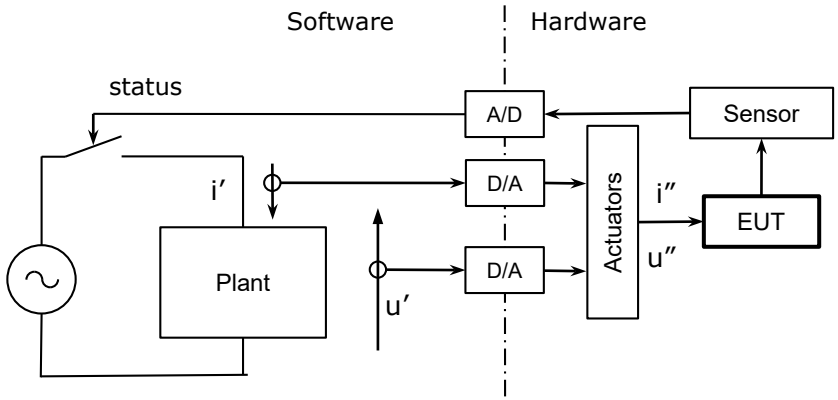
(2) depicts a corresponding PHIL test setup

Controller HIL (CHIL)



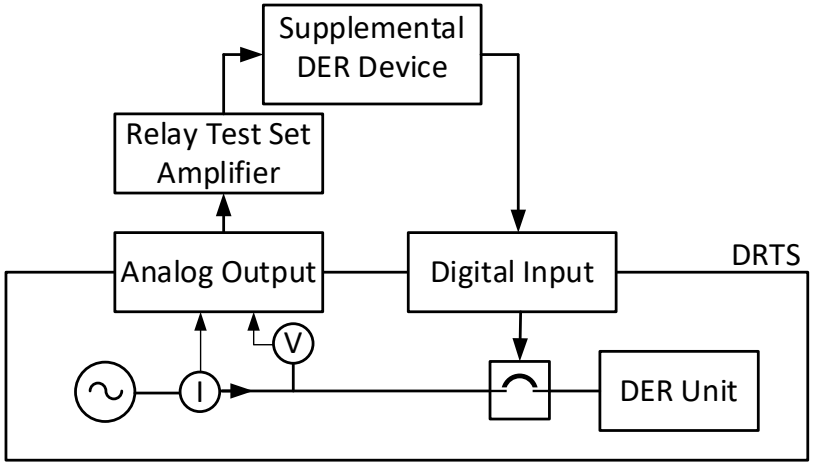
Interfacing EUT to the simulated ROS in a CHIL test setup

Example application: linking the EUT to the simulated ROS subsystem in of relay testing through actuators and sensors if required to adjust voltage and current levels, e.g., potential and current transformers.

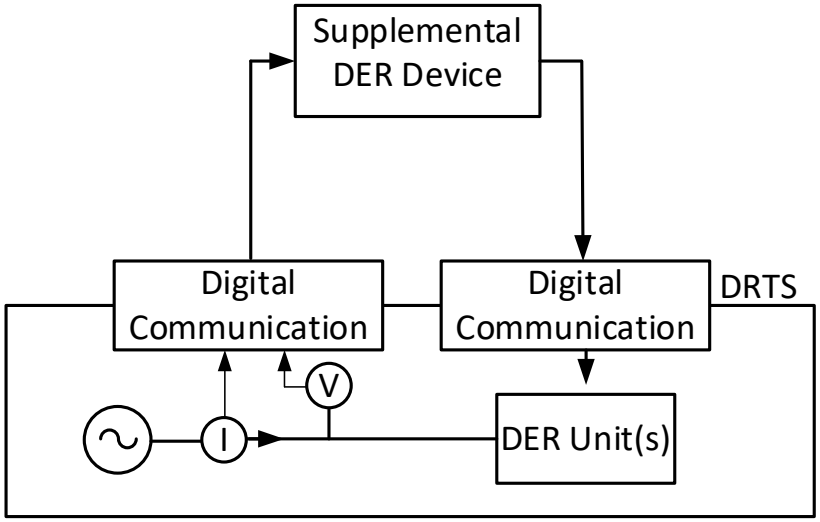


Controller HIL (CHIL)

Design evaluation studies may benefit from this method since supplemental DER devices do not fit within the scope for type testing. Controller HIL testing can show correct functionality of a supplemental DER device within a larger DER system prior to installation in a field site.



Using a Controller HIL-test setup to confirm operation of supplemental DER devices



Using a Controller HIL-test setup to confirm operation of a plant controller (a supplemental DER device)