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# Black Box Models and GTSOC

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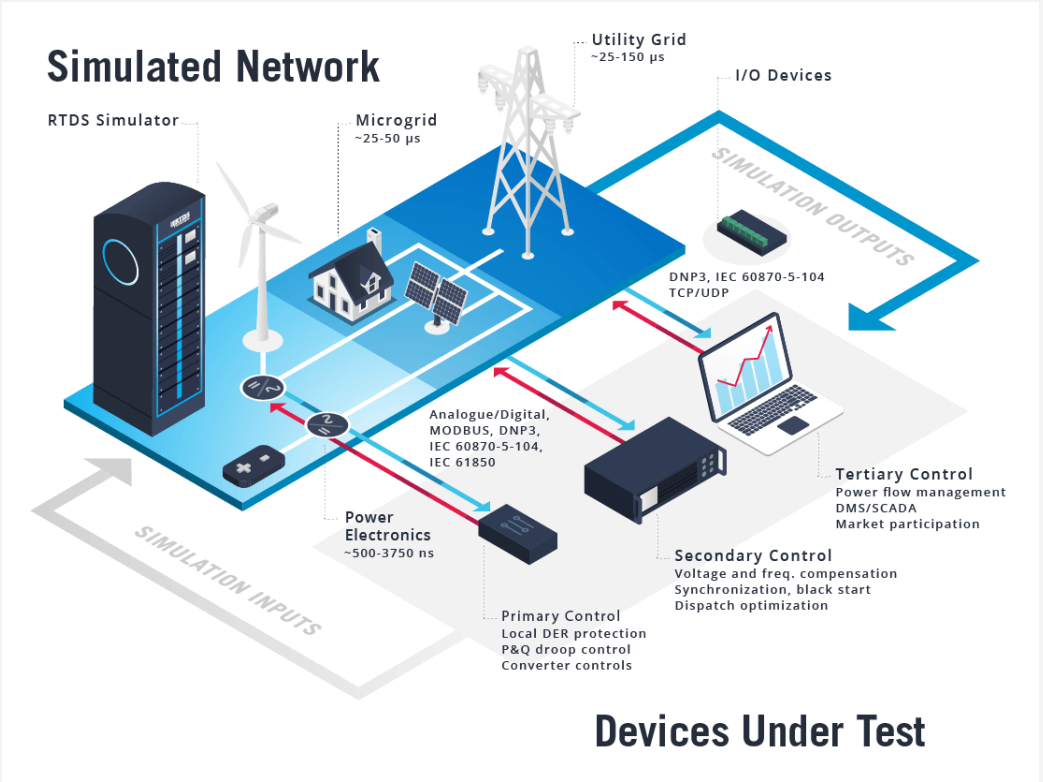
# Agenda

- Why Black Box Models?
- Techniques for Executing Blackbox Controls
- Introduction to GTSOC
- Deploying Blackbox Controls
- GTSOC Examples

# Why are Blackbox Models Important?

- Generic models have their limitations
- Tuning generic models can be very time consuming
- Controller circuitry may be tightly integrated with power circuitry
- Difficult to scale if a large number of controllers are involved
- Vendor's IP must be protected
- Customers want models that accurately reflect the real control and protection equipment provided by vendors
- The same code base used by vendors can be used to create the black box model



# Techniques for Executing Blackbox Controls

- Hardware
- Operating system
- Dynamic or Static library
- Real-time operation required

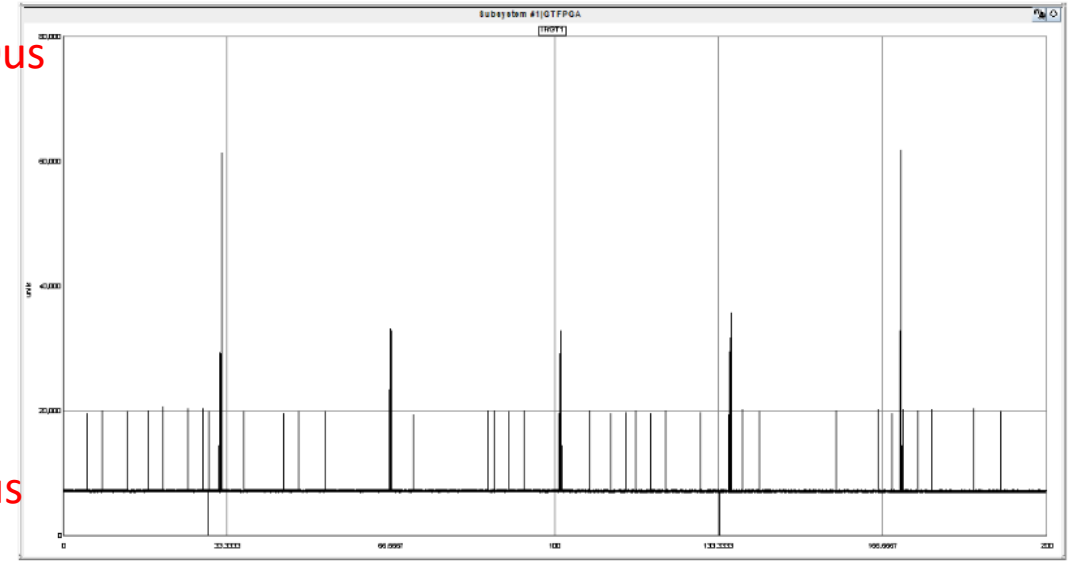
| Hardware \ Operating System | Windows | Linux | Bare metal |
|---|---|---|---|
| PC | Dynamic: .dll<br>Static: .lib | Dynamic: .so<br>Static: .a |  |
| ARM |  | Dynamic: .so<br>Static: .a | **Static: .a** |

# Techniques for Executing Blackbox Controls

× **Linux OS running dynamic library (.so)**

The problem is the **indeterministic** execution time spike ~ 200 us, which is hard to eliminate without third-party real-time OS support.

80us

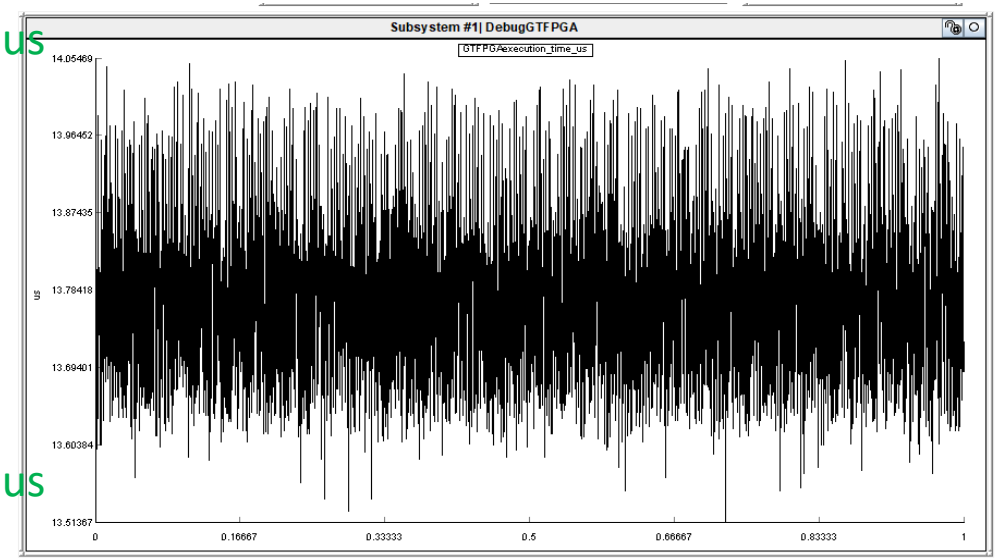


8us

✓ **Bare-Metal running static library (.a)**

Bare metal guarantees **deterministic** timing: <1us spike.

14.05us




13.51us

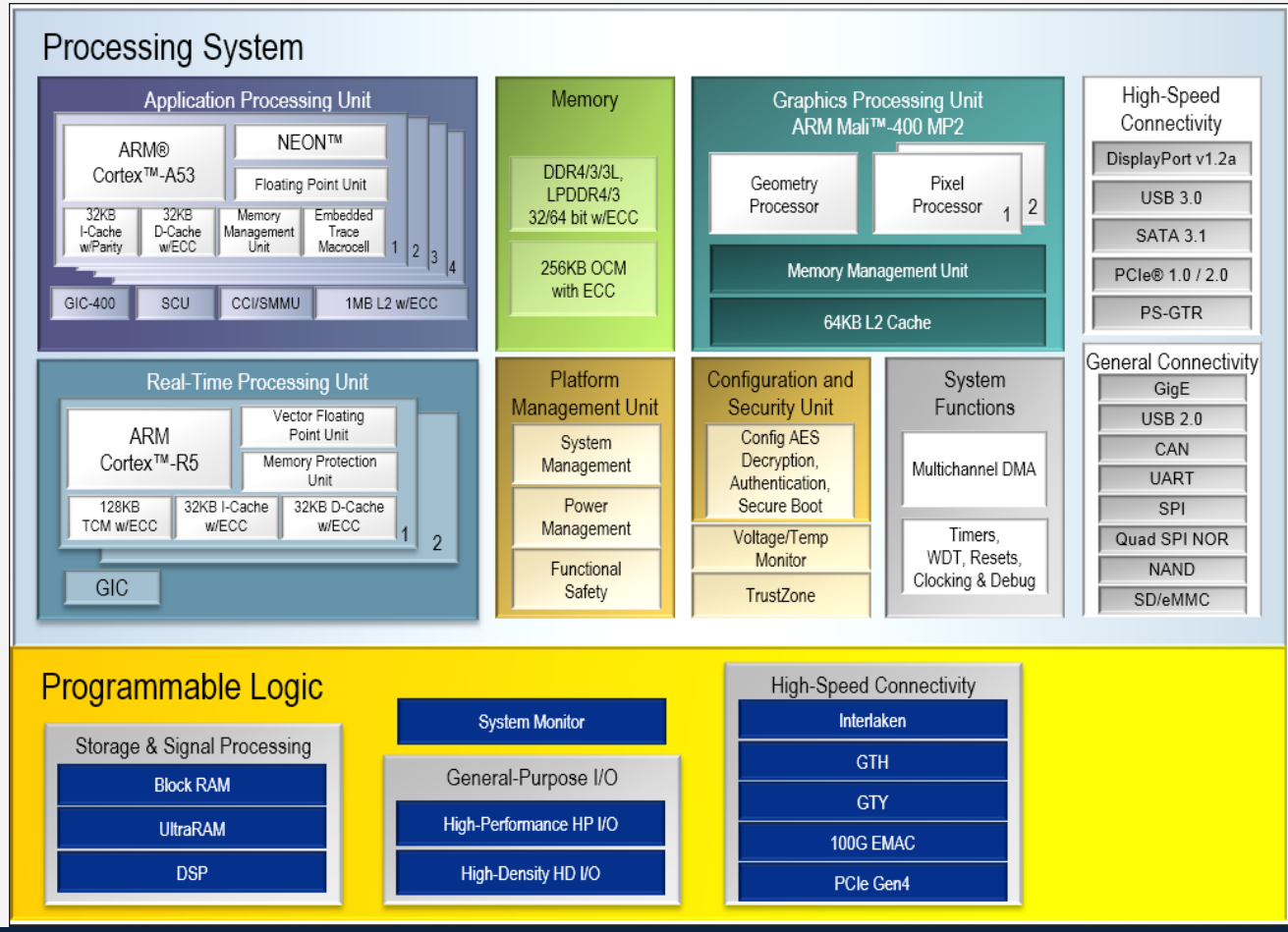
# Introduction to GTSOC

- GTSOC - integration of GTFPGA and Multi-Processor System-on-Chip (MPSoC)

- New applications using processors: e.g. Blackbox controller simulation


# Introduction to GTSOC

- **Xilinx Zynq UltraScale+ XCZU15EG**
- **Processing System (PS)**
  - 4 Application cores: ARM Cortex-A53
  - 2 Real-time cores: ARM Cortex–R5
  - 1 GPU core
  - High/low speed connectivity
- **Programmable Logic (PL)**
  - Larger than VC707-based GTFPGA
  - Seamless upgrade for existing GTFPGA applications

# Introduction to GTSOC

- GTSOC
- NovaCor only (Not PB5)



***GTSOC V1 UNIT***

**4 x ARM cores**

| | |
|---|---|
| 5 x .a | 5 x .a |
| 5 x .a | 5 x .a |

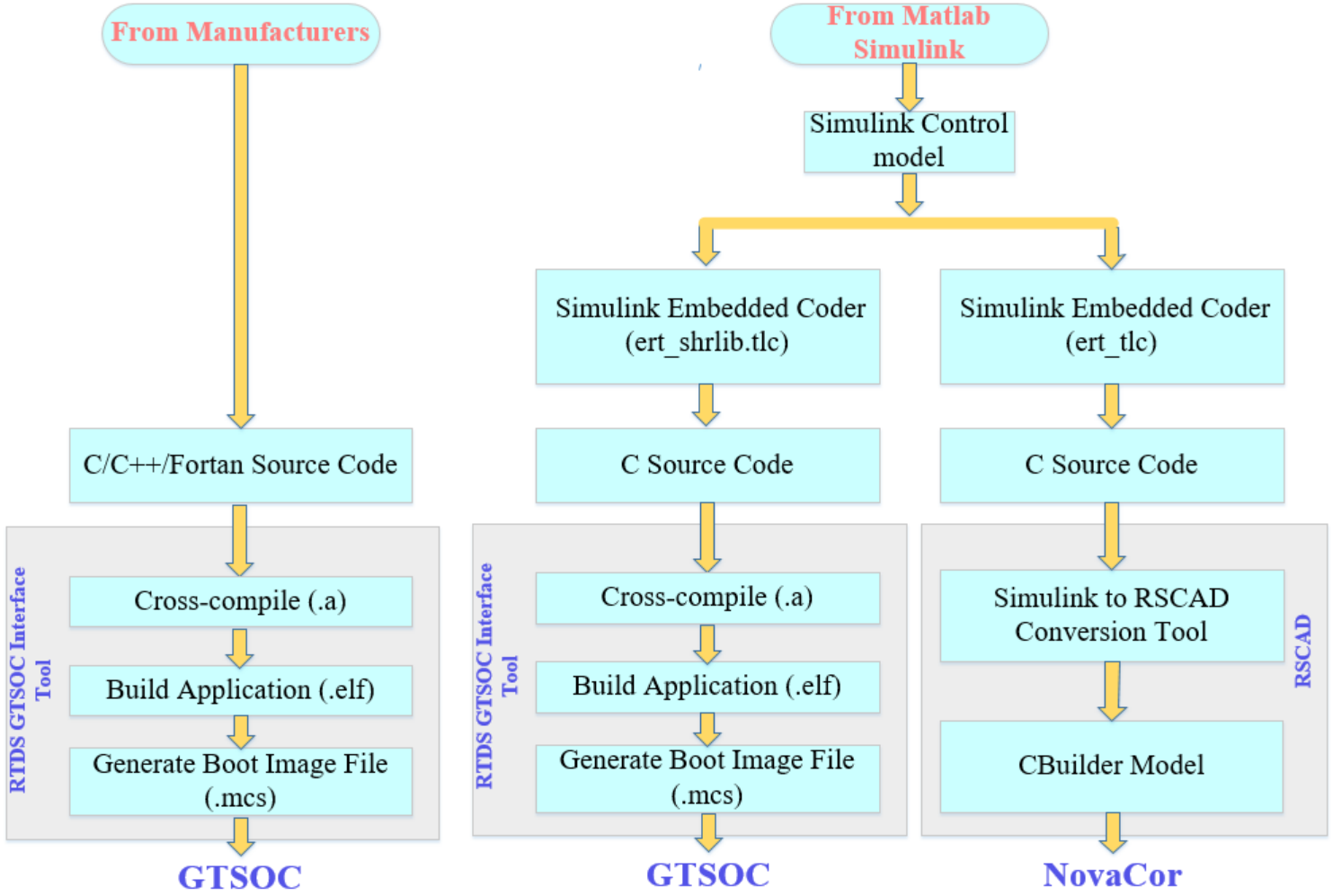
**4 x RTDS interface**

**Fibre cables**

***NOVACOR CHASSIS***

# Procedure For Deploying Blackbox Controls

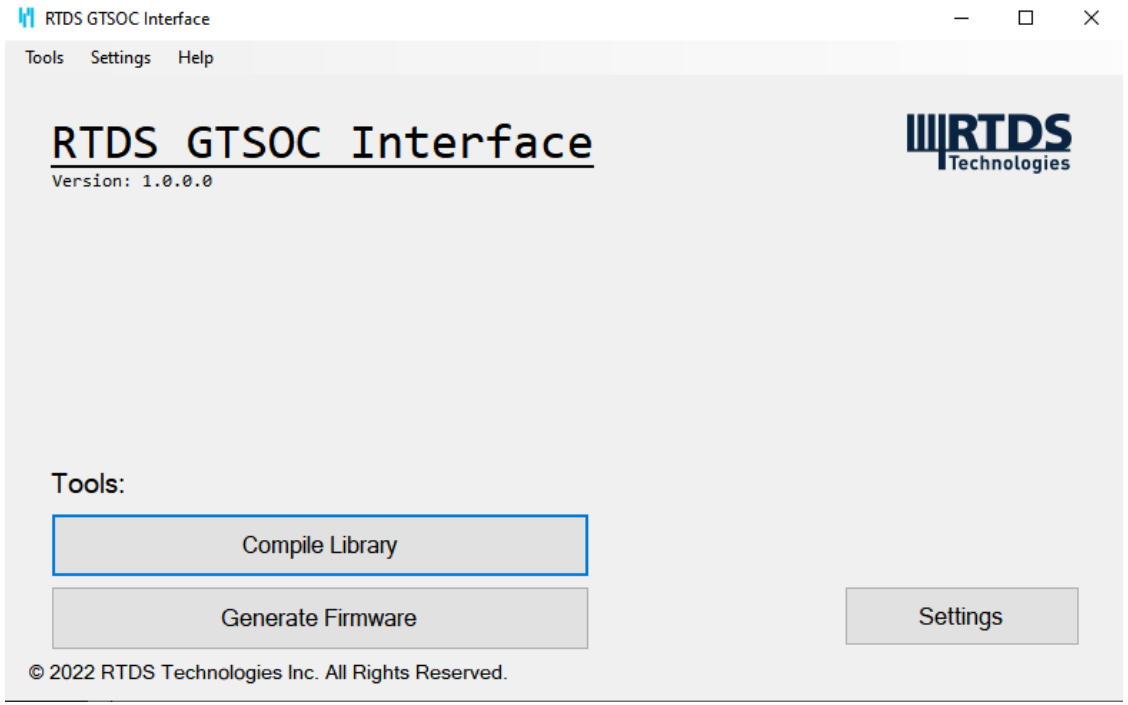
- From MATLAB Simulink
  - CBuilder model alternatively
- From Manufacturers (C/C++/Fortran)



# RTDS GTSOC Interface Tool

- RTDS GTSOC Interface Tool is provided to establish blackbox controller simulation on GTSOC automatically and quickly.
- Cross-compile the source C/C++/Fortran code to .a file.
- Automatically modify the wrapper C code and link the .a file to build application executable .elf file.
- Generate the GTSOC boot image (firmware) file .mcs.
- Download .mcs using RSCAD firmware Upgrade Utility

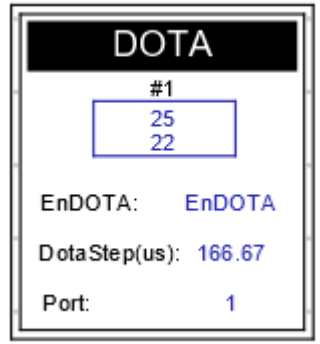
RTDS GTSOC Interface Tool

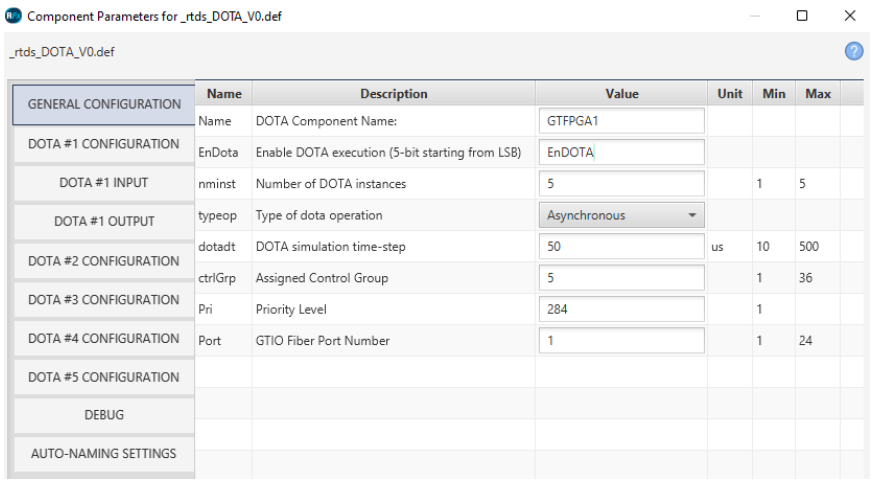


# RSCAD FX GTSOC DOTA Component

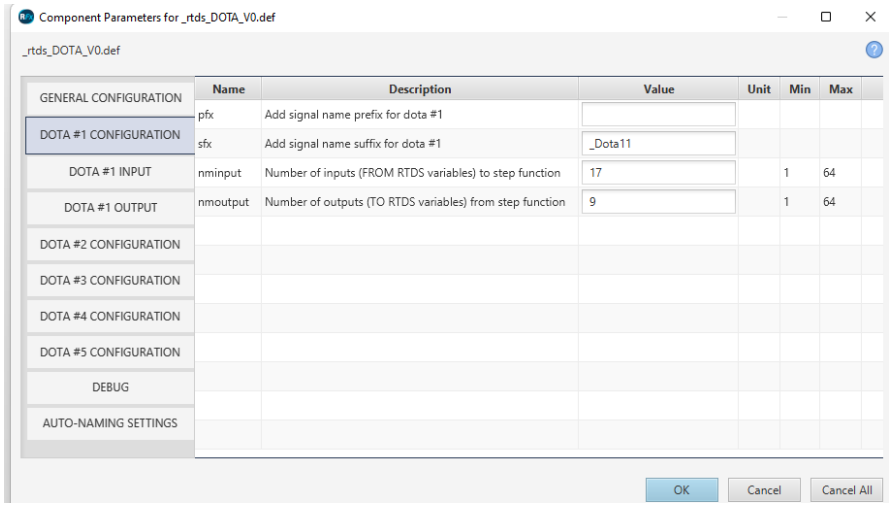
- Each GTSOC unit has one ARM Cortex-A53 Processsor with four cores
  - Each ARM Cortex-A53 core requires one DOTA component
    - Each DOTA component supports up to five DOTA instances
      - Each DOTA instance supports up to 64 inputs and 64 outputs
      - Each instance could be the same (multi-instance) or different

DOTA component



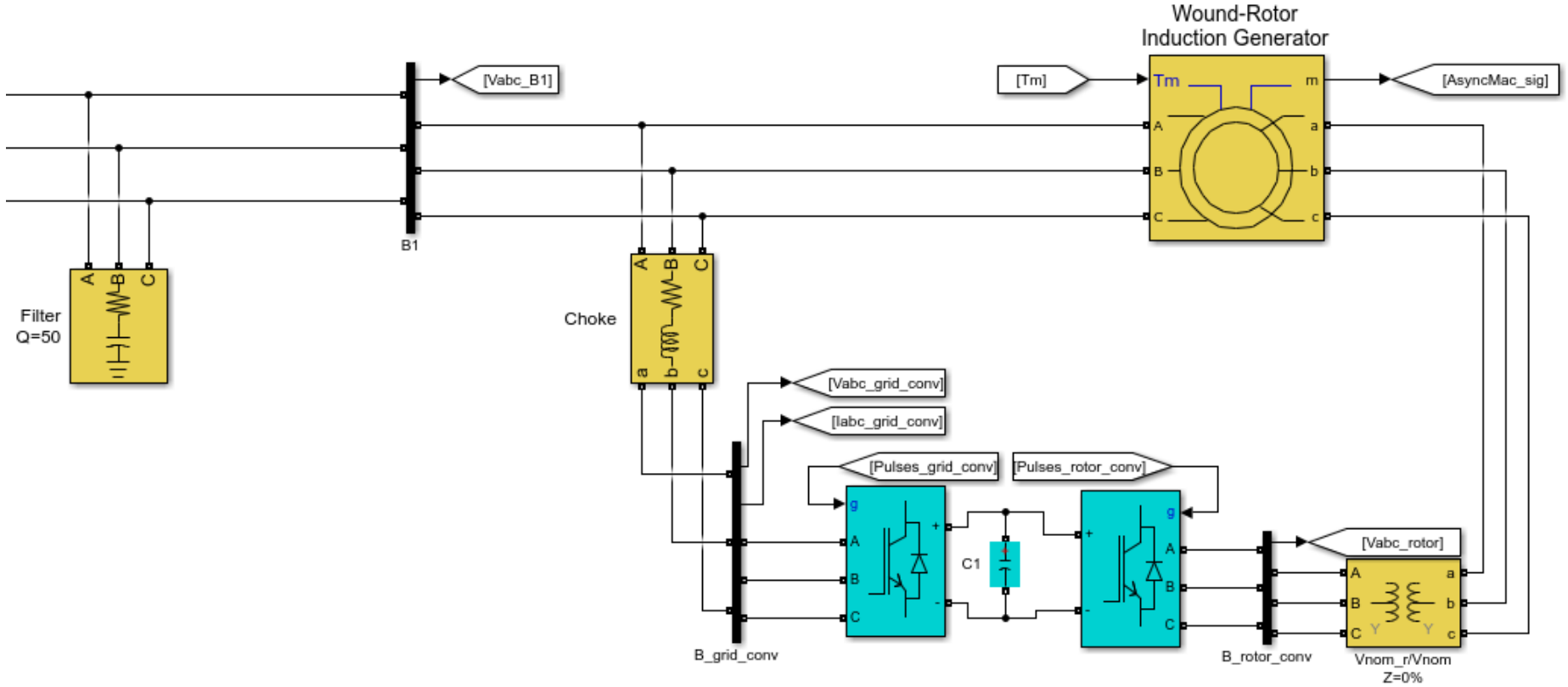

DOTA General Configuration




Single DOTA Configuration

# DFIG System Example

## Simulink DFIG System (Electrical System)



# DFIG System Example

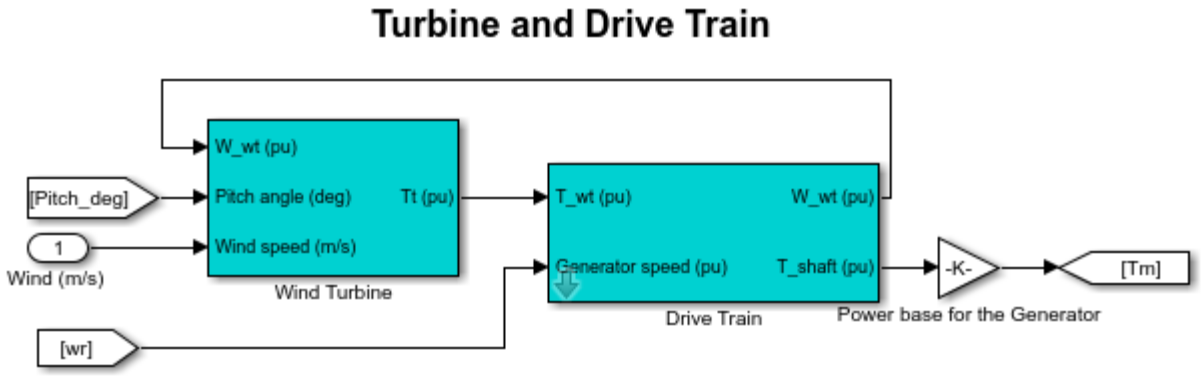
## Simulink DFIG System (Control System)

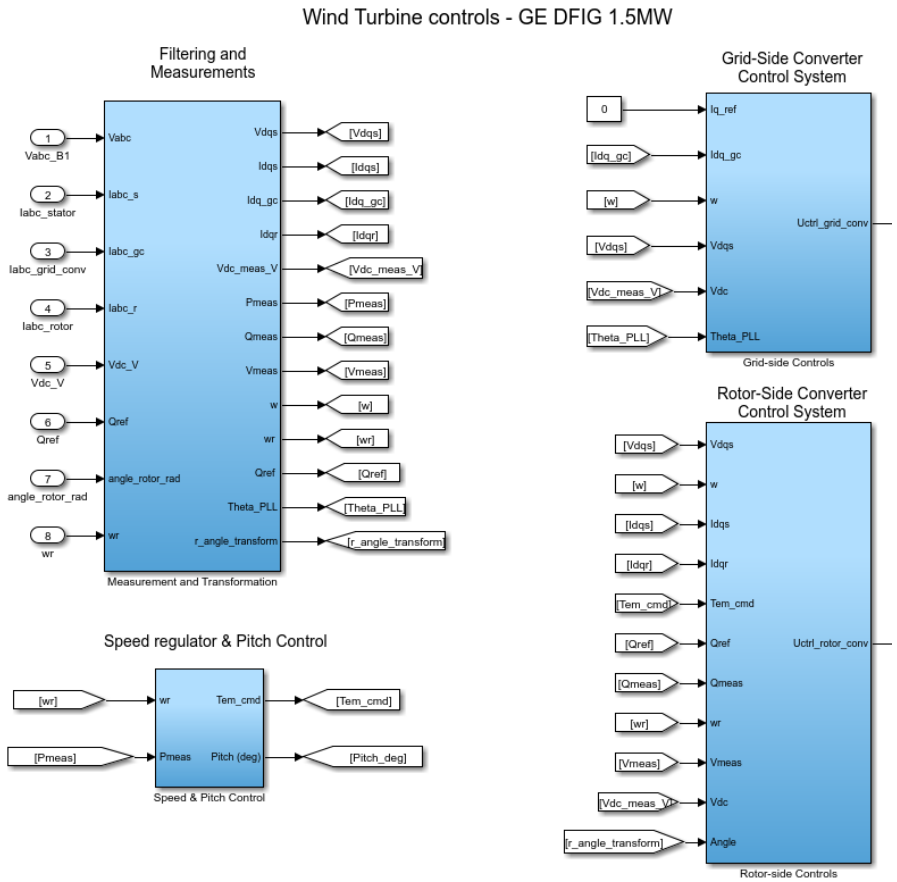
**Turbine and Drive Train:**

- Wind turbine
- Drive train

**Wind Turbine Controls**

- Filtering and measurements
- Grid-side converter control system
- Rotor-side converter control system
- Speed regulator & pitch control



# DFIG System Example

## RSCAD DFIG System

**Electrical System (on NovaCor):**

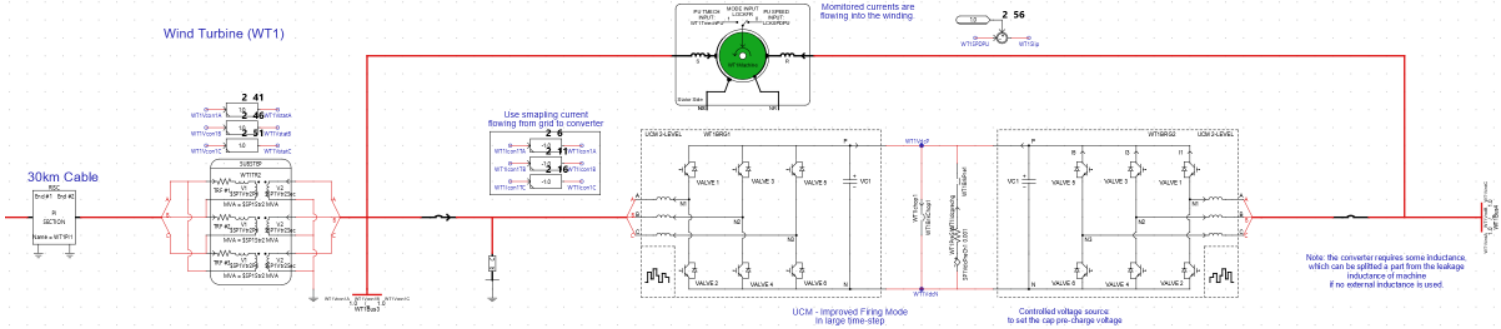
Same as the circuit in Simulink

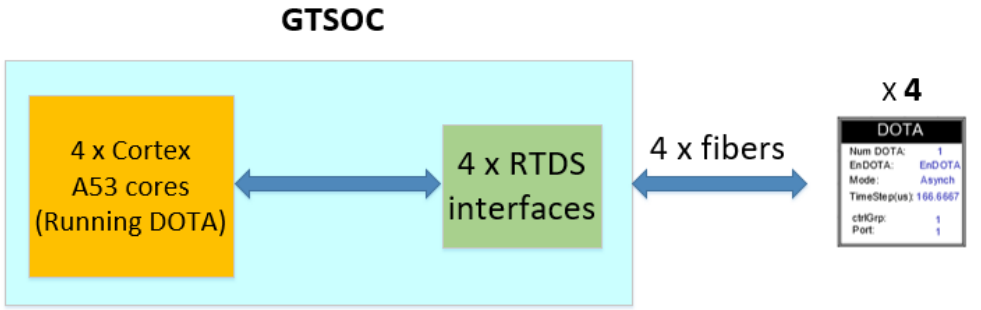
**Control System (on GTSOC):**

Filtering and measurements
Grid-side converter control system
Rotor-side converter control system
Speed regulator & pitch control

**Interface between NovaCor & GTSOC**

DOTA component: RTDS interface (Port 1-20)



# DFIG System Example

## Multi-Core and Multi-Instance Testing

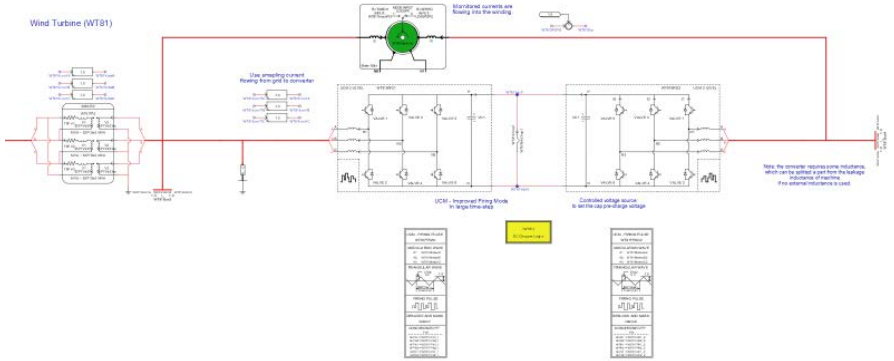
**Electrical system :**

21 DFIG systems, 2 AC Thevenin networks

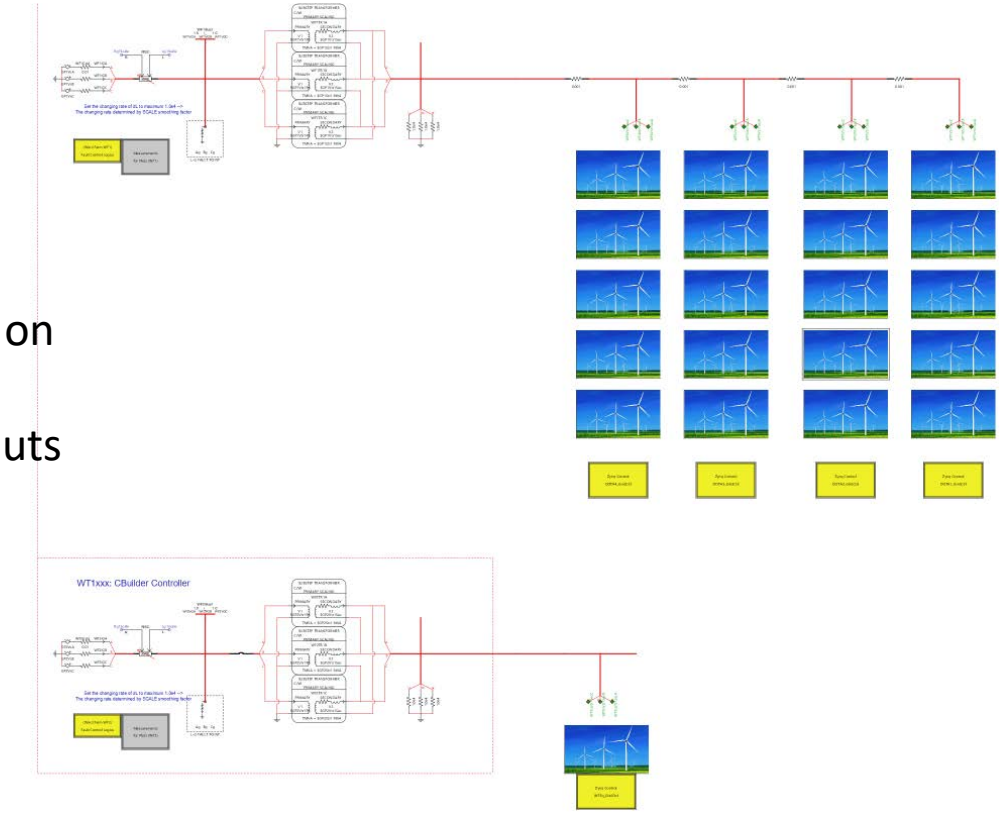
**Control system:**

20 DFIG controls on 4 GTSOC cores (every 5 DFIGs controls on one GTSOC core)

**Four DOTA components (**one per GTSOC core, each has 93 outputs and 53 inputs**)**



Single DFIG Electrical System



21 DFIG Electrical System

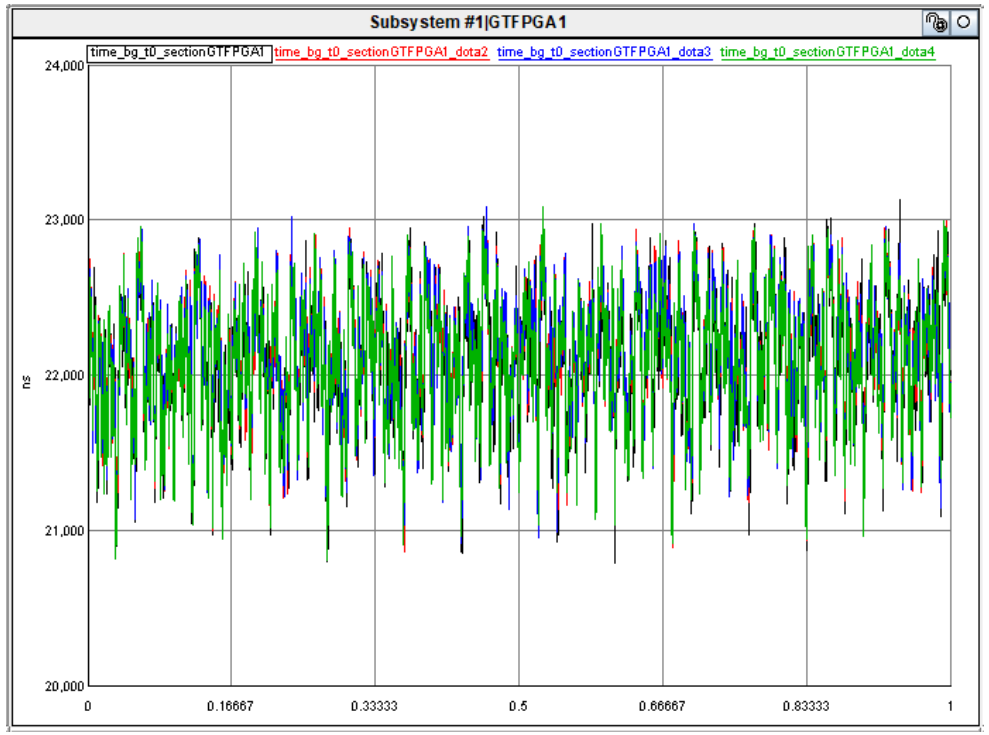
# DFIG System Example

## Multi-Core and Multi-Instance Testing - Timing

**20 DFIG DOTA Timing + Communication Timing (93 Outputs +53 Inputs):** 22us ± 1us jitter

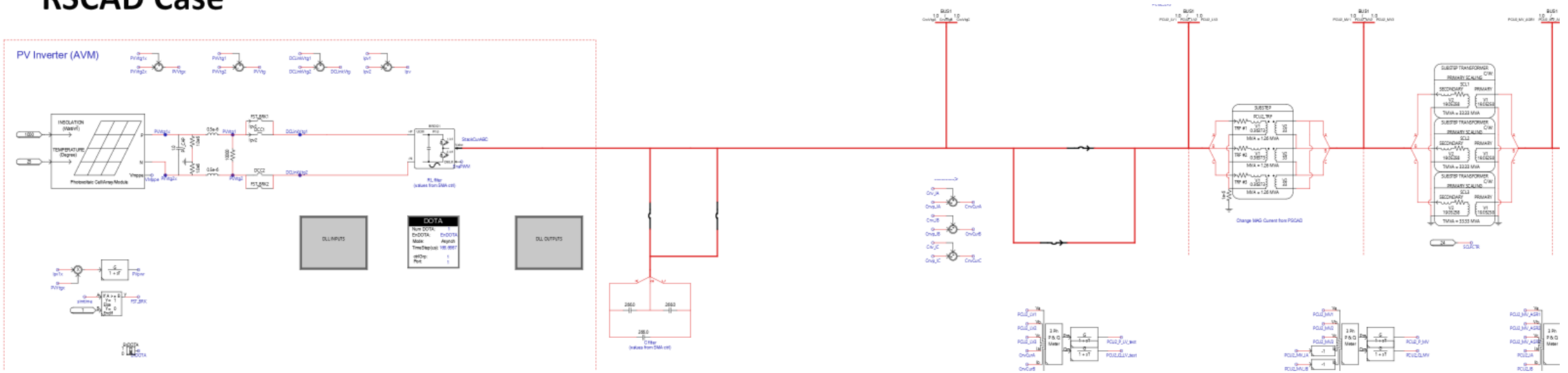
**C**ommunication : 6.3us

Each DFIG DOTA: (23-6.3)/5**=3.34us**



# SMA Inverter Example

## RSCAD Case

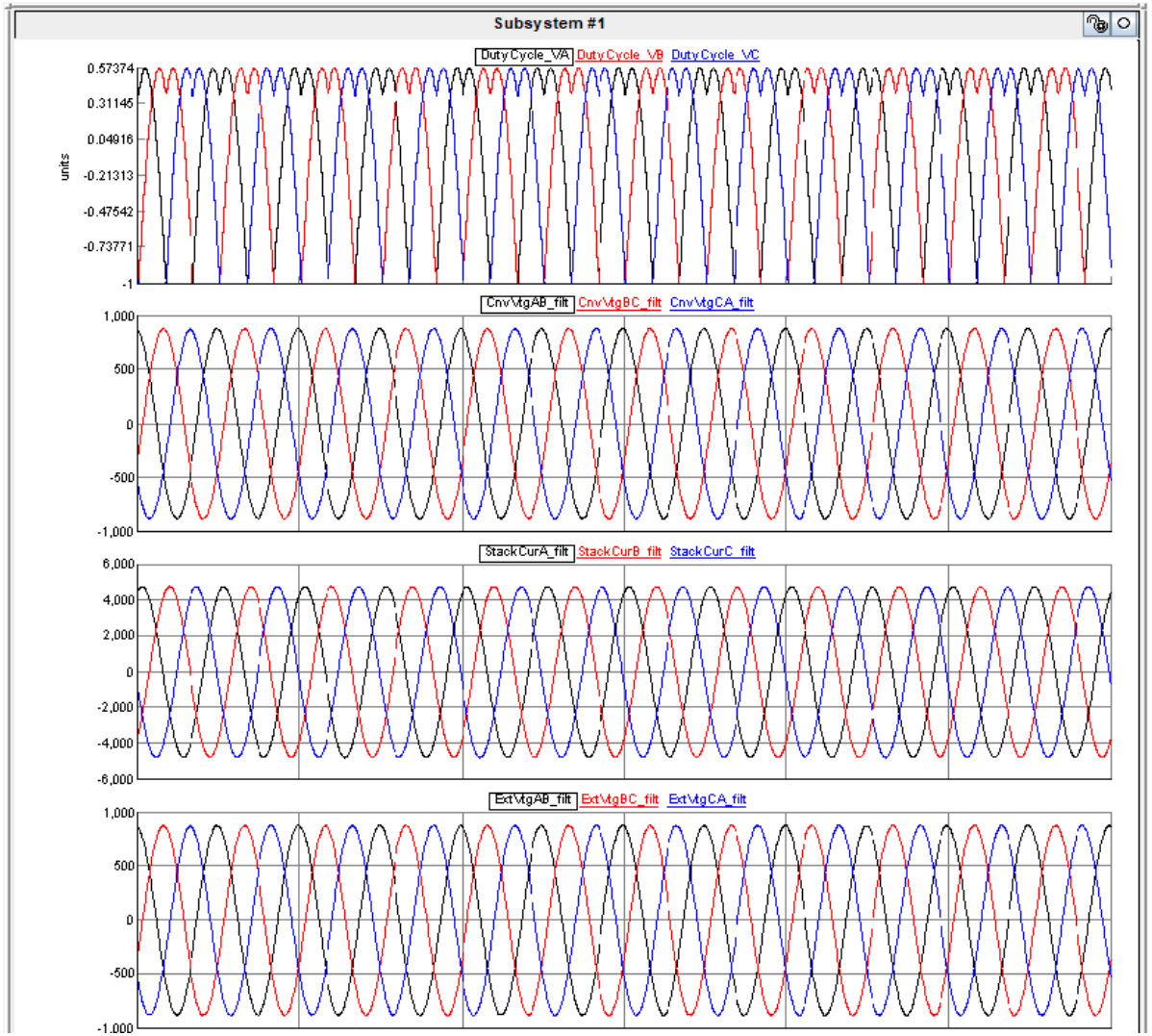



For the PV system:

- PV panel
- UCM to represent the grid-side converter
- Grid-side transformer, scaling transformer, and Thevenin equivalent AC source
- GTSOC time step size: 166.67us.
- Simulation time step size: 50us

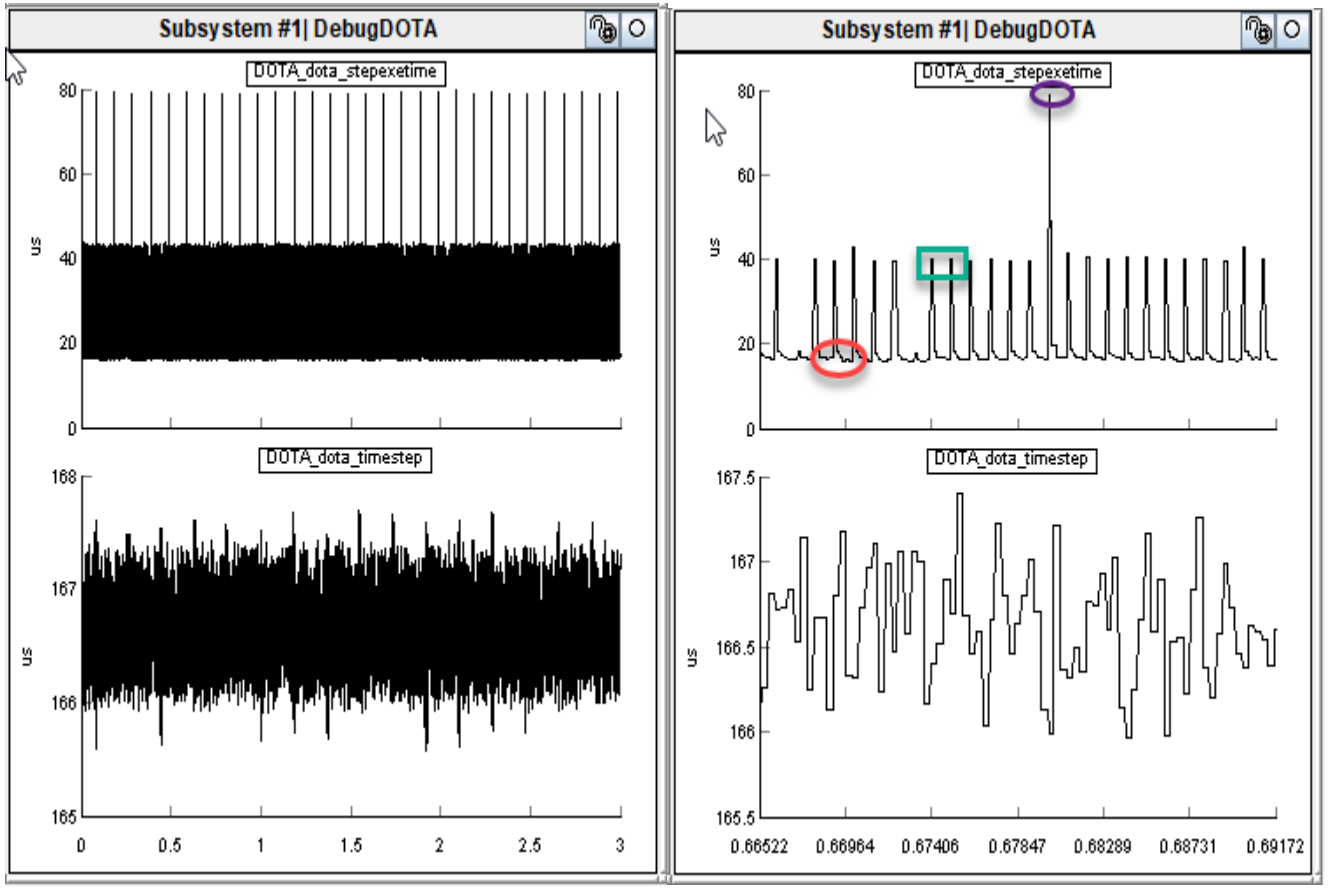
# SMA Inverter Example

- Also modelled SMA battery inverter
- Comparing results with PSCAD

# SMA Inverter Example

## Timing Statistics




DOTA execution time: periodic jumps (purple and green) are not spikes but scheduled controller tasking (e.g., protection).

# THANK YOU!
# QUESTIONS?