

IREQ PHIL SIMULATOR PROJECT UPDATE: Small-Scale Closed-Loop Testing Advancements and Full-Scale Amplifier

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Objective

Lead the energy transition at Hydro-Québec by developing a hybrid (virtual and real) T&D laboratory to study and integrate :

- Distributed Energy Resources
- Smart grids
- Microgrids

Large-scale transmission system simulated in real-time (Hypersim)



Design of the power amplifier (PA) topology					
Cascaded H- Bridge Transformerless High bandwidth	Development of the reduced-scale version of the PA				
	Cascaded H- Bridge	Design of a ge	eneral closed-loop interface Making a single full-scale H-		
<u>25 kV, 10 MVA</u>	Transformerless	Stable Precise	Bridge	Complete the	
	<u>208 V, 3 kVA</u>	High bandwidth	Experimental H- Bridge	PA	
\mathbf{V}			1 kV, 100 kW	3-phase	
	-		capability: 10x	capability	
		_	nominal current	overcurrent	
				DC to 1 kHz in closed-loop	

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Reduced-scale power amplifier

Goal:

<u>Validate</u> the PA topology, the control algorithms & the closed-loop interface

Rating: 208 V, 3 kVA

Isolated 2quadrant DC power supply H-Bridge



Design of the power amplifier (PA) topology				
Cascaded H-	Development of the reduced-scale version of the PA			
Transformerless	Cascaded H- Bridge	Design of a general closed-loop interface		
High bandwidth <u>25 kV, 10 MVA</u>	Transformerless High bandwidth 208 V, 3 kVA	Stable Precise High bandwidth		

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Stability issues in PHIL system

Ideal Transformer Method (ITM) is one of the most convenient interface methods:

- PA is a voltage source
- DUT current is injected in the simulator

The stability of this interface method is related to the <u>impedance ratio</u> between the ROS and the DUT taking in to account the hybrid nature of the system (i.e. continuous – discrete)

Closed-loop system stable if [1] :

 $|Z_ROS(z)| < |Z_DUT(z)|$ when $\angle Z_DUT(z) - \angle Z_ROS(z) = 180^{\circ}$



Example for a resistive DUT



Stable only if the Short Circuit Ratio (SCR) is > 50:

- R1 = 0.21 Ω
- L1 = 0.55 mH
- R2 = 14.4 Ω
- L2 = 15 μH
- Rf = 0.05 Ω
- Lf = 50 μH
- Cf = 22 μF

[1] O. Tremblay, H. Fortin-Blanchette, R. Gagnon and Y. Brissette, "Contribution to stability analysis of power hardware-in-the-loop simulators," in IET Generation, Transmission & Distribution, vol. 11, no. 12, pp. 3073-3079, 24 8 2017.



Relevance of the closed-loop PHIL



- If the simulated network needs to be 50 times stronger than a resistive DUT, the impact of the DUT on the ROS will be negligible (only 2% of impact).
- ⇒ closed-loop simulation is irrelevant using an infinite bus power system. Similar to open loop testing...

Relevant closed-loop tests should be able to represent high penetration of DUTs on the ROS:

- \Rightarrow Short-circuit ratio between 1 and 10 times the DUT power level
 - > The ITM is not appropriate for closed-loop PHIL!

The interface method must be energy conservative to ensure stability

⇒ Why not use a method that has been proven for more than 20 years in RTS to separate computation tasks?



Traveling wave interface method (Bergeron Line Model)

The secret behind real-time simulator

- A part of natural propagation delay of a transmission line is absorbed by the communication time between two processors
- ⇒ Large system impedance matrix can be divided into multiple smaller matrices that can be solved in parallel on many processors without numerical error.

The closed-loop system is stable since the trapezoidal integration method is used





Traveling wave interface method for PHIL

For PHIL, it is possible to add an artificial line (StubLine) between the ROS and DUT with exactly <u>one time step propagation</u> delay. However, there is a major drawback:

- It is required to add a real resistor Zc at the output of the PA
 - > High power losses in Zc must be considered (sizing of the PA, sizing and cooling of Zc)
 - Reduced voltage range at the output (voltage drop across Zc)
 - Zc cannot be changed easily (hardware)

Instead of a real resistor, a <u>fast speed control loop</u> is used to emulate the behaviour of Zc:











Experimental validation (PV inverter startup) – Wall outlet





Experimental validation (PV inverter startup) – PHIL





Experimental validation (PV inverter) – PHIL

Now, let's play with the system by doing events that are impossible to do with the wall outlet!



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	High bandwidth <u>208 V, 3 kVA</u>	High bandwidth	Experimental H- Bridge 1 kV, 100 kW Overload capability: 10x nominal current		

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Making a full-scale H-Bridge (Hardware)

Goal:





Making a full-scale H-Bridge (experimental results)

Smooth and fast switching, stable voltage

Square wave 50 Hz P = 100 kWTek _n_ M Pos: -4.400.us T Trig'd 1kV L -1kV M 5.00ms CH1 500V 8-Nov-18 02:26 150.002 M 5.00 JJs



Sine wave 50 Hz (PWM = 1000 Hz), 707 Vrms, 50 kW



Full voltage inversion at nominal power in less than 10 μ s.

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		Experimental H- Bridge	PA	
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Next step: complete the Power Amplifier

Optimize the design and connect the H-Bridges in cascade





Next step: complete the Power Amplifier

Optimize the design and connect the H-Bridges in cascade



n = 2 . . .







Next step: complete the Power Amplifier

Optimize the design and connect the H-Bridges in cascade



n = 18 . . .







Conclusion

IREQ PHIL simulator, a <u>unique research & testing infrastructure</u> to prepare the energy transition of Hydro-Québec.

To realize this system, full control of every technical aspects is required:

- Simulator's development to integrate seamless interface algorithms (traveling wave)
- FPGA technologies to implement fast control-loops (Zc emulation)
- Reduced-scale prototype to prove the concept
- Experimental bench for the hardware design of the full-size power amplifier



