Dual Power Hardware-in-the-Loop Simulation of Energy Storage Systems for Shipboard Applications

Matthew Bosworth[1], Karl Schoder[1], James Langston[1], Michael Steurer[1], Deanna Temkin[2], Tyler Boehmer[2]

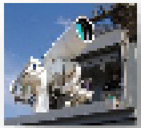
[1]Center for Advanced Power Systems, Florida State University
[2] The Johns Hopkins University Applied Physics Laboratory

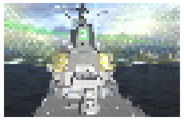
Energy Magazine Demonstration

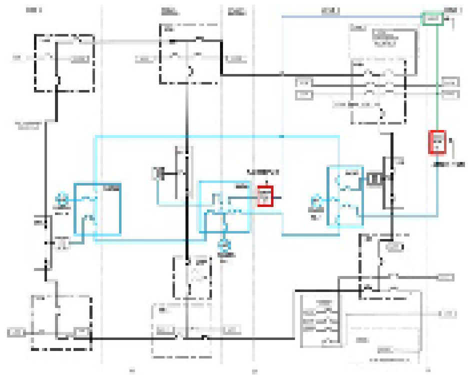
Modeling & Simulation

- DDG 51 Flt IIA & III VV&A'd Electrical System
- Detailed Mission Systems, including:

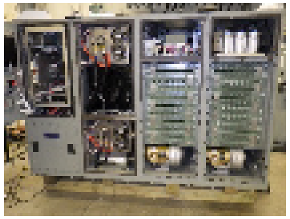

SEWIP


Laser

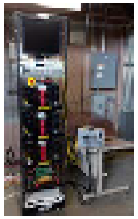

AMDR



+ Energy Storage Models & Hardware


EM-L (DRS)


FESS (GKN/UK)


JHU APL
Adaptive Power System
(APS)

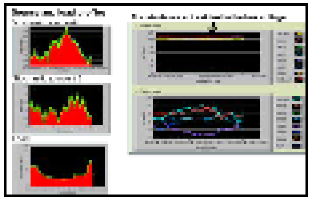
Real Time Dynamic Simulation
FSU CAPS

Knowledge

Control Hardware in the loop (CHIL)
Power Hardware in the loop (PHIL)

+ Power & Energy Management

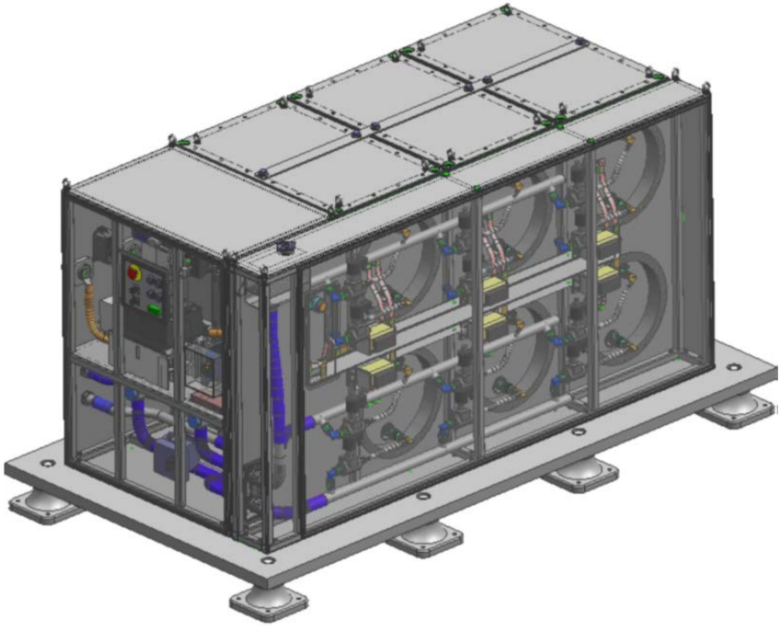
- Sandia NL Distributed Energy Management



Demonstrations Validate Interfaces for Pulsed High Energy Systems

Flywheel Energy Storage System (FESS)

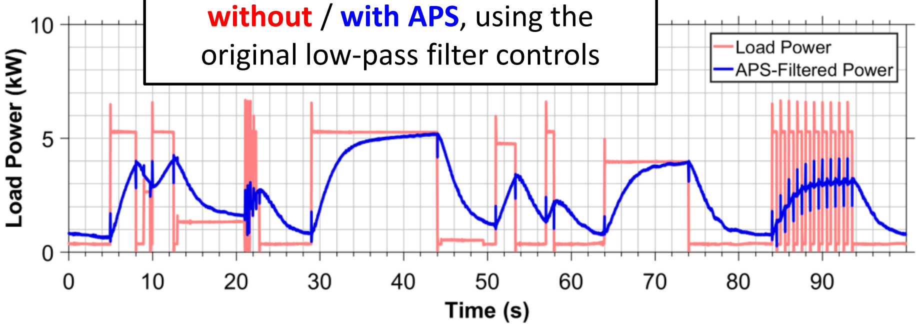
- Modular flywheel energy storage system
- Developed by GKN
- 20 MJ Unit
- Single Bidirectional DC Interface
  - 500 – 820 V
  - 320 kW charging or discharging



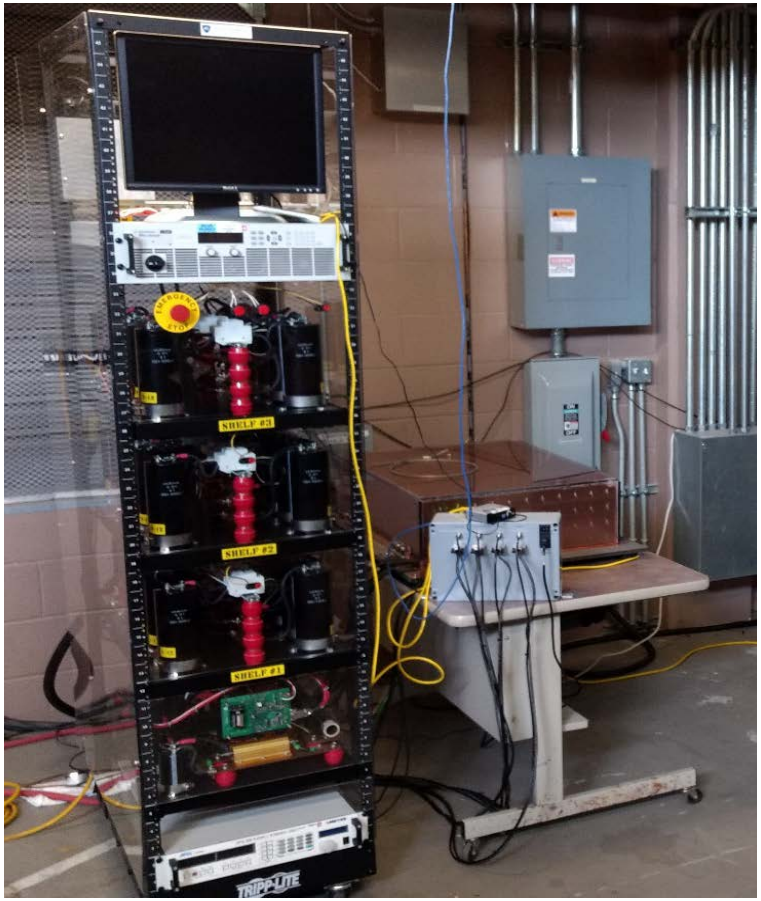
Adaptive Power System (APS)

- Developed by JHU/APL
- Created to protect the ship's electric plant and maintain power quality, satisfying both load and source needs
    - Provides smooth power profile to ship's generator
    - Maintains well-regulated voltage to dynamic loads
    - Is an enabling technology for emerging sensors and weapons

Notional power profile to generator **without** / **with APS**, using the original low-pass filter controls

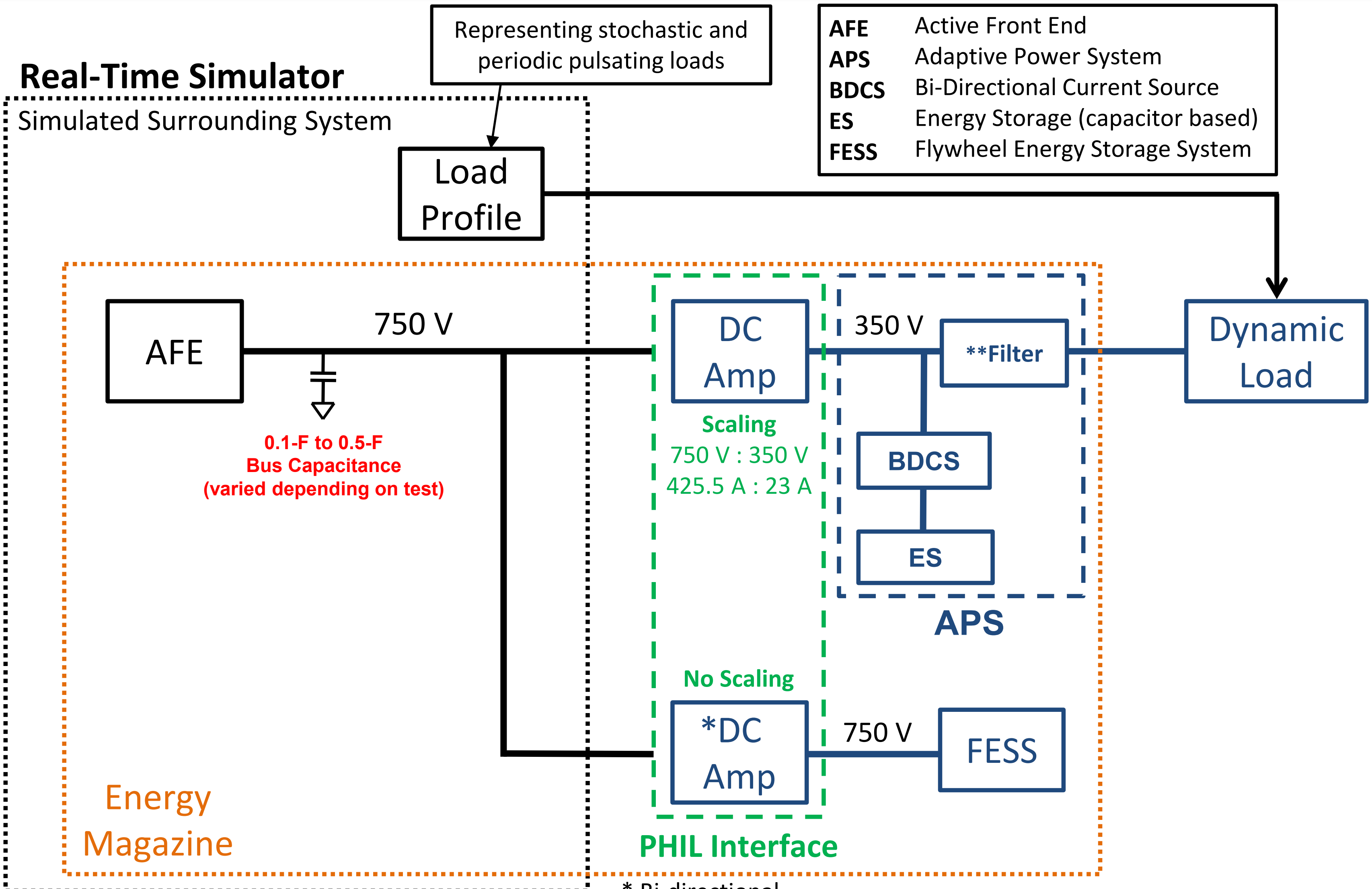


Prototype Module: 8 kW, 350 VDC bus, Energy Storage Capacitors run up to 800 V



Energy storage decoupled from regulated bus through a bi-directional DC/DC converter

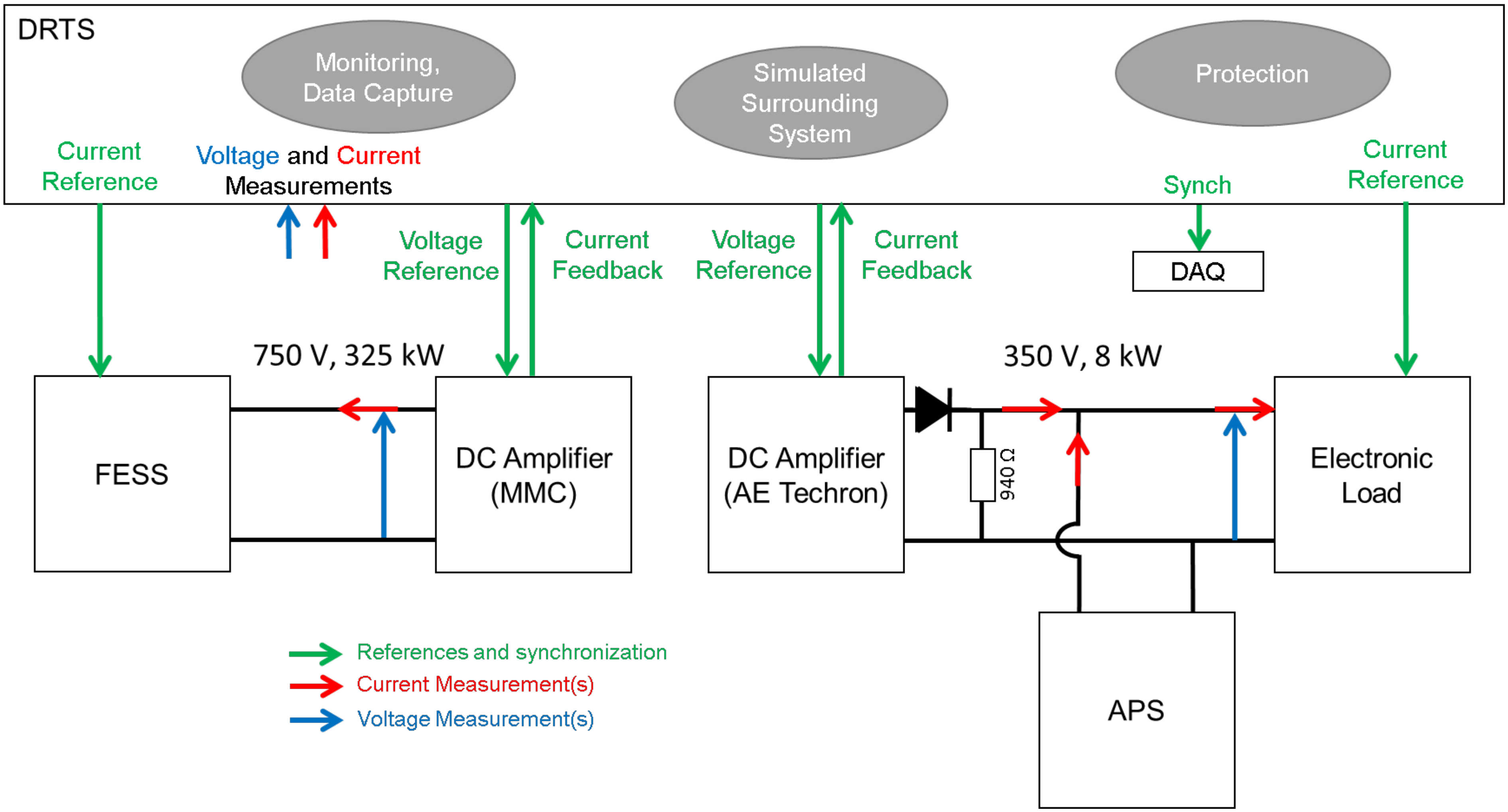
Linking FESS and APS via PHIL (Dual-PHIL)



* Bi-directional

** Filter removed when Virtual Capacitor Controls are used

Test Setup


DRTS
Monitoring, Data Capture
Simulated Surrounding System
Protection
Current Reference
Voltage and Current Measurements
Synch
Current Reference
Voltage Reference
Current Feedback
Voltage Reference
Current Feedback
DAQ
750 V, 325 kW
350 V, 8 kW
FESS
DC Amplifier (MMC)
DC Amplifier (AE Techron)
940 Ω
Electronic Load
APS
References and synchronization
Current Measurement(s)
Voltage Measurement(s)

System Capacitance Reduction via APS

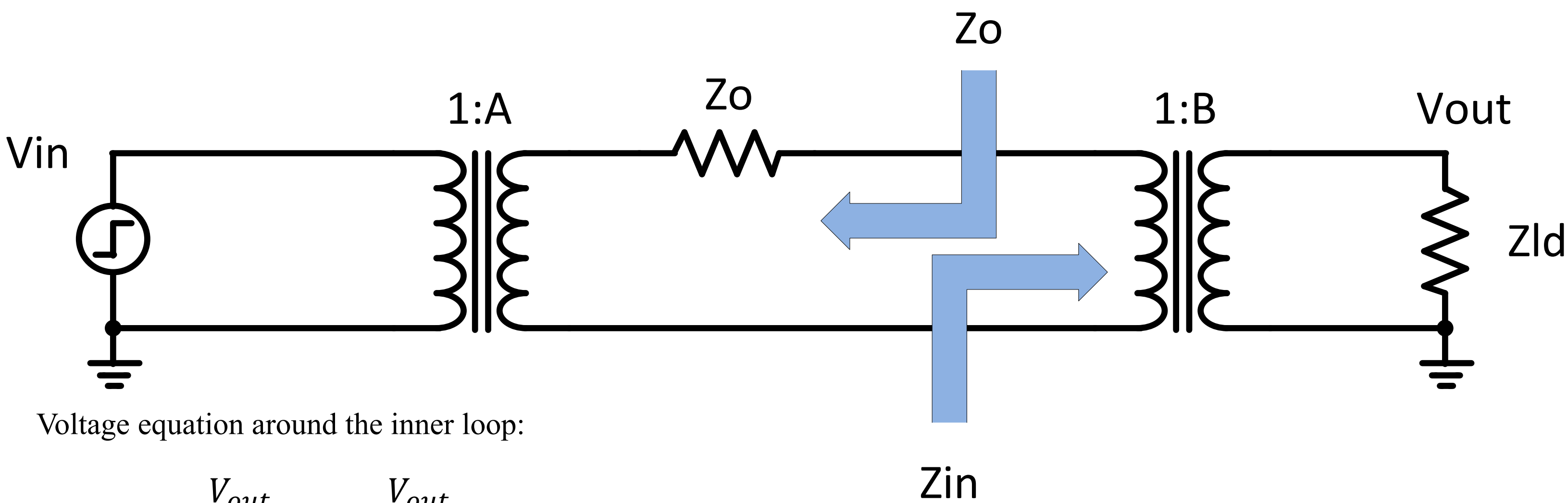
- **Background**
  - Without the APS, the 750 V bus requires C = 0.5 F to keep voltage within acceptable limits
- **Demonstration**
  - Reduce overall capacitance with APS' optimized useable energy storage
  - Modified the APS controls to provide a **Virtual Capacitance** characteristic
    - Appears much larger than physical capacitor as APS allows much large voltage swing
    - Translated to 750 V side, the total "physical" capacitance was
      - 0.1 F simulated on AFE side
      - 0.046 F in real on APS side
    - Reduction to 0.146 / 0.51 = **28.6% of original value**

      (includes 350 V bus capacitance which looks like 10 mF on 750 V bus)
  - Dynamic testing to examine dynamic behavior

Interface Stability Assessment - Motivation

Notional Multiple Stage System:

Transformers’ turns ratio represent the DC conversion ratios of power converters



Voltage equation around the inner loop:

$$V_{in}A - \frac{V_{out}}{Z_{ld}}BZ_o = \frac{V_{out}}{B}$$

$$\frac{V_{out}}{V_{in}} = \frac{AB}{(1 + \frac{B^2 Z_o}{Z_{ld}})}$$

$$\frac{V_{out}}{V_{in}} = \frac{AB}{(1 + \frac{Z_o}{Z_{in}})}$$

- Prior to connecting subsystems **– determine if stable standalone systems will remain stable when integrated**.
- For DC/DC Converters (constant power loads) Z_{in} is negative.
- If the magnitude of Z_{in} is equal to the magnitude of Z_o and if the angle of Z_o/ Z_{in} equals $\pm 180^\circ$, then the denominator goes to zero and the transfer function goes to infinity, resulting in an unstable condition

- **Even if the magnitudes of Z_o and Z_{in} are equal, stability can still be maintained as long as the phase of Z_o/Z_{in} is not close to +180° or –180°**

Interface Stability Assessment – PHIL Specific Considerations

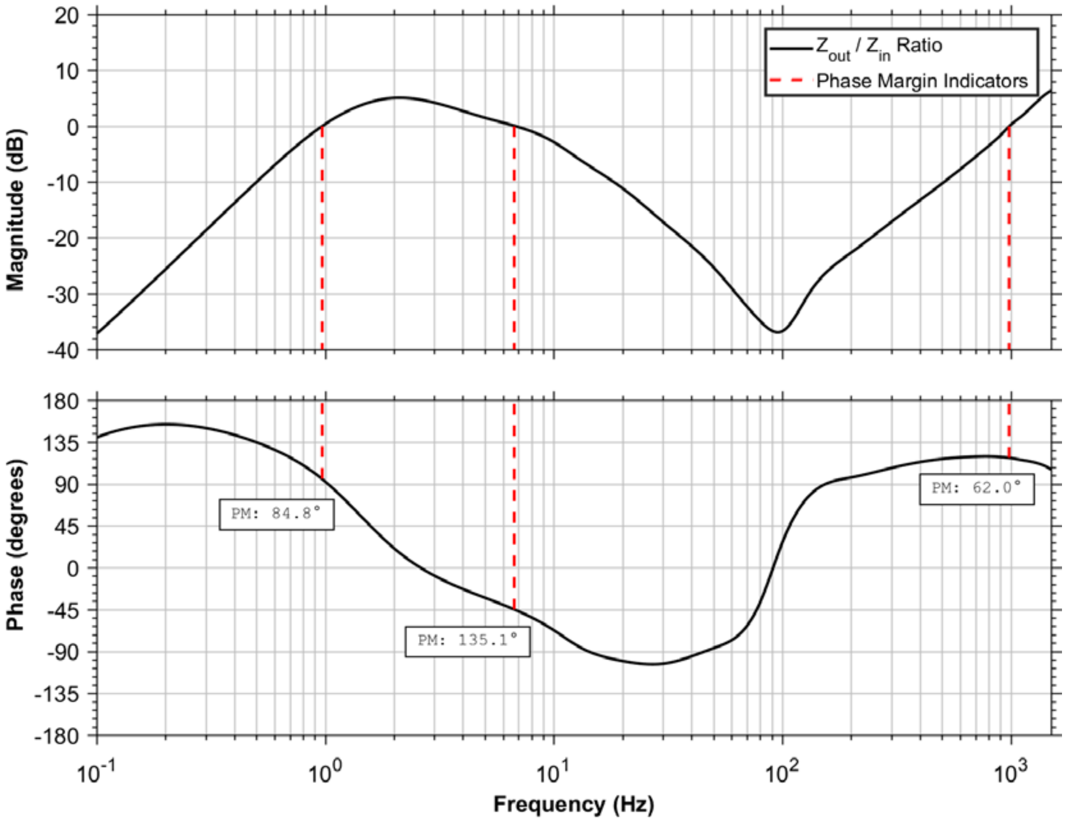
- Dual PHIL configuration has additional stability considerations due to:
  - Additional DRTS phase delays associated with
    - Time step
    - I/O communication
    - Computer processes
  - Response and impedance of the DC amplifiers

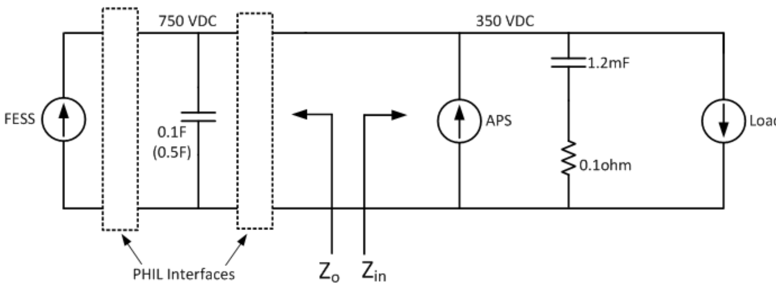
- Could result in interface instability regardless of individual subsystem stability

- Z_o and Z_{in} need to be determined by test, not solely by simulation
  - Difficult to accurately model the phase loss and impedances resulting from the DRTS and DC amplifier

Interface Stability Assessment , including the effects of the PHIL, must be performed prior to integrating the system.

Interface Stability Assessment – Dual PHIL Configuration Measurements





Z_o impedance measured into the PHIL interface
Z_{in} impedance looking into the APS

Phase Margin (PM) is determined where Z_o/Z_{in} is equal to 1 (0 dB)

$$PM = 180° - \left| angle\left(\frac{Z_o(s_c)}{Z_{in}(s_c)}\right) \right|$$

where s_c is the frequency (in rad/s) at which the magnitude of Z_o/Z_{in} is equal to 0 dB.

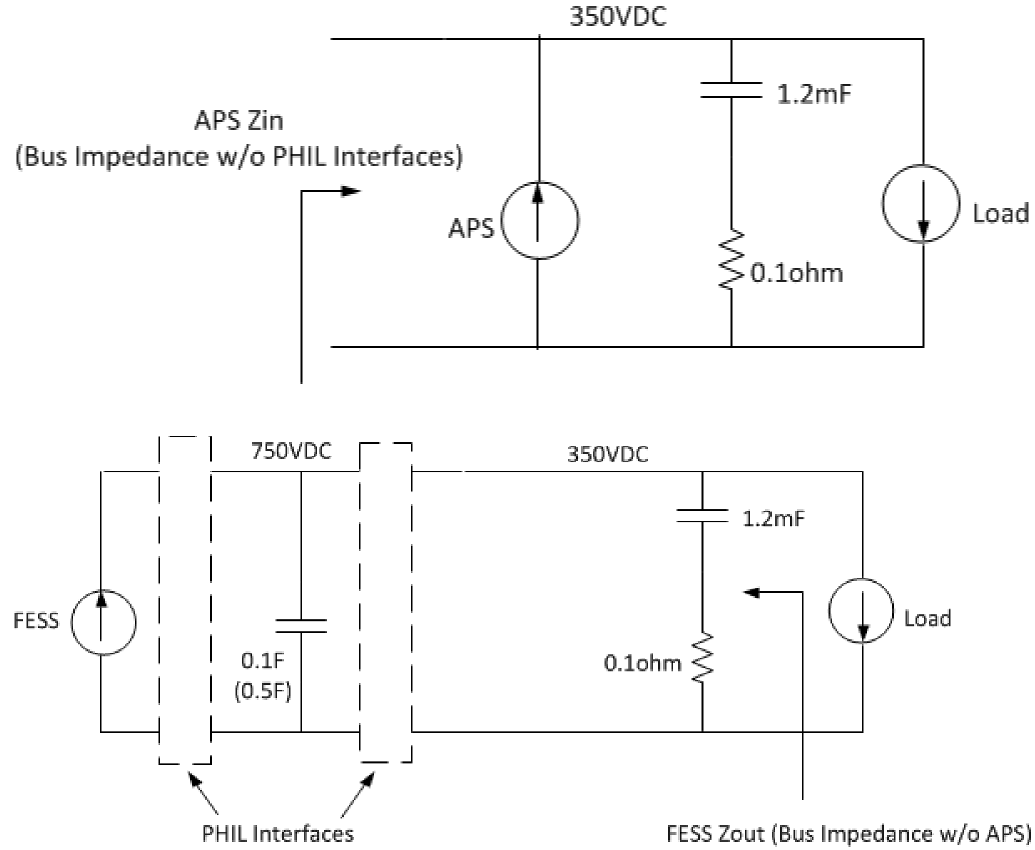
Conditions:
- 0.5 F bus capacitor
- Dual PHIL delays minimized by optimizing DRTS I/O configuration

Additional measurements verified interface stability for the bus capacitor equal to 0.1 F.

Resulting minimum phase margin is 62°, ample phase margin to proceed with integrating FESS and APS

Subsystems Bus Impedance

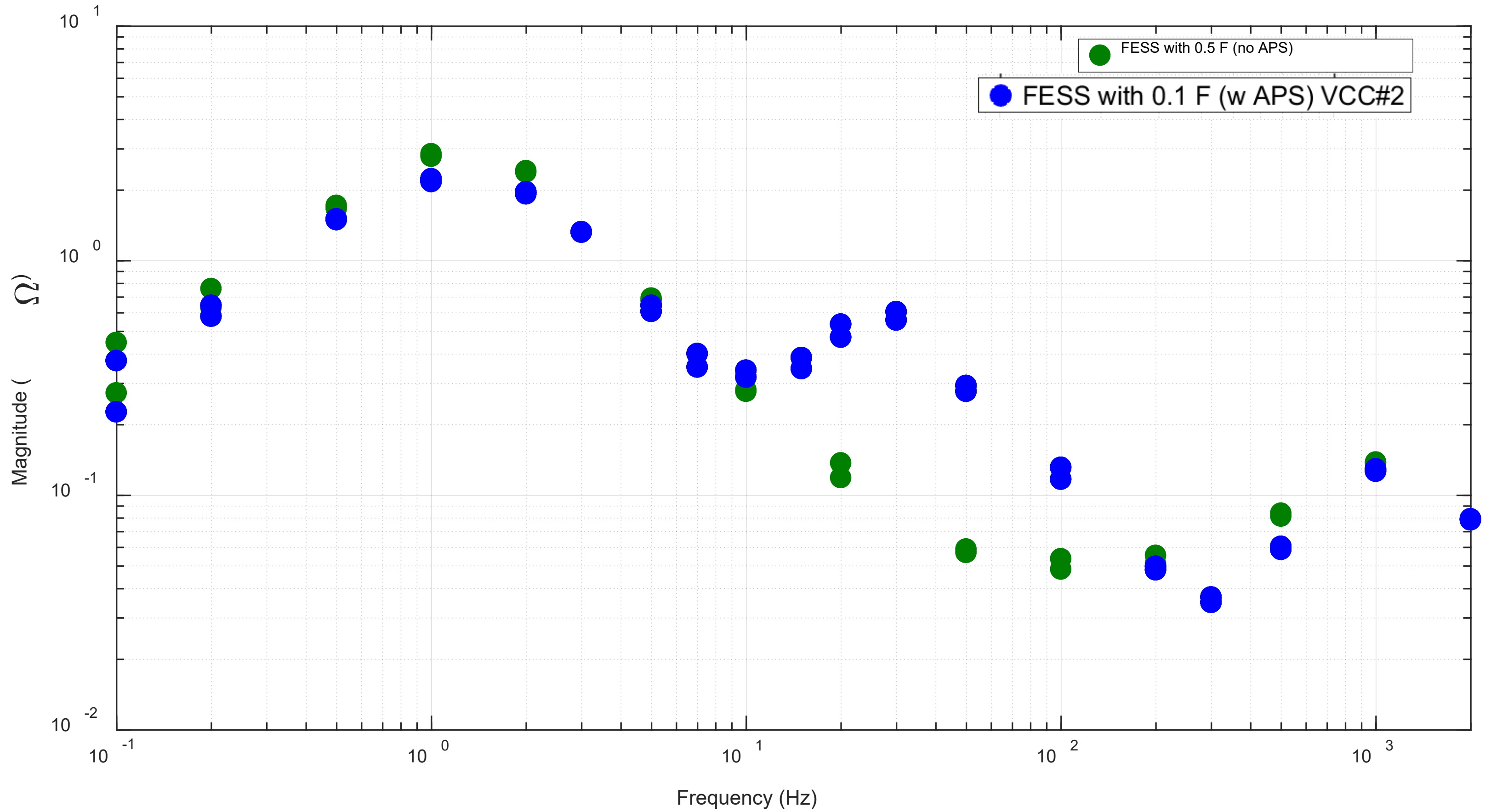
- Insight into system performance can be gained by examining the bus impedance curves
  - Explains which subsystem (FESS, APS, Bus Capacitance) provides the load demand for a given frequency
  - Provides indication of bus response for small signal disturbances

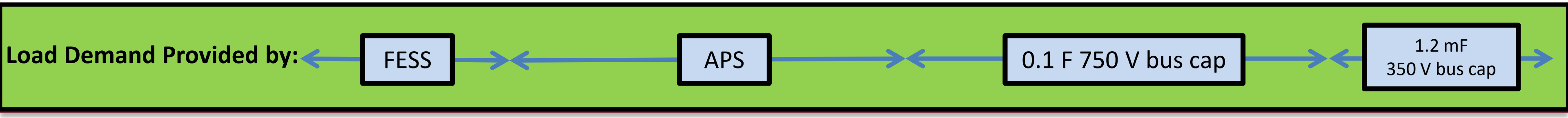


Because the subsystems are in parallel, the impedance curve values will be dominated by the subsystem with the lowest impedance for a given frequency range.

Bus Impedance (350 V side) with/without APS

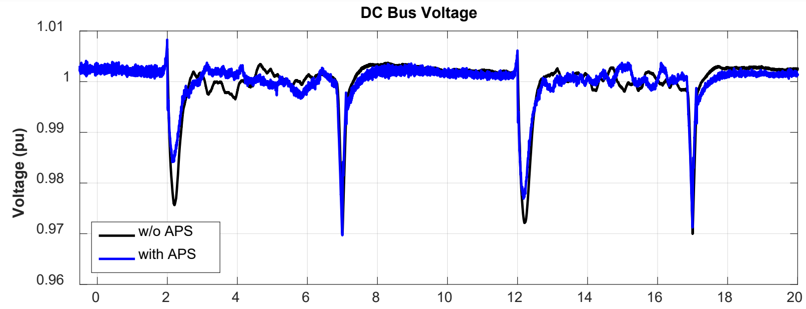
Bus Impedance without the APS, 0.5 F bus capacitor
Bus Impedance with the APS, 0.1 F bus capacitor



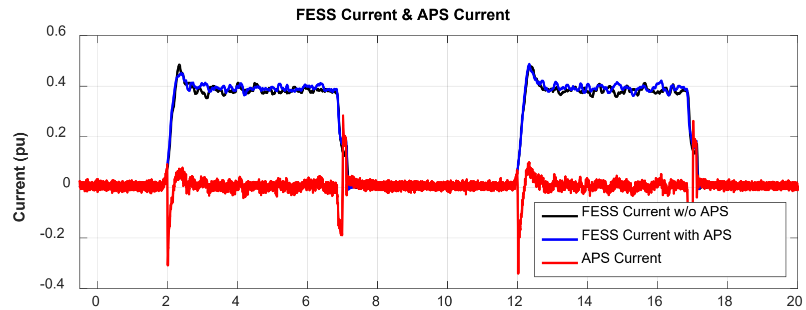


0.1 Hz Pulsed Load
(2 A to 13 A load step on 350 V side)

Normalized 750 V bus
- FESS with 0.5F + no APS
- FESS with 0.1F + APS

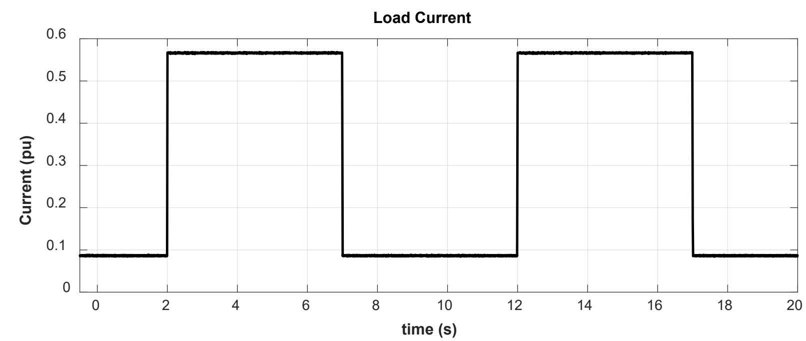


- FESS Current w/o APS
- FESS Current with APS
- APS Current



The FESS provides the low frequency load demand while the APS provides the higher frequency components of the load.

Load Current Profile



With APS, bus capacitance reduced from 0.5 F to 0.1 F, still achieving similar bus-voltage response, total system capacitance reduced by a factor of 3.5

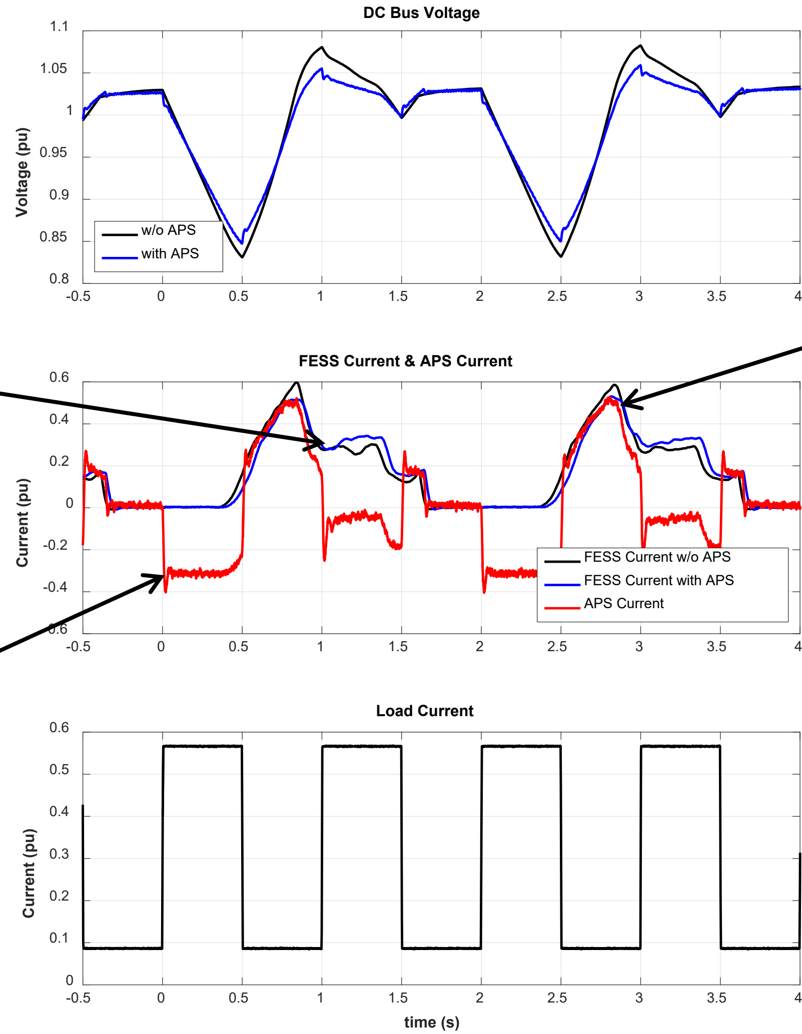
1.0 Hz Pulsed Load
(2 A to 13 A on 350 V side)

Normalized 750 V bus
- FESS with 0.5 F + no APS
- FESS with 0.1 F + APS

FESS is only providing energy every other load pulse

APS provides current, FESS does not

Load off, APS absorbs FESS current



- FESS Current w/o APS
- FESS Current with APS
- APS Current

Load Current Profile

With APS, bus capacitance reduced from 0.5 F to 0.1 F, still achieving similar bus-voltage response, total system capacitance reduced by a factor of 3.5

Results

- ✓ Successfully integrated APS and FESS as hybrid energy system
  - ✓ Combining long- and short-term energy
- ✓ Successful integrated two hardware systems of this size and incompatibility via dual Power Hardware-In-the-Loop (PHIL) interfaces.
- ✓ APS reduces overall system capacitance by more than a factor of 3
  - ✓ Potential size and weight benefits for a shipboard application.

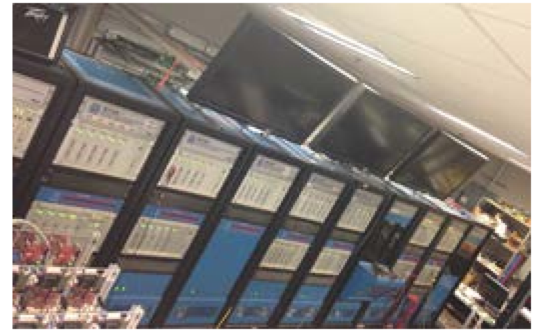
Potential Future Work

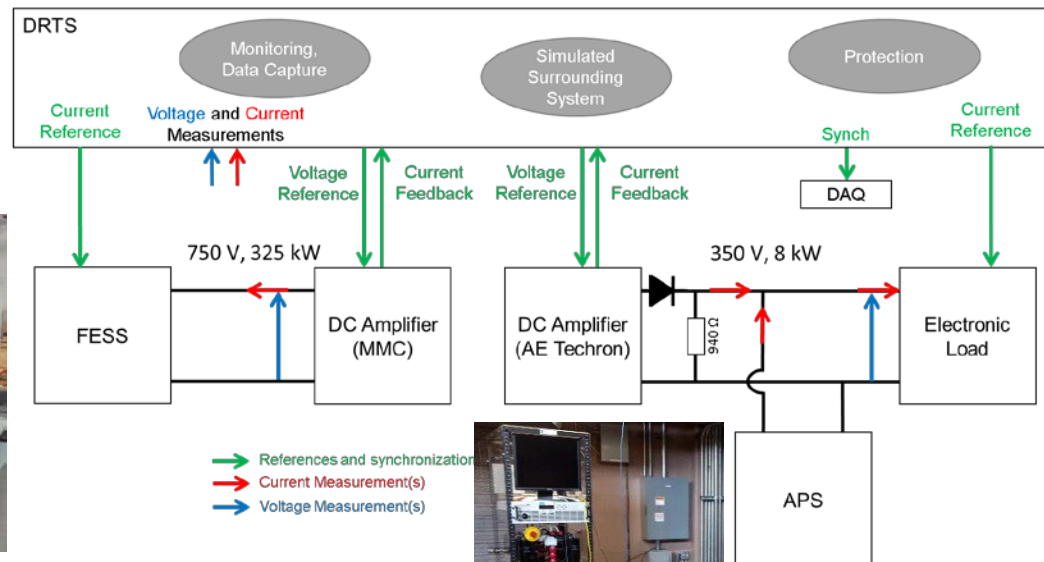
- Perform Dual PHIL testing on other energy storage systems with the APS
- Investigate using the APS under bus fault conditions as the APS is an inherently current limited bus capacitance
- Investigate using the APS as a bus stabilizer to integrate loads with sources that would otherwise be incompatible
- Improve APS performance (further reduction in system capacitance, improved bus voltage response, or improved power filtering) by increasing the APS bandwidth using state-of-the-art controls and power electronics

Backup

Outline

- Introduction and Motivation
- Dual-PHIL Test Setup
- Interface Stability Assessment
- Bus Impedance Examination
- Dynamic Test Results
- Conclusion

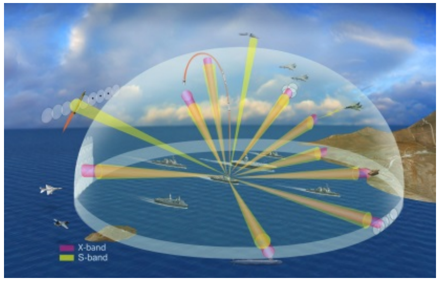




Introduction and Motivation

- Large pulsating loads on not-so-distant horizon for surface combatants
  - Lasers
  - Electromagnetic railguns
  - Unmanned vehicle launchers
  - Electromagnetic sensor systems
  - Electromagnetic countermeasures
  - Radars
- Power requirements for multiple pulsating loads (100s of kW to MW) will pose problems for non-IPS ships
- Short-term power consumption may exceed power delivery capability of the plant
- Shared energy storage may support
  - High power (beyond generation capacity) for short duration
  - High ramp rates
  - Power quality and continuity to critical loads

Electric Weapons



Electronic Sensors

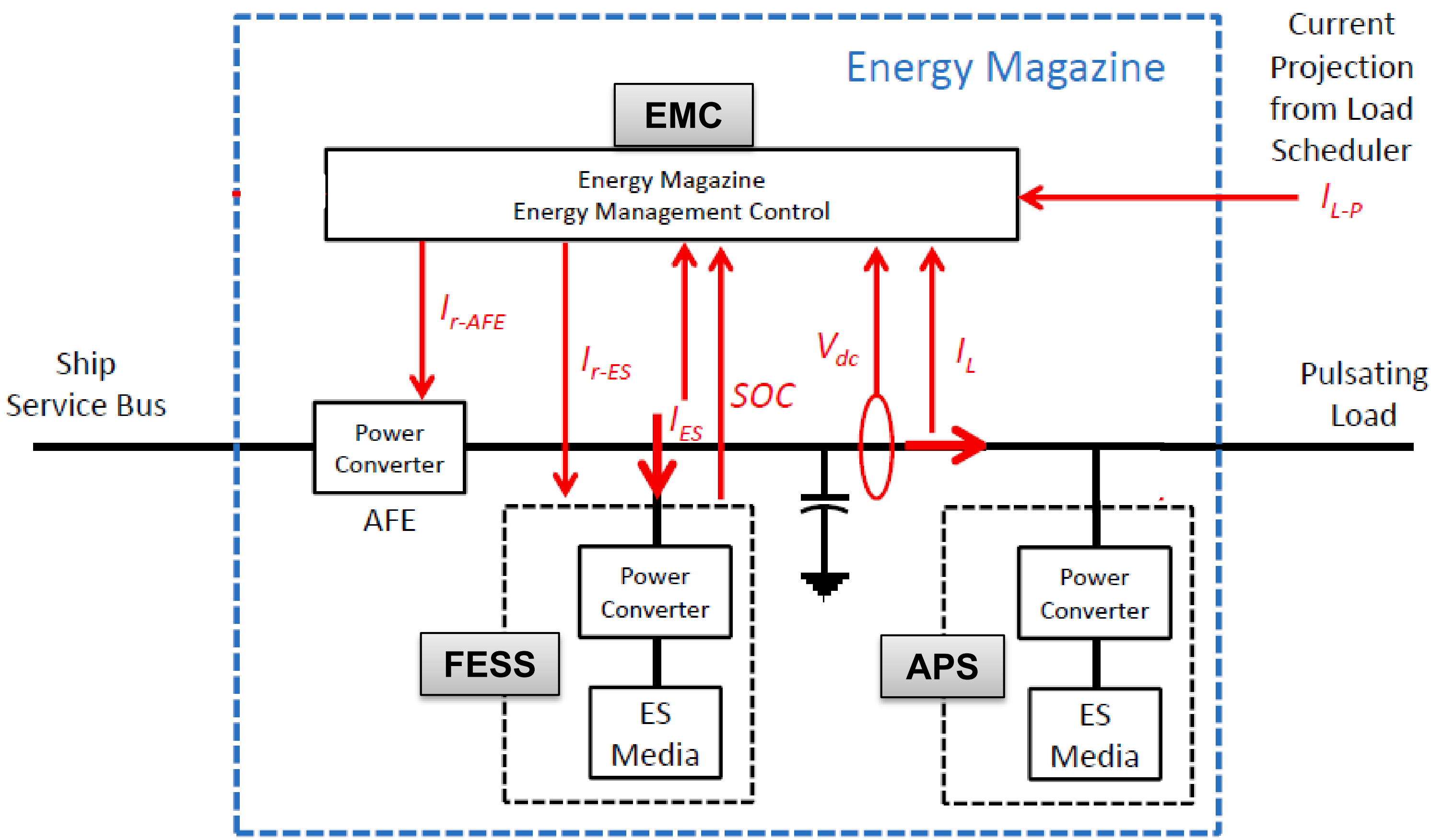
Electronic Countermeasures

Background and Goals

- Flywheel Energy Storage System (FESS)
  - Provides large amounts of energy for a long period of time
  - Cannot quickly respond to load demands
- Adaptive Power System (APS)
  - Can quickly support load demands
  - Cannot sustain high energy levels for a long period of time
- FESS and APS provide complementary functions, ideal for creating a high-performance hybrid energy system

- Create a hybrid energy storage system using the Flywheel Energy Storage System (FESS) and the Adaptive Power System (APS) and evaluate performance.
- Successfully demonstrate the dual Power-Hardware-In-the-Loop (PHIL) capability
  - Two hardware subsystems with incompatible interfaces integrated using the dual PHIL interfaces
    - FESS: 750 VDC, 320 kW
    - APS: 350 VDC, 8 kW
- Demonstrate the reduction in total system capacitance by using the APS in place of the FESS bulk bus capacitance.

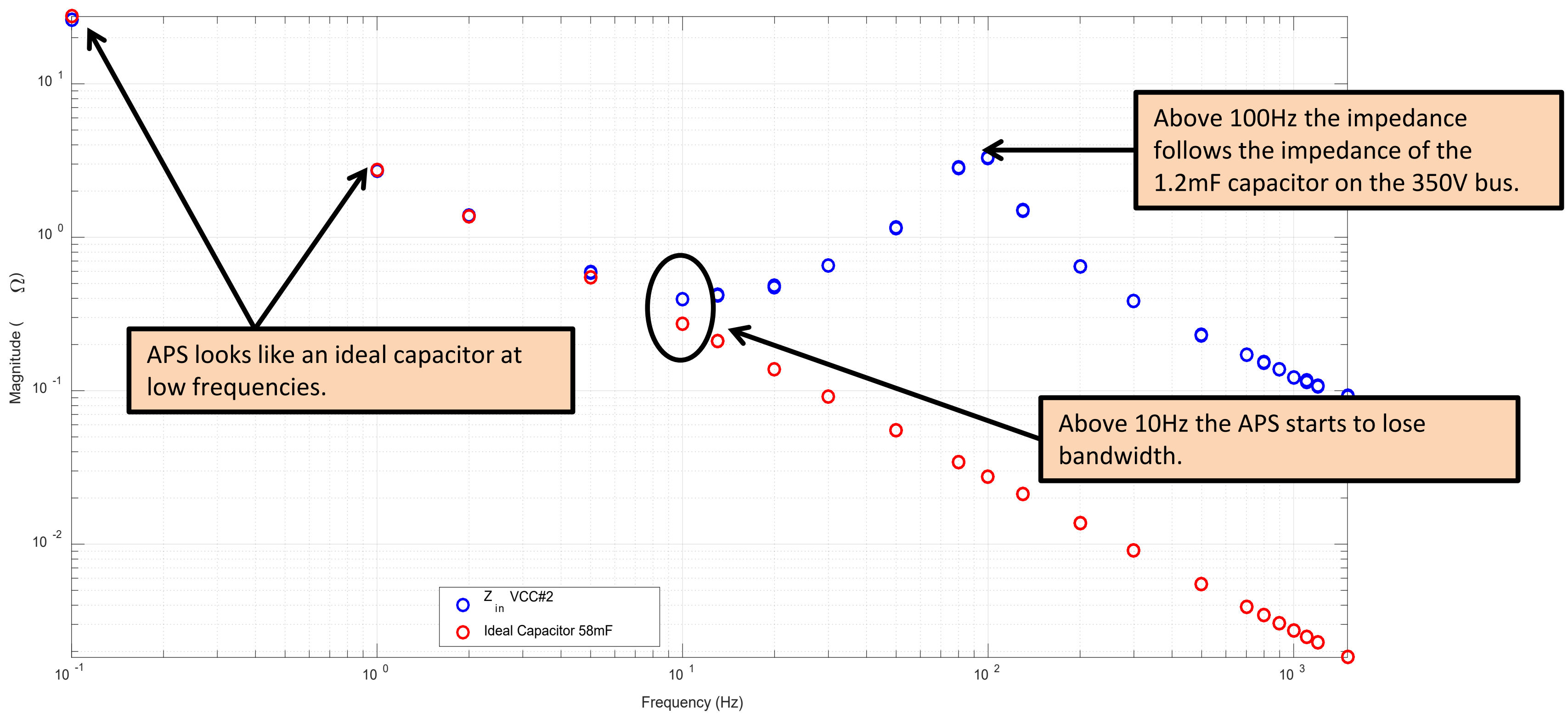
Energy Magazine with EMC, FESS and APS



APS Input Impedance vs. Ideal Capacitor (Virtual Capacitor Controls #2)

O APS Input Impedance (Bus Impedance w/o the FESS/PHIL interfaces)

O Impedance of an ideal 0.058F capacitor (0.5F on FESS side)

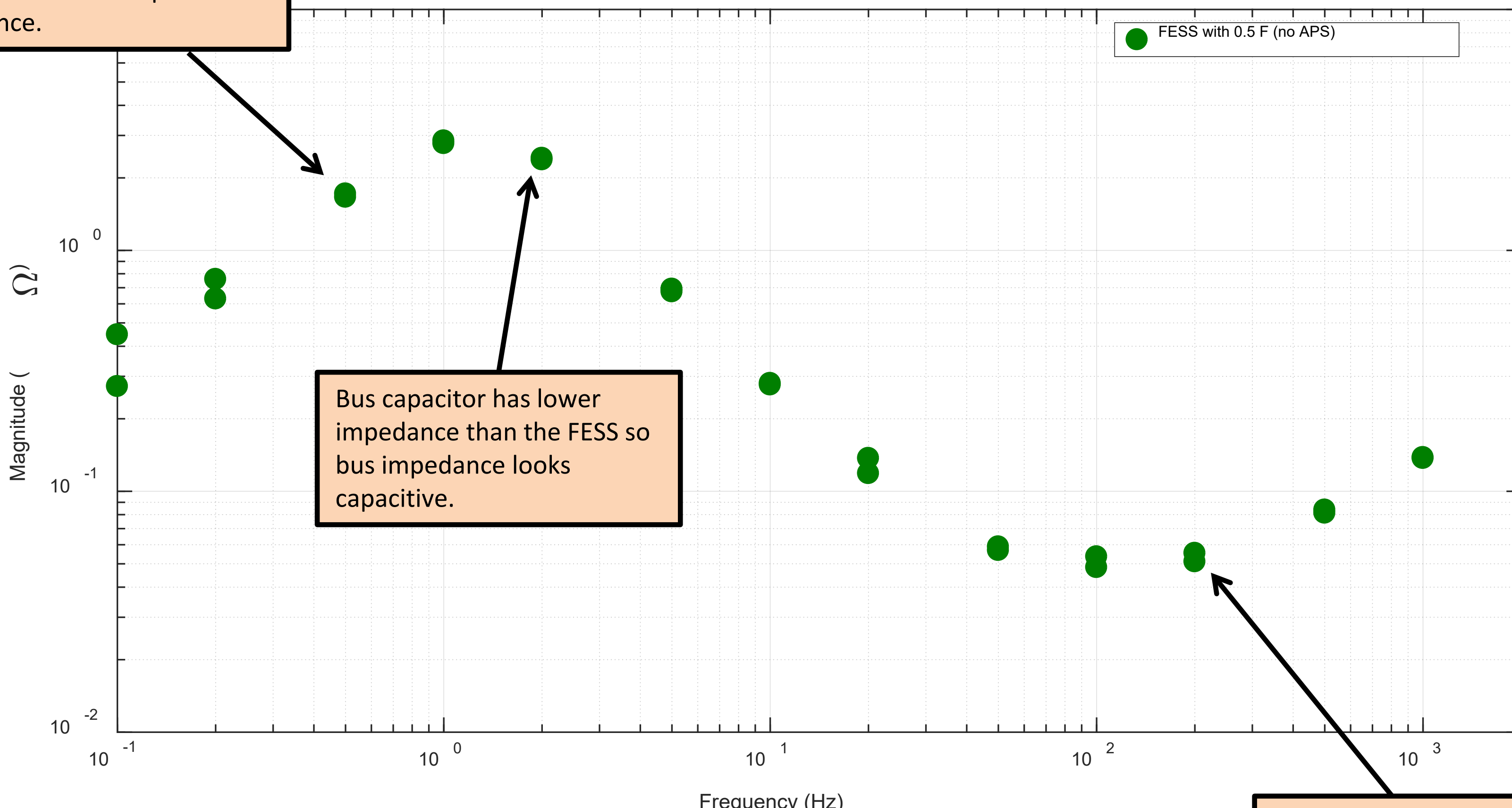


APS Control Loops have been modified to emulate a Virtual Capacitor (APS input impedance is determined by its controls)

Bus Impedance (350V side) without APS

FESS is losing BW but provides the load demand at very low frequencies since its impedance is smaller than bus capacitor impedance.

Bus Impedance without the APS, FESS capacitance = 0.5F
FESS in Discharging State



Bus capacitor has lower impedance than the FESS so bus impedance looks capacitive.

Bus impedance looks capacitive until cable inductance impedance is larger than capacitor impedance.

For frequencies less than 1 Hz the FESS provides the load demand.

System Capacitance Reduction via APS

Goal: Determine if the APS can reduce overall system capacitance (want to reduce the total volume of capacitance in system → 750-V bus capacitance + APS energy storage)

Background: Without the APS, the 750-V bus requires 0.5 F of capacitance to hold up bus due to FESS's slow slew rate

- ❑ To provide demonstration,
    - Reduced APS usable energy storage capability
    - Modified the APS controls to provide a **Virtual Capacitance** characteristic
        - The virtual capacitor looks much larger than the physical capacitance due to the intentional larger voltage swing on the APS physical capacitors.
- ❑ The 0.5-F capacitance on the FESS 750-V bus was then reduced to 0.1 F with the reduced energy-storage APS online. The APS reduced energy-storage capacitance is equivalent to 0.036 F of capacitance on the 750-V FESS side, resulting in a total system capacitance of 0.136 F.
- ❑ In the following slides the response with the 0.1-F capacitance with the reduced energy-storage APS is compared with the 0.5-F capacitance with FESS.

Voltage Response Comparison:

FESS with 0.5 F Bus Capacitor
versus
FESS with 0.1 F Bus Capacitor + APS online

Two key system parameters to measure APS performance:

1. Amount of reduction in system capacitance

2. Bus-voltage response (min/max bus voltage)
   - Must maintain similar or better bus-voltage response when compared to FESS with 0.5 F bus capacitance without the APS

Observations

- Successful integration of APS and FESS as hybrid energy storage system
  - APS provided fast dynamic energy
  - FESS provided slow dynamic energy
- APS reduced total capacitance by factor of 3.5
- Further performance improvement can be made
  - Enhanced FESS controls that minimize delays
    - External load projection could not entirely eliminate FESS control delays
  - Increase APS bandwidth
    - Emulate capacitor up to higher frequencies
    - Could improve total capacitance reduction by up to a factor of 6