Advanced Power Electronics Designs – Reliability and Prognostics

(Keystone Project 1)

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National Renewable Energy Laboratory
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DOE Vehicle Technologies Program
2022 Annual Merit Review and Peer Evaluation Meeting

ELT218

Overview

Timeline

- Project start date: FY 2019
- Project end date: FY 2024
- Percent complete: 70%

Barriers

- Barriers addressed
  - Cost
  - Performance
  - Reliability and lifetime

Budget

- Total project funding: $700,000
  - DOE share: $700,000
- Funding for FY 2021: $175,000
- Funding for FY 2022: $175,000

Partners

- Interactions/collaborations
  - Oak Ridge National Laboratory (ORNL)
  - Indiana Integrated Circuits (IIC)
  - DuPont
- Project lead
  - National Renewable Energy Laboratory (NREL)

Relevance

- Wide-bandgap (WBG) packaging designs must thermally allow for:
  - Higher operating temperatures
  - Higher heat fluxes/power densities
  - Hot spots
- Coefficient of thermal expansion (CTE) mismatch between layers of the module will impose stresses that can initiate and propagate defects:
  - Attach layer fatigue
  - Interconnect fatigue
- **New package designs must address thermal and reliability concerns and be evaluated under accelerated conditions that approximate real-world conditions.**

Milestones

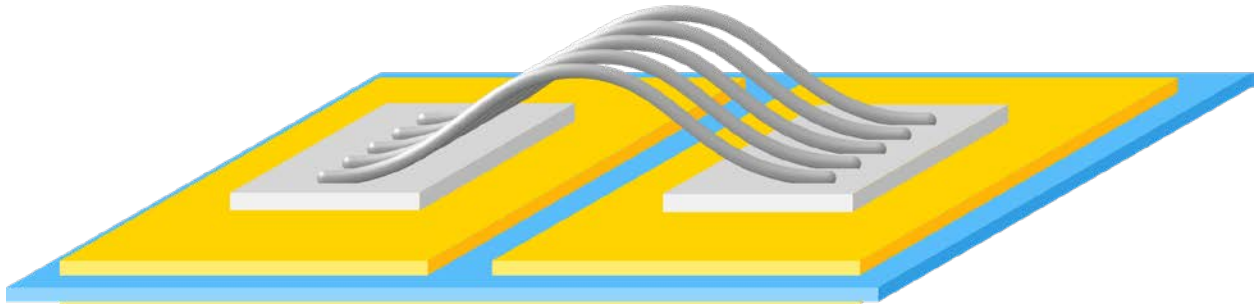
Date/Status	Description
September 2022 *(in progress)*	Milestone • Characterize devices/packages under thermal and vibration conditions and monitor component health through electrical precursor measurements and nondestructive characterization techniques.

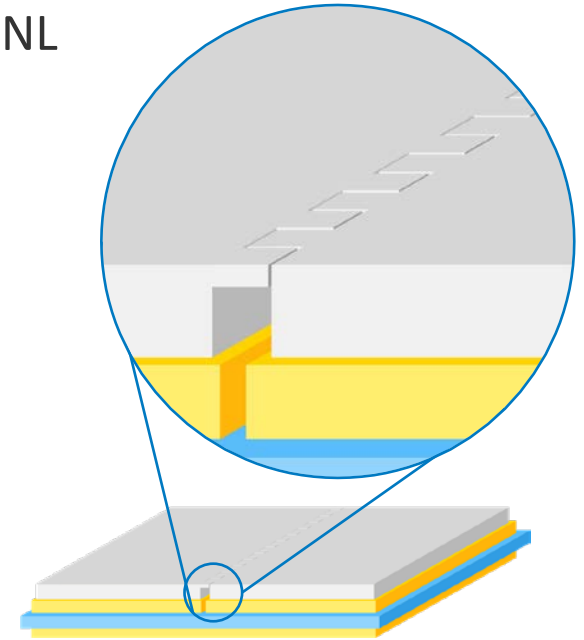
Approach

- **New package designs must address thermal and reliability concerns and be evaluated under accelerated conditions that approximate real-world conditions**
- NREL is closely working with ORNL and industry partners to evaluate new packaging materials and manufacturing techniques for WBG-based traction inverters
  - IIC: Quilt packaging via a chip-to-chip edge interconnect technology
  - DuPont: Organic direct-bond copper (ODBC) substrate as a replacement for ceramic substrates.

Approach

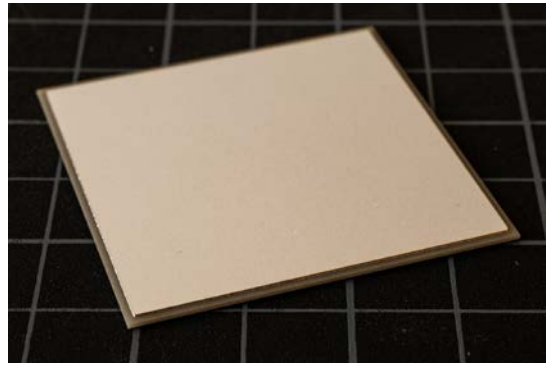
- Alternative interconnect designs are required as devices are reduced in size and spacing between devices is minimized.
- **Traditional wire interconnects or etched substrates for topside electrical connections will be replaced with direct chip-to-chip connection.**
- Devices are joined with quilt packaging, eliminating the need for wire bonds or other external electrical connection technology
  - Experimental samples have been designed in collaboration with IIC and ORNL
  - Reliability evaluation of first round of samples was completed at NREL.



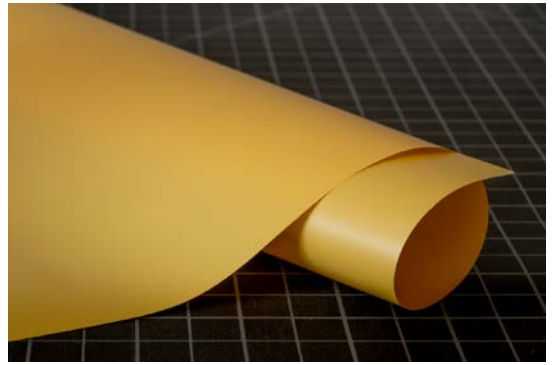


Approach

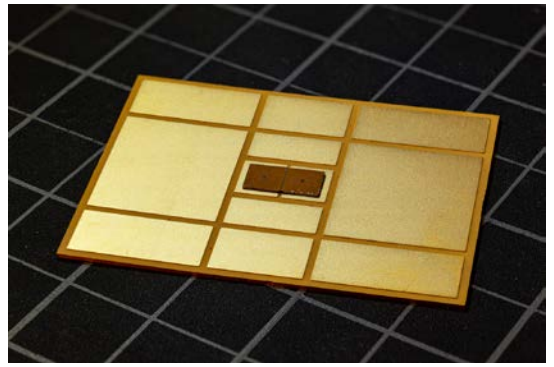
- **Alternative electrically insulated substrate designs are required to enable reliable packages that operate with higher power densities and higher temperatures**
- Traditional metalized ceramic substrate technologies:
  - Direct-bond copper (DBC)
    - Oxidation of copper (Cu) foils during bonding lowers melt temperature from 1,083°C to 1,065°C
    - Maximum metallization thickness of 1 mm
    - Must have metallization layers on both sides of the ceramic
    - Examples include aluminum oxide (Al_2O_3), aluminum nitride (AlN), and zirconia (ZrO_2)-doped high-performance substrates (HPS).
  - Active metal bonding (AMB)
    - Brazing process with silver-copper (Ag-Cu) alloy between Cu and ceramic at 850°C in vacuum
    - Requires more processing steps and is more expensive than DBC
    - Silicon nitride (Si_3N_4) substrate is an example.
- ODBC
  - A polyimide dielectric is bonded with metal through elevated temperature and pressure
  - No limitations in metal material or metallization thickness
  - Maintains electrical and thermal performance after 5,000 thermal shock cycles (−40°C to 200°C, 5-minute dwells).



Traditional substrate



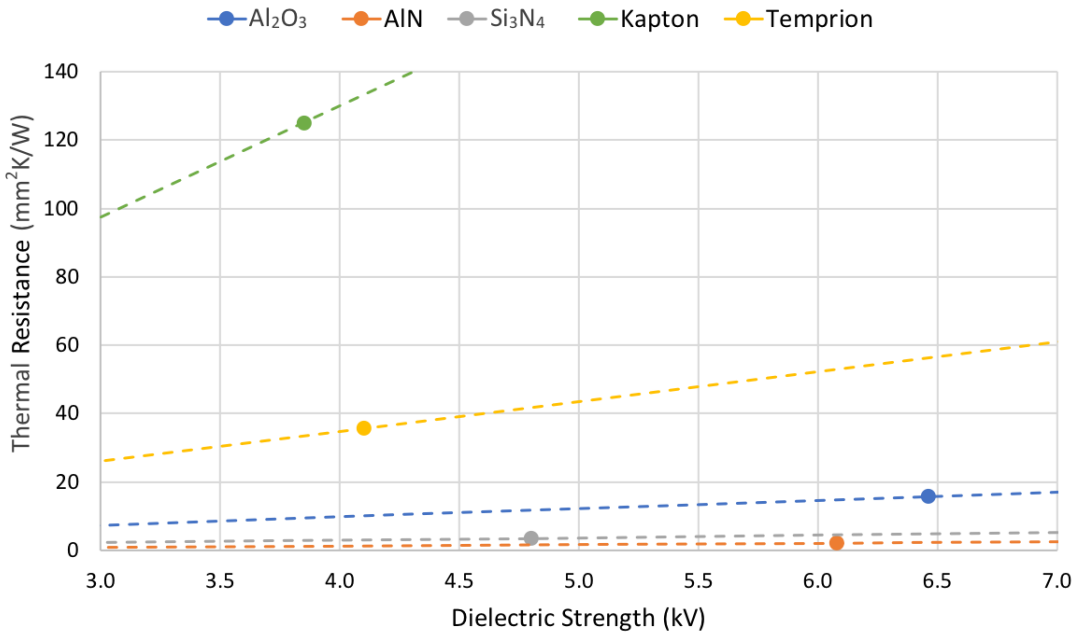
DuPont Temprion polyimide film



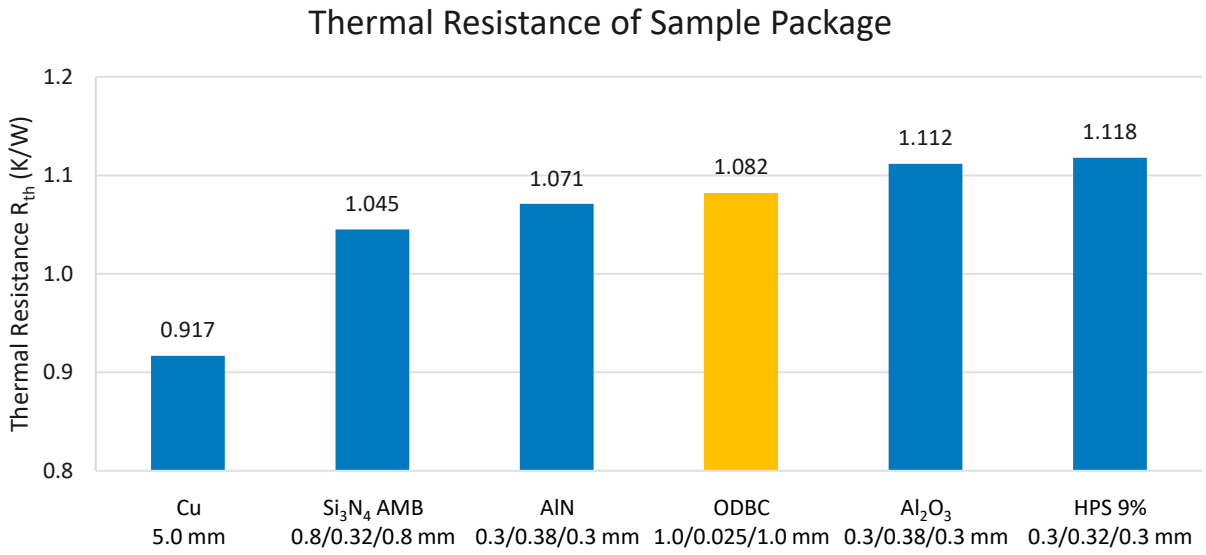
DuPont ODBC substrate

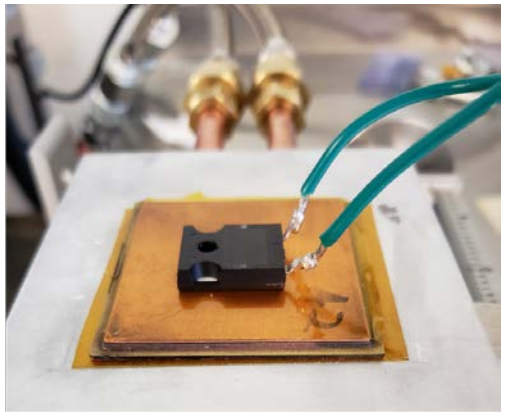
Approach

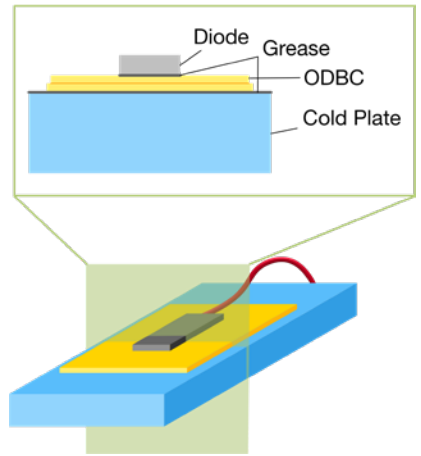
- Lower thermal conductivity of Temprion is offset by thicker topside metallization.



Insulator	Thickness (µm)	Dielectric Strength (kV/mm)	Dielectric Strength (kV)	Thermal Conductivity (W/[m·K])	Thermal Resistance (mm^2K/W)
Al_2O_3	380	17	6.5	24	16
AlN	380	16	6.1	180	2
Si_3N_4	320	15	4.8	90	4
Kapton	25	154	3.9	0.2	125
Temprion	25	164	4.1	0.7	36







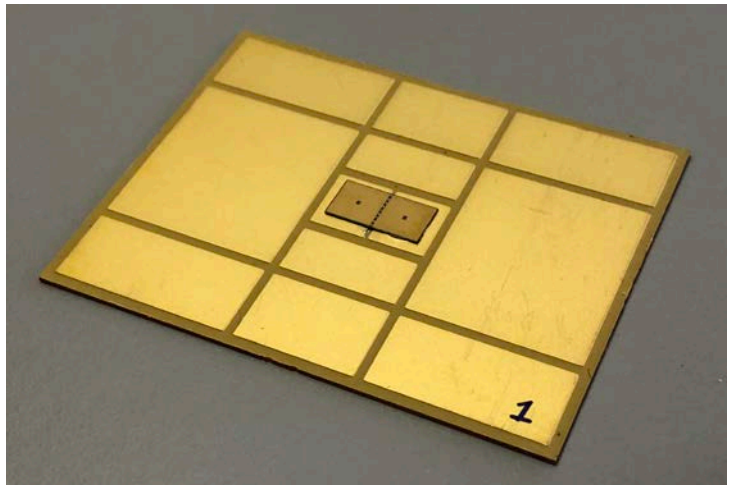
T3ster test setup

Technical Accomplishments and Progress

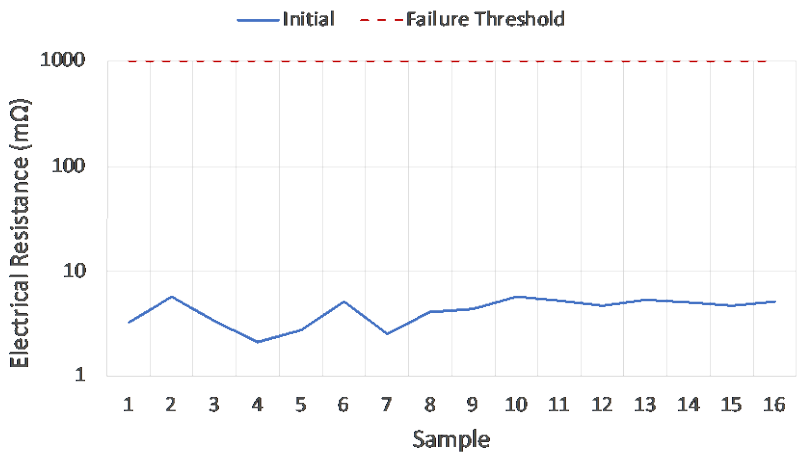
- Received next set of packages from IIC
- Wire bonds will attach dies to perimeter pads
- Samples will be characterized under accelerated power cycling, thermal cycling, and vibration conditions
  - Power cycling: 2 s on, 4 s off, current optimized for Δ60°C (AQG 324 QL-01)
  - Thermal cycling: −40°C to 150°C, 10°C/min ramp rate, 15-min soak, 1,000 cycles (JESD22-A104D)
  - Sinusoidal vibration: 20- to 1,000-Hz sweep, 5-g acceleration, 2-hour duration (IEC 60068-2-6).

IIC quilt packaging assemblies

Assembly No.	Nodule Anchor Length (µm)	Nodule Width (µm)	Accelerated Test
1	30/70	300	Power
2	30		Power
3			Thermal
4			Vibration
5	70		Power
6	30		Power
7	30/70		Thermal
8	70		Thermal
9		500	Power
10		700	Power
11		500	Thermal
12	30		Power
13	70		Vibration
14	30		Thermal
15		300	Thermal
16			Vibration



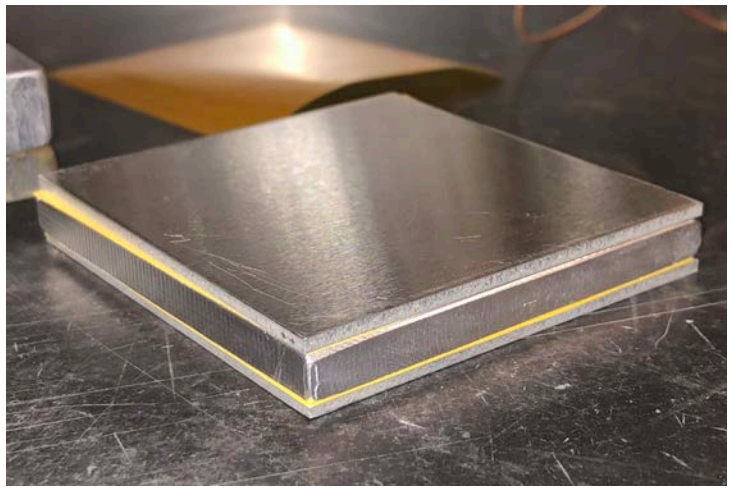
IIC package



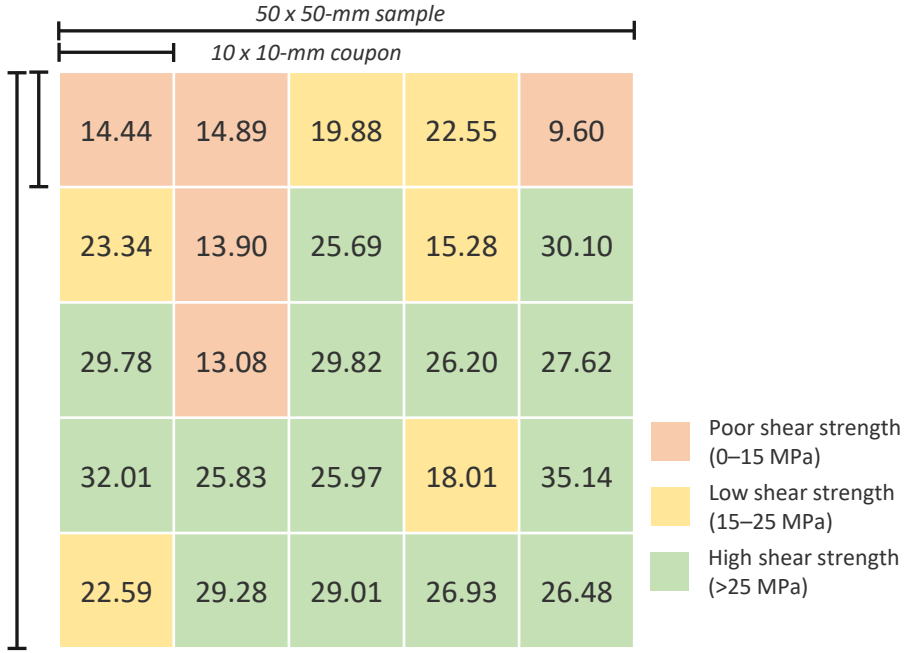
Nodule electrical resistance

Technical Accomplishments and Progress

- Completed bonding of ODBC and organic direct-bond aluminum (ODBA) samples for double-lap shear testing
  - Bonded ODBC samples at 250°C and 300°C
  - Bonded ODBA sample at 300°C
  - 50 × 50-mm samples were sectioned into 25 10 × 10-mm coupons for evaluation
  - 300°C ODBC coupons exhibited high shear strength, whereas ODBA and 250°C ODBC samples were weak
- Bonding in an inert atmosphere (N_2) and plating Al surfaces will improve bonding performance.



ODBA sample



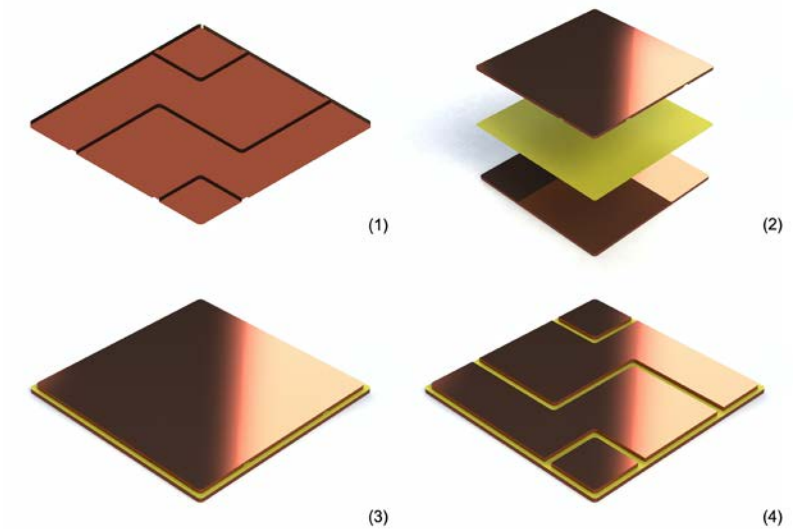
Shear strength (MPa) for ODBC 300°C sample

Shear fixture setup

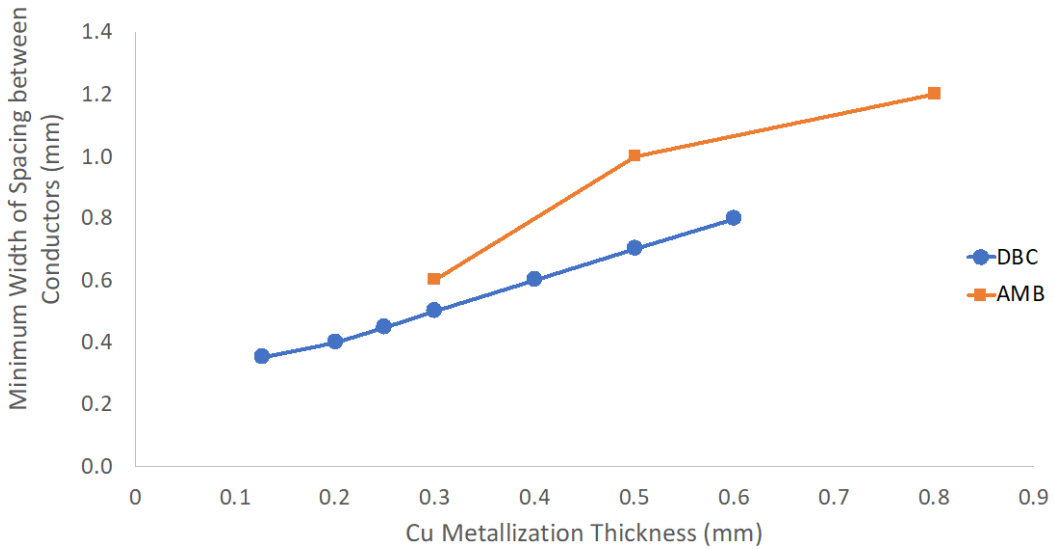
Technical Accomplishments and Progress

- The ability to bond thick copper metallization layers (1–1.5 mm) improves heat spreading directly below devices and lowers their junction temperatures
- Mechanical etching allows for fine width spacing (<1 mm) between conductor traces through thick metallization layers.

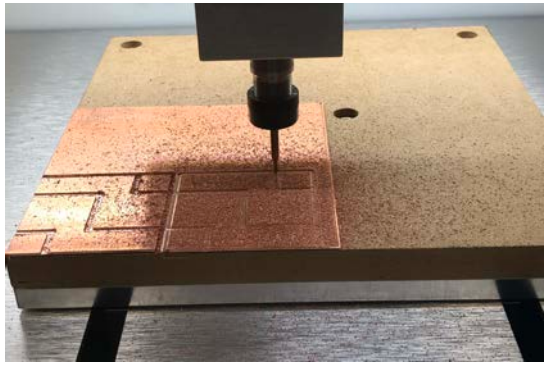
1. Mechanically etch bottom face of top metallization layer.
2. Assemble Temprion and metallization layers.
3. Apply temperature and pressure to substrate stack.
4. Mechanically etch top face of top metallization layer.



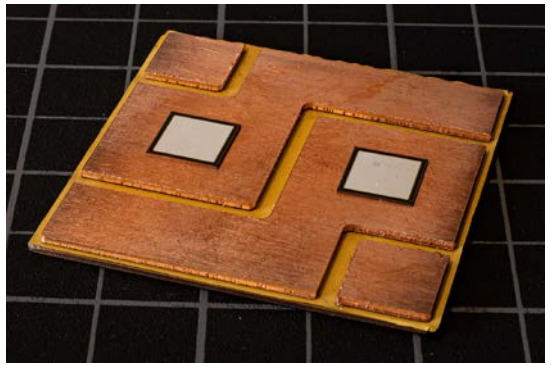
Substrate assembly process



Minimum width of spacing between conductors based on metallization thickness using chemical etching [1]



Machining process

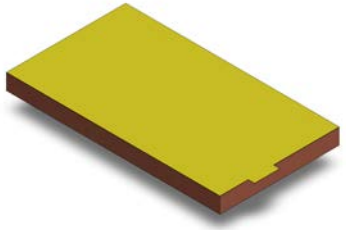


NREL prototype substrate

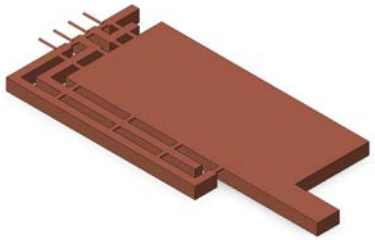
[1] Rogers Corporation. 2022. "curamik® Ceramic Substrates Technical Data Sheet." 2022. https://rogerscorp.com/-/media/project/rogerscorp/documents/advanced-electronics-solutions/english/data-sheets/technical-data-sheet-curamik-ceramic-substrates.pdf.

Technical Accomplishments and Progress

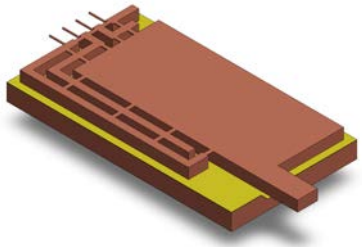
- Simplified packaging process has been envisioned with ODBC substrates in a double-side-cooled module.



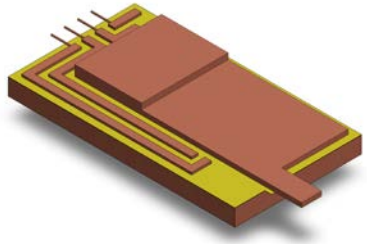
1. *Bond lower Temprion layer to lower cold plate.*



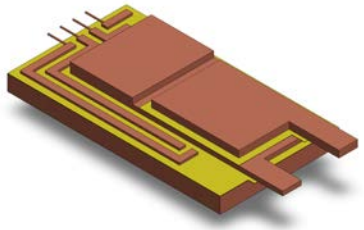
2. *Etch bottom face of drain busbar and traces.*



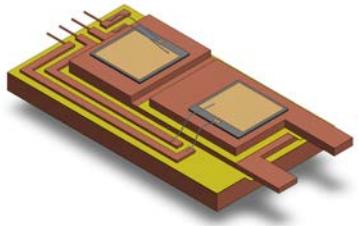
3. *Bond drain busbar and traces to lower Temprion layer.*



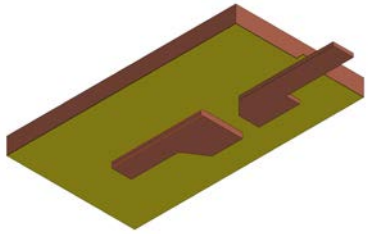
4. *Etch top face of drain busbar and traces.*



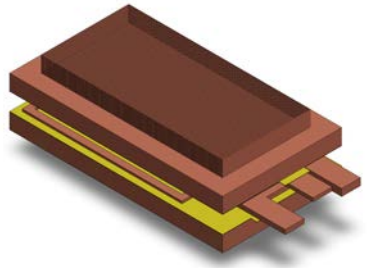
5. *Bond middle Temprion layer and output 2 busbar.*



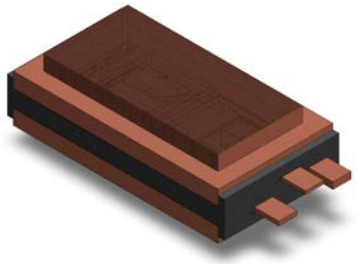
6. *Sinter and wire bond devices.*



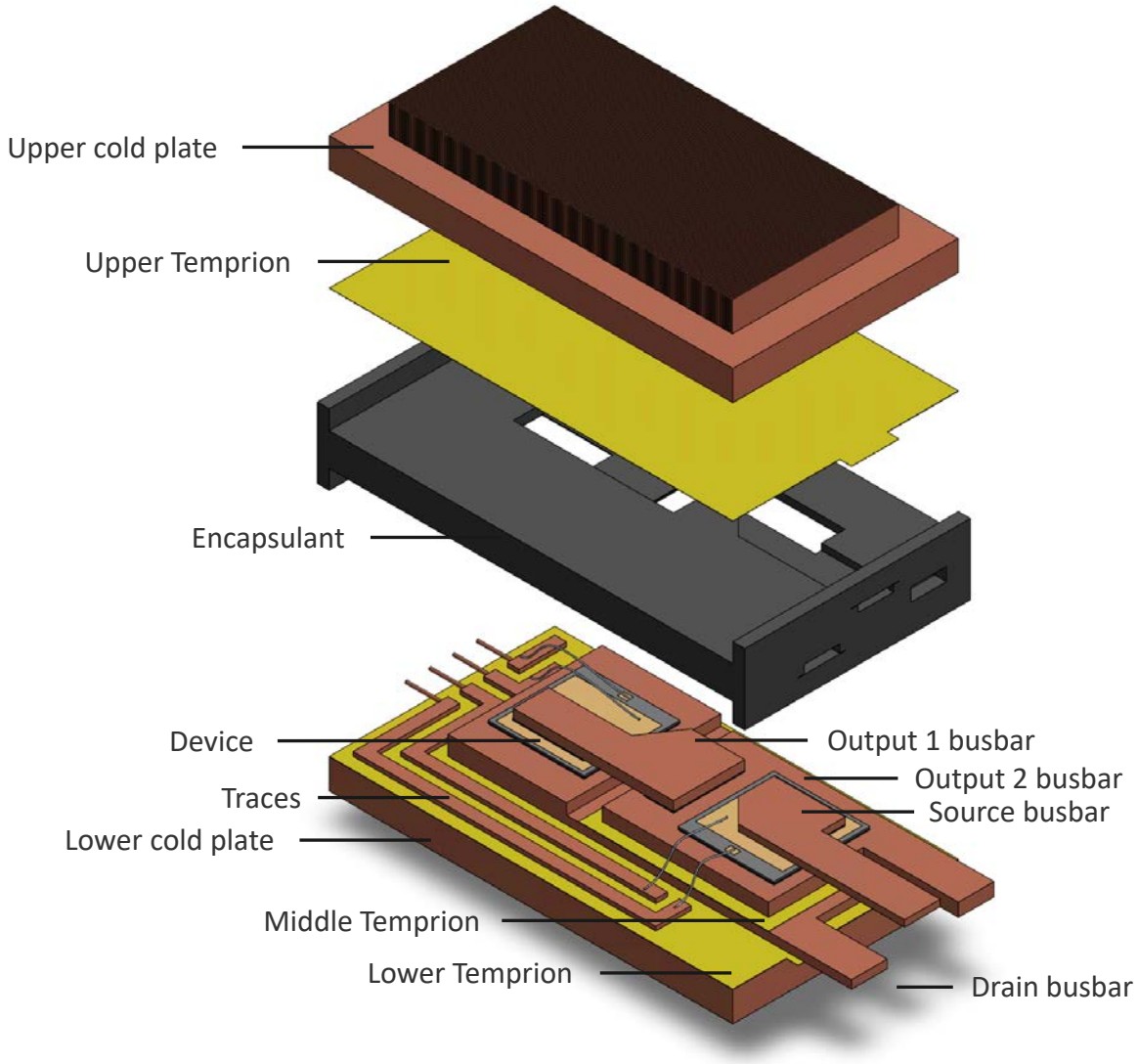
7. *Bond output 1 and source busbars to upper Temprion and upper cold plate.*



8. *Sinter previous assembly to devices.*



9. *Fill cavity with encapsulant.*



Responses to Previous Year Reviewers' Comments

The work is focusing on critical issues and new technologies that are needed. The reviewer would like to have seen this project take a broader look at interconnects, insulators, and conductors for power electronics.

As this project develops, the PI hopes to collaborate with additional companies that address other power electronics components.

The reviewer would like to see more involvement with vehicle OEMs.

IIC, DuPont, and this project's PI have presented to the U.S. DRIVE Electrical and Electronics Team (EETT) on these technologies, but additional interactions would be beneficial.

Sending out developed packages to industry with request to test these packages for a targeted application could accelerate commercialization of underlining technology.

The reviewer raises a good idea. Transitioning these packaging concepts to industry for commercialization is a critical goal. Sharing a development platform would enable a more rapid transfer of lessons learned to industry partners.

**Any proposed future work is subject to change based on funding levels.*

Collaboration and Coordination

- ORNL
  - Laboratory partner for electrical design of power electronics modules
- IIC
  - Industry partner for quilt packaging technology
- DuPont
  - Industry partner for ODBC technology.

Remaining Challenges and Barriers

- Thermal and reliability concerns of new electrical connect technology must be experimentally evaluated
  - Experimental characterization will be performed to evaluate nodule reliability under power, thermal, and vibration conditions
- New substrate technologies may be susceptible to unforeseen failure mechanisms
  - Past reliability evaluation of ODBC substrates has been promising, but full module assembly and evaluation in collaboration with ORNL is needed.

**Any proposed future work is subject to change based on funding levels.*

Proposed Future Research

- FY 2022
  - Evaluate second round of IIC quilt package samples under accelerated power cycling, thermal cycling, and vibration conditions
  - Bond and test additional double-lap shear samples between Temprion and Cu/Al/AlSiC metallization layers under optimized bonding conditions (temperature, pressure, inert atmosphere).
- FY 2023
  - Evaluate electrical, thermal, and reliability performance of assembled half-bridge module in collaboration with ORNL, IIC, and DuPont.

**Any proposed future work is subject to change based on funding levels.*

Summary

Relevance

- New package designs must address thermal and reliability concerns and be evaluated under accelerated conditions that approximate real-world conditions.

Approach

- Collaborate with ORNL and industry partners to evaluate new packaging materials and manufacturing techniques for WBG-based traction inverters.

Technical Accomplishments

- Completed shear testing of ODBC/ODBA double-lap samples.
- Developed etching process for ODBC/ODBA substrates.
- Prepared IIC quilt packaging samples for additional accelerated tests.

Collaborations

- ORNL
- IIC
- DuPont.

Acknowledgments

Susan Rogers, U.S. Department of Energy

NREL EDT Task Leader

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Team Members

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ORNL: Lincoln Xue
IIC: Jason Kulick
DuPont: Susan Herczeg
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Thank You

www.nrel.gov

NREL/PR-5400-82652

Reviewer-Only Slides

Publications and Presentations

Publications

- DeVoto, D. 2021. “Advanced Power Electronics Designs – Reliability and Prognostics.” 2021 DOE VTO Annual Progress Report.

Presentations

- DeVoto, D. 2022. “Advanced Power Electronics Designs/Power Electronics Materials and Bonded Interfaces.” Presented to the DOE VTO Electrical and Electronics Technical Team, January 2022.

Records of Invention/Patents

- DeVoto, D.; Major, J.; Bennion, K.; Narumanchi, S.; Paret, P.; Moreno, G.; and Cousineau, E. 2019. “Electronics Packaging using Organic Electrically Insulating Layers.” ROI 19-15, Non-Provisional Patent Application Numbers PCT/US19/65147 and 16/707,179, filed December 9, 2019.

Critical Assumptions and Issues

- Working with private industry involves protection of their intellectual property and limits public disclosure of traction inverter designs
  - Industry partners have presented directly to the U.S. Driving Research and Innovation for Vehicle efficiency and Energy sustainability (U.S. DRIVE) Electrical & Electronics Tech Team (EETT) and could be contacted for questions and additional information.
- The increase in power density from proposed packaging designs may require more aggressive cooling techniques
  - Accurate thermal modeling and experimental testing of proposed designs will enable an informed selection of appropriate cooling techniques that balance cooling performance with cost, volume/weight, and reliability targets.