Reliability Aspects of Power-Dense Electric-Drive Power Electronics

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Advanced Power Electronics and Electric Machines (APEEM) Group

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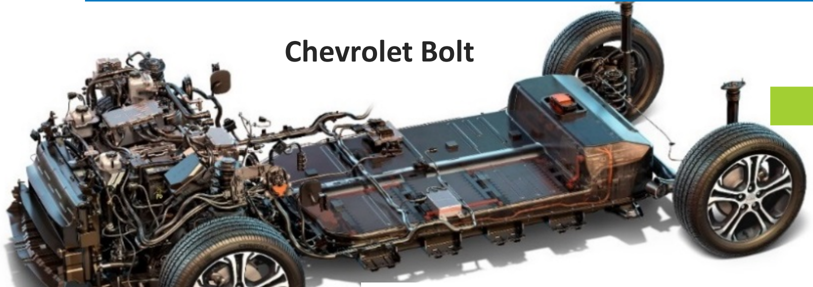
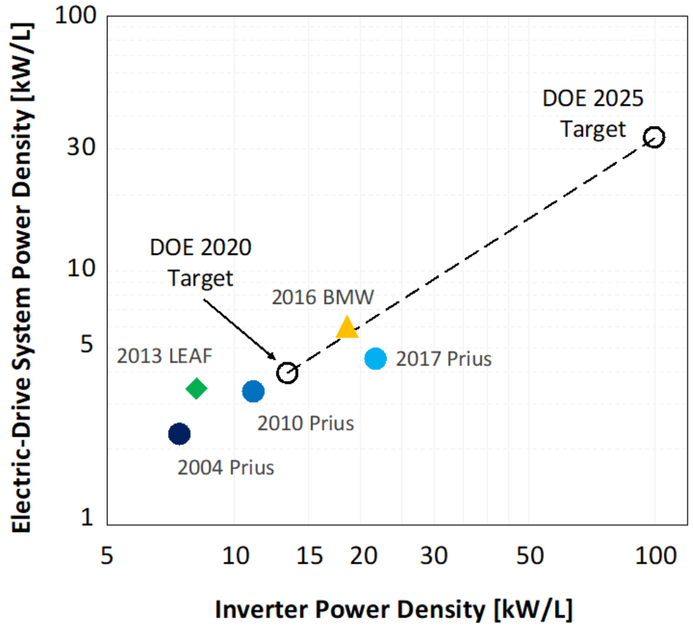
Research Pathway for Electric-Drive Vehicle Electrification





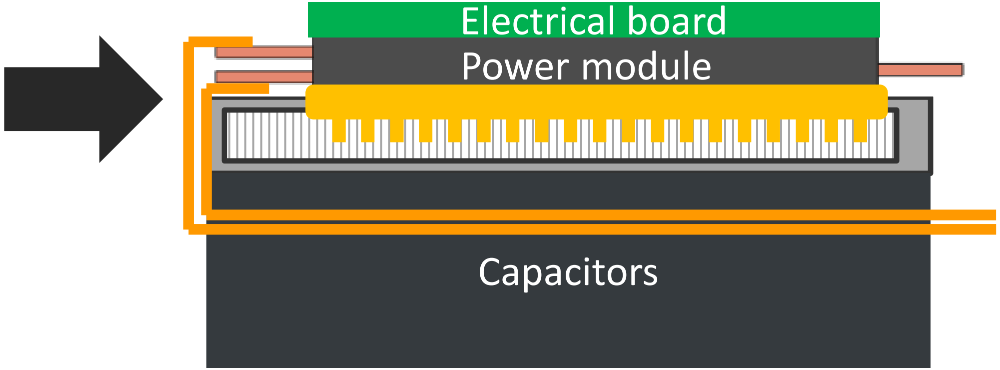
Future Mobility Design Concept

2025 Targets	
Cost	$6/kW (50% reduction)
Power Density	33 kW/L (850% increase)
Power Level	100 kW
Reliability/Lifetime	300,000 miles (100% increase)

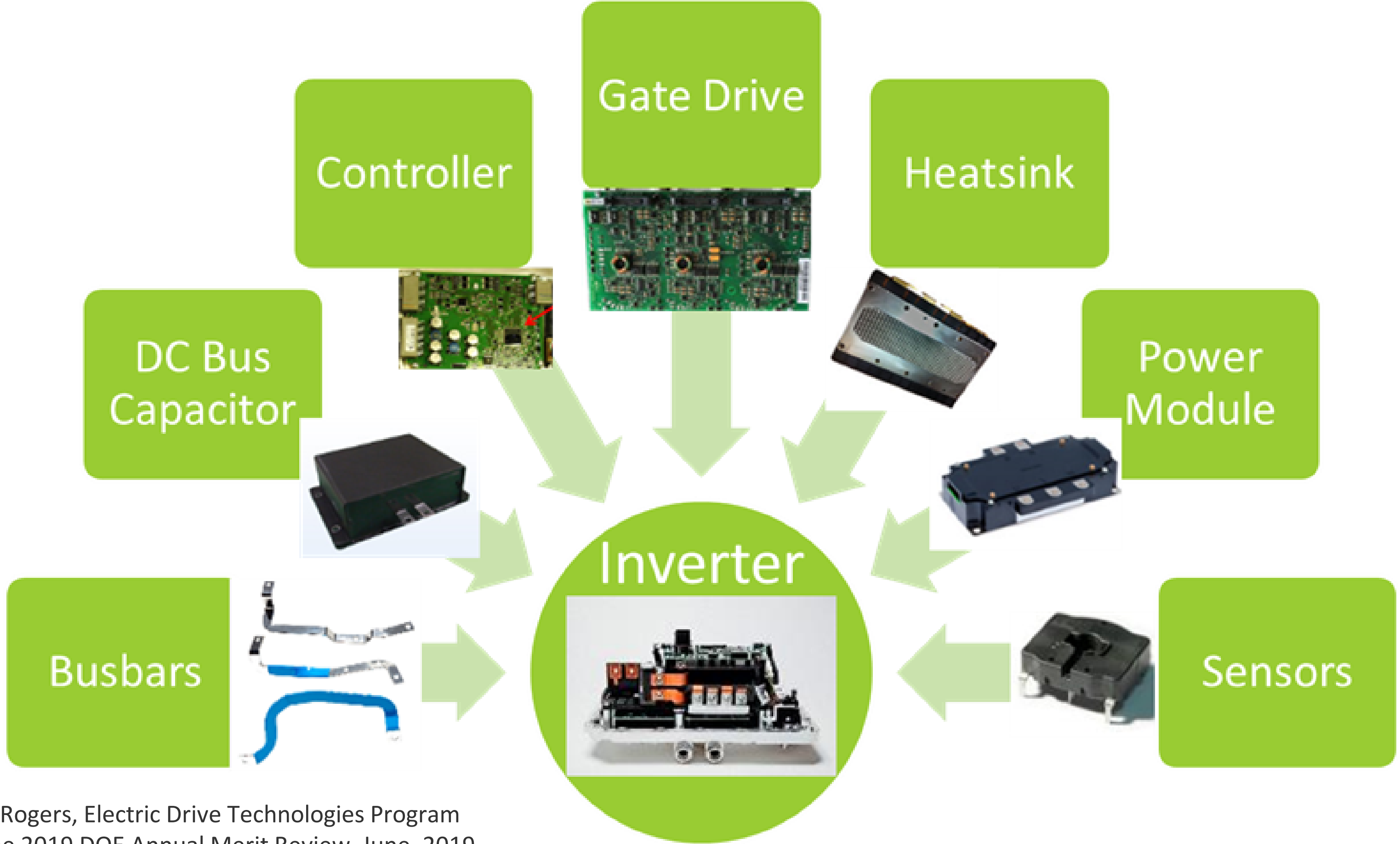
Source: Electrical and Electronics Technical Team Roadmap, https://www.energy.gov/sites/prod/files/2017/11/f39/EETT%20Roadmap%2010-27-17.pdf.

Future Power Electronics Designs – Example of Footprint/Volume Reduction

- Planar power electronics construction.
- Reduction in volume/size by a factor of 8 to 10—multiphysics, heterogeneous integration challenge.



Inverter – Constituents



Gate Drive

Controller

Heatsink

DC Bus Capacitor

Power Module

Inverter

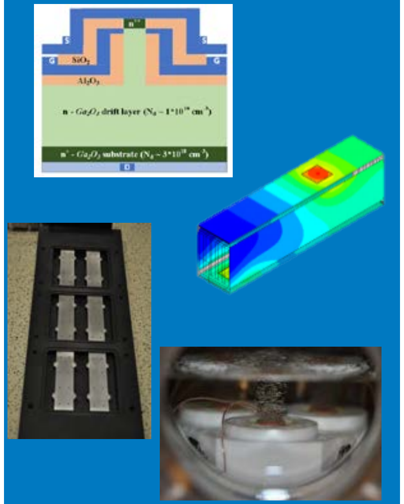
Busbars

Sensors

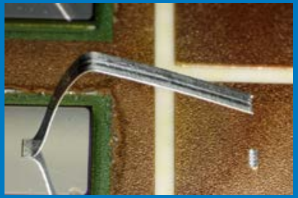
Source: Susan Rogers, Electric Drive Technologies Program Overview at the 2019 DOE Annual Merit Review, June, 2019.

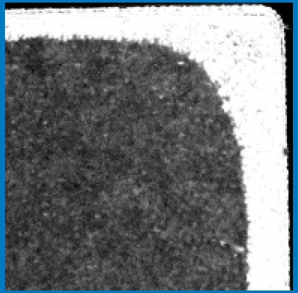
NREL APEEM Group Research Focus Areas

Power Electronics Thermal and Electro-Thermal

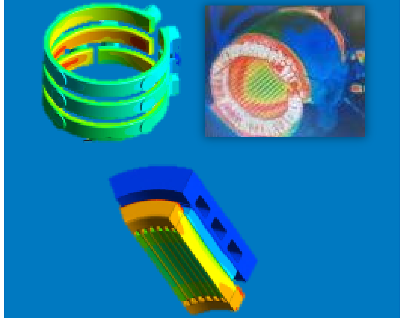


Advanced Packaging Designs and Reliability





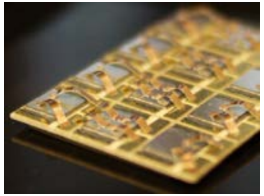
Electric Motor Thermal Management

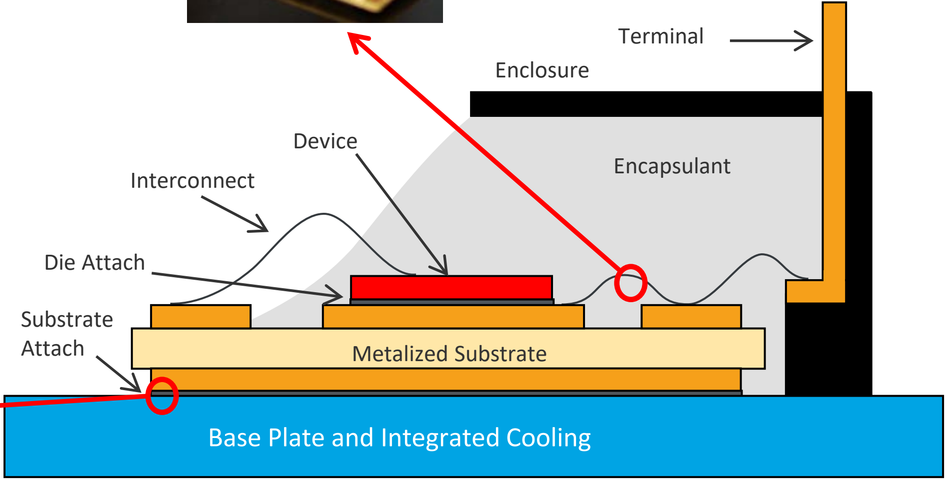


Packaging Performance and Reliability – Research and Development Pathway

- Improve reliability of new (high-temperature/wide-bandgap) technologies
- Develop predictive and remaining lifetime models
- Package parametric modeling

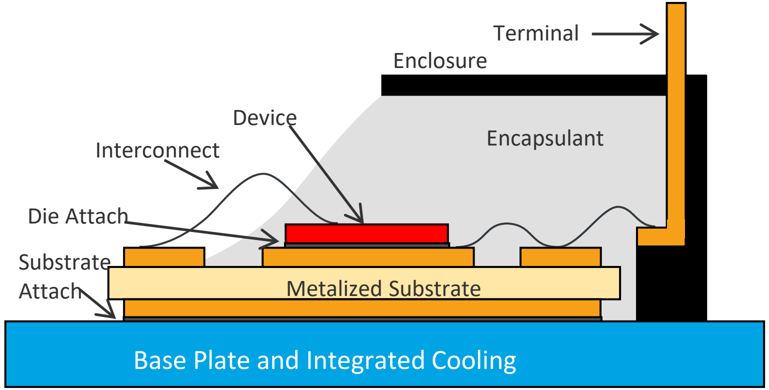
Electrical Interconnects

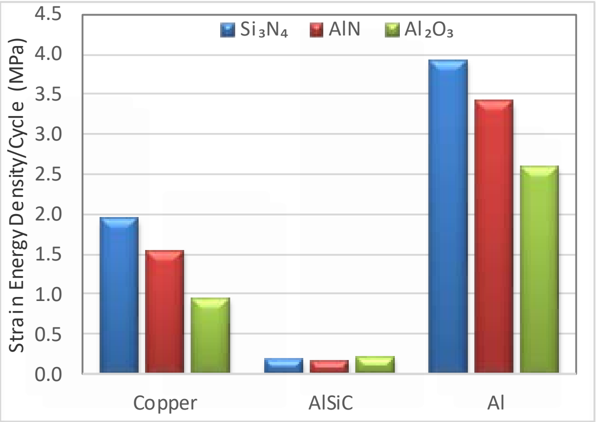




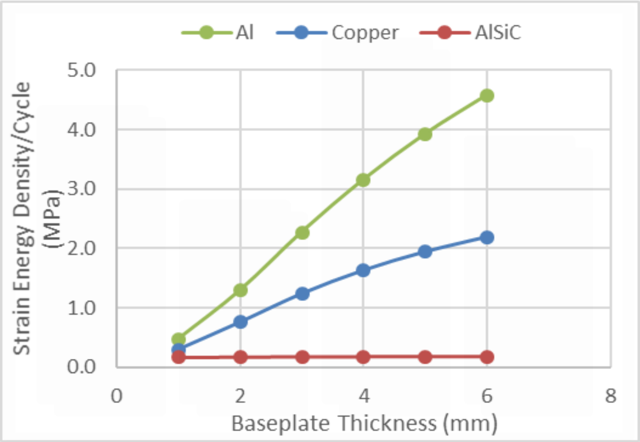
Bonded Interface

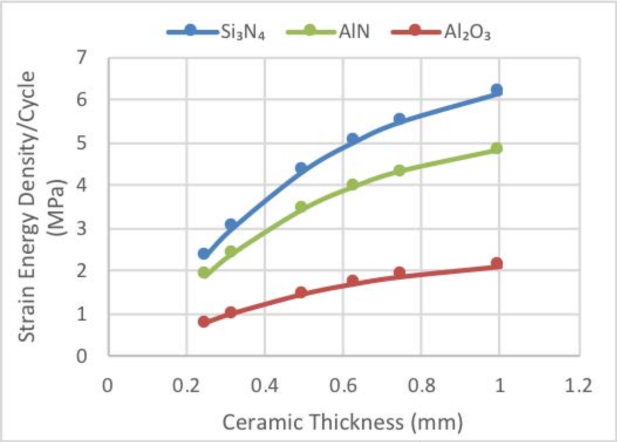
Thermomechanical Modeling – Parametric Design Study





Coefficient of Thermal Expansion (× 10^{-6}/K)
Silicon: 2.6
AlN: 4.5
Si_3N_4: 3.2
Copper: 16.5
Aluminum: 22.7
Sn63/Pb37 Solder: 24.7
Silver: 19.5

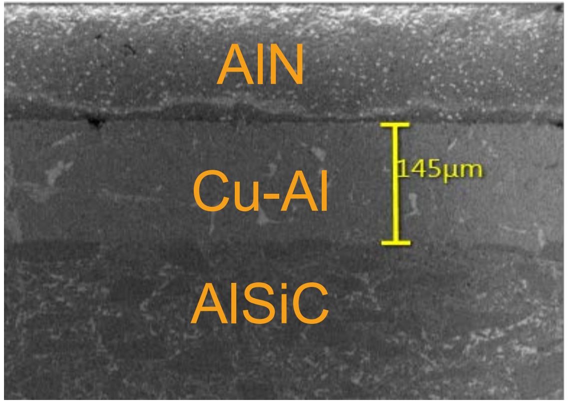




- The impact of material and geometric variations on the reliability of the substrate attach was investigated.

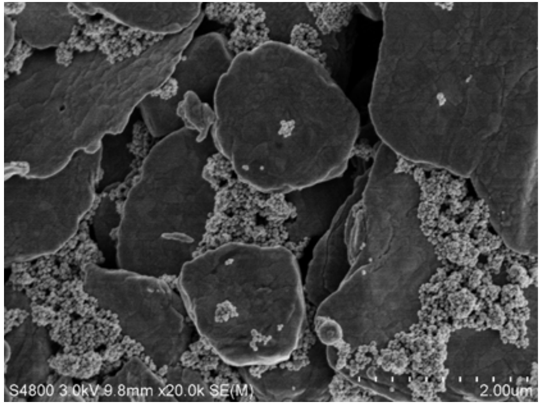
Substate Attach – Material Options

- High-Temperature Bonded Material
  - Georgia Tech
    - Cu/Al, Cu/Sn
  - Virginia Tech
    - Sintered Silver
      - Pressureless
      - Low-Pressure-Assisted
        - 3 MPa
        - 10 MPa
  - NREL
    - Sintered Silver (industry)
      - Pressureless



Cu-Al bond SEM image

Image credit: Darshan Pahinkar



Hybrid silver SEM image

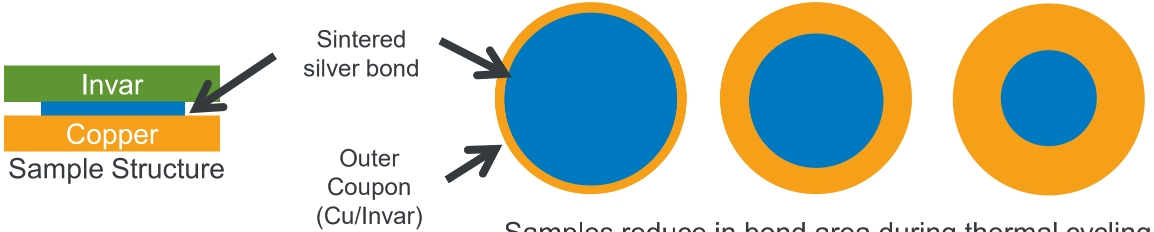
Image credit: Yansong Tan

Cu: Copper
Al: Aluminum
Sn: Tin
AlN: Aluminum Nitride
AlSiC: Aluminum Silicon-Carbide

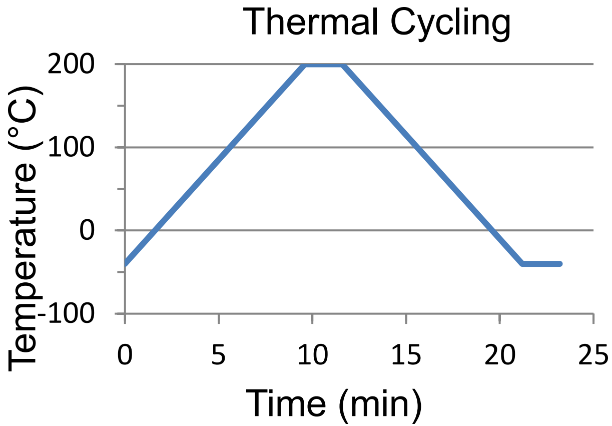
SEM – scanning electron microscope

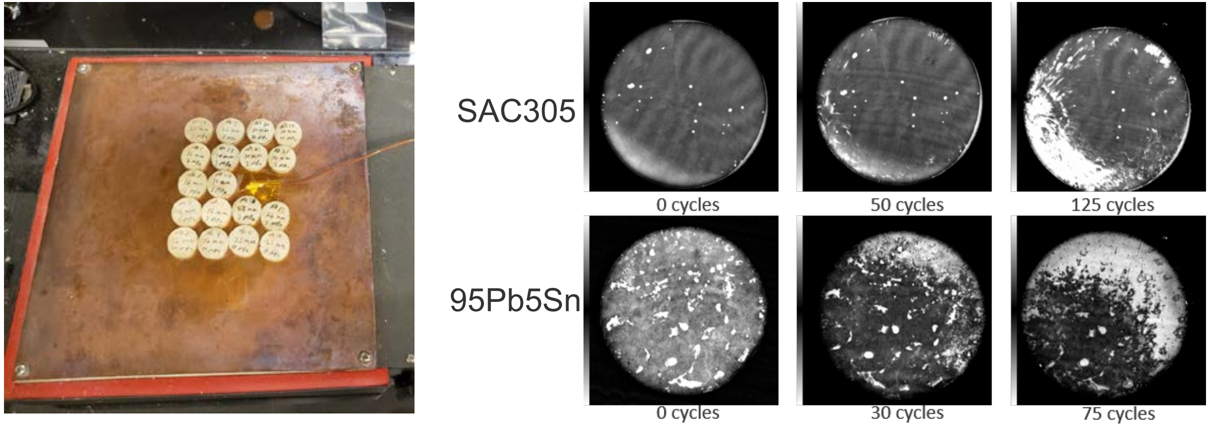
Substate Attach – Reliability Evaluation

25-mm diameter copper and invar coupons: non-plated (top), plated with 4-µm-thick silver (bottom)



Samples reduce in bond area during thermal cycling

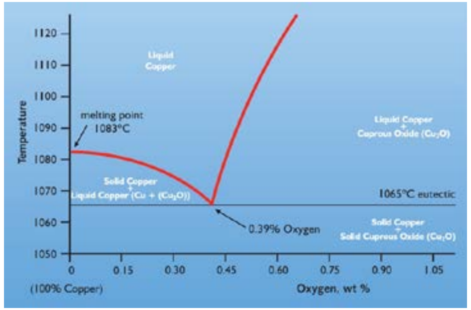


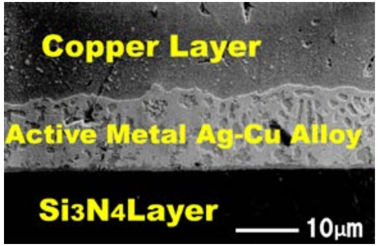


Samples placed on thermal platform for thermal cycling (left); acoustic microscope images of these samples are taken periodically (right)

Substrate Alternatives Research

- DBC (direct bond copper)
  - Oxidation of Cu foils during bonding lowers melt temperature from 1,083°C to 1,065°C
  - Maximum metallization thickness of 1 mm
  - Must have metallization layers on both sides of ceramic.
- AMB (active metal bonding)
  - Brazing process with Ag-Cu alloy between Cu and ceramic at 850°C in vacuum
  - Requires more process steps and is more expensive than DBC.
- ODBC (Organic Direct Bond Copper)
  - A polyimide dielectric is bonded with metal
  - No limitations in metal material or metallization thickness.

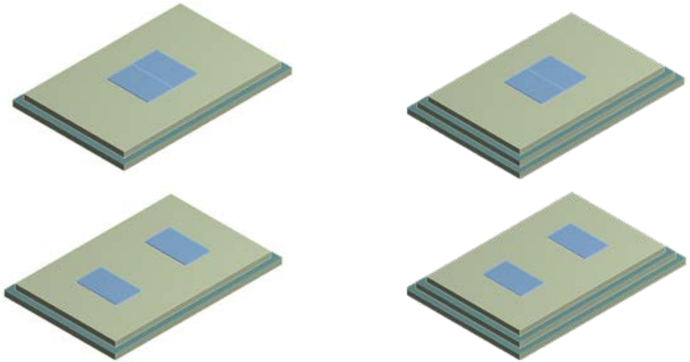


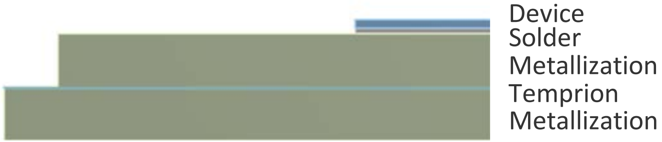


Substrate Thermal Modeling

- Completed thermal parametric analysis of quilt package devices mounted onto ODBC substrates
  - Device spacing: 0.01–4 mm
  - ODBC layers: single and double layers
  - ODBC thickness: 25 µm and 35 µm
  - Metallization thickness: 0.1–4 mm
  - Heat transfer coefficient: 1,000–30,000 W/(m^2·K) at 65°C.

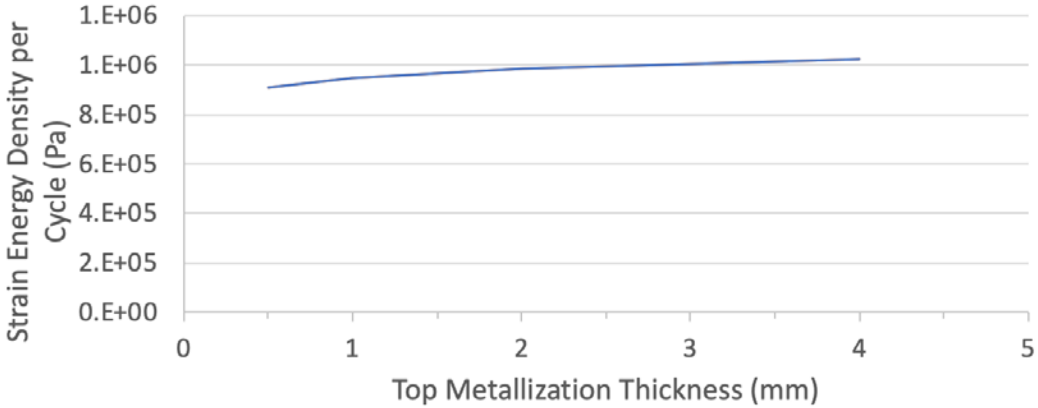
Layer	Material	Thickness (mm)
Devices	SiC	0.18
Die-Attach	SAC 305	0.1
Metallization Layers	Cu	0.1–4
Insulation Layers	ODBC	0.025, 0.035





Substrate Thermomechanical Modeling

- Thermomechanical analysis of device-attach solder layer was completed
  - Top metallization thickness was varied from 0.1 to 4 mm
  - Sample package thermally cycled between −40°C and 150°C
  - Strain energy density values were calculated within the solder layer
  - Modeling results indicate that strain energy density values do not significantly increase with top metallization thickness.

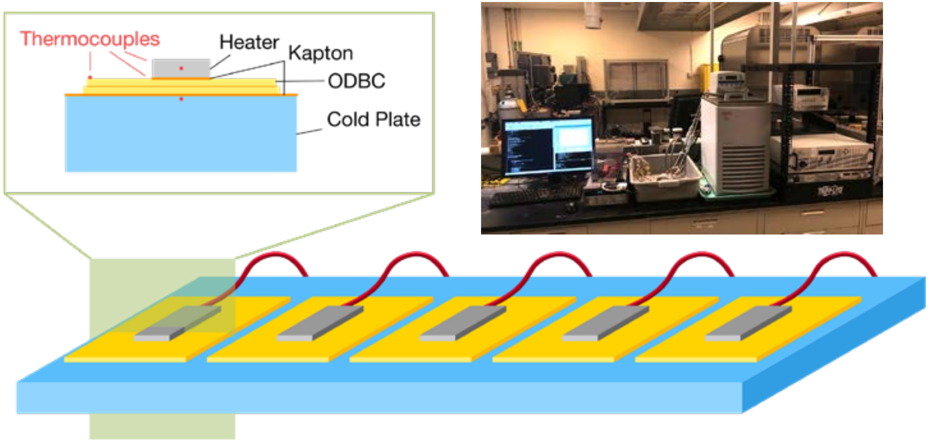


Substrate Accelerated Testing

- Thermal Shock: –40°C to 200°C, 5-minute dwells
- Thermal Aging: 175°C
- Power Cycling: 40°C to 200°C

- ODBC substrates reached 5,000 thermal shock cycles, 1,900 thermal aging hours aging, and 2,200 power cycles.
- No significant decease in electrical or thermal performance was observed.

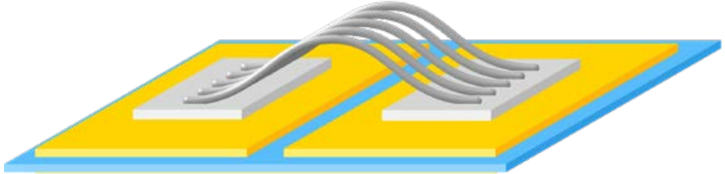

Substrates Undergoing Aging

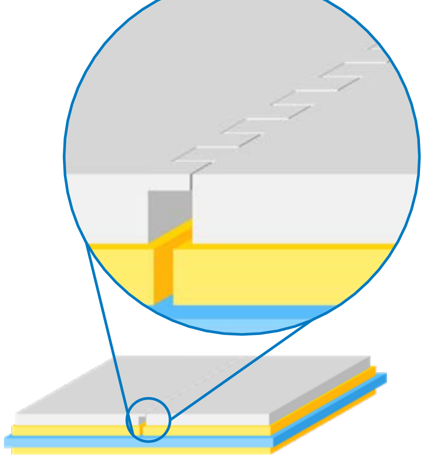


Power Cycling Test Setup

Electrical Interconnect Research

- Alternative interconnect designs are required as devices are reduced in size and spacing between devices is minimized.
- Traditional wire interconnects or etched substrates for topside electrical connections can be replaced with direct chip-to-chip connection.





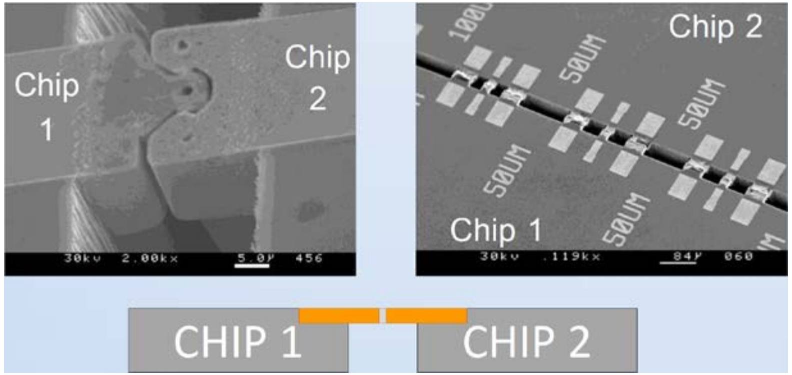
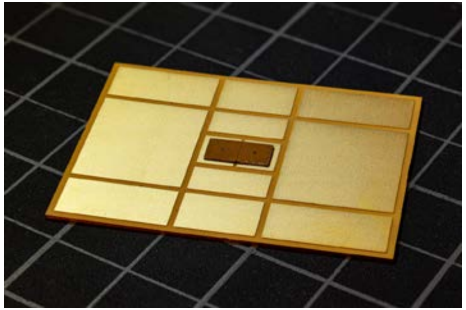


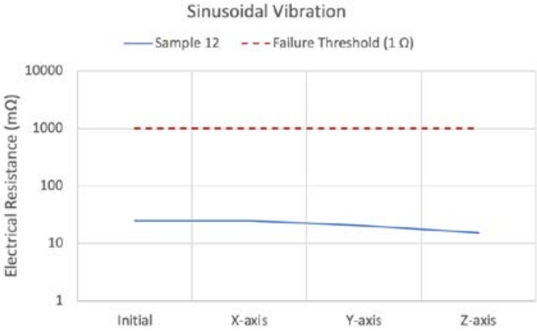
Image Credit: Indiana Integrated Circuits, https://www.eejournal.com/article/20150302-quilt/

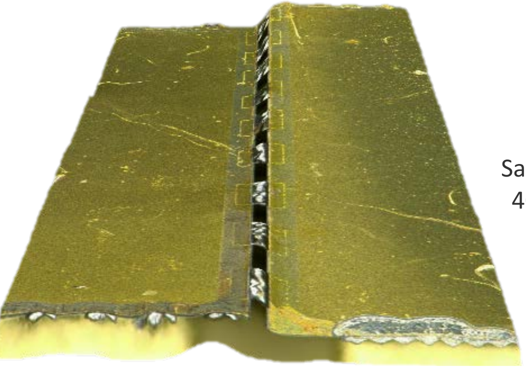
Quilt Packaging Reliability Experimental Evaluation

- Evaluated quilt packaging samples under thermal cycling and vibration experiments
  - *Sinusoidal Vibration:* 20-Hz to 1,000-Hz sweep, 5-g acceleration, 2-hour duration (IEC 60068-2-6)
  - *Mechanical Shock:* half-sine pulse, 30-g acceleration, 18-ms duration, repeating three times (IEC 60068-2-27)
  - *Thermal Cycling:* –40°C to 150°C, 10°C/min ramp rate, 15-min soak, 1,000 cycles (JESD22-A104D).
- Electrical resistance measurements increased significantly for all samples that were subjected to mechanical shock and thermal cycling tests.

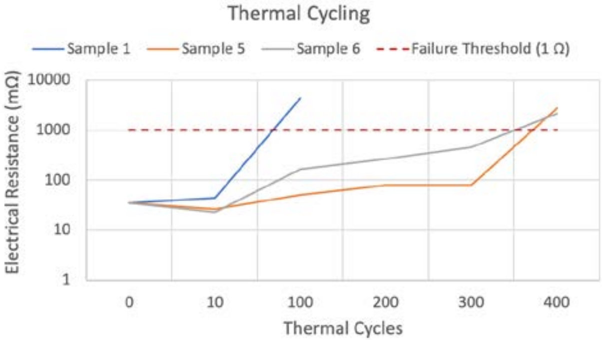


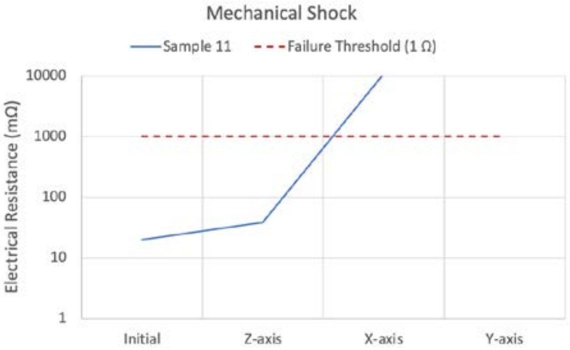
IIC Package on Dupont ODBC Substrate





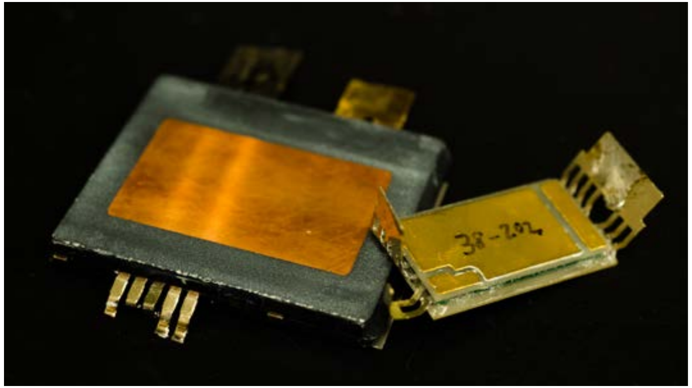
Sample 5 after 400 Thermal Cycles

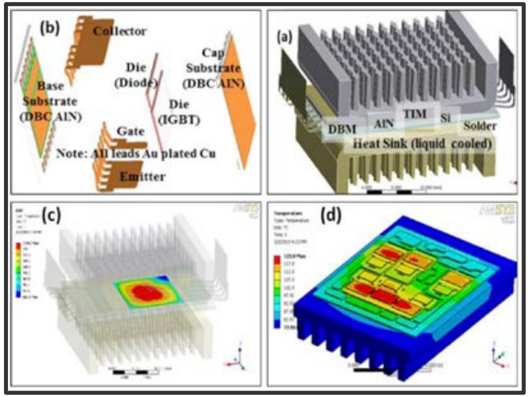


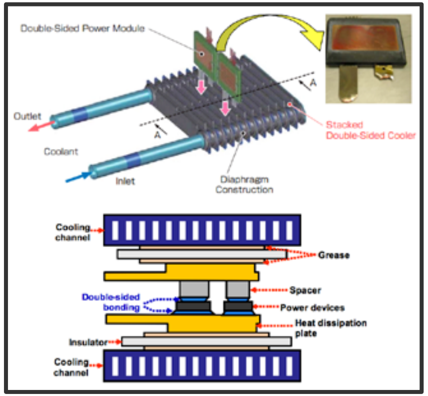


Nodule Electrical Resistance

Future Package Designs







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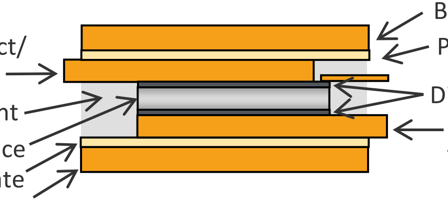
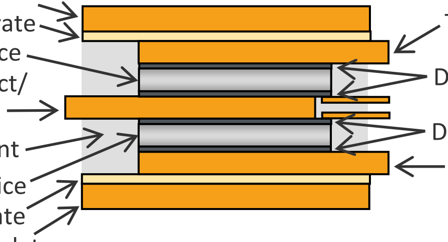


Baseplate
Polyimide Substrate
Interconnect/
Terminal
Die Attach
Encapsulant
Interconnect/
Terminal
Device
Polyimide Substrate
Baseplate



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More Information

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