



# Advanced Power Electronics Designs – Reliability and Prognostics

(Keystone Project 1)

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National Renewable Energy Laboratory  
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DOE Vehicle Technologies Program  
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ELT218

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# Overview

## Timeline

- Project start date: FY 2019
- Project end date: FY 2023
- Percent complete: 30%

## Budget

- Total project funding: \$350K
  - DOE share: \$350K
- Funding for FY 2019: \$175K
- Funding for FY 2020: \$175K

## Barriers

- Barriers addressed
  - Cost
  - Performance
  - Reliability and Lifetime

## Partners

- Interactions/collaborations
  - Oak Ridge National Laboratory (ORNL)
  - Indiana Integrated Circuits (IIC)
  - DuPont
- Project lead
  - National Renewable Energy Laboratory (NREL)

# Relevance

- Wide bandgap (WBG) packaging designs must thermally allow for:
  - Higher operating temperatures
  - Higher heat fluxes/power densities
  - Hot spots
- Coefficient of thermal expansion (CTE) mismatch between layers of the module will impose stresses that can initiate and propagate defects:
  - Attach layer fatigue
  - Interconnect fatigue
- **New package designs must address thermal and reliability concerns and be evaluated under accelerated conditions that approximate real-world conditions**

# Milestones

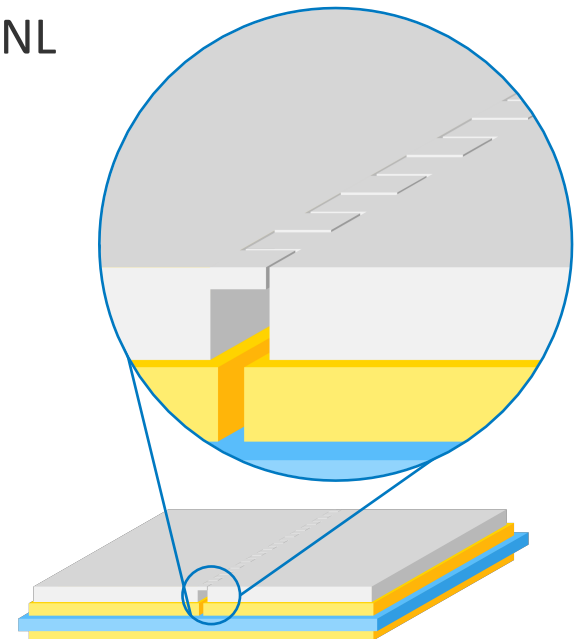
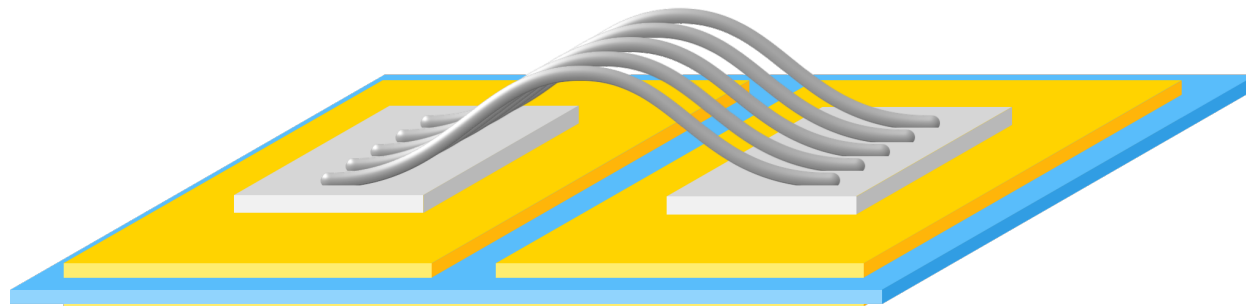
<b>Date/Status</b>	<b>Description</b>
December 2019 <i>(complete)</i>	Milestone <ul style="list-style-type: none"><li>• Evaluate thermal performance of organic direct-bond copper (ODBC) substrates</li></ul>
March 2020 <i>(complete)</i>	Go/No-Go <ul style="list-style-type: none"><li>• Receive first round of quilt-packaged devices from IIC</li></ul>
September 2020 <i>(in progress)</i>	Milestone <ul style="list-style-type: none"><li>• Characterize devices/packages under thermal aging, thermal cycling, and vibration conditions and monitor component health through electrical precursor measurements</li></ul>
September 2020 <i>(in progress)</i>	Milestone <ul style="list-style-type: none"><li>• Prepare report on research results</li></ul>

# Approach

- **New package designs must address thermal and reliability concerns and be evaluated under accelerated conditions that approximate real-world conditions**
- NREL is closely working with ORNL and industry partners to evaluate new packaging materials and manufacturing techniques for WBG-based traction inverters
  - IIC: Quilt packaging via a chip-to-chip edge interconnect technology
  - DuPont: ODBC substrate as a replacement of ceramic substrates

# Approach

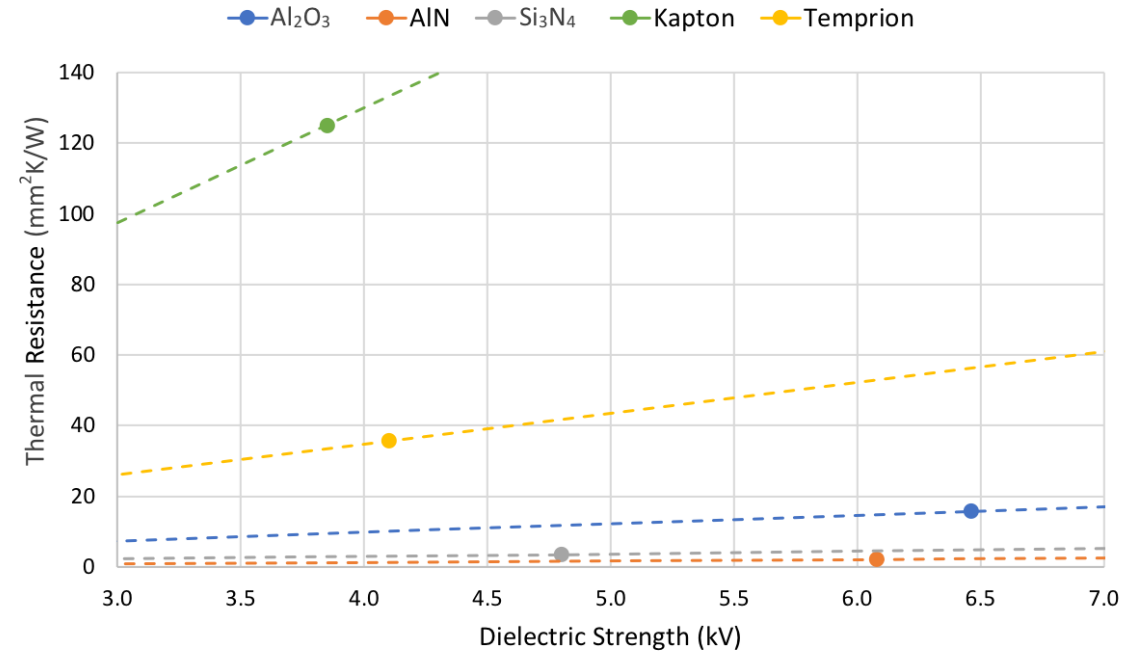
- Alternative interconnect designs are required as devices are reduced in size and spacing between devices is minimized
- **Traditional wire interconnects or etched substrates for topside electrical connections will be replaced with direct chip-to-chip connection**
- Devices are joined with quilt packaging, eliminating the need for wire bonds or other external electrical connection technology
  - Experimental samples have been designed in collaboration with IIC and ORNL
  - Reliability evaluation will be completed at NREL



# Approach

- **Alternative electrically insulated substrate designs are required to enable reliable packages that operate with higher power densities and higher temperatures**
- Traditional substrate technologies
  - Direct-bond copper (DBC)
    - Oxidation of copper (Cu) foils during bonding lowers melt temperature from 1,083°C to 1,065°C
    - Maximum metallization thickness of 1 mm
    - Must have metallization layers on both sides of the ceramic
    - Examples include aluminum oxide ( $\text{Al}_2\text{O}_3$ ), aluminum nitride (AlN), and zirconia ( $\text{ZrO}_2$ )-doped high-performance substrates (HPS)
  - Active metal bonding (AMB)
    - Brazing process with silver-copper (Ag-Cu) alloy between Cu and ceramic at 850°C in vacuum
    - Requires more processing steps and is more expensive than DBC
    - Silicon nitride ( $\text{Si}_3\text{N}_4$ ) substrate is an example
- ODBC
  - A polyimide dielectric is bonded with metal through elevated temperature and pressure
  - No limitations in metal material or metallization thickness

# Approach



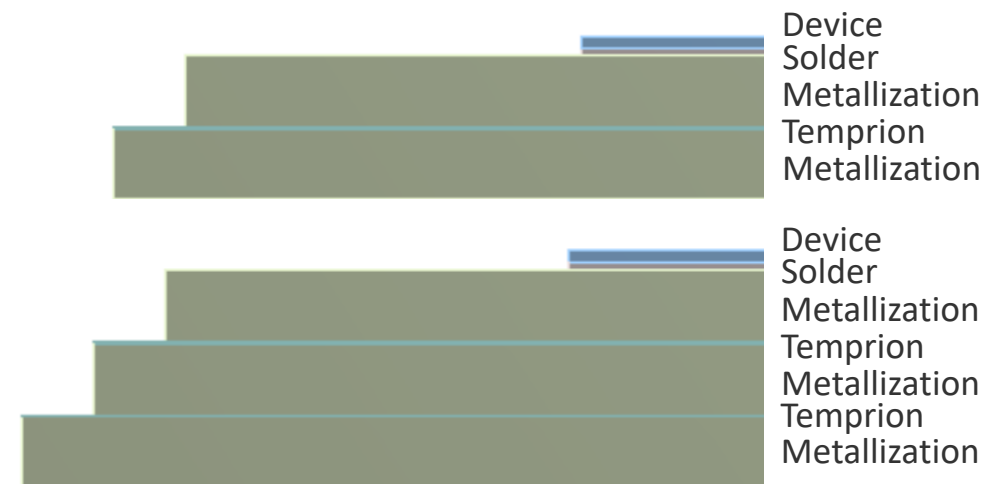
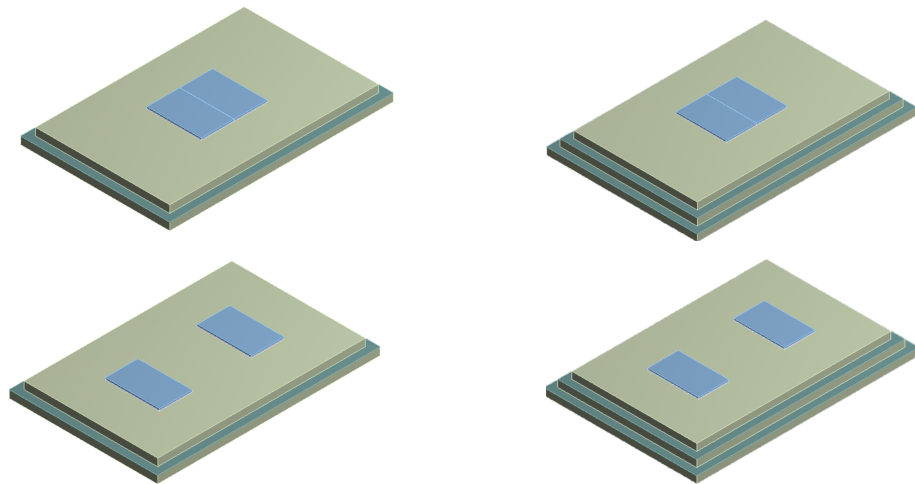
Insulator	Thickness (μm)	Dielectric Strength (kV/mm)	Dielectric Strength (kV)	Thermal Conductivity (W/[m·K])	Thermal Resistance (mm <sup>2</sup> K/W)
Al <sub>2</sub> O <sub>3</sub>	380	17	6.5	24	16
AlN	380	16	6.1	180	2
Si <sub>3</sub> N <sub>4</sub>	320	15	4.8	90	4
Kapton	25	154	3.9	0.2	125
Temprion	25	164	4.1	0.7	36



# Technical Accomplishments and Progress

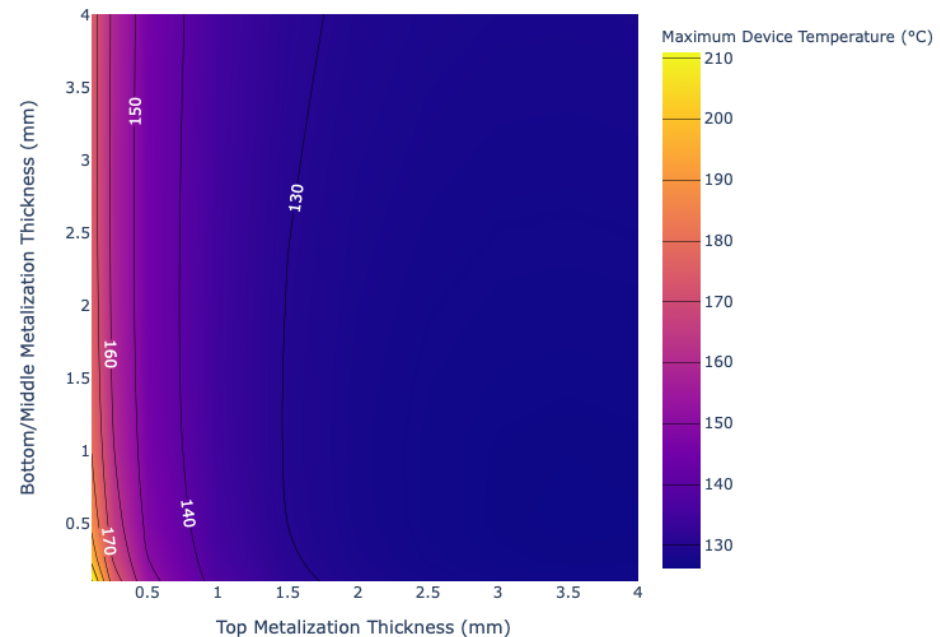
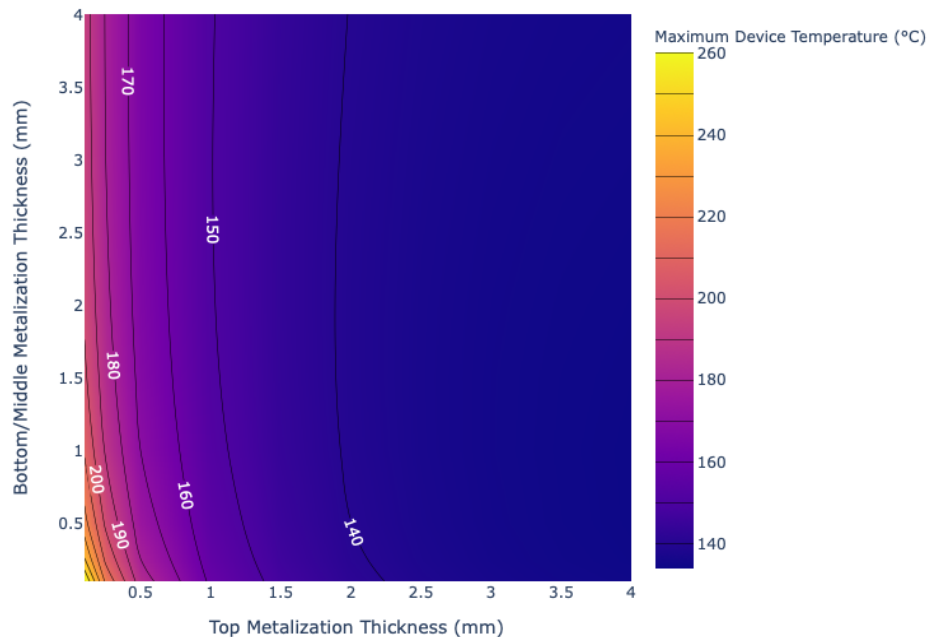
- Completed thermal parametric analysis of quilt package devices mounted onto ODBC substrates
  - Device spacing: 0.01–4 mm
  - ODBC layers: single and double layers
  - ODBC thickness: 25  $\mu\text{m}$  and 35  $\mu\text{m}$
  - Metallization thickness: 0.1–4 mm
  - Heat transfer coefficient: 1,000–30,000  $\text{W}/(\text{m}^2\cdot\text{K})$  at 65°C

Layer	Material	Thickness (mm)
Devices	SiC	0.18
Die-Attach	SAC 305	0.1
Metallization Layers	Cu	0.1–4
Insulation Layers	ODBC	0.025



# Technical Accomplishments and Progress

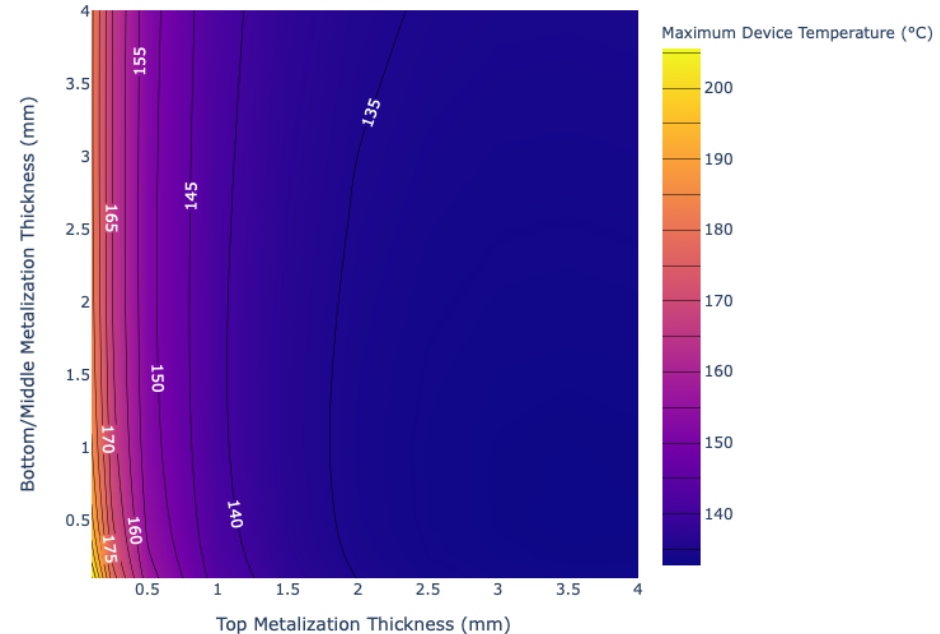
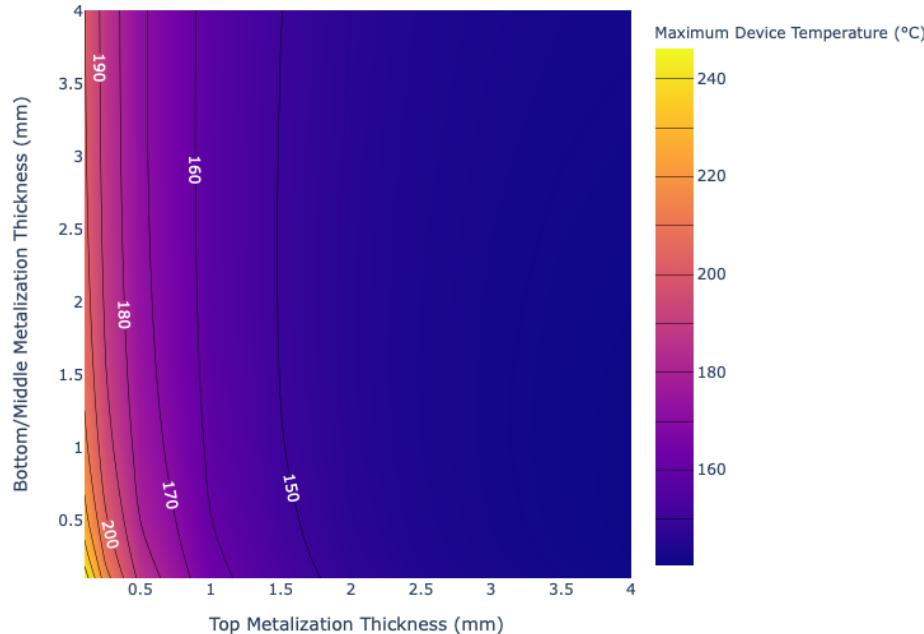
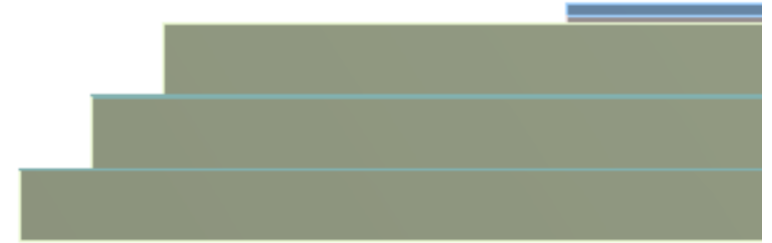
- Substrate designs can maintain device temperatures under 160°C
  - Top metallization layer must be approximately 1–1.5 mm thick in order to manage device temperatures
  - Bottom metallization layer thickness is less critical



Device temperatures for single-layer, 25- $\mu$ m ODBC with 0.01-mm device spacing (left) and 4-mm device spacing (right)

# Technical Accomplishments and Progress

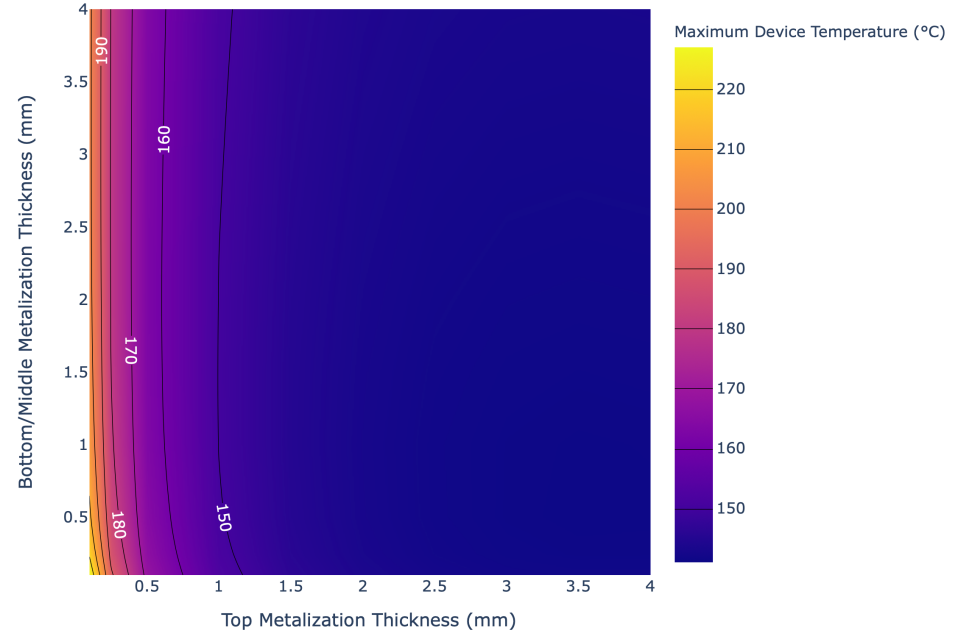
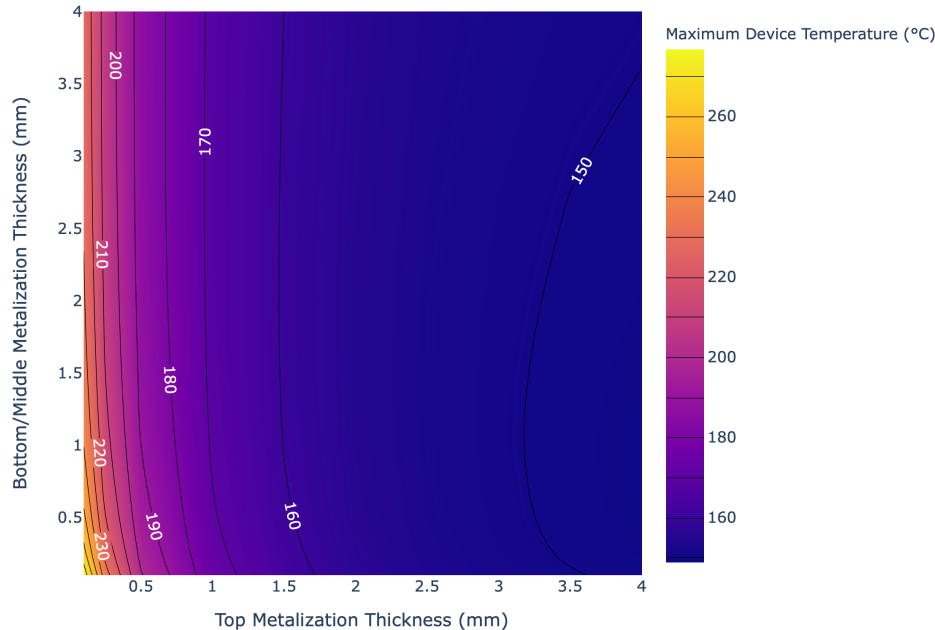
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  - Middle and bottom metallization layer thicknesses are less critical



Device temperatures for double-layer, 25- $\mu$ m ODBC with 0.01-mm device spacing (left) and 4-mm device spacing (right)

# Technical Accomplishments and Progress

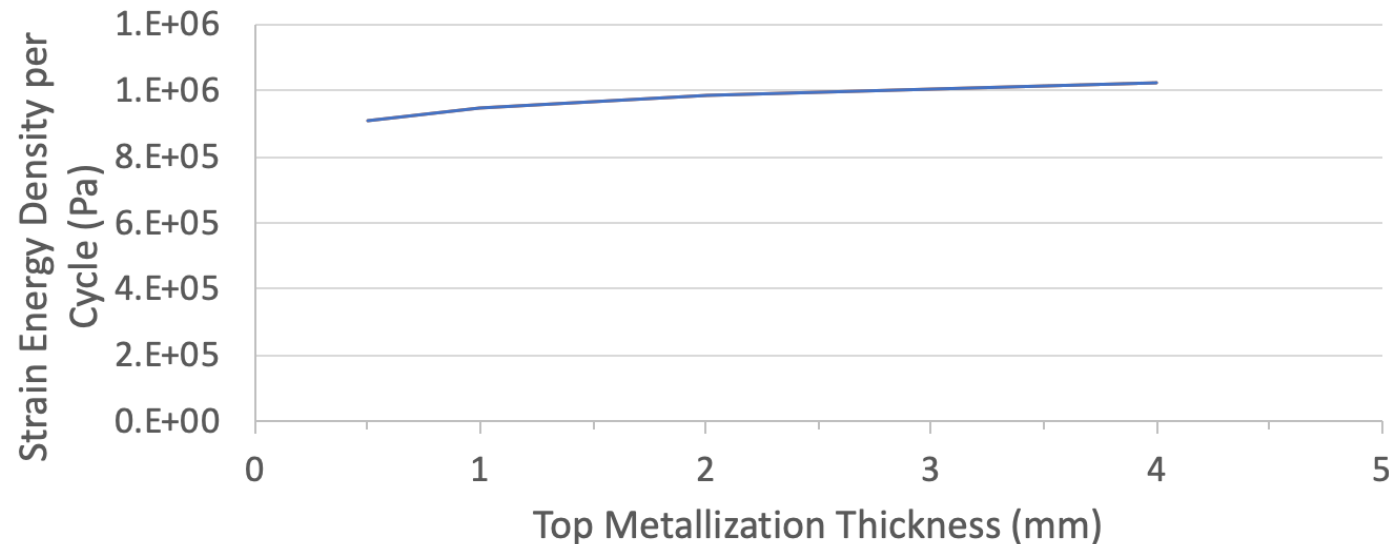
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Device temperatures for double-layer, 35- $\mu$ m ODBC with 0.01-mm device spacing (left) and 4-mm device spacing (right)

# Technical Accomplishments and Progress

- Thermomechanical analysis of device-attach solder layer was completed
  - Top metallization thickness was varied from 0.1 to 4 mm
  - Sample package thermally cycled between  $-40^{\circ}\text{C}$  and  $150^{\circ}\text{C}$
  - Strain energy density values were calculated within the solder layer
  - Modeling results indicate that strain energy density values do not significantly increase with top metallization thickness



# Technical Accomplishments and Progress

- First round of quilt-packaged devices have been delivered by IIC
  - Devices were mounted to DuPont ODBC substrates
  - Assemblies vary in nodule shape, length, and width
  - Scanning electron microscope (SEM) images show quality soldering at interface

IIC Quilt Packaging Assemblies

Assembly No.	Nodule Shape	Nodule Length	Nodule Width
1	Triangle	30 $\mu\text{m}$	100 $\mu\text{m}$
2	Rectangle	30 $\mu\text{m}$	300 $\mu\text{m}$
3	Triangle	30 $\mu\text{m}$	700 $\mu\text{m}$
4	Triangle	70 $\mu\text{m}$	300 $\mu\text{m}$
5	Triangle	70 $\mu\text{m}$	300 $\mu\text{m}$
6	Rectangle	30 $\mu\text{m}$	100 $\mu\text{m}$
7	Rectangle	30 $\mu\text{m}$	700 $\mu\text{m}$
8	Triangle	30 $\mu\text{m}$	300 $\mu\text{m}$
9	Triangle	70 $\mu\text{m}$	700 $\mu\text{m}$
10	Triangle	70 $\mu\text{m}$	300 $\mu\text{m}$
11	Rectangle	70 $\mu\text{m}$	100 $\mu\text{m}$
12	Rectangle	30 $\mu\text{m}$	100 $\mu\text{m}$

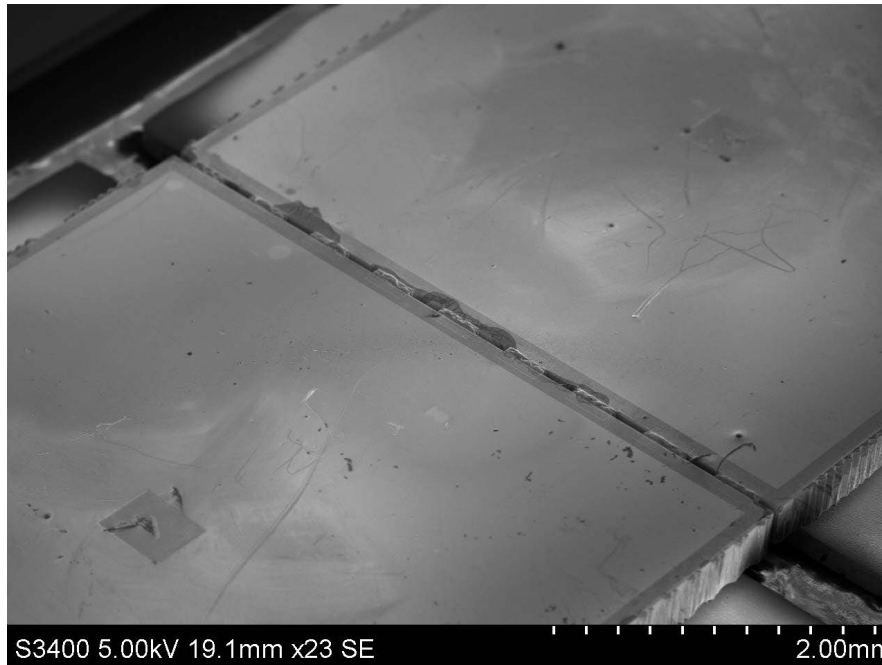
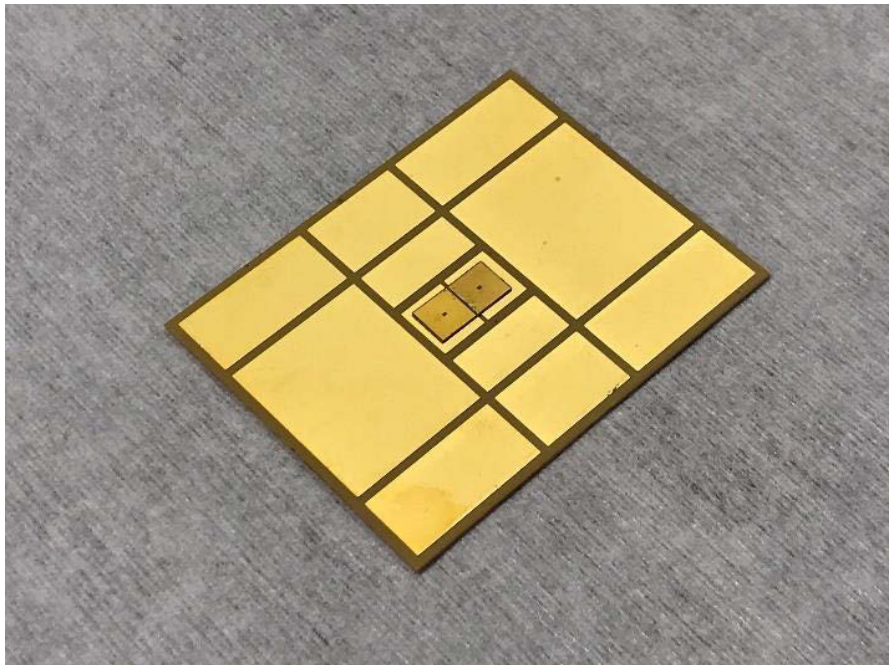


Image Credits: IIC

# Technical Accomplishments and Progress

- Samples will be characterized under accelerated thermal and vibration conditions
  - Sinusoidal Vibration: 20 to 1,000-Hz sweep, 5-g acceleration, 2-hours duration (IEC 60068-2-6)
  - Mechanical Shock: half-sine pulse, 30-g acceleration, 18-ms duration, repeating 3 times (IEC 60068-2-27)
  - Thermal Cycling:  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ,  $10^{\circ}\text{C}/\text{min}$  ramp rate, 15-min soak, 1,000 cycles (JESD22-A104D)

# Responses to Previous Year Reviewers' Comments

The reviewer stated that the approach seems promising. However, more and various aggressive temperature conditions should be examined, and an economically optimized and reliable approach with proper size should be investigated further, rather than limited environmental conditions.

Expanding environmental evaluations will be critical for an accurate evaluation of quilt packages and ODBC substrates.

The reviewer said the quilting approach is interesting, but from the slides it appears the technology is overlooking dual-sided cooled quilted power devices. The reviewer asked if quilting can be accomplished with a double-sided cooled power device. The results from the thermal aging, thermal shock, and power cycle look encouraging. Perhaps the project team could add bias humidity and operation life to the testing. The reviewer asked if the team can also quantify the number of interconnects between quilted die that are possible, and if the die need to be the same size and/or thickness to be quilted.

The reviewer raises several valid points. Design modifications should allow for dual-sided cooled packages, but this is outside the scope of the present work. If sufficient yield of samples are reached in FY 2020, bias humidity evaluation will be included.

*\*Any proposed future work is subject to change based on funding levels.*



# Collaboration and Coordination

- ORNL
  - Laboratory partner for design and assembly of power electronics modules
- IIC
  - Industry partner for quilt packaging technology
- DuPont
  - Industry partner for ODBC technology

# Remaining Challenges and Barriers

- Thermal and reliability concerns of new electrical connect technology must be experimentally evaluated
  - Thermal modeling has been completed to determine impact of positioning devices more closely to each other
  - Experimental characterization will evaluate nodule reliability under power, thermal, and vibration conditions
- New substrate technologies may be susceptible to unforeseen failure mechanisms
  - Past reliability evaluation of ODBC substrates has been promising, but full module assembly and evaluation in collaboration with ORNL is needed

# Proposed Future Research

- FY 2020
  - Evaluate devices/packages under thermal and vibration conditions
  - Evaluate thermomechanical behavior of quilt packaging geometry
- FY 2021
  - Evaluate thermal and reliability performance of assembled half-bridge module in collaboration with ORNL, IIC, and DuPont

# Summary

## Relevance

- New package designs must address thermal and reliability concerns and be evaluated under accelerated conditions that approximate real-world conditions

## Approach

- Collaborate with ORNL and industry partners to evaluate new packaging materials and manufacturing techniques for WBG-based traction inverters

## Technical Accomplishments

- Completed thermal and thermomechanical modeling of devices connected by quilt packaging and mounted to ODBC substrates
- First round of quilt-packaged devices have been delivered by IIC

## Collaborations

- ORNL
- IIC
- DuPont

## Acknowledgments

Susan Rogers, U.S. Department of Energy

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# Thank You

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[www.nrel.gov](http://www.nrel.gov)

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