Crystalline Silicon Photovoltaic Module Manufacturing Costs and Sustainable Pricing: 1H 2018 Benchmark and Cost Reduction Road Map

Michael Woodhouse, Brittany Smith, Ashwin Ramdas, and Robert Margolis

National Renewable Energy Laboratory

NREL is a national laboratory of the U.S. Department of Energy
Office of Energy Efficiency & Renewable Energy
Operated by the Alliance for Sustainable Energy, LLC

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications.

Contract No. DE-AC36-08GO28308

Technical Report
NREL/TP-6A20-72134
Revised February 2020

Crystalline Silicon Photovoltaic Module Manufacturing Costs and Sustainable Pricing: 1H 2018 Benchmark and Cost Reduction Road Map

Michael Woodhouse, Brittany Smith, Ashwin Ramdas, and Robert Margolis

National Renewable Energy Laboratory

Suggested Citation
Woodhouse, Michael. Brittany Smith, Ashwin Ramdas, and Robert Margolis. 2019. *Crystalline Silicon Photovoltaic Module Manufacturing Costs and Sustainable Pricing: 1H 2018 Benchmark and Cost Reduction Roadmap*. Golden, CO: National Renewable Energy Laboratory. https://www.nrel.gov/docs/fy19osti/72134.pdf.

NREL is a national laboratory of the U.S. Department of Energy
Office of Energy Efficiency & Renewable Energy
Operated by the Alliance for Sustainable Energy, LLC

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications.

Contract No. DE-AC36-08GO28308

Technical Report
NREL/TP-6A20-72134
Revised February 2020

National Renewable Energy Laboratory
15013 Denver West Parkway
Golden, CO 80401
303-275-3000 • www.nrel.gov

NOTICE

This work was authored by the National Renewable Energy Laboratory, operated by Alliance for Sustainable Energy, LLC, for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. Funding for this work was provided by the U.S. Department of Energy Office of Energy Efficiency and Renewable Energy Solar Energy Technologies Office. The views expressed herein do not necessarily represent the views of the DOE or the U.S. Government.

Errata

This report, originally published in February 2019, was revised in February 2020. The names of firms were removed from Figure 8, and the Siemens direct chlorination or hydrochlorination with trichlorosilane (TCS) technology identifiers were combined.

Acknowledgments

This work was funded by the U.S. Department of Energy's Solar Energy Technologies Office. We would like to acknowledge the following individuals for their helpful comments, corrections, and contributions: David Feldman (NREL), Ran Fu (NREL), Matthew Page (NREL), David Young (NREL), Pauls Stradins (NREL), Charlie Gay (DOE Solar Energy Technologies Office), and all the solar industry stakeholders who contributed to this analysis. We also thank Al Hicks (NREL) for technical illustrations, Billy Roberts (NREL) for supply-chain maps, and Jarett Zuboy for editorial support.

List of Acronyms

2N	99% pure
9N	99.9999999% pure
11N	99.999999999% pure
Al-BSF	aluminum back surface field
ARC	anti-reflective coating
ASP	average selling price
BOM	balance of module
BOS	balance of system
CapEx	capital expenditure
COGS	cost of goods sold
c-Si	crystalline silicon
CVD	chemical vapor deposition
Cz	Czochralski
DS	directional solidification
DW	diamond wire
EBIT	earnings before interest and taxes
EPC	engineering, procurement, and construction
EU	European Union
EVA	ethylene-vinyl acetate
FBR	fluidized bed reactor
GAAP	generally accepted accounting principles
H	half (1H = first half, etc.)
IBC	interdigitated back contact
IFRS	International Financial Reporting Standards
I-V	current-voltage
J-box	junction box
mg-Si	metallurgical grade silicon
MSP	minimum sustainable price
MT	metric tons
NREL	National Renewable Energy Laboratory
OpEx	operating expenses
PECVD	plasma-enhanced chemical vapor deposition
PERC	passivated emitter and rear cell
PERL	passivated emitter rear locally diffused
PERT	passivated emitter and rear totally diffused
POE	polyolefin encapsulant
PSG	phosphosilicate glass
PV	photovoltaics
R&D	research and development
SG&A	sales, general, and administrative
SHJ	silicon heterojunction
SiH_4	silane
TCS	trichlorosilane
TMA	trimethyl aluminum
TPO	thermoplastic polyolefin

Executive Summary

Over the past decade, the crystalline-silicon (c-Si) photovoltaic (PV) industry has grown rapidly and developed a truly global supply chain, driven by increasing consumer demand for PV as well as technical advances in cell performance and manufacturing processes that enabled dramatic cost reductions. Although these developments spurred PV adoption worldwide, they also created a highly competitive, volatile, and uncertain market environment.

This report updates the National Renewable Energy Laboratory's (NREL's) c-Si supply-chain costs and projections with the goals of tracking industry progress, clarifying current cost structures, comparing manufacturing economics across regions, and mapping potential pathways toward additional cost reductions. We employ NREL's bottom-up cost modeling methods and accepted accounting frameworks to estimate costs and minimum sustainable prices (MSPs) for each step in the c-Si supply chain: polysilicon, ingots and wafers, cells, and modules. The following are key results.

Our first half of 2018 (1H 2018) MSP benchmark is $0.37/W for monocrystalline-silicon passivated emitter and rear cell (PERC) modules manufactured in urban China. The supply-chain costs for this benchmark build from $15/kg for polysilicon, to $0.12/W MSP for wafers, to $0.21/W MSP for monocrystalline PERC cells. The remaining price elements for module MSP include $0.14/W for module assembly costs and a $0.02/W (15%) module operating margin.

Manufacturing in rural China results in the lowest-MSP wafers, cells, and modules. Although most Chinese production has occurred in urban locations to date, rural Chinese areas with lower labor and electricity costs and lower margins are capable of producing the world's lowest-MSP wafers, cells, and modules. The factory-gate MSPs of modules manufactured in China, Taiwan, Malaysia, and the Philippines are $0.05–$0.20/W (11%–37%) lower than MSPs of modules manufactured in South Korea, the United States, and Germany (Figure ES-1, next page).[1]

The gaps between MSPs in different countries have narrowed over the past decade as the global c-Si PV supply chain has matured. In particular, innovations that have increased the use of automation in manufacturing and thus reduced labor requirements have been effective in narrowing the gaps in MSPs across countries. Examining how further advances in manufacturing processes and module architectures could continue to narrow the gaps in MSPs across countries is an important area for future research.

Benchmark c-Si module MSPs declined $1.18/W (76%) between 2010 and 1H 2018. From 2010 to 2015, the reduction was $0.90/W due to polysilicon price reductions, reduced silver consumption during cell conversion, process engineering, and economies of scale. From 2015 to 1H 2018, the reduction was $0.28/W due to the transition to PERC cell architecture and diamond wire (DW) wafering as well as process engineering and economies of scale (Figure ES-2).

[1] Because we assume substantial national integration of supply chains—with each country producing the wafers and cells used in its modules—the cost differentials compound at each supply-chain step. In practice, many manufacturers source upstream supply-chain components from lower-cost areas (e.g., U.S. and German module manufacturers import cells), which reduces their production costs and MSPs.

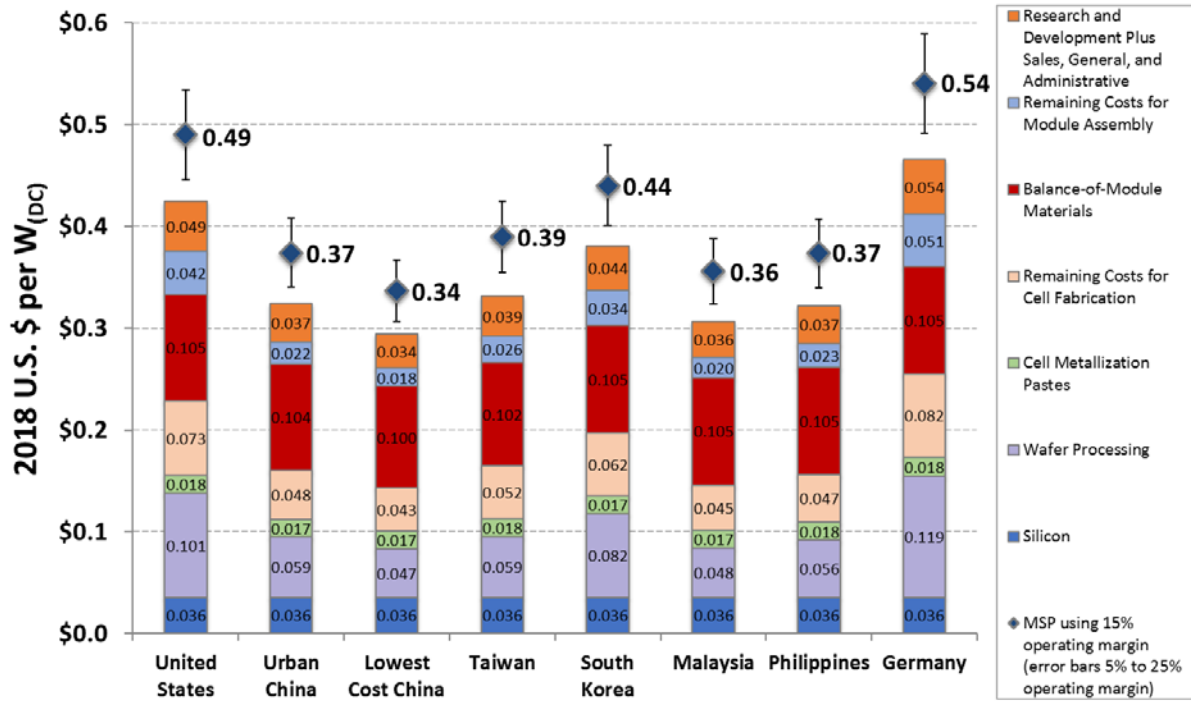


Figure ES-1. Benchmark 1H 2018 MSPs for 60-cell monocrystalline PV modules

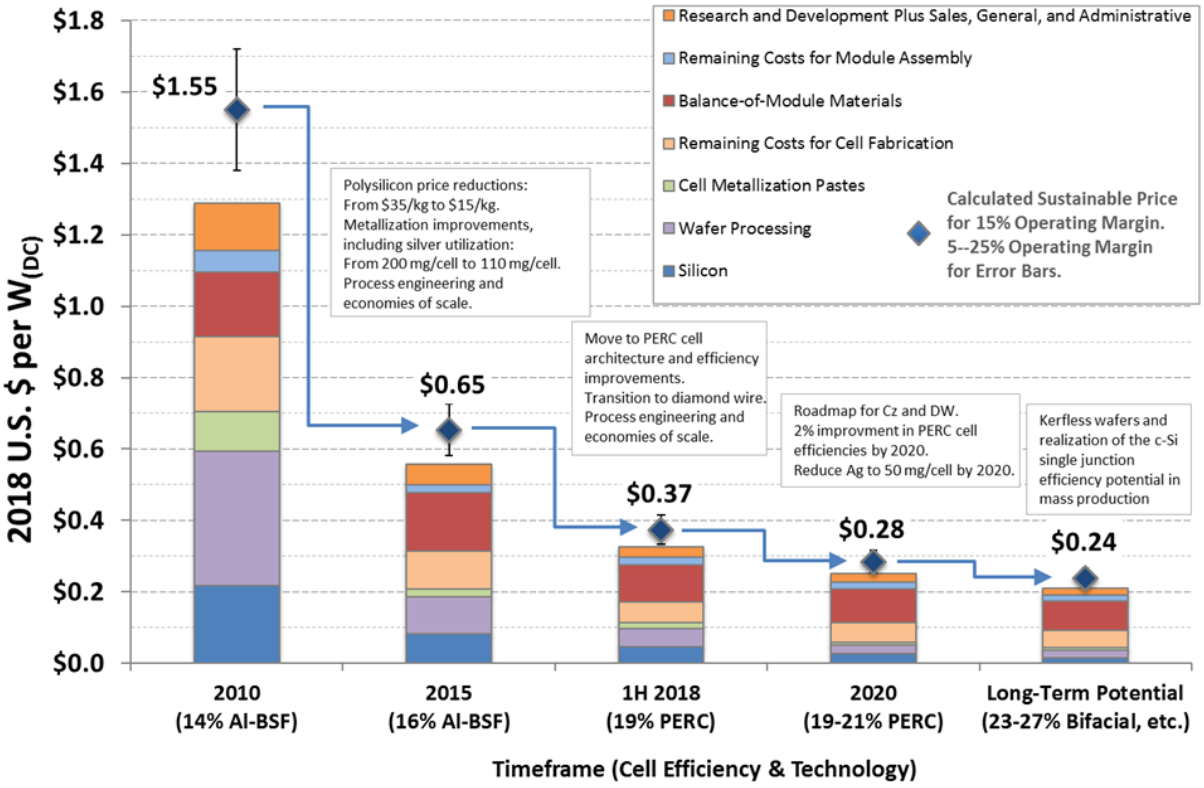


Figure ES-2. Historical, 1H 2018 benchmark, and projected module pricing based on technology advancements and historical economies of scale

Economies-of-scale and market forces that drive pricing levels throughout the supply chain are not included in the projections after 1H 2018.

The cost-reduction road map illustrated in this paper yields monocrystalline-silicon module MSPs of $0.28/W in the 2020 time frame and $0.24/W in the long term (i.e., between 2030 and 2040). These MSPs would be lower by 25% (in 2020) and 35% (in the long term) than our 1H 2018 benchmark. Our road map to the 2020 target depends on thinner wafers, continued transition to DW wafering, reducing silicon and silver utilization, and improving cell efficiencies. Our long-term road map relies on a transition to kerfless wafering and increasing cell efficiencies beyond 23%, which would require advanced cell architectures beyond PERC (Figure ES-2).

Realizing our 2020 cost-reduction road map improvements could help align c-Si module market prices with calculated MSPs that are based on Greenfield manufacturing capacity with positive operating margins. Average module market prices in 2018 have been in the range of $0.20/W to $0.40/W—which is mostly below our 1H 2018 MSP benchmark. This misalignment between market pricing and our modeled MSPs is reflected in negative operating margins for most PV companies. Our road map identifies near-term technology-based cost reductions that could be sufficient to make 2H 2018 market prices sustainable by 2020.

Realizing the technological advancements envisioned in our longer-term road map could provide even deeper c-Si module MSP reductions and/or improved PV system and lifecycle economics. On a per-watt basis, passivated emitter and rear totally diffused (PERT), silicon heterojunction (SHJ), and interdigitated back contact (IBC) cells currently cost more than standard aluminum back surface field (Al-BSF) and PERC cells owing to smaller production scales and use of *n*-type wafers. However, if demand for high efficiency cell architectures grows, these advanced cell technologies may gain market share and their MSPs may decline below our estimates due to benefits from economies of scale. These cell technologies also might offer benefits beyond those reflected in the module price. Cells with higher efficiencies could reduce per-watt balance-of-module and balance-of-system costs. In addition, various cell and module characteristics could improve complete lifecycle system-level PV economics.

In addition, although c-Si remains the dominant PV technology, it would need to continue to compete against evolving alternative PV technologies such as cadmium telluride (CdTe), copper indium gallium diselenide (CIGS), and perovskite modules. This competition would likely drive innovation and cost reductions across all technologies while presenting additional opportunities for system optimization.

Table of Contents

List of Figures

List of Tables

1 Introduction

Over the past decade, the crystalline-silicon (c-Si) photovoltaic (PV) industry has grown rapidly and developed a truly global supply chain. Since 2014, c-Si has accounted for more than 90% of PV production, and it approached 96% of production in 2017 (Mints 2018). Its growth has been driven by increasing consumer demand for PV as well as technical advances in cell performance and manufacturing processes that have enabled dramatic cost reductions. The global spread of the PV supply chain has resulted from the widespread availability of adaptable manufacturing infrastructure, access to capital, and government incentives in many countries and subnational jurisdictions.

Figure 1 is a schematic of the c-Si PV supply chain. Polycrystalline silicon or "polysilicon" is the feedstock used to make monocrystalline- or multicrystalline-silicon ingots, which are then sliced into wafers, fabricated into cells, and finally manufactured into completed modules.

Figure 2 (next page) shows the global distribution of the c-Si PV supply chain at the end of 2017. It is categorized into polysilicon, wafers, cells, and modules, because ingot and wafer production typically occur in concert. Polysilicon production was dominated by China, South Korea, Germany, and the United States in 2017. China and Taiwan dominated wafer and cell production, while module production primarily took place in China, Malaysia, and South Korea. Figure 3 shows details for China and surrounding areas. Jiangsu is China's leading province for c-Si PV-related manufacturing. However, other Chinese provinces and Asian countries have recently experienced very rapid growth in PV manufacturing.

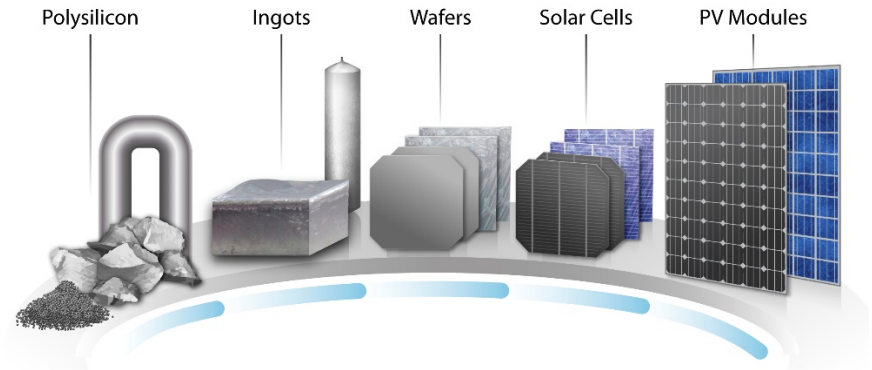


Figure 1. Schematic of c-Si PV module supply chain

The numerous companies entering the PV industry have encountered dynamic market forces and large, sudden price fluctuations. In 2005, average module selling prices were around $4/W, and module demand was very high in some markets owing to high feed-in-tariff rates. Five years later, the market had grown, but average module selling prices were about 50% lower because of an oversupply environment. At the time (2010), considerable disagreement existed about the potential for continued rapid price declines, but ultimately the pace of price reductions accelerated. The average module selling price was below $1/W by 2012 (Mints 2018).

Figure 2. c-Si supply chain for the largest 393 PV-related companies at the end of 2017, based on BNEF (2018) and IHS (2018)

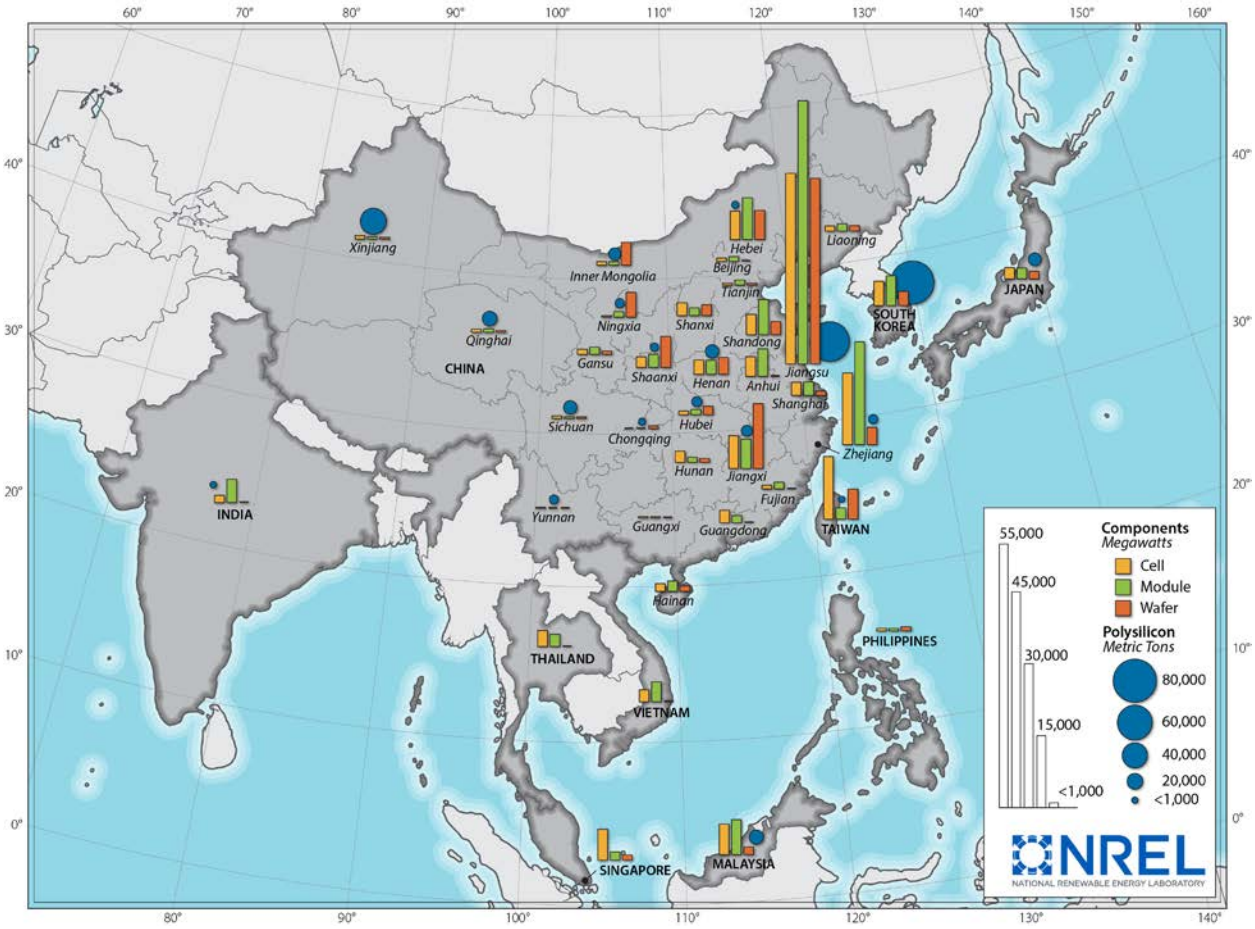


Figure 3. c-Si supply chain in China and surrounding areas at the end of 2017, based on BNEF (2018) and IHS (2018)

In 2018, module prices declined to $0.20–$0.40/W owing to a highly competitive and oversupply environment. The challenge for PV manufacturers is to deliver an industry-respected, high-quality, high-efficiency, bankable, and warrantied product at a competitive selling price—while also reaping an acceptable profit margin. The price pressure of this challenge is passed throughout the supply chain, from modules up through polysilicon production. In this type of competitive environment, it is important to understand the bottom-up cost of current manufacturing as well as potential cost-reduction opportunities that could enable manufacturers to become profitable while maintaining low prices or even reducing prices further.

Documenting the trajectory of c-Si PV prices and the state of the industry enables ongoing monitoring of progress and can validate (or invalidate) expectations of market paradigms over time. A detailed analysis of the supply chain also enables comparison of regional performance, identification of technology improvement opportunities, and mapping of optimal paths toward both expanded and profitable PV manufacturing.

This report updates c-Si PV supply-chain costs and projections generated from detailed bottom-up cost modeling at the National Renewable Energy Laboratory (NREL), which began in 2010 and resulted in our first monocrystalline-silicon PV road map in 2013 (Goodrich et al. 2013). The goal of the report is to provide credible, industry-relevant, and objective analysis of PV manufacturing costs. After a discussion of our data and methods in Section 2, the report is organized by supply-chain step: Section 3 is about polysilicon manufacturing, Section 4 about ingots and wafers, Section 5 about cell conversion, and Section 6 about module assembly. Key manufacturing processes, historical and current cost estimates, and potential road maps to further cost reductions are described. Section 7 highlights important results and areas for further research.

2 Data and Methods

The NREL bottom-up cost-modeling approach is based on the following general process steps, which draw on information from academic and national laboratory researchers, startup companies, multinational corporations, and other PV research and industry participants:

1. Conduct a detailed literature and patent survey of the general technology characteristics and trends.
2. Develop a detailed step-by-step process flow to represent how the current or proposed technology is (or would be) built in a high-volume manufacturing environment.
3. Identify relevant materials and equipment suppliers that specialize in each step of the manufacturing process.
4. Network with materials and equipment suppliers to collect relevant insights about the supply chain and cost-of-ownership inputs. When possible, work closely with multiple equipment vendors for each step in the manufacturing process to organize equipment information into a cost-of-ownership estimator that uses the international standard cost-of-ownership protocol for semiconductor manufacturing equipment, referred to as SEMI E35 (SEMI International Standards 2018).
5. Compile and review the inputs and results with integrated manufacturers.
6. Continuously seek to refine the accuracy and relevance of the results over time.

The following subsections detail the cost inputs, including fixed and variable costs (Section 2.1); research and development (R&D) and sales, general, and administrative (SG&A) costs (Section 2.2); and profit margin (Section 2.3).

2.1 Fixed and Variable Costs

We organize fixed and variable cost calculations based on standard accounting practices, for both our total cost calculations and our calculations of costs by process step. Two frameworks are most typically used, accepted, and understood by the financial and investing communities: the U.S. Generally Accepted Accounting Principles (GAAP) put forth by the Financial Accounting Standards Board, and the International Financial Reporting Standards (IFRS) established by the International Accounting Standards Board.

Under both GAAP and IFRS, the first general cost category—which is typically the first line item on a company's income statement—is the cost of goods sold (COGS), sometimes called the cost of sales or the cost of revenue. COGS should include all direct costs for converting raw input materials into finished inventory that is ready for shipping to customers. These direct costs include fixed and variable elements.

In general, fixed costs represent what is essential for sustaining company management as well as the committed, long-term investment in manufacturing infrastructure. For PV manufacturing, fixed investments are typically reported as a depreciation expense following a linear annual schedule. The initial investments are referred to as capital expenditures (CapEx) and the depreciation expenses are eligible for a tax deduction for a given number of years which typically defines the useful lifetime of the equipment. The length of the schedule varies from 5–

10 years for manufacturing equipment and 15–25 years for buildings and other facilities. In this report, CapEx investments are translated into an average annual depreciation expense by taking the total initial CapEx and dividing by the number of years that the depreciation expense tax deduction is available. For the purpose of our analysis, we assume equipment and facilities have no residual value and would need to be replaced and updated at the end of their depreciation schedule.

Variable costs (or "cash" costs) are typically compiled at the conclusion of each accounting period, either on a full fiscal year or quarterly basis. Cash costs include the cost of material to be converted into the product, any other consumable materials, all direct manufacturing labor costs, electricity for the equipment and building, and any spare parts or labor for maintenance. These items are typically paid for with working capital, which is the cash available to a firm at a point in time. Cash costs indicate whether sale of a product at current or projected market prices would cover the costs that otherwise could be avoided by shutting down production. In some cases, a firm may continue selling at prices below cash costs. Although this is not a viable long-term business strategy, firms often do it to gain sales and market share in the short term. Such firms must be careful to maintain adequate working capital (to avoid bankruptcy) and to continue to push their manufacturing costs down. Covering or surpassing both variable and fixed costs also helps firms acquire and retain equity financing in order to expand their operations and gain market share.

The fixed and variable cost elements that we collect include the following (Robinson et al. 2015):

- Variable (cash) cost elements within COGS
    - Input materials
    - Direct manufacturing labor
    - Electricity
    - Maintenance of manufacturing equipment and facilities
- Fixed (non-cash) cost elements within COGS
    - Manufacturing equipment
    - Building and any facility-related expenses that can be capitalized

2.2 R&D and SG&A Costs

Beyond the items typically included in COGS, expenses associated with long-term competitiveness include R&D and SG&A. Depending on the nature of the activities and the tax codes of the reporting authorities, R&D expenses can be amortized over multiple accounting periods or paid with working capital and recorded as an expense during the given accounting period. SG&A expenses—which include overhead personnel and other administrative expenses such as compensation for executives, human resources, and accounting staff—are typically expensed as incurred within a given accounting period.

Because the resources committed to R&D and SG&A vary widely across companies, constructing a bottom-up cost model for these items can be difficult. We rely on statistics from company income statements, where R&D and SG&A expenses are typically reported separately from COGS. Publicly traded companies are required to disclose these items per the standards of public equity trading exchanges. Based on the income statements of the top 12 publicly traded PV firms—with total revenues of approximately $22.5 billion in 2016—we calculated R&D expenses as 1.98% ± 0.76% of revenues and SG&A expenses as 10.7% ± 1.69% of revenues (±90% confidence intervals). Thus, throughout the rest of this report, we set R&D expenses at 2% and SG&A expenses at 11% when calculating overhead expenses.

2.3 Profit Margin

Estimating the profit margin required for a firm to keep operating or expand is a complex calculation based on the firm's stage of growth, expected returns, working capital needs, and other factors. The profit margin a firm can actually attain depends on its cost structure and the industry's supply and demand situation. Figure 4 shows gross profit margins, or "gross margins" (calculated by subtracting COGS from revenues and dividing the result by revenues), and operating profit margins, or "operating margins" (calculated by deducting R&D and SG&A expenses from the gross profit margin and dividing the result by revenues), for 16 publicly traded PV manufacturing firms since 2010 based on data from Bloomberg L.P. (2018). The gross margin has typically remained below 20% since 2011 and has varied by more than 50% in the past two years. The operating margin has remained below 10% since 2011 and has typically gone negative in at least one quarter each year.

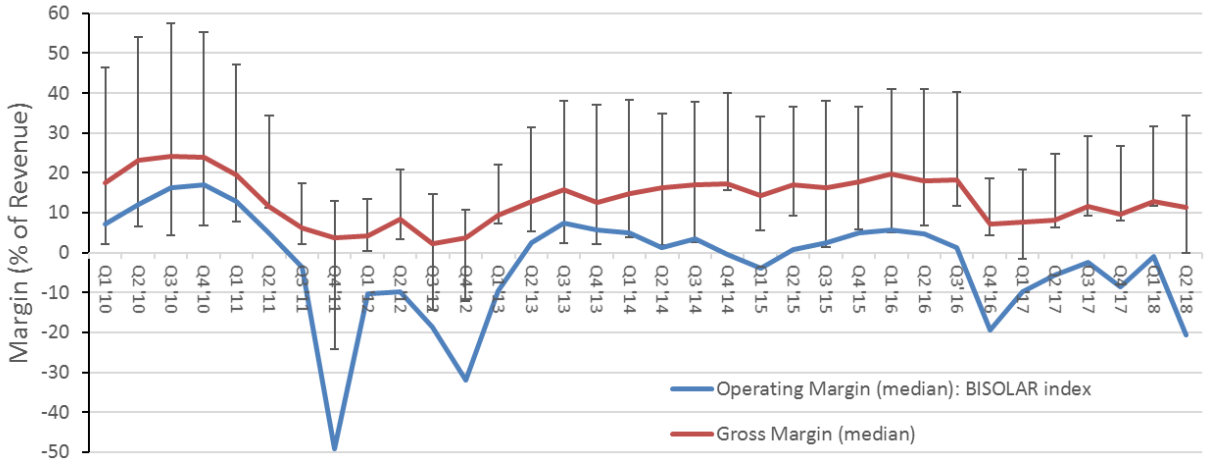


Figure 4. Gross margins for 16 publicly traded PV manufacturers with lines showing median values and error bars showing 20th and 80th percentiles, and operating margin median from the BISOLAR index reported on Bloomberg L.P. (2018)

Figure 5 displays module prices per watt as a function of total global shipments during 1999–2017 based on data from Mints (2018), showing prices dropping by nearly an order of magnitude over the interval represented in Figure 4. Despite the PV industry's recent unstable and relatively low operating margins, it has continued to attract considerable investment and experience rapid growth.

Generally, firms can survive if their revenue is greater than their variable costs. However, for the purposes of this report, we assume a positive operating margin is needed to sustain a business over the long term. To estimate the minimum sustainable price (MSP) for a given PV product, we evaluate a range of margins in this report. All MSP values presented in this report are quantified for three cases: low case, base case, and high case. The low-case MSPs are estimated assuming a 5% operating margin, the base-case MSPs use a 15% operating margin, and high-case MSPs use a 25% operating margin. These are indicated on subsequent graphs by a diamond for the base case, and by overlapping whisker error bars for the low and high cases.

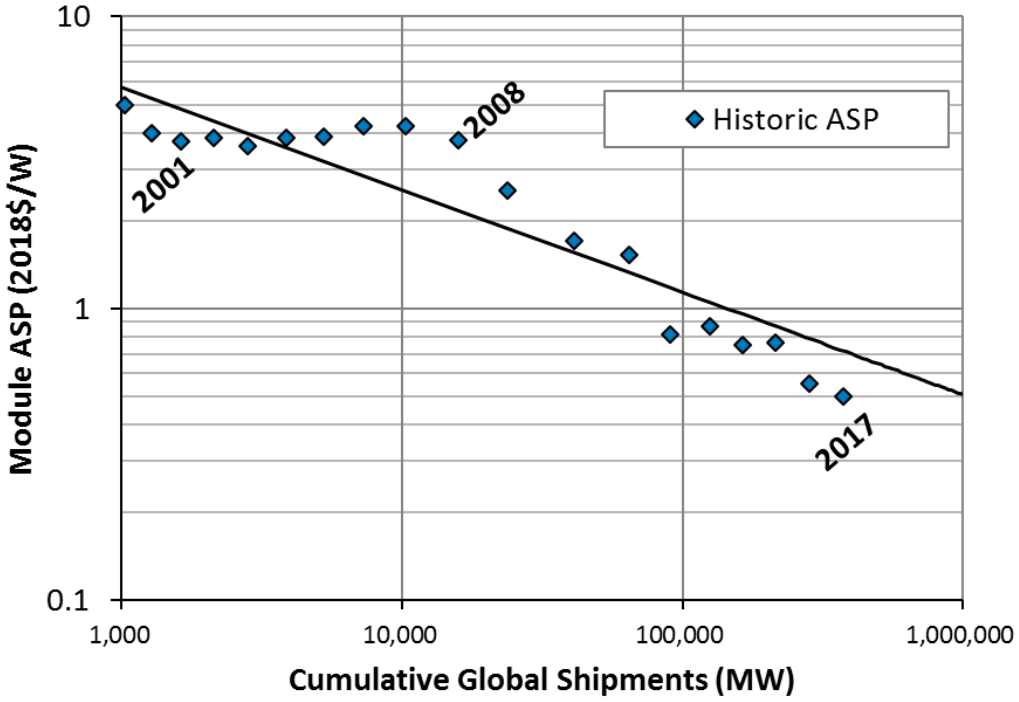


Figure 5. PV module cumulative global shipments and average selling price (ASP), 1999–2017 (logarithmic scales), based on data from Mints (2018)

3 Polysilicon

A wide range of patents, trade secrets, and material-processing routes differentiates various approaches to polysilicon production. We focus on the two most commonly discussed approaches with significant market share: 1) the Siemens chemical vapor deposition (CVD) method, which has greater than 90% market share and typically uses the trichlorosilane ($HSiCl_3$, or TCS) precursor; and 2) the fluidized bed reactor (FBR) method, which has 3%–5% market share and uses the monosilane (SiH_4, or silane) precursor exclusively (Fu, James, and Woodhouse 2015; Bernreuter 2016).

The precursors are manufactured from metallurgical-grade silicon (mg-Si), which is defined as 99% pure silicon (also referred to as "2 nines" or 2N). TCS is manufactured using hydrochloric acid via various synthesis routes (such as direct chlorination or hydrochlorination). Monosilane can be manufactured from hydrochloric acid, magnesium, sodium, or lithium compounds and other compounds (Seetharaman et al. 2013). The final polysilicon product of either process is typically 9N, which is often referred to as "solar grade," or 11N, which is called "electronic grade." These labels are misleading, however, because the PV industry uses both grades and higher purity can yield higher cell efficiencies (Coletti 2011).

We model two Siemens processes that rely on TCS to produce 9N ("solar grade") polysilicon, or "electronic grade" polysilicon up to 11N purity. We also model an FBR process that uses silane and produces polysilicon at purity grades from 8N to 11N.

In general, the Siemens process involves passing a gaseous TCS or silane precursor over heated silicon filaments that are housed within bell-shaped reaction vessels. The precursor is cracked into pure silicon, which deposits onto the filaments. Various hydrogen-, silicon-, and chlorine-containing compounds are also recovered, separated, and recirculated back into the bell jars. Details on how these compounds are handled and recirculated differ depending on the precursor synthesis technique for a given system, because some remaining compounds can serve as inputs to synthesize new mg-Si into TCS or silane precursors. Ultimately, the Siemens CVD process yields U-shaped silicon rods that are later broken into chunks and sealed in plastic bags with an inert gas like argon.

To initiate the FBR process, a floating bed of silicon beads is created by directing the fluidizing gases silane and hydrogen upward through the entrance of a very large, inverted cone-shaped reaction vessel. Through careful control of the temperature differential between the fluidized silicon beads and the walls of the reactor, the silane compound is then cracked into additional silicon layers that build up layer-upon-layer onto the surface of the beads. Eventually—once the downward gravitational pull of the FBR beads overwhelms the upward force of the fluidizing gases—the heaviest beads fall to the bottom of the reactor cone, where they are collected. The end result of the FBR process is granular polysilicon.

Owing to their fundamental differences in production, the Siemens and FBR approaches have different variable and fixed cost drivers. Table 1 provides a high-level overview of the most recent and relevant inputs that we collected and used within our cost models, based on state-of-the-art greenfield production facilities large enough to realize economies of scale (about 15,000 metric tons [MT] per year) (Fu, James, and Woodhouse 2015). Additional cost inputs include

per-unit costs for labor, electricity, and additional consumables. International labor rates are publicly available from the U.S. Bureau of Labor Statistics (BLS 2018). Electricity rates for a number of countries are available from the U.S. Energy Information Administration (EIA 2018).

Table 1. Overview of Inputs Used in NREL's Polysilicon Cost Models

Typical 2017 Variable Cost COGS Elements for Polysilicon Production	
Principal input materials	Siemens: mg-Si, HCl, H_2, Si filaments, argon, and packing bags FBR: seed granules, SiH_4, H_2
Labor intensity (range is for United States/EU–China)	Siemens: 25–16 MT/year per direct employee FBR: 50–30 MT/year per direct employee
Energy input requirements	Siemens: 50–65 kWh/kg equivalent for electricity and steam for solar grade (9N), 65–80 kWh/kg equivalent for electricity and steam for electronic grade (11N). FBR: 30–40 kWh/kg equivalent including electricity and natural gas
Maintenance needs	Annual cost equivalent to 4% of the original equipment and facilities investment
Typical 2018 Fixed Cost COGS Elements per kg of Polysilicon Production at 15,000 MT/year Scale	
CapEx including engineering, procurement, and construction (EPC)	Original CapEx of: (1) Siemens solar grade: $40–$45/kg in the United States, South Korea, or Europe and $30–$35/kg in China. (2) Siemens electronic grade: $45–$50/kg in the United States, South Korea, or Europe and $35–$40/kg in China. (3) FBR: $45–$55/kg in the United States, South Korea, or Europe and $35–$45/kg in China. As an industry convention, the CapEx is then allocated over a 10-year straight-line depreciation schedule.
Remaining Fixed Operating Expenses	
R&D	2% of revenues
SG&A	11% of revenues

Figure 6 shows the resulting direct manufacturing cost—per kilogram of polysilicon chunk—for each major step of the Siemens process using hydrochlorination TCS synthesis within the United States, assuming greenfield production of solar-grade polysilicon (9N) at 15,000 MT/year for a total CapEx of $40/kg. The convention for the polysilicon industry is to assume a 10-year linear depreciation schedule for the capital equipment purchase and EPC charges, and a 20-year linear depreciation schedule for any onsite buildings. The costs in Figure 6 sum to $15.4/kg, where roughly 20% is from mg-Si, 25% from other materials, 12% from energy, 12% from labor, 10% from maintenance, and 21% from depreciation.

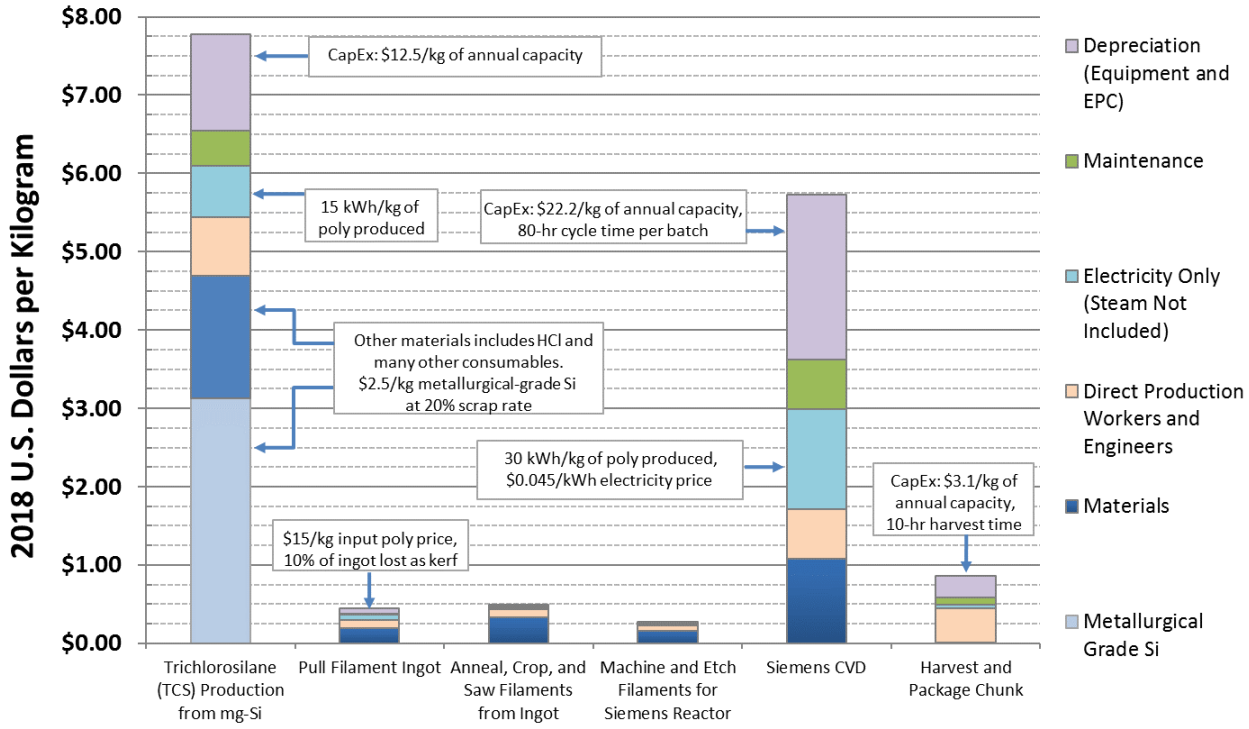


Figure 6. Direct manufacturing cost estimates for U.S. polysilicon production using the Siemens CVD/TCS hydrochlorination approach

The analysis assumes 2018 state-of-the-art greenfield manufacturing capacity of solar grade polysilicon (9N) at 15,000 MT/year, which corresponds to $40/kg total CapEx (including EPC) allocated over 10-year straight-line depreciation.

The cost structure shown in Figure 6 would vary based on manufacturing location, resulting from different local labor and electricity rates as well as proximity to and relationships with suppliers. Even if the same firm were to use the same technology in different locations, there would often be significant differences in the initial CapEx, primarily because different EPC costs arise owing to region-specific EPC labor and construction material costs. For example, it would be advantageous to be located near specialty pipe suppliers who can supply key plant components at relatively low cost.

As an initial estimate, the CapEx for a greenfield polysilicon plant within the United States, European Union countries, South Korea, or Japan would be about 25% higher than a similar plant in a lower-cost region including China. This is shown more explicitly in Figure 7, which compares total polysilicon production costs and MSPs between U.S. and Chinese locations. The costs in this figure include the direct manufacturing costs shown in Figure 6 as well as R&D and SG&A costs, while MSPs are denoted above the bars by diamond markers with whiskers that include operating margins. The two Chinese locations were chosen to represent a higher-cost urban site and a lower-cost rural site, because most Chinese production has occurred in urban locations to-date, but plants are also being developed in rural areas with lower labor and electricity rates.

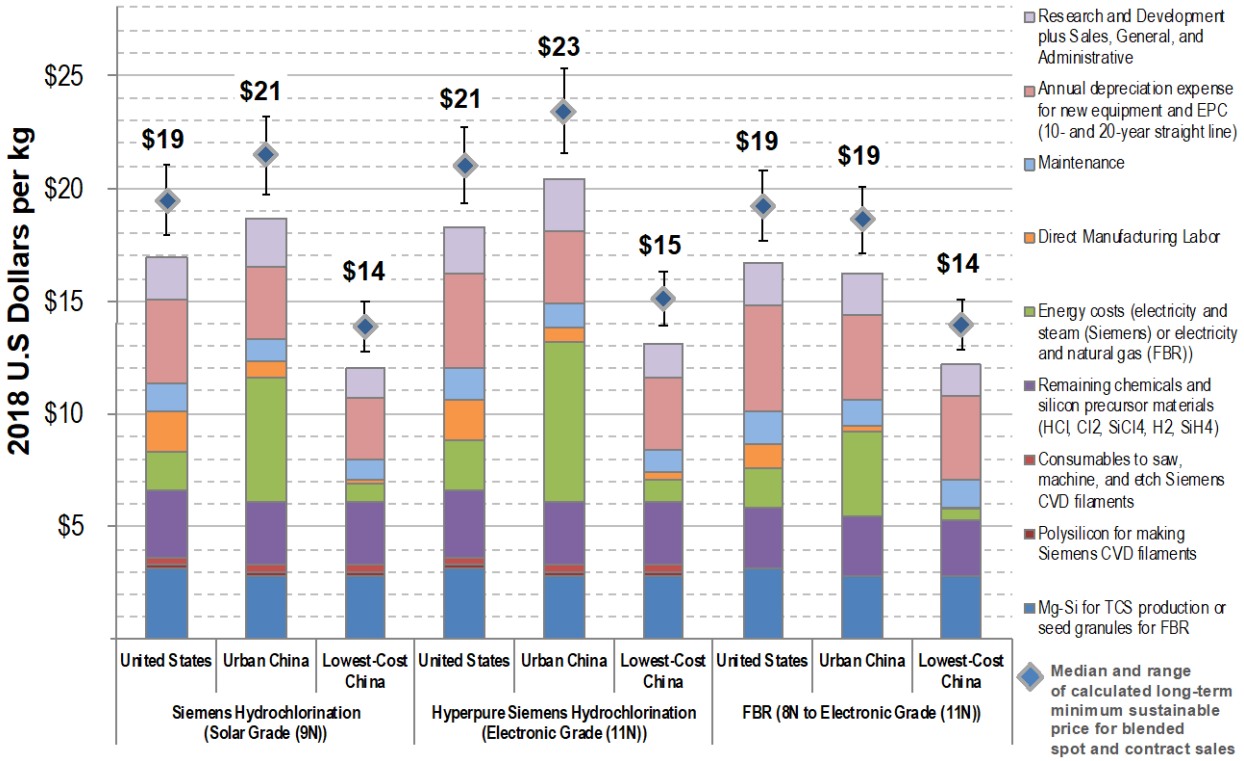


Figure 7. Total manufacturing cost and MSP estimates for Siemens and FBR polysilicon production using state-of-the-art technologies

The analysis assumes 2018 state-of-the-art greenfield manufacturing capacity of 15,000 MT/year.

For the two Siemens processes, the urban Chinese location is calculated be more expensive than the U.S. location by about $2/kg. However, for the FBR process, the U.S. location would be slightly more expensive than the urban Chinese location. The FBR process differs significantly from the two Siemens processes in that energy use is approximately half. For both Siemens processes and the FBR process, MSPs would be $5–$6/kg lower in the rural Chinese location than in the U.S. location. This reflects the market trend to expand into areas that combine the lowest CapEx, lowest direct manufacturing cash costs, and greatest access to capital.

Our modeling suggests FBR's cash costs ($7—$10/kg) are lower than for Siemens ($8–$15/kg). The use of FBR also enables unique and potentially important options related to the ingot and wafer steps of the supply chain, highlighting the need to understand implications along the entire value chain when examining the long-term competitiveness of various processes. The granule-sized polysilicon resulting from the FBR process permits more infilling of a crucible, which increases the initial "charge weight" (weight of polysilicon added to the crucible), reduces the amount of time to reach this weight, and thus would increase productivity and reduces costs. The granule product is also more suited to continuous-Czochralski (Cz) ingot pulling, which could enable higher-quality crystals as well as cost reductions compared with batch Cz processes (Bernreuter 2014). The limited market size of FBR relative to Siemens reflects technology execution that has historically been limited to just a few players.

Reported polysilicon production costs and prices vary from our estimates. Commonly, polysilicon firms only report cash costs, which ranged from $6/kg to $27/kg in 2017. Figure 8

depicts major polysilicon firms, their cash costs, and their market shares. Thus, our state-of-the-art cash cost estimates of $8–$15/kg (Siemens) and $7–$10/kg (FBR) are at the lower end of the reported range.

Our median estimated MSPs of $14–$23/kg (Siemens) and $14–$19/kg (FBR)—which include all-in production costs plus sustainable margins—tend toward the higher end or above the 2016/2017 global ASP for solar grade polysilicon of $14–$18/kg (Osborne 2017). One reason for the difference could be our assumption of a 2018 benchmark state-of-the-art greenfield facility. In practice, many existing polysilicon firms use legacy assets that may have had a different initial CapEx (for example if purchased during a bankruptcy proceeding), or might have different depreciation expenses and schedules, or are operating while fully depreciated. In addition, differences between our assumed operating margins versus actual operating margins can explain some of the differences between our calculated MSP values versus market pricing.

The remainder of our analysis assumes a single, global polysilicon MSP of $15/kg. This MSP represents the higher end of China's least-expensive polysilicon (Figure 7). All other supply-chain steps are nationally integrated in our analysis, with each country assumed to produce the wafers and cells used in its modules. However, because few countries have polysilicon capacity (as illustrated in Figure 2), we assume a global polysilicon supply base for our ingot and wafer model in the following section.

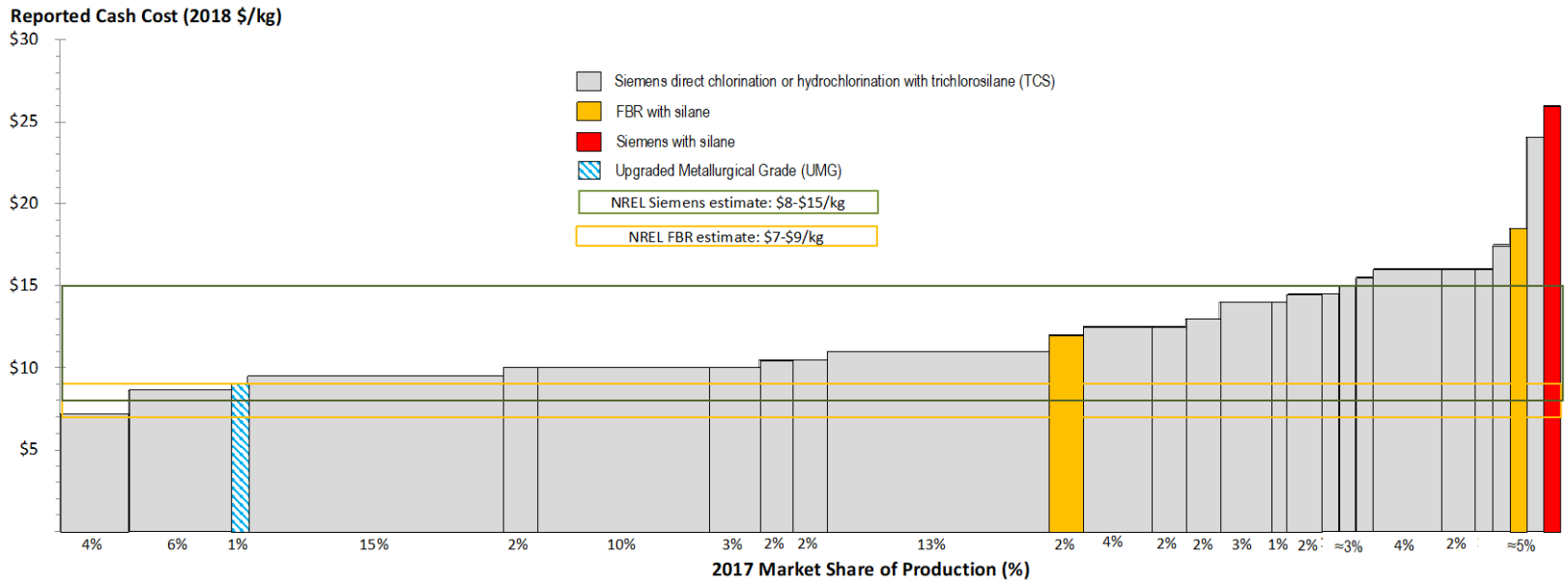


Figure 8. Cash costs reported by the world's largest polysilicon producers and each firm's share of the global 450,000–500,000 MT of production in 2017 (Bernreuter 2016)

unless otherwise indicated, these firms have most of their manufacturing operations in China.

4 Ingots and Wafers

This section provides manufacturing process descriptions, current modeled costs, and a cost road map for c-Si ingots and wafers.

4.1 Manufacturing Processes

The PV industry currently uses two primary routes for converting raw polysilicon feedstock into finished wafers: the monocrystalline route using the Cz process, and the multicrystalline route using the directional solidification (DS) process. The primary differences between these two approaches are in how the polysilicon is melted, how it is formed into an ingot, the size of the ingot, and how the ingots are shaped into bricks for wafer slicing.

The Cz method creates a cylindrical ingot, and this is followed by multiple steps of band and wire sawing to produce wafers, as depicted in Figure 9. For a typical 24-in diameter crucible loaded with an initial charge weight of about 180 kg, approximately 35 hours are required to melt the polysilicon in a Cz crucible, dip the seed crystal into the melt, and pull out the neck, shoulder, body, and end cone. The result is a cylindrical Cz ingot with a mass of 150–200 kg (Steps 3–7 in Figure 9). To leave metals and other contaminants behind, it is necessary to leave 2–4 kg of pot scrap in the crucible.

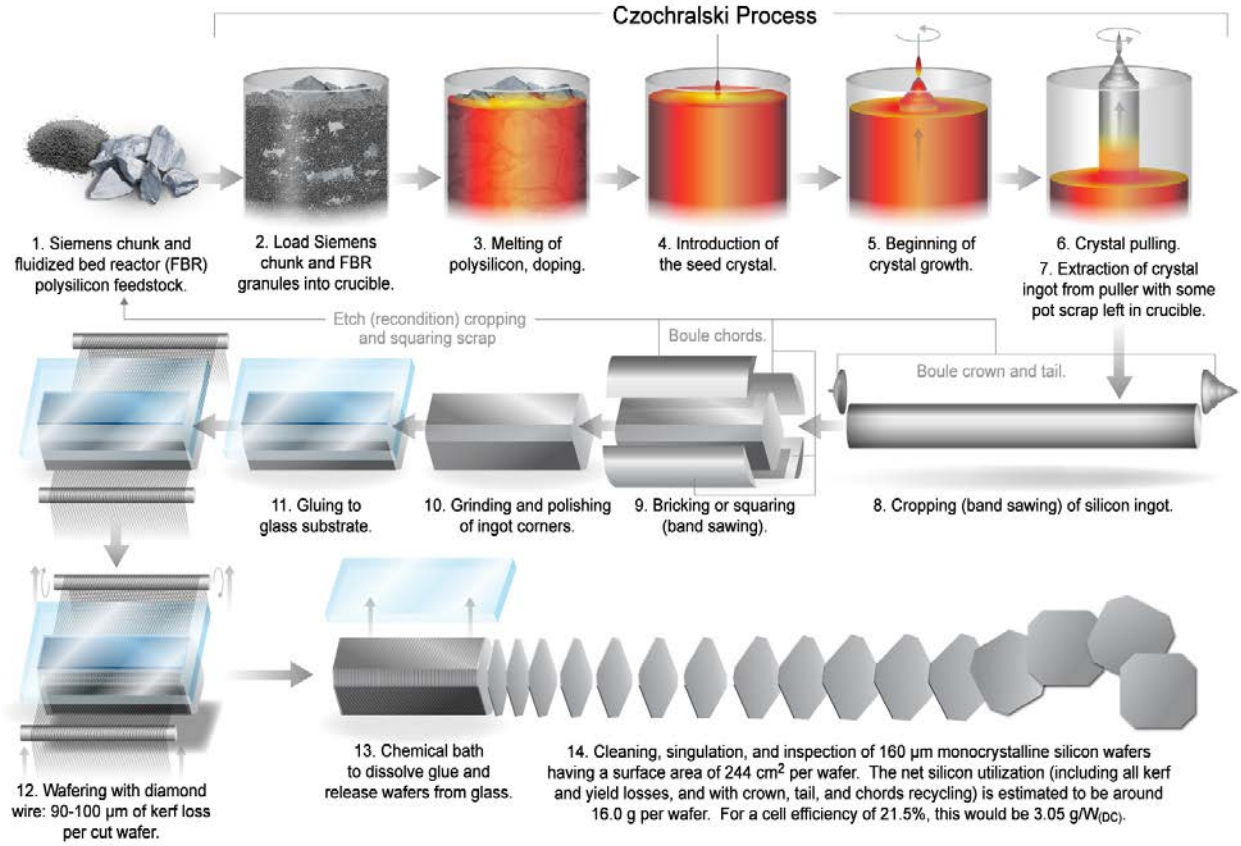


Figure 9. Process flow for making monocrystalline-silicon wafers via Cz crystal growth

A mixture of Siemens chunk and FBR granules are melted in a Cz ingot puller, and the ingot is then shaped and sliced into wafers.

Prior to 2005, monocrystalline-silicon modules were often composed of circular cells that had been fabricated on wafers cut directly from cylindrical ingots. However, today most Cz ingots are trimmed into "pseudo-square" bricks that permit greater cell packing density on modules while minimizing ingot and wafering costs. The pseudo-square cross section is made by sawing the ingot lengthwise after cropping off the tops and tails, as depicted in Steps 8 and 9 of Figure 9. The exposed surfaces then undergo polishing and grinding to produce smooth surfaces and rounded corners (Step 10). The current industry trend is to produce Cz wafers in the "M2 format," which is a specific 156.75 mm x 156.75 mm flat-to-flat cross-section with total surface area of 244 cm^2. After gluing the pseudo-square brick to a glass plate (Step 11), the entire unit is placed into a wire sawing machine where strands of wire slice the brick into individual wafers—like a baker slices a loaf of bread (Step 12). The glue is dissolved by immersing the sliced brick and glass backing plate in a chemical bath (Step 13). This ultimately produces around 5,000–6,000 wafers per ingot. Finally, the wafers are cleaned and inspected for signs of breakage.

Multicrystalline DS wafers are fabricated from shorter but much wider and heavier ingots—around 800 kg—that assume a cube shape when the polysilicon is melted within a quartz crucible. The process is depicted in Figure 10. After the polysilicon is melted, the DS process is induced by creating a temperature gradient where the bottom surface of the crucible is cooled at a certain rate. Similar to Cz ingots, sections of DS ingots produced during cropping and squaring can be remelted for later ingot generations. In the case of DS ingots, however, the topmost section is usually not recycled owing to the high impurity concentration.

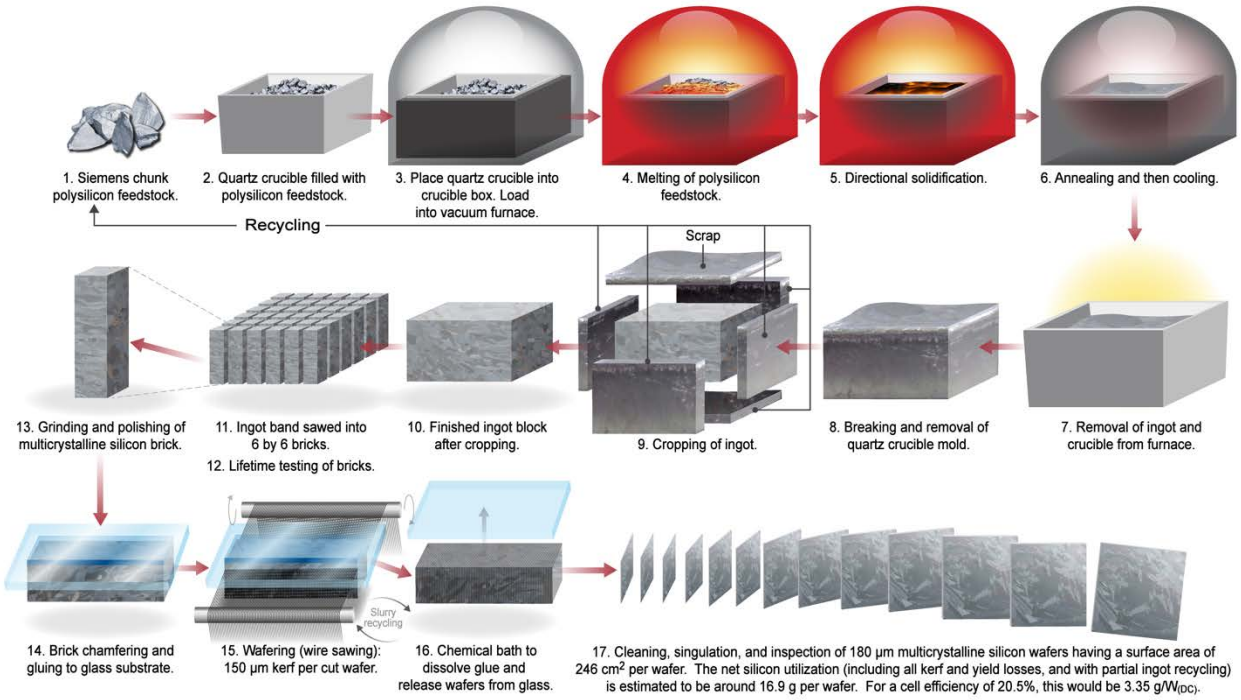


Figure 10. Process flow for making multicrystalline-silicon wafers via DS

Because the process begins with a cube-shaped melting crucible, DS ingots and wafers are naturally square in shape, making it easy to create multicrystalline-based cells that can occupy essentially the entire area within a complete module. About 76 hours are required to produce a typical DS-silicon ingot, which is sawn into 36 bricks from a 6 x 6 cutout. A typical finished brick (Step 13 in Figure 10) has a 156.75 mm x 156.75 mm full-square cross-section (246 cm^2 of surface area) and a height of 286 mm, which yields 1,040 wafers per brick when the wafer thickness is 180 µm and there is 95 µm of kerf loss per wafer. Thus, 35,000–40,000 wafers are produced per DS ingot.

4.2 Modeled Current Costs

Table 2 provides an overview of the variable and fixed elements needed to calculate the costs for ingot and wafer processes. Figure 11 (monocrystalline Cz) and Figure 12 (multicrystalline DS) show aggregated step-by-step cost details for each of the four primary workstations in a model ingot and wafer manufacturing facility in urban China, where most mono- and multicrystalline ingot and wafer production occurs.

Translating input polysilicon costs ($/kg) into net silicon wafer costs ($/wafer) depends on:

1. How much silicon is present in a finished wafer
2. Kerf losses during ingot cropping, squaring, grinding, and polishing
3. Kerf losses during wafer slicing
4. Identification of which sections of an ingot can be remelted and which cannot
5. Accounting for pot scrap left in the crucible
6. Accounting for all yield losses occurring between producing an ingot and containerizing fully finished and crack-free wafers.

The first step is to calculate the mass of silicon present in a finished wafer. Assuming a typical wafer thickness of 160 µm and an M2 format surface area of 244 cm^2, we calculate a silicon mass of 9.10 g in a finished monocrystalline wafer (the density of silicon is 2.33 g/cm^3). For a multicrystalline wafer, assuming a typical wafer thickness of 180 µm and a surface area of 246 cm^2, we calculate a silicon mass of 10.3 g in a finished multicrystalline wafer. Using our $15/kg input polysilicon price yields a first-order estimated silicon cost of $0.136 for each monocrystalline Cz wafer and $0.155 for each multicrystalline DS wafer.

Next, the amount of silicon lost over the course of making an ingot and making the finished wafers must be accounted for. This includes material produced as sawing dust (referred to as "kerf") during cropping, squaring, grinding, polishing, and wafering, all of which is far too contaminated for direct reuse. In principle, all these kerf losses could be recycled and repurified, but in practice this is generally cost prohibitive.

Typically, 90–120 µm of silicon are lost per wafer during wafer slicing, with the range representing the tradeoff between higher kerf loss due to using thicker wire but also improved wire life and higher sawing equipment uptime. Our cost model results reflect a 1H 2018 achievable but state-of-the-art value of 95 µm of kerf loss per wafer. For the wafers described here, the physical wafer plus wafer slicing kerf loss brings the silicon cost to $0.217 per

monocrystalline Cz wafer and $0.236 per multicrystalline DS wafer. The kerf losses from ingot cropping, squaring, grinding, and polishing account for only about 5% of the total net kerf loss. We also account for yield losses throughout the entire process. This includes pot scrap losses (Cz process) or ingot top losses (DS process); both of these scrap types contain too many contaminants to be used. Another significant yield loss results from the fact that many wafers do not pass inspection tests owing to microcracks and/or contactless electrical performance characterization.

Table 2. Overview of Inputs Used in NREL's Cz and DS Ingot and Wafering Cost Models

2017–2018 Typical Variable Cost COGS Elements for Ingots and Wafering	
Polysilicon consumption	A function of wafer thickness (160–180 µm) and kerf losses (90–120 µm per wafer). The net silicon utilization is also a function of yield losses during ingot cropping and squaring, wafer slicing, microcrack inspection, and contactless carrier lifetime testing.
Remaining consumables	Cz or DS crucibles, seed crystals, dopants (B_2O_3 for p-type base, or phosphorous for n-type base),a insulation chamber and graphite heating elements, argon gas, cutting blades for cropping and squaring, cooling water, brick adhesive, grinding and polishing materials, steel or diamond wire, cutting fluid (slurry or water for diamond wire), and aqueous-based solutions for wafer cleaning.
Labor	0.9–1.3 direct laborers per MW, depending on local labor rates and company experience.
Electricity	Total of 0.7–1.1 kWh per Cz wafer or 0.3–0.4 kWh per DS wafer.
Maintenance	Per annum cost equivalent to 4% of the original equipment and facilities investment.
2017–2018 Typical Fixed Cost COGS Elements for Ingots and Wafering, in Facilities with Annual Production Capacity of 1 GW	
Depreciation on capital equipment	Original CapEx of $0.07–$0.10/W of capacity for Cz and $0.02–$0.05/W of capacity for DS. A working assumption is 7-year straight-line depreciation for DS furnaces, 10-year straight-line depreciation for Cz pullers, and 7-year straight-line depreciation for all other testing, ingot-shaping, and wafering equipment.
Depreciation of manufacturing facilities	Original CapEx of $0.02–$0.06/W for new facilities, 20-year straight-line depreciation.
Remaining Fixed Operating Expenses	
R&D	2% of value-added revenues (total revenues minus polysilicon input cost)
SG&A	11% of value-added revenues (total revenues minus polysilicon input cost)

[a] P-type wafers are used in cell types that are widely available on the 2018 market, namely the standard aluminum back surface field (Al-BSF) cells and passivated emitter and rear cells (PERC). N-type wafers are less common but are needed for some advanced cell architectures.

From this, we can calculate net silicon utilization, which represents the net mass of input polysilicon material needed to produce a finished wafer after accounting for the wafer thickness, kerf losses, pot scrap, ingot top, and other yield losses. In state-of-the-art 2018 facilities, 1 kg of polysilicon input to the crucible yields 62–63 Cz wafers or 57–59 DS wafers, equivalent to a net

silicon utilization of around 16.0 g per M2 format Cz wafer or 17.2 g per DS wafer. This results in a final total net silicon cost of $0.238 per wafer for monocrystalline Cz and $0.254 per wafer for multicrystalline DS. The polysilicon costs shown in Figure 11 and Figure 12 illustrate where polysilicon is used or lost as kerf or yield losses during each step of wafer fabrication.

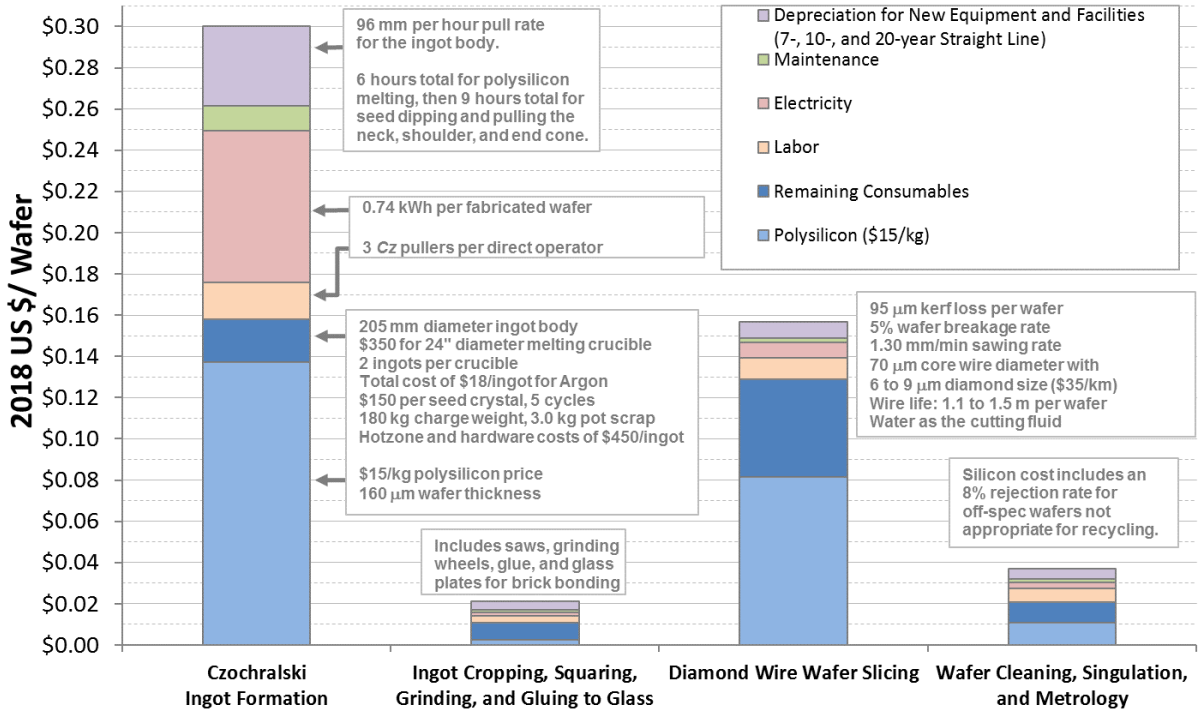


Figure 11. Step-by-step costs for monocrystalline Cz wafer manufacturing in urban China

The analysis assumes a 1-GW manufacturing facility in urban China, 244-cm2 wafer area (M2 format), 160-μm wafer thickness, 16 g of net silicon per wafer, and 0.86 kWh of total electricity per wafer.

Beyond the other consumables identified in Figure 11 and Figure 12, we estimate the remaining direct manufacturing costs within COGS (labor, electricity, maintenance, and depreciation) by working with the relevant materials suppliers and manufacturing equipment vendors to obtain cost-of-ownership information for each tool. The costs by step in Figure 11 and Figure 12 are based on data provided by five equipment vendors and two integrated manufacturers that have significant activities in Asia.

The ability to commission manufacturing facilities in essentially any country leads to some simplifying assumptions for country-by-country cost calculations. First, although some shipping and logistics costs vary between countries, all the consumables needed to convert raw polysilicon into wafers could be easily acquired from numerous suppliers and shipped essentially anywhere on the globe. Fully functioning, quality manufacturing equipment is also available for purchase from different equipment vendors, and all vendors are generally willing to sell to almost anyone in the world at guaranteed throughput and yields. Most equipment vendors can also provide local workforce training if the customer requests it.

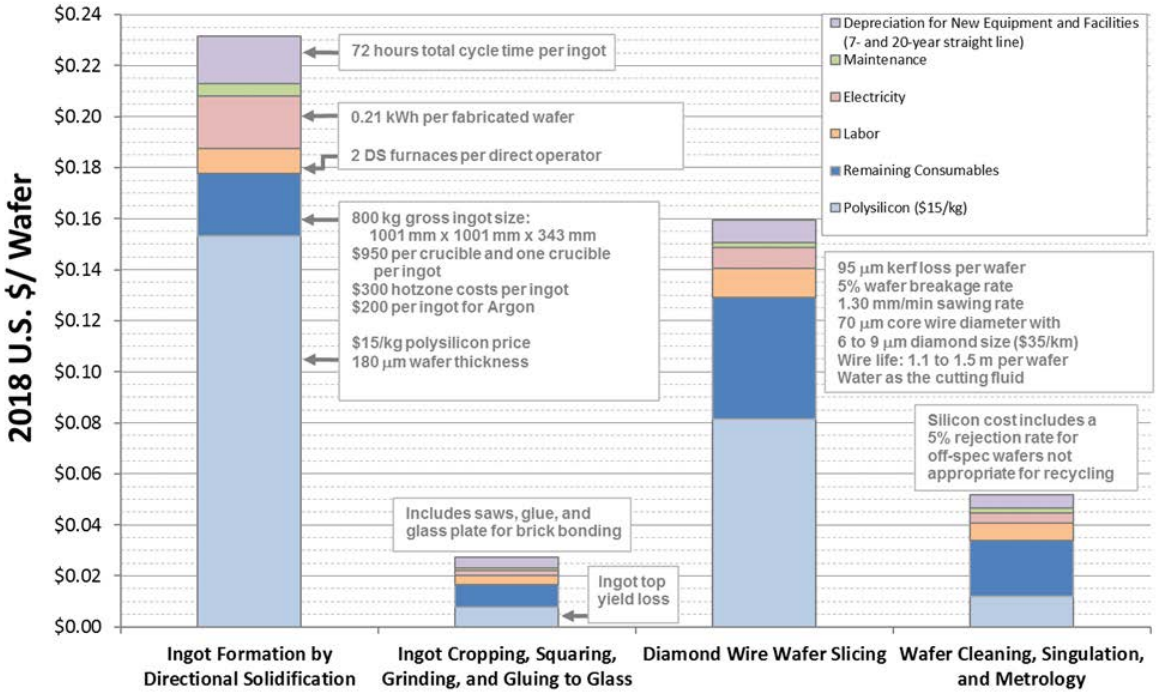


Figure 12. Step-by-step costs for multicrystalline DS *p*-type wafer manufacturing in urban China

The analysis assumes a 1-GW manufacturing facility in urban China, 156.75 mm x 156.75 mm wafers, 180-μm wafer thickness, 17.2 g of net silicon per wafer, and 0.35 kWh of total electricity per wafer.

Overall equipment CapEx can also be reduced by a larger scale of purchase, because the per-tool price from equipment vendors depends on how many tools are purchased. The depreciation expenses in Figure 11 and Figure 12 represent CapEx for state-of-the-art greenfield manufacturing facilities with an annual production volume equivalent to 1 GW, which is a large enough production volume to achieve most benefits available from economies of scale (it could be described as occurring near the bottom of the CapEx-as-a-function-of-scale curve).

Using these simplifying assumptions about technology availability (and not accounting for tariffs or other trade barriers) we find that country-by-country differences in wafer manufacturing costs are largely driven by differences in labor and electricity rates as shown in Figure 13. Fabrication costs are lower for multicrystalline DS wafers than for monocrystalline Cz wafers, primarily because of ingot size: 150–200 kg for monocrystalline Cz ingots versus 700–900 kg for multicrystalline DS ingots. The larger multicrystalline DS ingots reduce net $/wafer CapEx while saving roughly 50% in total electricity costs and 25% in labor costs. These costs gaps between mono- and multicrystalline could narrow as Cz ingot mass increases (see Section 4.3). In addition, our modeled Cz wafer is 12% lighter and produces 5% more power than our modeled DS wafer,[2] which may add value to the Cz wafer that is not captured by the $/wafer metric.

[2] Assuming 20.5% efficiency for cells made from DS wafers and 21.5% efficiency for cells made from Cz wafers.

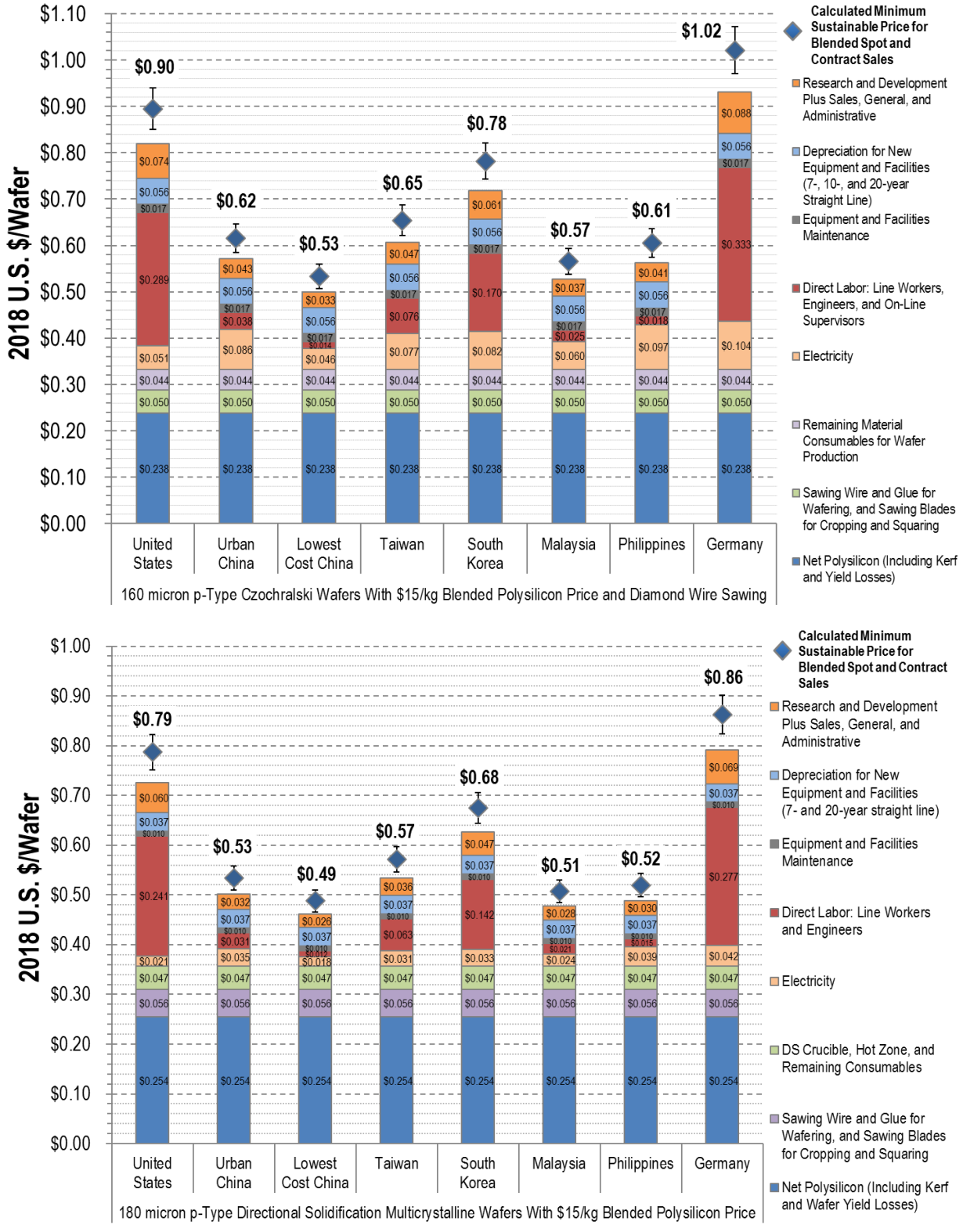


Figure 13. Total monocrystalline Cz (top) and multicrystalline DS (bottom) wafer costs by country

The analysis assumes no materials or cost differences due to currency translations, and equal transport of technology, materials, and equipment across borders. It does not include tax exemptions or import tariffs.

4.3 Cost Road Map

Wafer prices have declined by a factor of three over the past six years, mostly owing to industry scale-up and technology advancement (Figure 14 and Figure 15). Declining polysilicon prices have had the largest single impact. Spot and contract prices for polysilicon reached $475/kg during the production shortages of 2008, but within four years polysilicon capacity increased by a factor of six, and average annual prices fell to $35/kg (BNEF 2018, World Energy Council 2017). Over the past six years, the average annual polysilicon price has declined by at least another factor of two (Bloomberg L.P. 2018). The average polysilicon price for the first three quarters of 2018 was $14–$15/kg (BNEF 2018). Technology advancements such as diamond wire (DW) sawing have reduced costs while reducing kerf losses.

Even without further polysilicon price reductions, wafer costs could be reduced further if ingot and wafer producers could make additional advancements to reduce net silicon utilization. Projections of wafer thickness trends and kerf/yield losses based on ITRPV Working Group (2018) could be used to estimate future cost reductions for the Cz and DS wafer production processes. The price breakdowns for these potential future projections are depicted in Figure 14 and Figure 15 to the right of the historical price data.

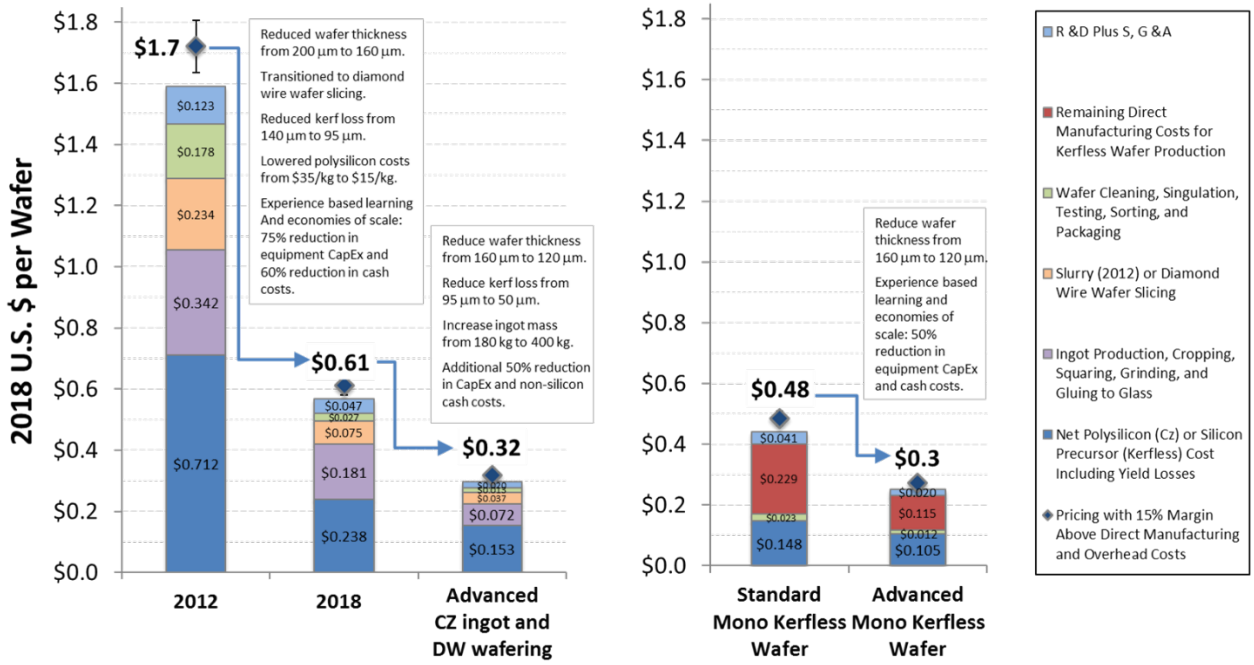


Figure 14. Modeled costs and MSPs for past, present, and projected monocrystalline wafers

The analysis assumes Asia-based production of 244-cm^2 (M2 format) wafers and a $15/kg polysilicon cost, and it does not include tax exemptions or import tariffs.

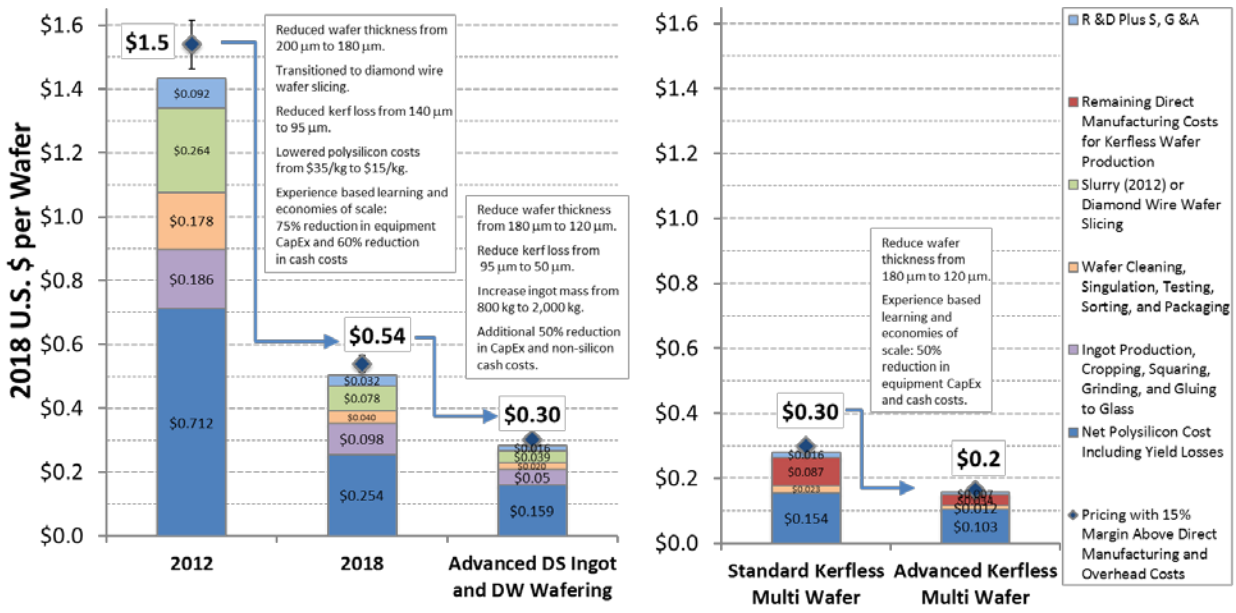


Figure 15. Modeled costs and MSPs for past, present, and projected multicrystalline wafers

The analysis assumes Asia-based production of 246-cm2 multicrystalline wafers and a $15/kg polysilicon cost, and it does not include tax exemptions or import tariffs.

Other potential methods to reduce ingot costs include a larger charge weight and continuous-Cz pulling. Both Cz and DS crucibles could be loaded to a greater polysilicon charge weight by pouring FBR granules over the top of Siemens chunks. FBR polysilicon could also enable continuous-Cz pulling. Each of these advances could lower the net per-wafer CapEx and cash costs.

Finally, on the rightmost side of Figure 14 and Figure 15, we show price breakdowns for an alternative wafer-production system, referred to as "kerfless" wafering. In the kerfless process, each wafer is formed individually, so there are no material losses due to sawing and no high-energy ingot production. However, kerfless wafer production has yet to demonstrate scale and throughput that are competitive with traditional wafer production, which has endured long enough to develop many cost-saving advancements. The standard kerfless cost model assumes currently available technology but at a scale of multiple gigawatts of annual production. The advanced kerfless cost model assumes cost reductions by producing thinner wafers and realizing savings related to additional economies of scale and learning-by-doing.

5 Cell Conversion

This section provides manufacturing process descriptions, current modeled costs, and a comparison of cell conversion costs for a range of PV technologies.

5.1 Manufacturing Processes

Cell conversion entails exposing silicon wafers to a series of wet chemical treatments, high-temperature gaseous diffusions, coating depositions, and metallization steps. The exact sequence and manufacturing tools used depend on the cell architecture.

The standard full-area aluminum back surface field (Al-BSF) cell conversion process has been the mainstay of high-volume mono- and multicrystalline c-Si manufacturing for decades (Goodrich et al. 2013). This process is depicted in Figure 16. The steps in this process include:

1. Wafer saw damage removal and surface texturization by a wet chemical process.
2. High-temperature diffusion of gaseous $POCl_3$ into the wafer's front surface.
3. Wet chemical etching of the phosphosilicate glass (PSG) layer that forms after the $POCl_3$ is driven into the wafer and the wafer cools.
4. Deposition of a hydrogenated silicon nitride (SiN_x:H) anti-reflection and surface passivation layer on top of the phosphorous-doped frontside.
5. Screen-printing aluminum (Al) and silver (I) pastes on the front and back.
6. Annealing and paste cofiring.

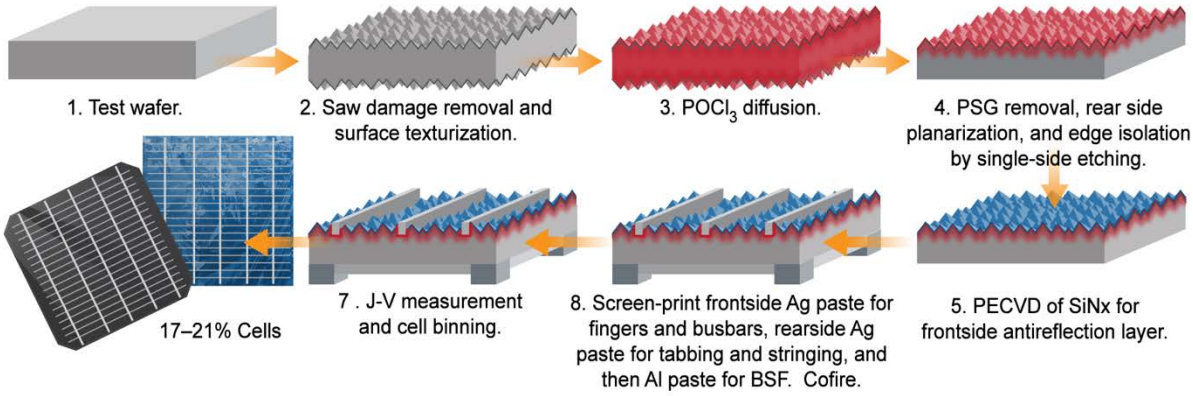


Figure 16. Process flow for manufacturing standard full-area Al-BSF cells

At the start of the manufacturing line, wafers are typically screened for any obvious visible cracks and broken pieces by rapid-screening. At the end of the line, completed cells are typically run though a "flash tester" that quickly blasts each cell with a known amount of light (most commonly 1,000 W/m^2) while measuring the current-voltage characteristics. Wafers that do not pass the inspection tests at the start of the line—and any completed cells that do not meet the predetermined electrical performance threshold at the end of the line—are discarded as a yield loss.

Advances such as the SiN_x:H antireflection layer, front surface passivation layer, and better screen-printing techniques have enhanced the standard Al-BSF technology incrementally (Swanson 2007, 2005). However, passivated emitter and rear cell (PERC) processing has become widely used to improve sunlight conversion efficiencies—up to 1.5% in absolute cell efficiency—beyond those possible via the standard full-area Al-BSF architecture (Goodrich et al. 2013). PERC market share grew rapidly from around 0% in 2010 to about 25%–30% in 2017 (ITRPV Working Group 2012, 2018) through the construction of manufacturing facilities with annual production capacities greater than 1 GW. The PERC market share is projected to reach about 60% by 2030 (ITRPV Working Group 2018).

The technical advantage of the PERC architecture lies primarily in its ability to reduce electrical recombination losses while increasing light reflection on the cell bottom. Mitigating these losses raises the cell efficiency and can be achieved by inserting a one- or two-material stack on the wafer backside, in between the silicon substrate and the bottom aluminum metallization. It is still necessary to enable points of direct contact between silicon and aluminum, which spurred development of equipment capable of patterning precise laser-drilled holes and trenches. Most of the interface between the silicon and aluminum paste is still covered by the passivation layer. Figure 17 shows the process flow for PERC cells. Step 5, Step 6 (backside reflection and surface passivation), and Step 7 are the additional steps required for PERC. Otherwise, the PERC process flow borrows the same equipment as for standard full-area Al-BSF cells.

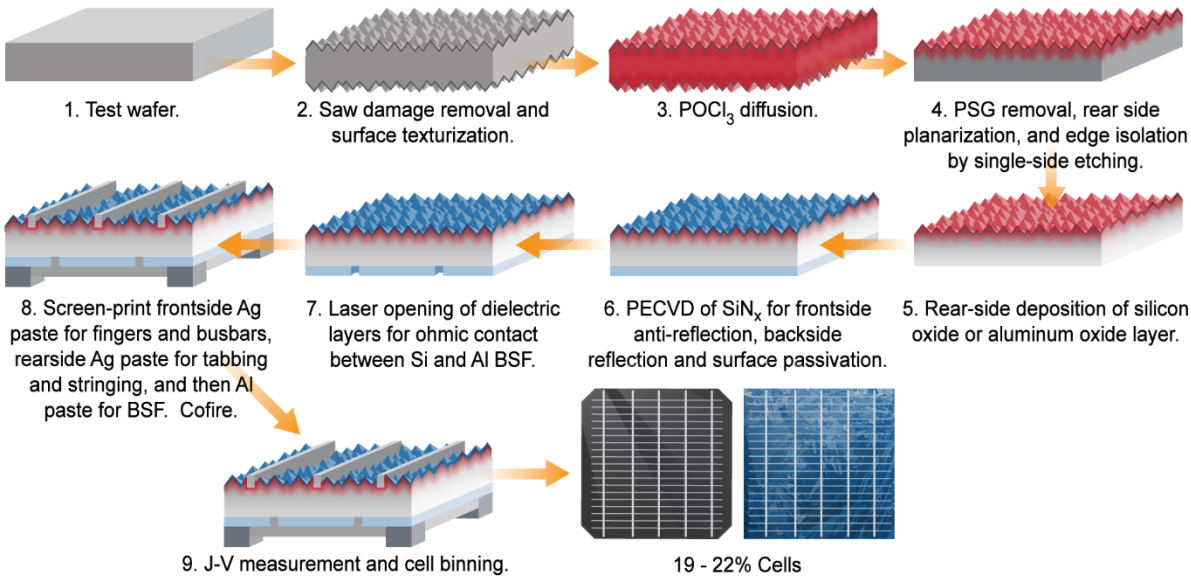


Figure 17. Process flow for manufacturing standard full-area PERC cells

5.2 Modeled Current Costs

The scale of PERC manufacturing provides precedent for the materials, labor, and electricity costs as well as the CapEx required for all-new manufacturing capacity. These are summarized in Table 3. Figure 18 summarizes our modeled cost-of-ownership information for each step, assuming a 1-GW manufacturing site located in urban China.

The material costs shown in Figure 18 are a function of the consumption per cell multiplied by the cost per unit. For example, metallization (screen-printing of silver and aluminum pastes) is the single largest direct cost for cell conversion, at 24% of the total cost. For a five-busbar design, the industry-standard material requirements for this step are currently around 80–110 mg of silver paste for the cell frontside, 20–50 mg of silver paste for the backside, and 1.3–1.5 g of aluminum paste for the backside. Based on 1H 2018 silver and aluminum pricing (LME 2018a, 2018b) and the composition of these pastes including additives, we calculate total metallization paste materials costs of \$0.015 ± \$0.002/W, with 58% due to frontside silver, 19% to backside silver, and 23% to backside aluminum.

Table 3. Overview of Inputs Used in NREL's PERC Cell Conversion Cost Models

Variable Cost COGS Elements for Cell Conversion	
Principal input materials	Wafers. Aqueous-based solutions for surface texturization and PSG removal (KOH, HF, HNO_3, HCl). $POCl_3$ and/or BBr_3. SiH_4 and NH_3 precursors for SiN_x:H by plasma-enhanced chemical vapor deposition (PECVD). Trimethyl aluminum (TMA) for PERC. Ag and Al metallization pastes and screens for printing. Clean dry air, N_2, and O_2 gases used throughout the process.
Labor	0.8–1.2 direct employees per MW of PERC cell production.
Electricity	Total of 0.4–0.6 kWh per monocrystalline and multicrystalline PERC cell.
Maintenance	Annual cost equivalent to 3% of the original equipment investment.
Fixed Cost COGS Elements for Cell Conversion	
Depreciation on capital equipment	Total equipment CapEx of \$0.04–\$0.08/W for standard cell lines. Total equipment CapEx of \$0.06–\$0.10/W and facility CapEx of \$0.03–\$0.06/W for PERC cell lines. For baseline total equipment and facilities CapEx: wafer testing (\$0.010/W), saw damage removal and surface texturization (\$0.027/W), $POCl_3$ diffusion and PSG removal (\$0.023/W), front and backside anti-reflection and passivation layers (\$0.039/W), laser contact opening (\$0.006/W), screen-print and cofire (\$0.016/W), and cell testing and packaging (\$0.012/W). Five-year straight-line depreciation.
Depreciation of manufacturing facilities	\$0.03–\$0.06/W total for new building and facility CapEx. 20-year straight-line depreciation.
Remaining Fixed Operating Expenses	
R&D	2% of value-added revenues (total revenues minus wafer cost).
SG&A	11% of value-added revenues (total revenues minus wafer cost).

Figure 18 also includes the typical electricity and CapEx costs for conveyers and robotic handling equipment. Robotic handling increases yield, although some human labor is required for logistics operations including receiving wafers and completing cell packaging and shipping. Workers are also needed on an automated cell conversion line to monitor and maintain the equipment and inspect in-process cells randomly for visible defects. The total costs for monocrystalline PERC cell conversion, in an urban Chinese location as shown in Figure 18, come to \$0.0632/W.

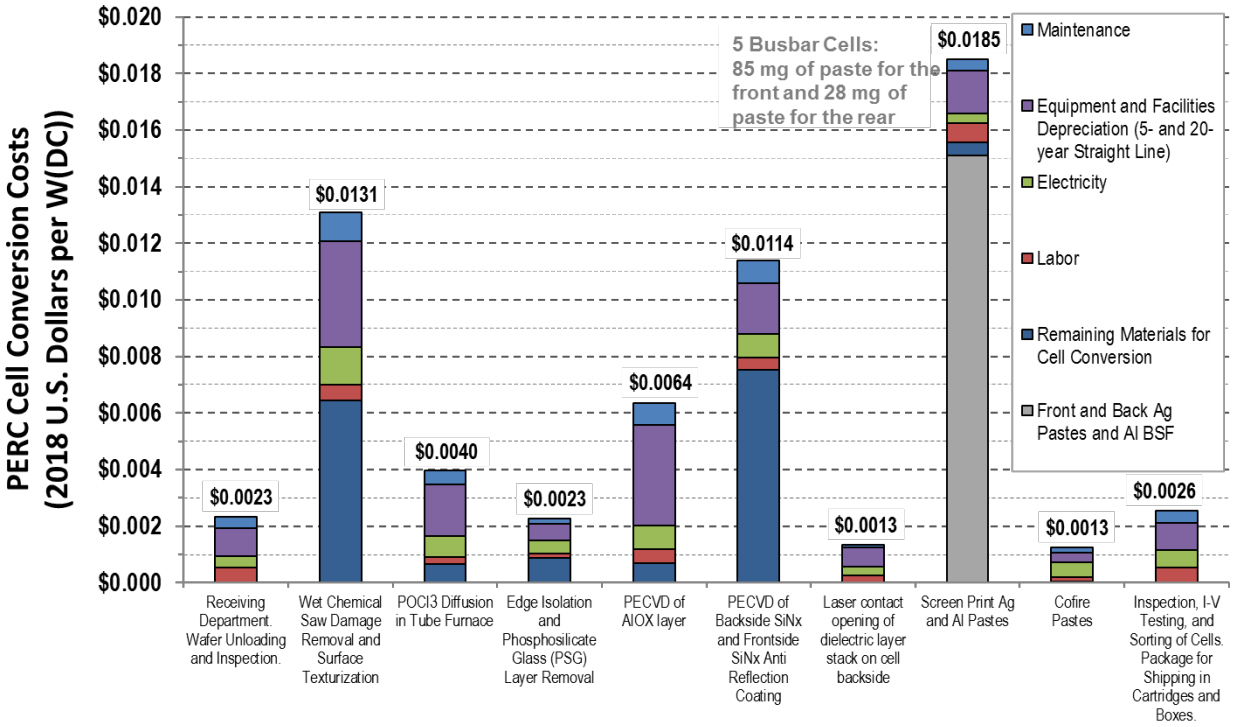


Figure 18. Step-by-step costs for monocrystalline PERC cell fabrication in urban China

The analysis assumes a 1-GW greenfield manufacturing facility in urban China, for 244-cm^2 cells on M2 format *p*-type Cz wafers, at 21.5% efficiency. I-V = current-voltage.

The technical expertise and tools needed to manufacture standard and PERC cells at high volume with guaranteed and respectable efficiencies are now widely available. If a company can find suitable equipment vendors and materials suppliers and make an adequate investment, large-scale cell conversion could occur essentially anywhere. Thus—assuming free trade of input materials as well as relatively low logistics and currency-exchange costs—the key differentiators in costs across countries could again be electricity and labor rates.

Figure 19 shows cost model results for PERC manufacturing sites located within different countries. The country-by-country wafer costs are derived from Figure 13 after dividing by the cell power in watts, which has a significant impact on country cell conversion comparisons. The United States, Germany, and South Korea have the highest labor costs, while the Philippines, Germany, and urban China have the highest electricity costs. The cost disparities between countries are greater for monocrystalline cell conversion than for multicrystalline cells.

Because cell manufacturing firms often rely on wafers imported from other countries, it is also important to estimate cell MSPs using imported wafer pricing. For example, when using lowest-cost China wafer MSP, the calculated cell MSPs for mono- PERC production move down to $0.24/W for the United States, $0.22/W for South Korea, and $0.25/W for Germany. When using lowest-cost China multi- wafer MSP, the calculated cell MSPs for multi- PERC production move down to $0.23/W for the United States, $0.22/W for South Korea, and $0.25/W for Germany.

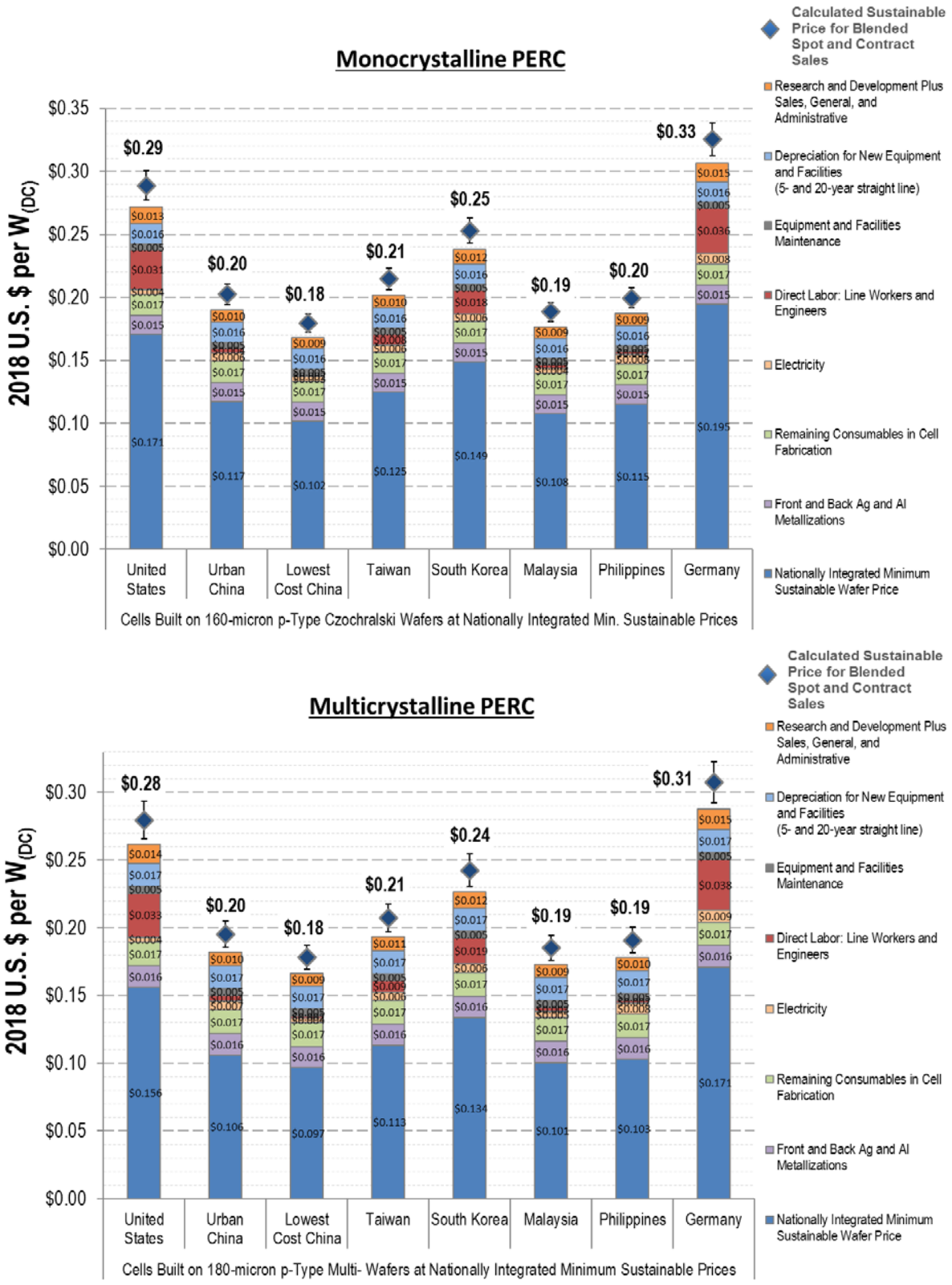


Figure 19. Monocrystalline (top) and multicrystalline (bottom) PERC conversion costs by country

The analysis does not include tax exemptions or import tariffs, and it uses wafer prices by country from Figure 13.

5.3 Cell Technology Comparison

Although cell costs have been reduced dramatically, opportunities for cell improvements remain. Beyond PERC, other cell conversion options that could deliver higher efficiencies than the standard full-area Al-BSF efficiency include the silicon heterojunction (SHJ), passivated emitter rear locally diffused (PERL), passivated emitter rear totally diffused (PERT), and interdigitated back contact (IBC) technologies. The technical expertise and high-volume manufacturing capabilities for these options have historically been limited to a small number of players, but this is rapidly changing. All of these cell architectures have fully licensable intellectual property, and all but one (IBC) are known to have multiple vendors for turnkey manufacturing solutions that are available for production scales between 50 MW and multiple gigawatts.

Figure 20 compares our modeled cost results for standard Al-BSF, PERC, PERT, SHJ, and IBC (see the appendix for detailed process flows and stepwise costs). The PERT, SHJ, and IBC costs are projections based on facilities with 1 GW of annual production in urban China; standard and PERC cells are already produced far above that scale and are modeled for 2-GW facilities.

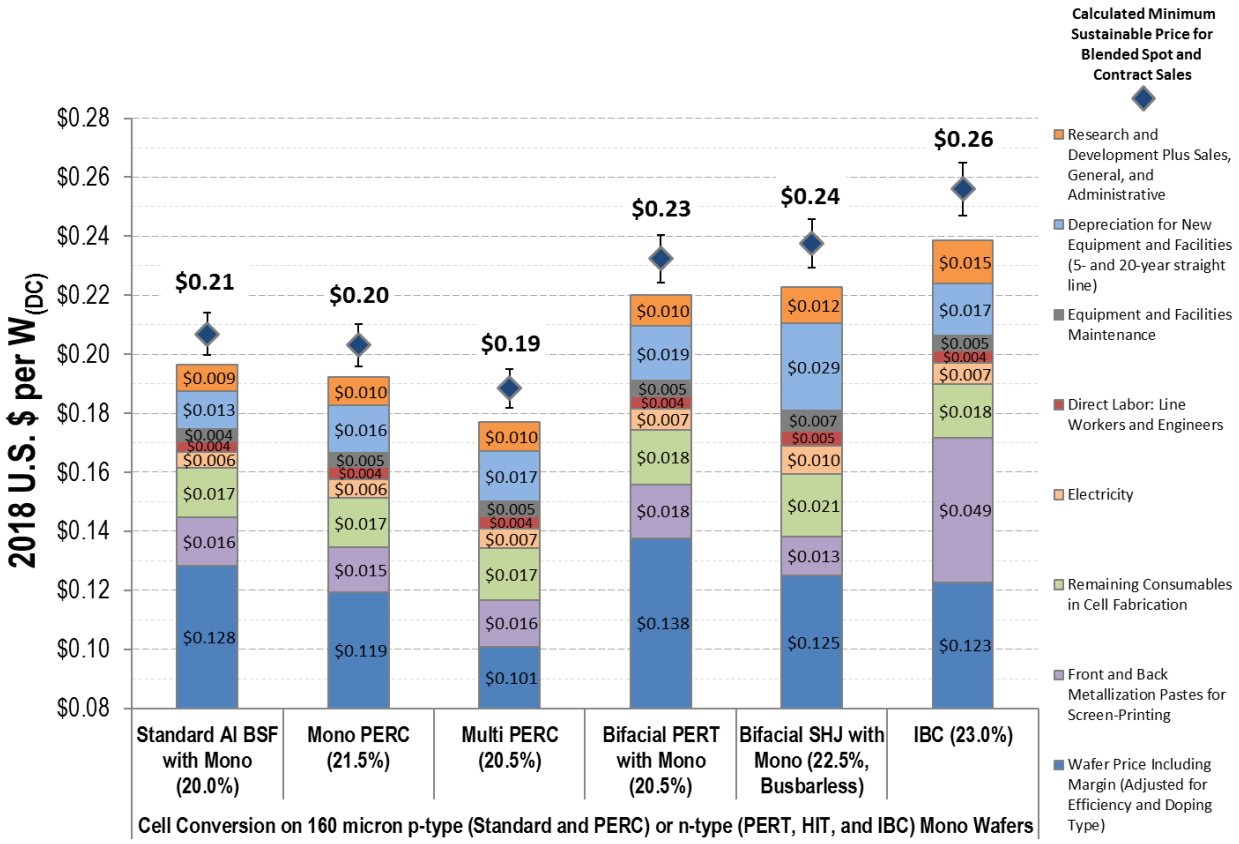


Figure 20. Modeled costs and MSPs for Al-BSF, PERC, PERT, SHJ, and IBC cell technologies

The analysis assumes facilities in urban China and does not include tax exemptions or import tariffs. The projected PERT, SHJ, and IBC costs are based on facilities with 1 GW of annual production. For standard and PERC cells, 2-GW facilities are assumed.

A 10% per-wafer *n*-type price premium (on top of a current assumption of $0.61 per *p*-type Cz wafer) is applied to the *n*-type cell architectures PERT, SHJ, and IBC. The IBC technology represented here is based on screen-printing, tube furnace diffusions, and wet chemical cleaning steps, and it does not include passivated contacts, although other IBC cell designs have been proposed or demonstrated. For SHJ and PERT process flows, less variation exists in high-volume production or even across different research groups.

These results indicate there could be cost premiums for the highest-efficiency technologies (SHJ and IBC), associated with the additional processing steps—and thus additional CapEx investment—required. The PERT, SHJ, and IBC technologies would also have a higher CapEx owing to smaller production scales than the standard and PERC cells (Goodrich et al. 2013). In addition, prices for the *n*-type wafers recommended for PERT, SHJ, and IBC cells could be about 5%–15% higher than prices for the *p*-type wafers used in standard and PERC cells, because the *n*-type supply chain is not as fully developed. However, increasing demand for higher-efficiency *n*-type cells could likely drive further cost reductions, which could eventually close the price gap between *p*- and *n*-type cells.

Although higher-efficiency cells can cost more per watt, they may provide benefits at the balance-of-module (BOM) and balance-of-system (BOS) levels. In addition, emerging technologies may provide lifecycle economic benefits not reflected in the initial per-watt cost. For example, some technologies include a better temperature coefficient, the potential for backside light harvesting via bifacial structures, and/or improved reliability. These same efficiency and energy yield benefits of new technologies could also show improvements when comparing their levelized cost of electricity lifecycle metrics.

6 Module Assembly

This section provides manufacturing process descriptions, current modeled costs, and a cost road map for module assembly.

6.1 Manufacturing Processes

The module-assembly step in the c-Si supply chain involves electrically connecting cells into strings, arranging parallel cell strings into an array, electrically connecting the strings with metallic ribbons, mounting the array onto a layer of encapsulant on top of a sheet of glass or backsheet, and laminating another sheet of encapsulant and front glass onto the whole assembly. The typical front and back encapsulants are thermoplastic material that melts when heated during the lamination process—thereby encasing the entire assembly between a sheet of glass on the front and either a backsheet or another sheet of glass on the back. The ribbons are fed through a hole in the back glass or backsheet and interwoven on the back of the module within a junction box, which contains diodes to reduce cell mismatch and serves as the point of contact between modules in an installed system. Finally, an extruded aluminum frame is typically put around the perimeter of the module.

Figure 21 shows a representative process flow and schematic for a complete 60-cell monocrystalline-silicon module assembly. Some firms have been developing glass-glass modules without an aluminum frame, while monocrystalline and multicrystalline busbarless, 72-cell, 96-cell, frameless, and glass-glass module options (including but not limited to options using bifacial cells) are also available.

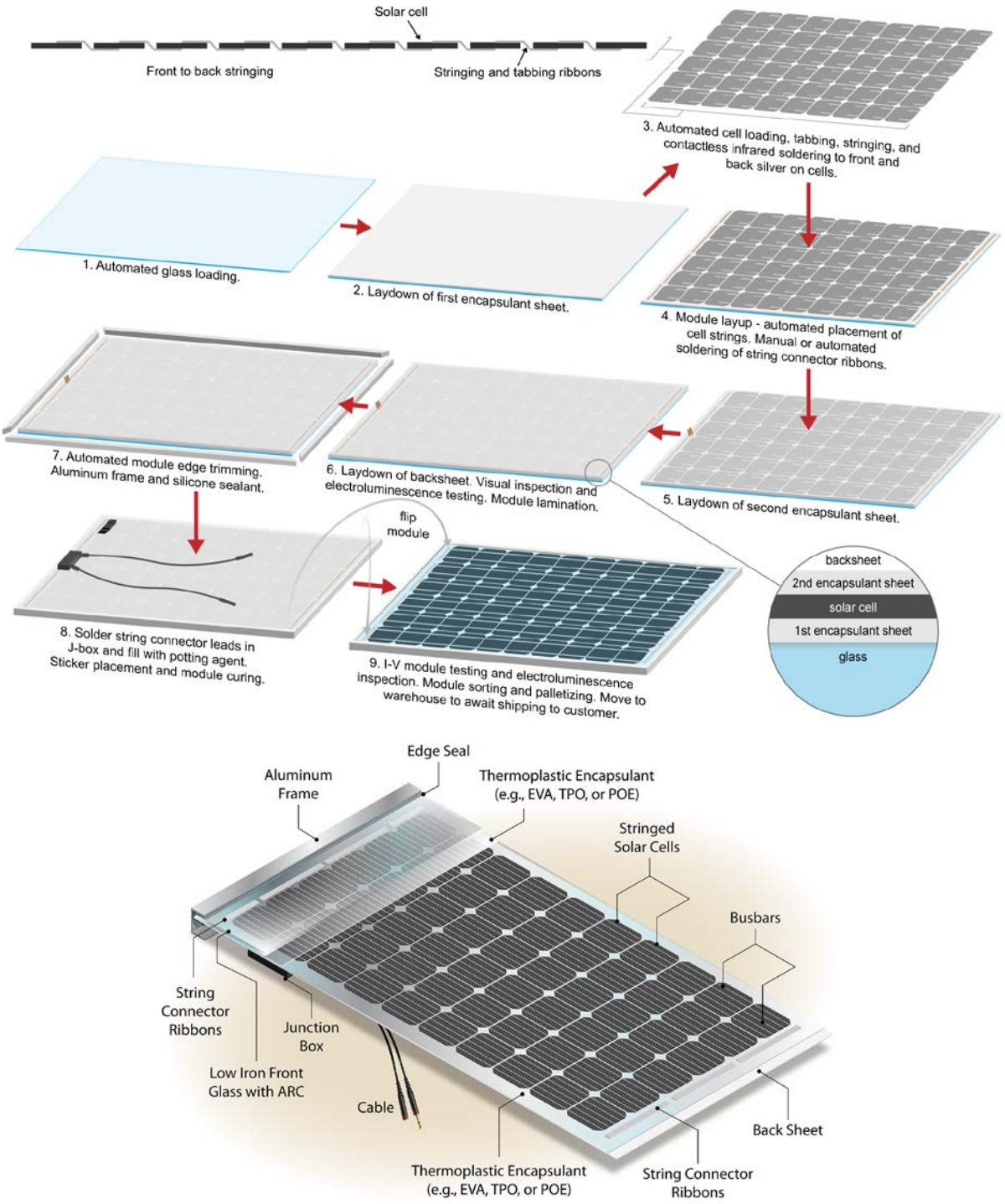


Figure 21. Process flow (top) and finished product (bottom) for standard 60-cell monocrystalline-silicon module assembly

J-box = junction box, ARC = anti-reflective coating, EVA = ethylene vinyl acetate, TPO = thermoplastic polyolefin, POE = polyolefin encapsulant.

6.2 Modeled Current Costs

Module assembly can be accomplished using varying degrees of manual labor and automation. Even if a firm fully automates all steps, the CapEx for module assembly is currently the lowest CapEx among all steps in the supply chain: likely U.S. $3–$5 million to start a 100-MW annual capacity module assembly plant, or U.S. $20–$30 million to purchase all the equipment for a fully scaled 1-GW plant. This is roughly half the CapEx for entry into Cz wafer production or cell conversion activities. Several equipment firms offer turnkey module assembly solutions, and it is generally easy for prospective module assembly firms to find various cell suppliers. Because of the relatively low financial barriers to entry and fully accessible technology solutions, module assembly is the easiest way to become engaged in PV manufacturing, and the global PV industry includes hundreds of module assembly firms.

Table 4 summarizes our module assembly cost inputs, which are based on state-of-the art automated practices and current global market prices for materials. Figure 22 shows our modeled cost results for each process step for monocrystalline PERC module assembly (excluding cell costs), assuming the module facility is located in urban China and has an annual production capacity greater than 1 GW. The total cost per watt from this figure corresponds to approximately $0.13/W. Materials constitute more than 80% of the costs, while the next largest cost categories are equipment and utilities, which mainly occur in the inspection, electroluminescence, and lamination step.

Table 4. Overview of Inputs Used in NREL's Module Assembly Cost Model

Variable Cost COGS Elements for Module Assembly	
Principal input materials	Cell stringing and tabbing ribbons, front glass, backsheet, ethylene-vinyl acetate (EVA) encapsulant (2 sheets), Al frame and edge sealant, junction box, junction box potting agent and tape, and coded module sticker label.
Labor	0.5–0.7 direct employees per MW (automated) or 1–2 direct employees per MW (more labor-driven options).
Electricity	20–25 kWh per 60-cell module.
Maintenance	Annual cost equal to 4% of original equipment investment.
Fixed Cost COGS Elements for Module Assembly	
Depreciation on capital equipment	Total equipment CapEx of $0.03–$0.05/W for standard and PERC modules. 5-year straight-line depreciation.
Depreciation of manufacturing facilities	20-year straight-line depreciation. $0.04/W total building and facility CapEx.
Remaining Fixed Operating Expenses	
R&D	2% of value-added revenues (total revenues minus cell cost).
SG&A	11% of value-added revenues (total revenues minus cell cost).

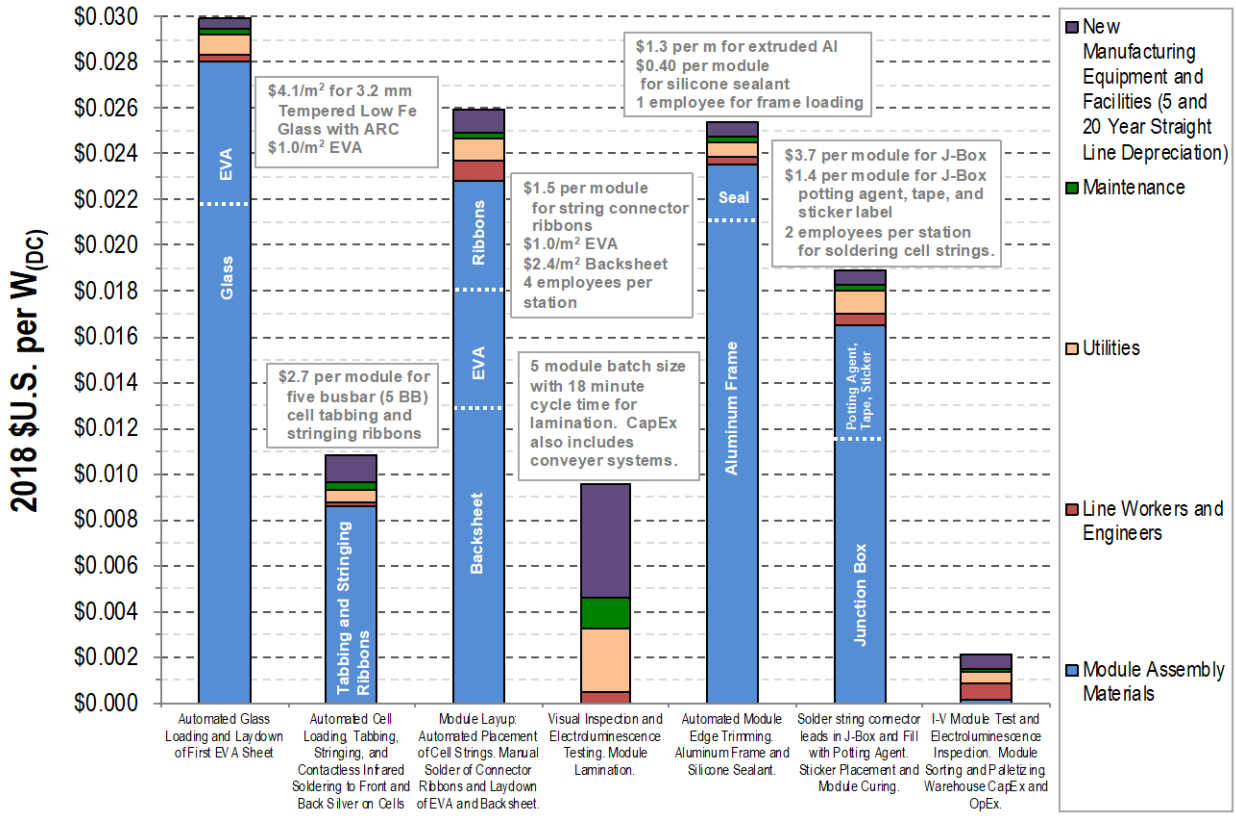


Figure 22. Step-by-step costs for monocrystalline PERC module assembly

The analysis assumes 310-W modules with 60 mono-PERC cells (244-cm^2 cells) at a facility with greater than 1.0 GW annual production in urban China. OpEx = operating expenses.

Figure 23 shows total monocrystalline module assembly costs by country, which now include nationally-integrated cell costs and MSP values. Cell costs are primarily responsible for the difference between countries, although module-assembly labor costs also differ, as do electricity costs to a lesser extent. This results in a $0.20/W price range between the lowest-cost (rural China) and highest-cost (Germany) locations. This large range exists in part because we assume substantial national supply-chain integration, with each country assumed to produce the wafers and cells used in its modules.[3]

However, such national integration is atypical. For example, lower-cost cells from other countries are often imported and used to manufacture modules locally. Thus, it is also important to estimate module assembly MSPs using imported cell pricing. For example, when using lowest-cost China mono-PERC cell MSP, the calculated MSPs for module assembly move down to $0.40/W for the United States, $0.39/W for South Korea, and $0.41/W for Germany.

The cost structure for the MSP for monocrystalline PERC module manufacturing in urban China is shown in Figure 24 using GAAP and IFRS accounting categories. This differs from Figure 23 in that the margins for each component in the supply chain are aggregated into a single margin value. Similarly, material costs are aggregated and reported for what is acquired externally for each step in the supply chain. The depreciation expense is compiled for each step in the supply

[3] We assume all countries in 1H 2018 had access to polysilicon near $15/kg.

chain by dividing the original CapEx by the period of depreciation (5–20 years, depending on the item). We calculate total 1H 2018 variable costs around $0.245/W, total COGS around $0.285/W, and all-in production costs around $0.325/W. The calculated range of sustainable operating margin (or earnings before interest and taxes, EBIT) equal to 5%–25% of revenues would be available to pay taxes, pay interest to debt holders, and provide earnings for equity owners.

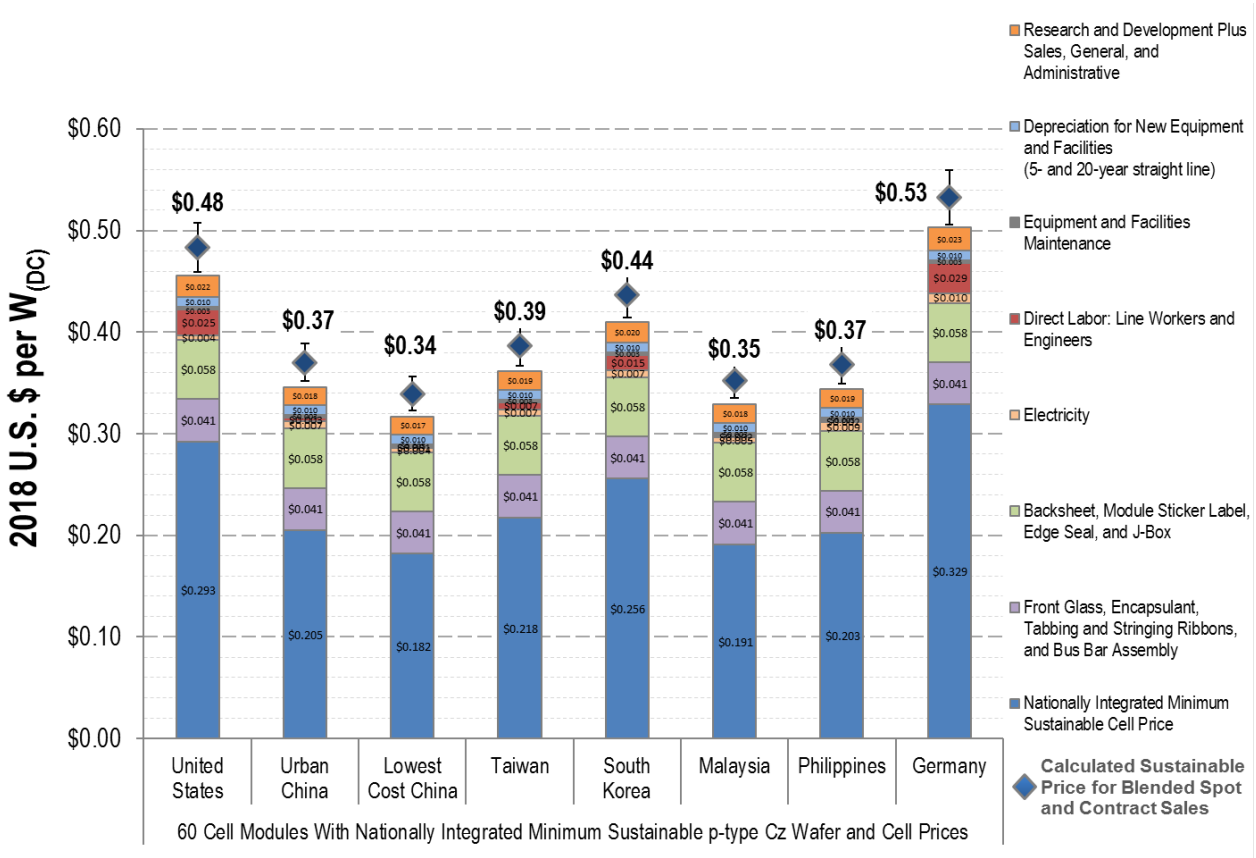


Figure 23. Monocrystalline PERC module assembly costs by country

The analysis does not include tax exemptions or import tariffs, and it assumes module efficiency of 19% (310 W, 60 cells, 1.650 x 0.992 m^2) with cell prices carried over from Figure 19.

The prices in Figure 23 may be slightly elevated relative to some regions which use accounting practices that differ from those assumed for the purposes of this report. Longer equipment and building depreciation schedules, as well as permission of amortization of R&D expenditures, could reduce calculated costs by $0.04—0.05/W. Additionally, the prices shown in this figure do not take shipping costs, minimum import prices, or tariffs into account. The impact of shipping costs to the landed price to customers could become more important over time. This is because if module prices continue to fall, shipping costs could likely represent a growing fraction of the total module cost.

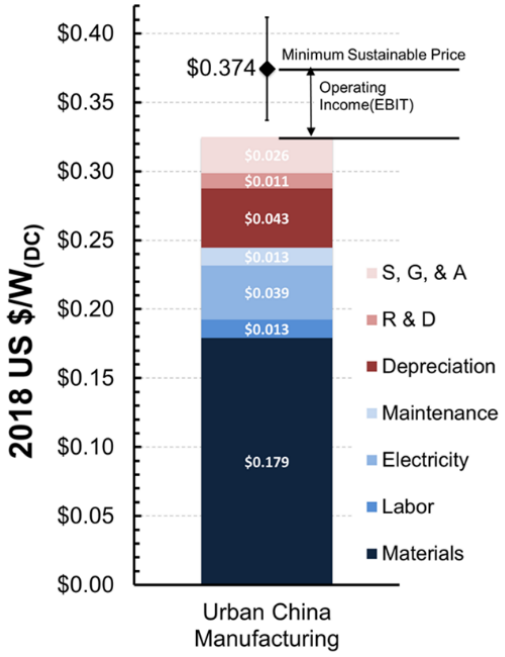


Figure 24. Breakdown of monocrystalline PERC module full supply-chain costs using GAAP and IFRS categorization

6.3 Comparison of Cell Technologies and Cost Road Map

The historical and projected improvements in per-watt module cost depend primarily on improvements in the preceding supply-chain steps, with module assembly processes playing a smaller role. In particular, cell technology has been transitioning from standard Al-BSF (which still accounts for most global production) to higher-efficiency PERC (see Section 5.1), and additional improvements in both technologies could be possible.

Figure 25 compares modeled current costs and MSPs for modules made with standard Al-BSF, PERC, PERT, SHJ, and IBC cells. These results assume encapsulant, backsheet, cell interconnection, and tabbing and stringing are consistent across all technologies. This is an oversimplification and thus an area that warrants further analysis. For example, in the case of bifacial modules, the opaque backsheet might be replaced with a second sheet of glass so that more light can get to back of the cell. In this analysis, the maximum price difference between technologies is only $0.04/W.

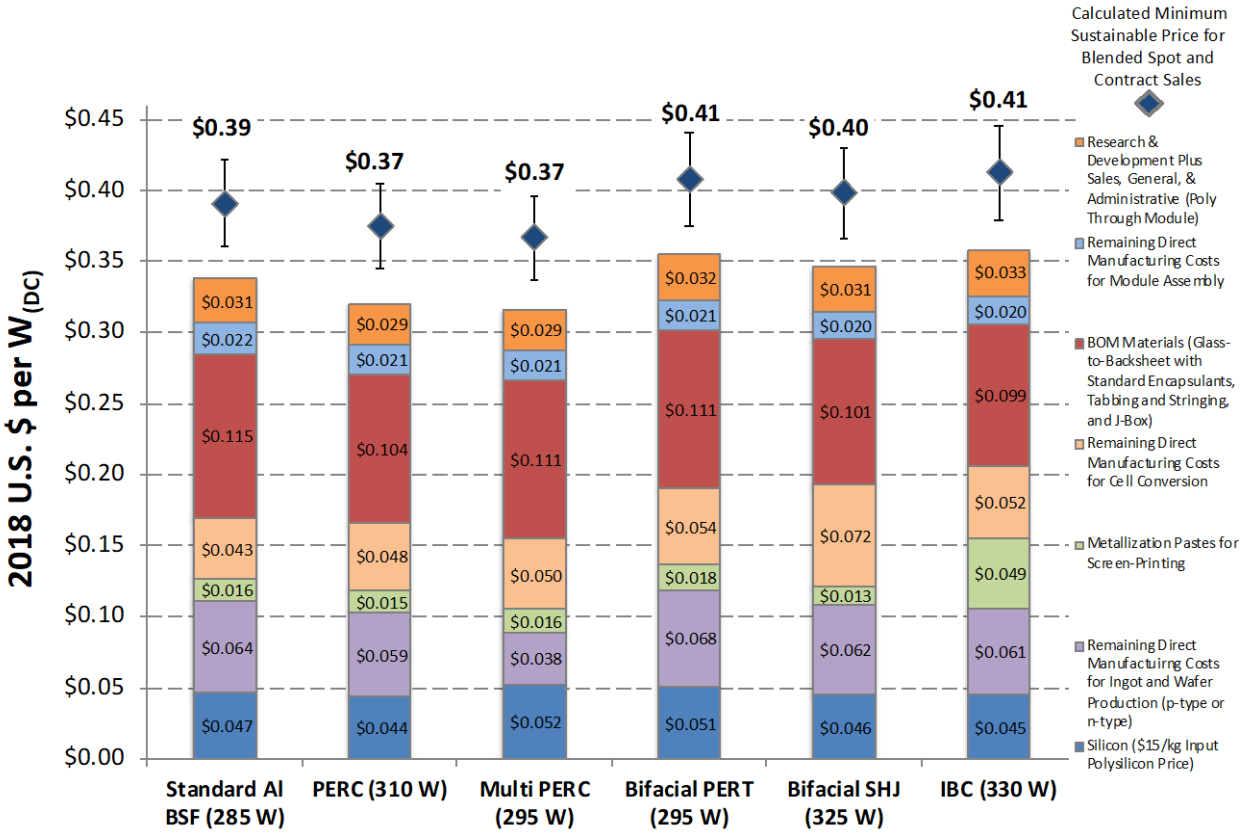


Figure 25. 1H 2018 benchmark module costs and MSPs by cell technology

This analysis assumes manufacturing of 60-cell modules in urban China, and it does not include tariffs.

Figure 26 summarizes historical and projected module costs and MSPs based on Al-BSF cells (in 2010 and 2015) and PERC or other advanced technology cells (2018 and later). In the first half of 2018, the price has shrunk to a quarter of what was modeled in 2010. This was due to reductions in polysilicon prices, a decrease in silver consumption by nearly half and other metallization improvements, improvements in economies of scale and process engineering, and adoption of the PERC architecture and DW wafering.

Going forward, the MSPs are projected to potentially drop another 25% by 2020, roughly, with the potential for additional long-term reductions. These projections are based on detailed modeling of technology advancements in wafering, metallization, and cell efficiencies. The 2020 projection assumes improvements in Cz ingot growth and DW wafering, as well as a 2% absolute increase in PERC cell efficiency and reducing silver consumption by half. The long-term projection (i.e., between 2030 and 2040), assumes adoption of kerfless wafer production techniques and cell architectures that could be capable of achieving even higher efficiencies. Additional price declines could be achieved as the scale of annual installations (and production) increases, which may be compounded by the general trend of increasing inverter loading ratios (EIA 2018). The long-term projection for $0.24/W in this report is below what would be required to achieve the 2030 SunShot goal of 3 cents/kWh ($0.25/W module) for utility-scale PV (Tinker 2018).

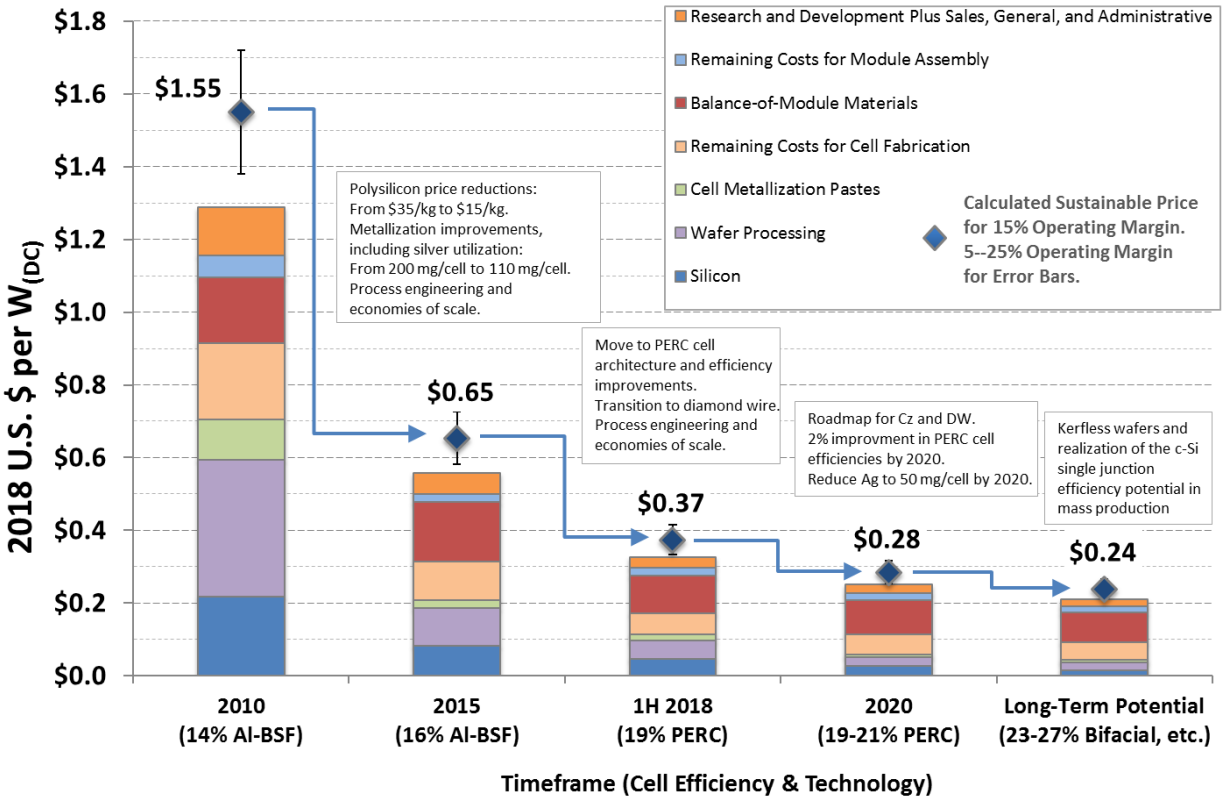


Figure 26. Modeled costs and MSPs for past, present, and projected c-Si modules

This analysis does not include tax exemptions or import tariffs. Efficiencies shown are for full module area, 1.650 m x 0.992 m 60-cell modules.

7 Conclusions

In this report, we examine historical cost reductions, current cost structures, and potential future cost reductions for production of c-Si PV modules and upstream supply-chain products: polysilicon, ingots and wafers, and cells. We also evaluate regional production cost structures. This analysis is meant to track progress and facilitate future progress in c-Si PV manufacturing. The following are key results.

Our 1H 2018 MSP benchmark is $0.37/W for monocrystalline-silicon PERC modules manufactured in urban China. The supply-chain costs for this benchmark build from $15/kg for polysilicon, to $0.12/W for DW wafers, to $0.21/W for monocrystalline PERC cells. The remaining price elements include $0.14/W for module production and a $0.02/W (15%) module operating margin. We benchmark monocrystalline PERC cells because of their combination of low cost and high efficiency, and because the PERC market share has grown rapidly to about 30% today (ITRPV Working Group 2018). Our benchmark also assumes all manufacturing occurs in China owing to that country's continued dominance across the c-Si PV supply chain. We assume polysilicon is produced by emerging low-cost manufacturers in rural China, and wafers, cells, and modules are produced in urban China, which remains the leading area for these elements of the supply chain.

Manufacturing in rural China results in the lowest-MSP wafers, cells, and modules. Although most Chinese production has occurred in urban locations to date, rural Chinese areas with lower labor and electricity costs and lower margins could produce the world's lowest-MSP wafers, cells, and modules. MSPs for these products are slightly higher in urban China, Taiwan, Malaysia, and the Philippines. Among the three higher-cost countries we analyzed, Germany has the highest wafer, cell, and module MSPs, followed by the United States and South Korea. Higher labor costs and margins increase MSPs in these countries. Because we assume substantial national integration of supply chains—with each country producing the wafers and cells used in its modules—the cost differentials compound at each supply-chain step.[4] For example, the module MSP is $0.12/W higher in the United States than in urban China: $0.05/W due to the wafering step, $0.03/W due to the cell conversion step, and $0.03/W due to the module assembly step.[5] Overall, the MSPs of modules manufactured in China, Taiwan, Malaysia, and the Philippines would be $0.05–$0.20/W (11%–37%) lower than the MSPs of modules manufactured in South Korea, the United States, and Germany. In practice, many manufacturers source upstream supply-chain components from lower-cost areas (e.g., U.S. and German module manufacturers import cells), which reduces their production costs and MSPs.

The gaps between MSPs in different countries have narrowed over the past decade as the global c-Si PV supply chain has matured. This can be observed in comparison to our previous publications, specifically (Fu, et al. 2015; Goodrich, et al. 2013b; Goodrich, et al. 2011). In particular, innovations that have increased the use of automation in manufacturing and thus reduced labor requirements have been effective in narrowing the gaps in MSPs across countries. Examining how further advances in manufacturing processes and module architectures could continue to narrow the gaps in MSPs across countries is an important area for future research.

[4] We assume all countries in 1H 2018 had access to polysilicon near $15/kg.
[5] The values associated with each step do not sum to the total $0.12/W difference because of rounding.

For example, in the United States, labor's shares of manufacturing costs are 50% for wafers, 30% for cells, and 15% for modules. Lower labor costs are the primary reason for urban China's MSP advantage over the United States. In urban China, labor's shares of manufacturing costs are only 11% for wafers, 5% for cells, and 2% for modules.[6] Conversely, relatively low labor requirements—along with relatively low U.S. energy costs—give the United States its sole edge in supply-chain costs over urban China: for Siemens polysilicon production. However, if module prices continue to drop, shipping costs may begin to outweigh savings in labor costs.

Benchmark c-Si module MSPs declined $1.18/W (76%) between 2010 and 1H 2018. From 2010 to 2015, the reduction was $0.90/W due to polysilicon price reductions, reduced silver consumption during cell conversion, process engineering, and economies of scale. From 2015 to 1H 2018, the reduction was $0.28/W due to the transition to PERC cell architecture and DW wafering as well as process engineering and economies of scale.

Our cost-reduction road map could yield monocrystalline-silicon module MSPs of $0.28/W in the 2020 time frame and $0.24/W in the long term. Compared with our 1H 2018 benchmark, these MSPs would be lower by 25% (in 2020) and 35% (in the long term). Our road map to the 2020 target depends on thinner wafers, continuing the transition to DW wafering, reducing silicon and silver utilization, and improving cell efficiencies. Our long-term road map hinges on transitioning to kerfless wafering and increasing cell efficiencies to greater than 23%. Solar shingles and modules with half-cut cells are beginning to show market traction, but they are not evaluated in this study and will be modeled in a future cost benchmark report.

Realizing our 2020 cost-reduction road map improvements could help align c-Si module market prices with calculated MSPs that are based on Greenfield manufacturing capacity with positive operating margins. Average module market prices in 2018 have been in the range of $0.20/W to $0.40/W—mostly below our 1H 2018 MSP benchmark. This misalignment between market pricing and modeled MSPs is reflected in negative operating margins for most PV companies (Figure 4), though it may also partially result from the use of legacy or fully depreciated equipment with different depreciation schedules than those assumed in this report. Our road map identifies near-term cost reductions that could be sufficient to make 2H 2018 market prices sustainable by 2020.

Realizing the technological advancements envisioned in our longer-term road map could provide even deeper c-Si module MSP reductions and/or improved PV system and lifecycle economics. On a per-watt basis, PERT, SHJ, and IBC cells currently cost more than standard Al-BSF and PERC cells owing to smaller production scales and use of *n*-type wafers. However, if these advanced cell technologies gain market share, their MSPs could decline below our estimates. These cell technologies also might offer benefits beyond those reflected in the module price. Cells with higher efficiencies could reduce per-watt BOM and BOS costs. In addition, various cell and module characteristics could improve lifecycle PV economics. Woodhouse et al. (2016), for example, show how different combinations of module prices, efficiencies, degradation rates, and system lifetimes could achieve the same lifetime (levelized cost of energy)

[6] The calculations of labor's share of manufacturing costs at each supply-chain step exclude the costs related to each upstream step: wafer costs exclude polysilicon costs, cell costs exclude wafer costs, and module costs exclude cell costs. The calculations are based on monocrystalline-silicon wafers, cells, and modules.

targets. If the c-Si PV manufacturing and installation industries continue to mature, the module supply chain could evolve to meet increasing demands for optimal system-level lifetime performance. Exploring these tradeoffs is an important area for future research.

At an even broader level, c-Si module technologies would continue to compete against evolving alternative PV technologies such as cadmium telluride (CdTe), copper indium gallium diselenide (CIGS), and perovskite modules. This competition could likely drive innovation and cost reductions across all technologies while presenting additional opportunities for system optimization.

References

Bernreuter, Johannes. 2014. FBR polysilicon technology – promise or hype? PV-tech.org, Accessed September 12, 2018.

Bernreuter, Johannes. 2016. The Polysilicon Market Outlook 2020. Bernreuter Research.

Bloomberg L.P. 2018. "Bloomberg Terminal." Accessed June 12, 2018.

BLS (U.S. Bureau of Labor Statistics). 2018. "International Labor Comparisons." Accessed March 2018. https://www.bls.gov/fls/

BNEF. 2018. Bloomberg New Energy Finance. New York. https://www.bnef.com/. Accessed September 10, 2018.

Coletti, Gianluca. 2011. Impurities in silicon and their impact on solar cell performance: Utrecht University.

EIA (U.S. Energy Information Administration). 2018. Solar Plants Typically Install More Panel Capacity Relative to Their Inverter Capacity. https://www.eia.gov/todayinenergy/detail.php?id=35372

———. 2018. "Electricity." Accessed July 2018. https://www.eia.gov/electricity/

Feldman, David J, and Robert M Margolis. 2018. Q1/Q2 2018 Solar Industry Update. NREL/PR6A20-72036. National Renewable Energy Lab (NREL), Golden, CO

Fu, Ran, Ted L James, and Michael Woodhouse. 2015. "Economic measurements of polysilicon for the photovoltaic industry: market competition and manufacturing competitiveness." *IEEE Journal of Photovoltaics* 5 (2): 515–524.

Goodrich, Alan, Peter Hacke, Qi Wang, Bhushan Sopori, Robert Margolis, Ted L James, and Michael Woodhouse. 2013a. "A wafer-based monocrystalline silicon photovoltaics road map: Utilizing known technology improvement opportunities for further reductions in manufacturing costs." *Solar Energy Materials and Solar Cells* 114: 110–135.

Goodrich, Alan, Douglas M Powell, Ted L James, Michael Woodhouse, and Tonio Buonassisi. 2013b. "Assessing the Drivers of Regional Trends in Solar Photovoltaic Manufacturing." *Energy and Environmental* Science 6(10): 2811–2821.

Goodrich, Alan, Ted L James, and Michael Woodhouse. 2011. Solar PV Manufacturing Cost Analysis: U.S. Competitiveness in a Global Industry (Presentation). Golden, CO: National Renewable Energy Laboratory. NREL/PR-6A20-53938.

IHS Markit. 2018. IHS Technology: Global Solar Intelligence Service. https://technology.ihs.com/Services/438743/global-solar-intelligence-service/ Accessed June 12, 2018.

ITRPV Working Group. 2012. International Technology Roadmap for Photovoltaics (ITRPV) 2011 Results. ITRPV Report Third Edition. SEMI, Berlin, Germany. www.itrpv.net

ITRPV Working Group. 2018. International Technology Roadmap for Photovoltaics (ITRPV) 2017 Results. ITRPV Report Ninth Edition. SEMI, Berlin, Germany. www.itrpv.net

LME (London Metal Exchange). 2018a. LME Aluminum. https://www.lme.com/Metals/Non-ferrous/Aluminium.

LME (London Metal Exchange). 2018b. LME Silver. https://www.lme.com/Metals/Precious-metals/LME-Silver.

Mints, Paula. 2018. Photovoltaic Manufacturer Capacity, Shipments, Price & Revenues 2017/2018. SPV Market Research.

Osborne, Mark. 2017. Daqo benefits from spike in polysilicon prices in Q3. https://www.pv-tech.org/news/daqo-benefits-from-spike-in-polysilicon-prices-in-q3.

Robinson, Thomas R, Elaine Henry, Wendy L Pirie, Michael A Broihahn, and Anthony T Cope. 2015. *International Financial Statement Analysis, (CFA Institute Investment Series)*: John Wiley & Sons.

Seetharaman, Seshadri, A McLean, R Guthrie, and S Sridhar. 2013. *Treatise on process metallurgy*. Vol. 2: Elsevier.

SEMI International Standards. 2018. SEMI E35-0618: Guide to Calculate Cost of Ownership (COO) Metrics for Semiconductor Manufacturing Equipment. SEMI International Standard Brussels.

Swanson, Richard M. 2005. "Approaching the 29% limit efficiency of silicon solar cells." Photovoltaic Specialists Conference, 2005. Conference Record of the Thirty-first IEEE.

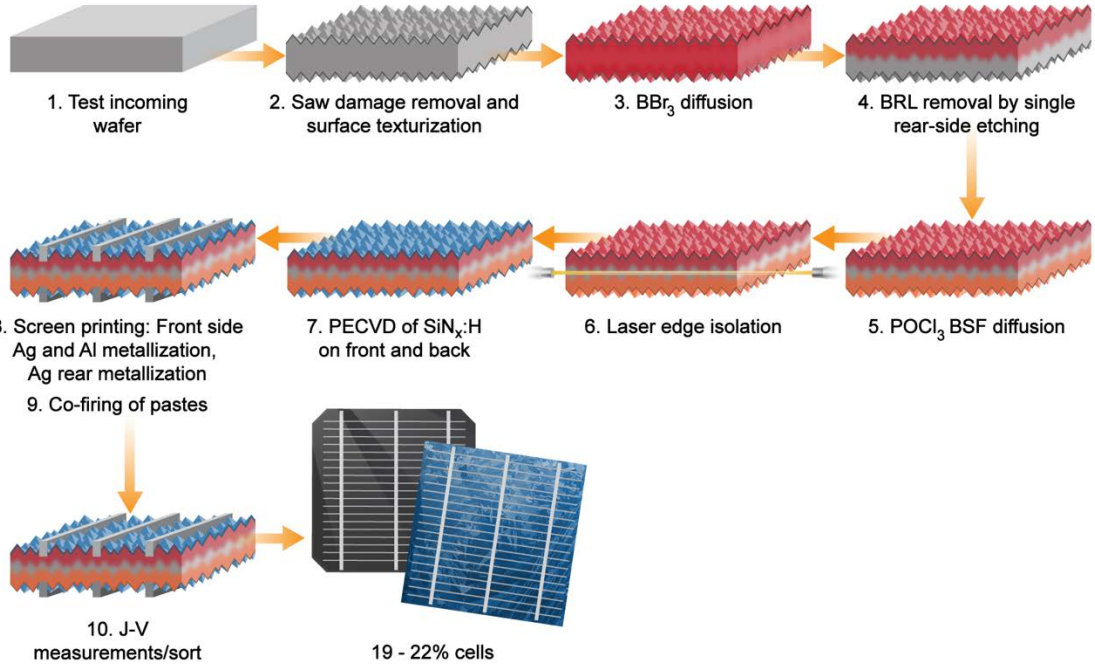
Swanson, Richard M. 2007. "Developments in silicon solar cells." Electron Devices Meeting, 2007. IEDM 2007. IEEE International.

Tinker, Lenny. 2018. “Photovoltaics Subprogram.” Solar Energy Technology Office Portfolio Review, Washington, DC. https://www.energy.gov/sites/prod/files/2018/02/f49/SETO%202018%20Portfolio%20Review%20-%20Day%201%20Keynote%20PV.pptx

Woodhouse, M., R. Jones-Albertus, D. Feldman, R. Fu, K. Horowitz, D. Chung, D. Jordan, and S. Kurtz. 2016. *On the Path to SunShot: The Role of Advancements in Solar Photovoltaic Efficiency, Reliability, and Costs*. NREL/TP-6A20-65872. Golden, CO: National Renewable Energy Laboratory. https://www.nrel.gov/docs/fy16osti/65872.pdf.

World Energy Council. 2017. World Energy Resources: Solar | 2016. https://www.worldenergy.org/wp-content/uploads/2017/03/WEResources_Solar_2016.pdf.

Appendix: Emerging Cell Technologies



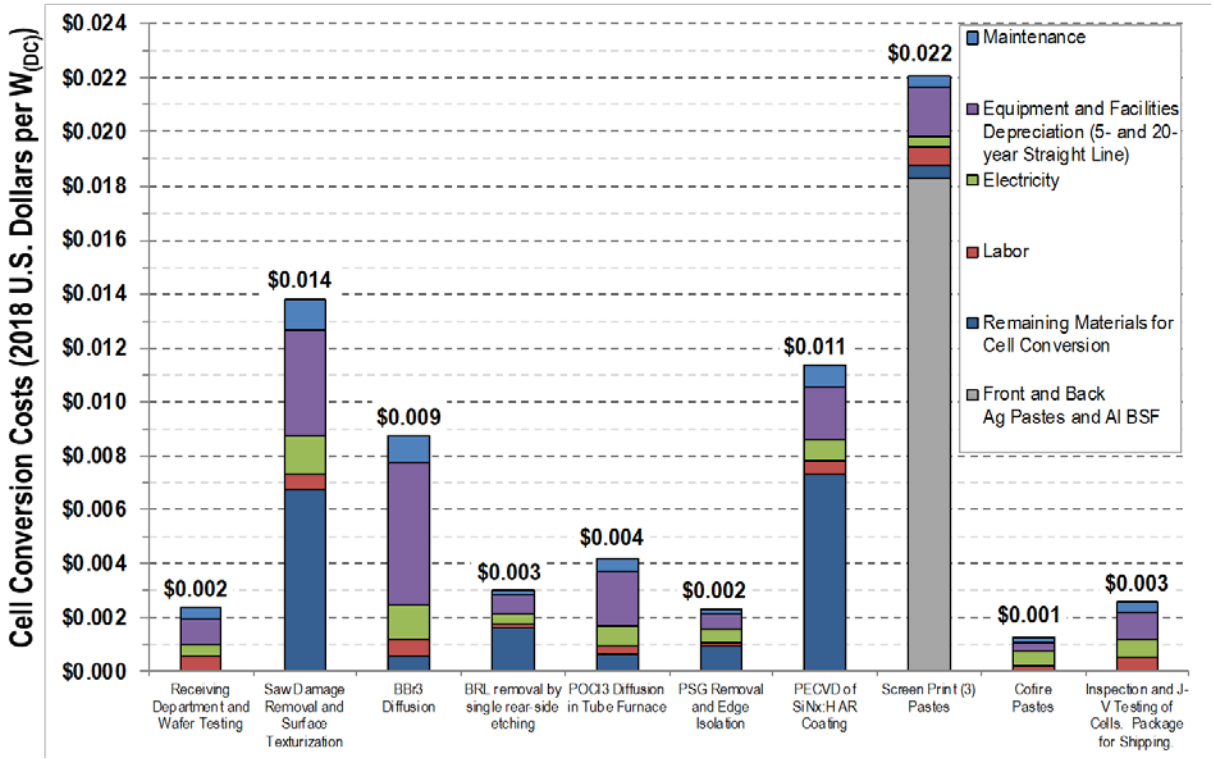


Figure A-1. *n*-PERT cell process flow and costs by step

This analysis assumes manufacturing in urban China, 20.5% efficient cells that are 244 cm^2. Abbreviations shown: AR: anti-reflective; BRL: boron-rich layer

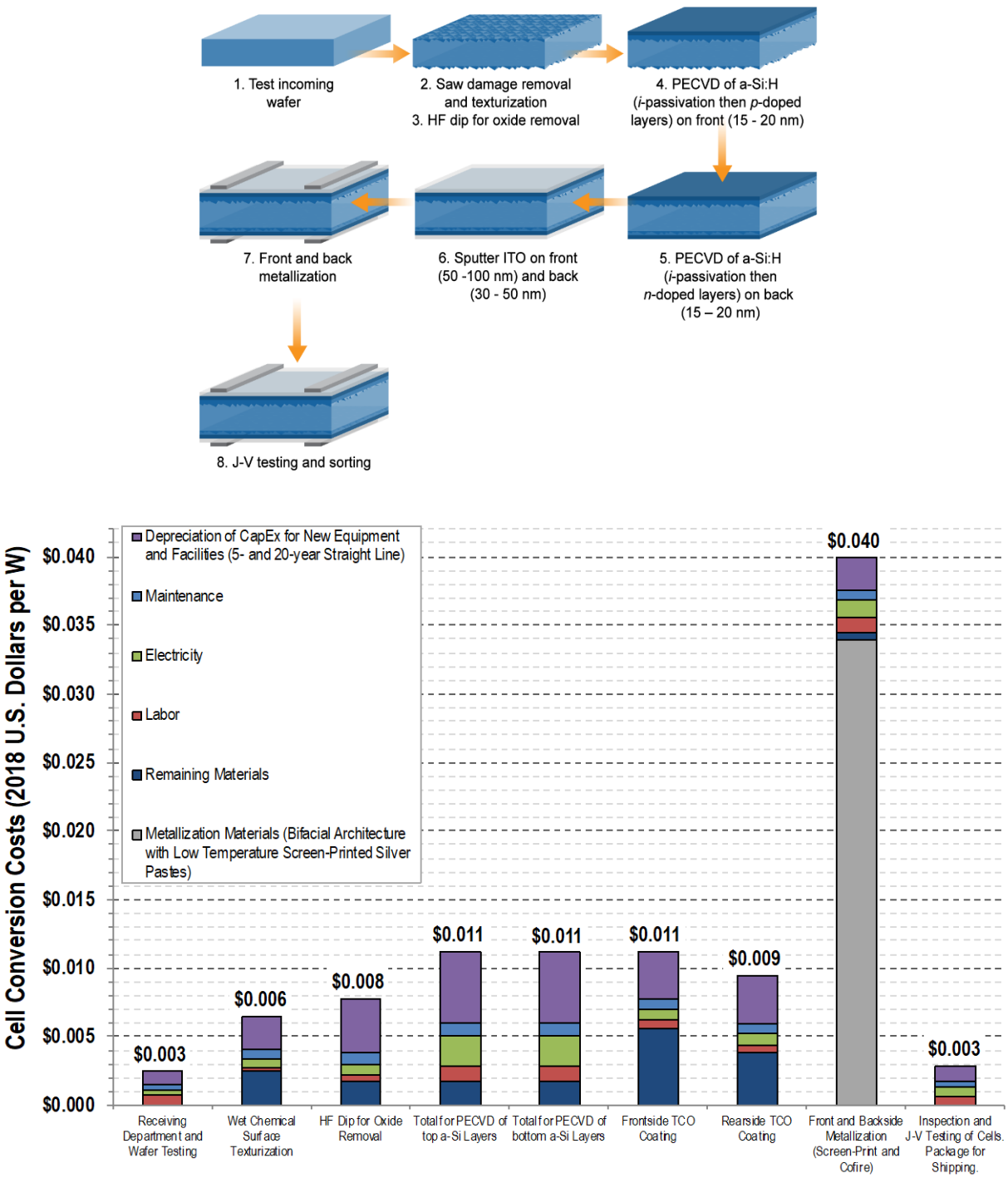


Figure A-2. Screen-printed SHJ cell process flow and costs by step

This analysis assumes manufacturing at a 2-GW greenfield facility in urban China, 22.5% efficient cells that are 244 cm^2. ITO: indium tin oxide; a-Si: amorphous silicon; TCO: transparent conductive oxide

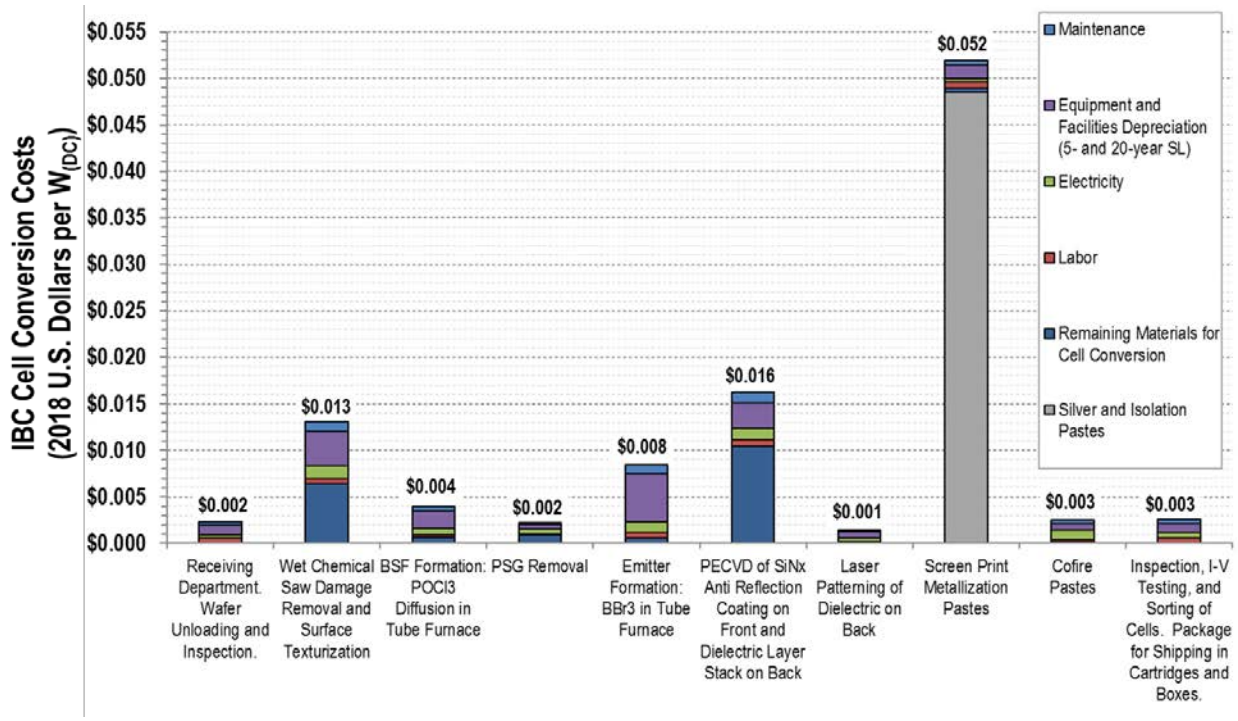


Figure A-3. Screen-printed IBC cell costs by step

This analysis assumes manufacturing at a greenfield facility in urban China, 23.0% efficient cells that are 244 cm^2 on *n*-type M2 format wafers. Abbreviations shown: PSG: phosphorous silicate glass