Trends in SiC MOSFET Threshold Voltage and ON-Resistance Measurements from Thermal Cycling and Electrical Switching Stresses

Preprint

Joseph P. Kozak and Khai D. T. Ngo
Virginia Tech

Douglas J. DeVoto and Joshua J. Major
National Renewable Energy Laboratory

Presented at the 10th International Conference on Integrated Power Electronics
Stuttgart, Germany
March 20–22, 2018

Suggested Citation
Kozak, Joseph P., Khai D. T. Ngo, Douglas J. DeVoto, and Joshua J. Major. 2018. "Trends in SiC MOSFET Threshold Voltage and ON-Resistance Measurements from Thermal Cycling and Electrical Switching Stresses: Preprint." Golden, CO: National Renewable Energy Laboratory. NREL/CP-5400-70550. https://www.nrel.gov/docs/fy18osti/70550.pdf.

NREL is a national laboratory of the U.S. Department of Energy
Office of Energy Efficiency & Renewable Energy
Operated by the Alliance for Sustainable Energy, LLC

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications.

Conference Paper
NREL/CP-5400-70550
September 2018

Contract No. DE-AC36-08GO28308

NOTICE

This work was authored in part by the National Renewable Energy Laboratory, operated by Alliance for Sustainable Energy, LLC, for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. Funding provided by the U.S. Department of Energy Office of Energy Efficiency and Renewable Energy Advanced Manufacturing Office. The views expressed in the article do not necessarily represent the views of the DOE or the U.S. Government. The U.S. Government retains and the publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes.

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications.

U.S. Department of Energy (DOE) reports produced after 1991 and a growing number of pre-1991 documents are available free via www.OSTI.gov.

Cover Photos by Dennis Schroeder: (left to right) NREL 26173, NREL 18302, NREL 19758, NREL 29642, NREL 19795.

NREL prints on paper that contains recycled content.

Trends in SiC MOSFET Threshold Voltage and ON-Resistance Measurements from Thermal Cycling and Electrical Switching Stresses

Joseph P. Kozak, Center for Power Electronic Systems (CPES), Virginia Tech, Blacksburg, VA. USA
Douglas J. DeVoto, National Renewable Energy Laboratory (NREL), Golden, CO. USA
Joshua J. Major, National Renewable Energy Laboratory (NREL), Golden, CO. USA
Khai D.T. Ngo, Center for Power Electronic Systems (CPES), Virginia Tech, Blacksburg, VA. USA

Abstract

Integrating SiC power MOSFETs is very attractive for advancing power electronic systems, yet the system reliability with new devices remains in question. This work presents two accelerated test experiments to further investigate the packaging and semiconductor failures of a TO-247 SiC MOSFET. First, a variation on power cycling experiments—switching cycling—is introduced. Traditional power cycling experiments utilize conduction losses to self-heat the device where a large temperature swing causes degradation at the packaging level. However, by decreasing the on-time such that the device only turns on and immediately turns off, the temperature swing is decreased and the semiconductor itself is degraded. This work shows experimental device degradation caused by continuous switching events—switching cycling, at 90% of the device's breakdown voltage. Second, thermal cycling experiments were conducted between -40°C and 175°C to observe degradation in the mechanical packaging of the device. Experimentally-measured changes in threshold voltage and ON-resistance are recorded in both experiments and compared. These results also illustrate the spectrum between device and package degradation from accelerated test methods.

1 Introduction

The integration of wide-bandgap (WBG) materials into power semiconductor devices is a necessary step to advance power electronics systems to be lighter, smaller, and more efficient. Silicon carbide (SiC) power metal oxide semiconductor field effect transistors (MOSFETs), in comparison to silicon devices, have most notable advantages in electrical breakdown field, thermal conductivity, electron saturation drive velocity, and irradiation tolerance [1-3]. Stevanovic et al. [3] indicate that the increase in critical electric field strength from utilizing SiC will decrease the size of insulating (or blocking) layers within transistors. This decrease in blocking layer size, in conjunction with higher doping concentrations, will result in lower ON-resistance (R_{DSon}) values with respect to comparable silicon devices. In addition, transistors capable of sustaining higher operating temperatures (SiC can on average maintain a 25°C higher operating temperature than Si [2]) are highly attractive for many applications.

While the material characteristics of SiC are known, and significant research has been invested into characterizing SiC MOSFETs for circuit applications, the degradation of these devices under various operating conditions (including switching frequency) is not fully understood [4]. This work aims to expand on traditional accelerated tests, with the intent of understanding the range of package and semiconductor device failures. This can help in designing in-situ prognostic circuits to determine the remaining useful lifetime of a commercially-available device.

To determine lifetime of power semiconductor devices, numerous traditional accelerated tests are typically used. Some of the most common are thermal cycling, power cycling, and gate biasing tests [5-11]. Stressing the devices in these different ways will accelerate the progression of failure mechanisms within the packaged device that normally require years of field operation to develop. The most common failure mechanisms are within the packaging level and include wire bond lift-off and solder delamination. These mechanisms are most often stressed through thermal and power cycling accelerated tests [12]**.** High temperature gate bias (HTGB) experiments are commonly used to stress the oxide layer of the semiconductor device [6, 9, 13]. Recent research has been working to connect these failure mechanisms with various device characteristics or electrical measurements as precursor parameters**.** For solder delamination or wire bond lift-off, the most common precursor parameter is the device R_{DSon} [5, 14]. For degradation of the oxide layer, changes in threshold voltage (V_{th}) is a very common precursor parameter [10, 15-17]. This work aims to expand on these existing accelerated aging tests by introducing switching cycling to stress a 1200 V, 10A, TO-247 SiC MOSFET [18] under continuous switching events.

Changes in V_{th} and R_{DSon} are investigated through the two different stress tests—thermal cycling and switching cycling. Section 2 introduces the new type of accelerated test called switching cycling. An automated, clamped, inductive circuit test was constructed such that switching events would stress the semiconductor device under various operating conditions. Section 3 explains the second experiment—a traditional thermal cycling stress experiment. Finally, overall conclusions comparing the degradation of the two devices are discussed in Section 4.

2 Switching Cycling

Traditional power cycling experiments utilize self-heating effects caused by conduction losses within a device [11]. Normally, a "control device" external to the device-under-

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications

test (DUT) allows current to flow, heating up the DUT until it reaches a maximum temperature (T_{max}). Upon reaching this T_{max}, the control device turns off and the DUT is cooled to a minimum temperature (T_{min}). The experiment continues until the desired number of cycles is reached or the device fails. Like thermal cycling, the most common failure mechanisms for power cycling also includes bond wire lift-off [19, 20], and solder delamination [21, 22].

The experiment presented in this work varies from traditional power cycling. The stress on the DUT is not controlled by an external device, nor is the DUT stressed through a large temperature swing, caused by conduction losses. The stress is primarily generated through the switching events. For this reason, a clamped inductive circuit (Fig. 1), normally used to investigate transistor switching characteristics, was selected as the primary stress circuit topology.

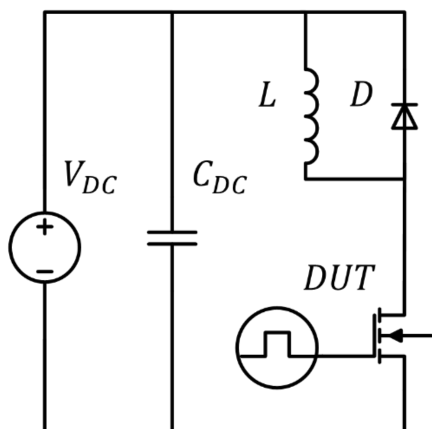

Figure 1 General clamped, inductive circuit

The clamped circuit was selected to utilize the nature of the freewheeling diode to better control the current and stress energy applied through the DUT. The experiment is designed to stress the device through continuous switching events, and the resulting switching losses. The switching events are applied to understand how switching events degrade the semiconductor and the device package. The switching cycling experiment is compared against a dc-bias test that holds the same relative drain-source voltage (V_{DS}) but does not switch. Both experiments are conducted at 90 percent of the breakdown voltage (V_{BD}). It can be seen that switching events will increase degradation within the same amount of time in comparison to only a high dc-bias.

2.1 Experimental Design and Results

A test circuit was designed to continuously stress the DUT while monitoring the V_{DS} and current waveforms. The test circuit and auxiliary equipment are connected through a general-purpose interface bus (GPIB) network and controlled through MATLAB. Through this network, the circuit automatically stresses the device for a designated amount of time/cycles and monitors $V_{DS,}$ drain-source current (I_{DS}), gate-source voltage (V_{GS}), and temperature. The test equipment and GPIB network can be seen in Fig. 2.

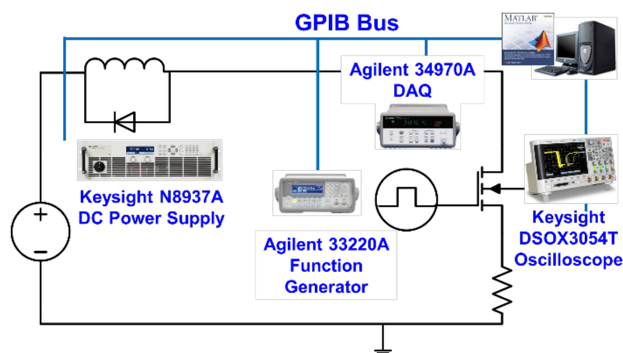

Figure 2 Full test circuit topology

To demonstrate this accelerated test method and determine what failure mechanisms are most affected by switching events, initial experimental tests were conducted at 90 percent of the V_{BD}, with V_{DS} set to 1450 V (Fig. 3). V_{GS} was set to +20/-5 V for switching cycling and was held at -5 V for dc-bias testing.

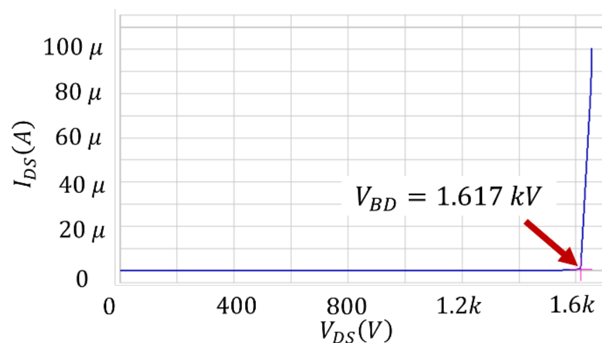

Figure 3 Measured V_{BD} used to determine the test conditions described in Table I

For switching cycling, the switching frequency was set to 4 kHz with a total on-time of 150 ns. In this way, the conduction channel is opened and closed quickly to minimize self-heating effects from conduction losses. The degradation of R_{DSon} was expected to be smaller in comparison to the results of thermal cycling; the V_{th} changes were expected to be larger. Zheng [9] shows this trend, but with minimal energy applied across the drain-source of the device.

Table I shows the selected circuit components and their corresponding values. The gate loop and power loop were optimized such that the main stresses applied onto the device would be from the switching event and not excessive voltage or current overshoot, or convective heating. The overall test platform is shown in Fig. 4.

The chosen DUTs were initially characterized in an Agilent B1505A curve tracer. After every six hours of testing, the devices were removed from the circuit and re-characterized. Figure 5 shows the V_{DS} and I_{DS} switching waveforms from switching cycling. The dc-bus was set to 1450 V, and the maximum current reached 23.5 A. A single device has been demonstrated under each of the test conditions.

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications

TABLE I
Experimental parameters and component part numbers

Parameter	Numerical Quantity
Input Voltage, V_{DC}	1450 V (max)
Input Capacitance, C_{in}	$820uF$
Inductor, L	11.214 uH
Shunt Resistor, R_{shunt}	0.02558 Ω
Power Diode, D1	DH40-18A
DUT	C2M0280120D
ON-time, t_{on}	150 ns
Frequency, f_s	4 kHz

Curve tracer measurements taken every six hours from both the switching cycling and dc-bias tests are shown in Figs. 6-10. The measurement test conditions were comparable with those listed on characteristic curves of the device datasheet [18]. The transfer characteristics (Figs. 6 and 7) were taken with a V_{DS} of 20 V. A second, more sensitive test was conducted where V_{DS} was set to equal V_{GS} and the I_{DS} current was measured as V_{GS} was swept. These results (Fig 8) show the large shift in V_{th}. It can be seen that within the first 12 hours of testing no major degradation occurred and V_{th} was approximately 2.5 V, but between the 12-18 hours of testing, V_{th} increased to approximately 3 V—a 20 percent increase.

R_{DSon} measurements (Figs. 9 and 10) were taken with V_{GS} set to 20 V and sweeping I_{DS}. Only at the 24-hour measurement can a change be seen in the switching cycling results. The maximum change of R_{DSon} in switching cycling was calculated to be two percent. These results lend credence to the hypothesis that switching cycling stresses the device semiconductor to a greater extent than the device package.

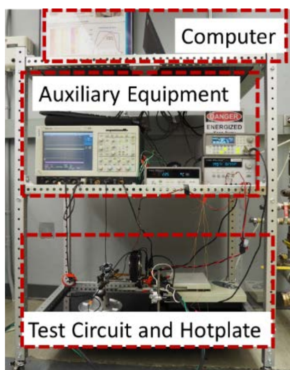

Figure 4 Switching cycling test bench

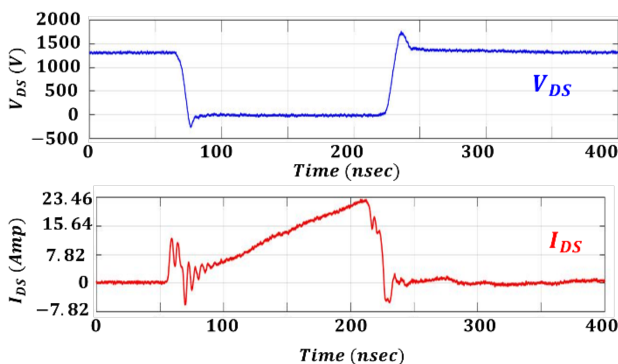

Figure 5 V_{DS} (top) and I_{DS} (bottom) switching events of the DUT performed under the conditions listed in Table I

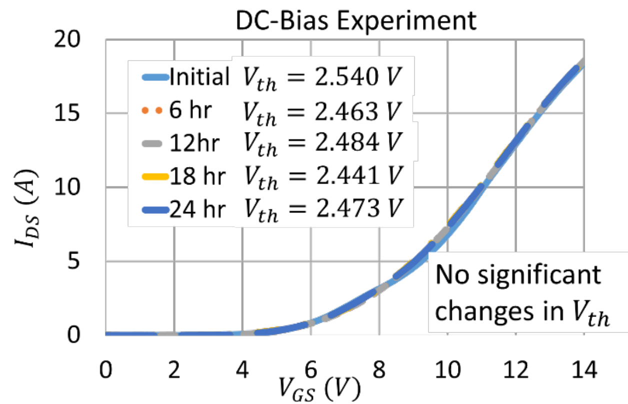

Figure 6 Changes in transfer characteristics for dc-bias test where V_{DS} equals 20 V

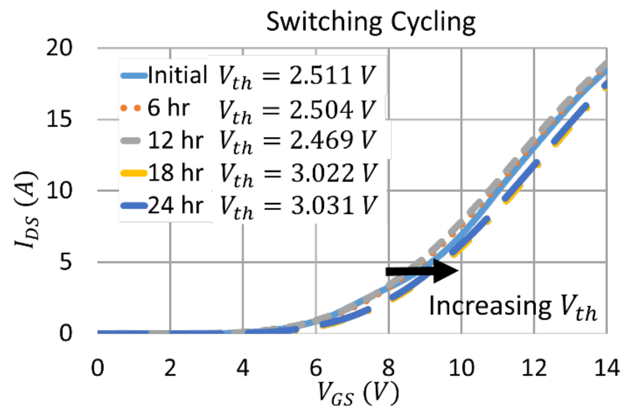

Figure 7 Changes in transfer characteristics for switching cycling experiments

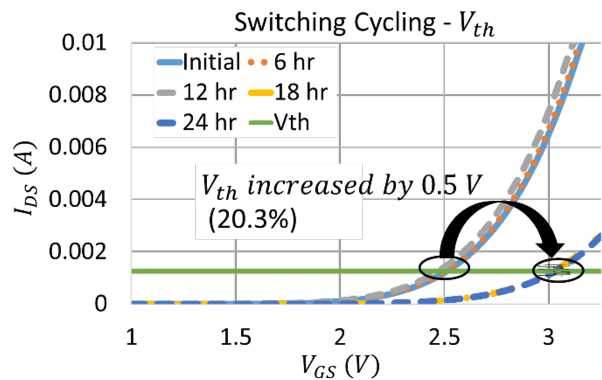

Figure 8 Changes in threshold voltage of switching cycling experiments (zoomed in of Fig. 7)

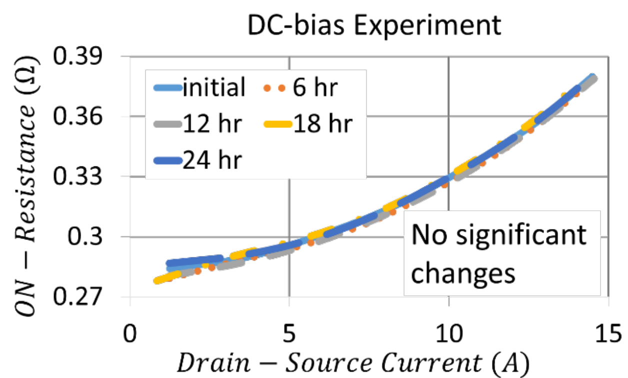

Figure 9 Changes in ON-resistance for dc-bias experiments

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications

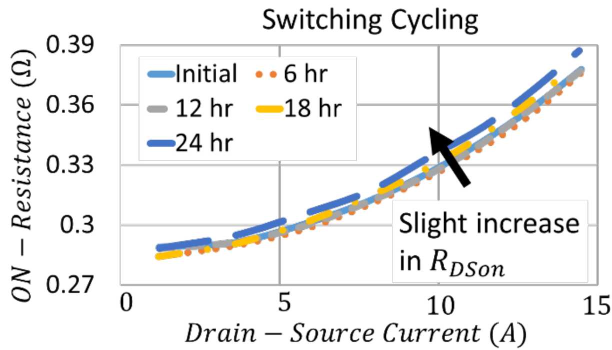

Figure 10 Changes in ON-resistance for switching cycling experiments

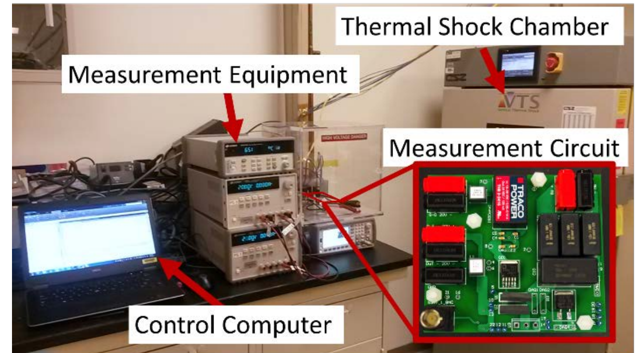

Figure 11 Thermal cycling test bench

3 Thermal Cycling Degradation

3.1 Introduction and Expected Degradation

Traditional thermal cycling tests allow for thermo-mechanical reliability evaluation of a package. Thermal cycling is defined here as exposing a packaged device to temperature variations through an externally created thermal profile [23]. Differences in coefficients of thermal expansion between the device and packaging layers will create, grow, and propagate cohesive fractures, or cracks, within a bonding layer, such as solder, or adhesive fracture between layers within the package. These cracks will expand until a failure condition is achieved within the layer such as solder delamination, or bond wire lift-off [5, 21].

A 1200V, 10A, TO-247 packaged SiC power MOSFET [18] was subjected to thermal cycling in a thermal shock chamber. Wires were soldered onto the device and connected to a specially-designed measurement circuit external to the chamber. The experimental testbed and measurement circuit are shown in Fig. 11. In this way, both V_{th} and R_{DSon} measurements could be taken at both the maximum and minimum (175°C and -40°C, respectively) cycle temperatures. This results in a difference of 215°C between the temperature extremes.

The V_{th} measurements were taken with V_{GS} equalling V_{DS}, and the voltage was swept until I_D reached 1.25 mA. The R_{DSon} measurement was taken with a V_{GS} of 20 V and a I_{DS} of 3 A. V_{DS} was then measured across the device and R_{DSon} was calculated by (1).

$$R_{DSon} = \frac{V_{DS(on)}}{I_{DS}} \quad (1)$$

While these measurements were taken for each cycle to observe progressive degradation for each cycle, a full analysis was conducted for temperatures ranging from -50°C to 175°C in 25°C increments. Data acquisition was automated in MATLAB to assure consistency between all measurements.

3.2 Experimental Results

Before thermal cycling experiments were conducted, a sensitivity analysis was conducted for the shock chamber and measurement equipment. Systematic uncertainty of the test system was calculated and incorporated in the results for V_{th}; the measurement error for R_{DSon} was found to be negligible. Experimental measurements of V_{th} and R_{DSon} were swept at increasing temperatures every 100 cycles. The R_{DSon} measurements and normalized measurements are shown in Fig. 12 and 13. V_{th} measurements are shown in Fig. 14. For each, the results are shown for every 500 cycles until 1500 cycles.

Figures 12 and 13 show that after 1500 cycles, changes in R_{DSon} measurements have occurred. Within the first 1000 cycles, a decrease in R_{DSon} at low temperatures was observed, along with a slight increase at higher temperatures. However, after 1500 cycles, a large increase is seen within the complete temperature range. Figure 13 shows the changes in R_{DSon} normalized to the initial measurement; the maximum change in R_{DSon} is 15 percent. It is speculated that this change is caused by a crack propagation in the solder layer, or a wire bond lift-off [14, 21].

No major changes can be seen in the V_{th} measurements. All results are within the statistical bounds of the measurements. It is believed that the shift from initial results to 500 cycles is a result of burn-in effects. V_{th} degradation is understood to be caused more by semiconductor stresses, like high electric field on the gate [6, 7, 13, 15]. Overall, experimental results show changes consistent with other traditional thermal cycling experiments [23].

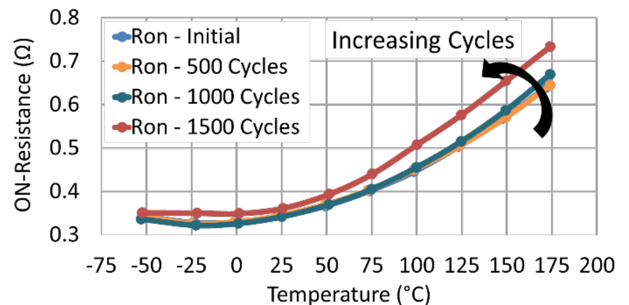

Figure 12 Experimental results for changes in R_{DSon}

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications

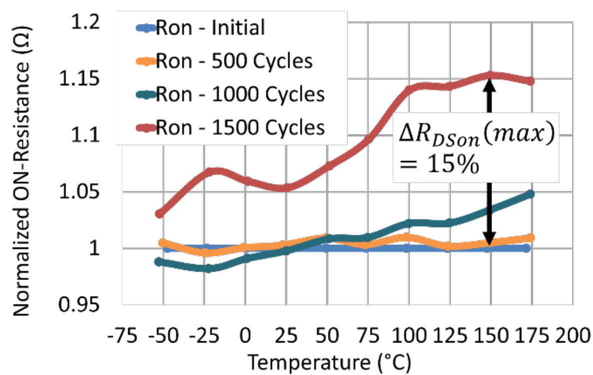

Figure 13 Normalized results for changes in R_{DSon}

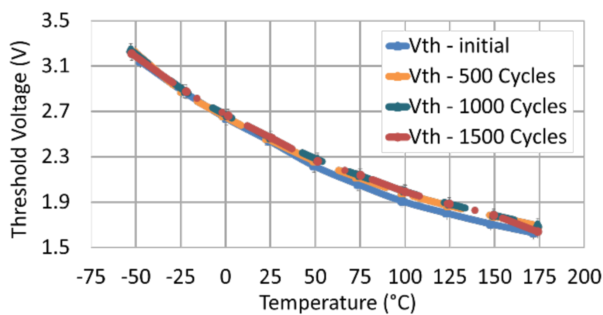

Figure 14 Experimental results for changes in V_{th}

4 Conclusion and Future Work

Both cycling experiments have shown degradation of the same type of SiC power MOSFET. The changes in R_{DSon} from the thermal cycling suggest that the packaging solder layer or the wire bonds are degrading. Because of the large step increase, it can be mostly assumed to be a wire bond lift-off. In comparison, the V_{th} of the device was not changed at all.

Comparing the dc-bias experimental results with those from switching cycling shows negligible changes in R_{DSon}, but considerable changes in V_{th}. Overall, constant switching events in switching cycling cause degradation in semiconductor level parameters, while thermal cycling shows degrading in the device package.

This work provides two novelties. First is the introduction and creation of an automatic, switching cycle test where a SiC MOSFET is stressed through switching events with high voltage applied across the device. The second novelty is the comparison of these results to the degradation from a traditional thermal cycling test. Failure mechanisms, which have previously been linked with external environmental and internal electrical and thermal stresses, have been monitored via device characteristics under varying frequency-domain accelerated cycling tests.

Future work includes additional switching cycling experiments, as well as completing additional accelerated lifetime tests. Changing the frequency domain from transient events that occur in nanoseconds, to minutes for passive thermal cycling, will separate and identify the dominant failure mechanism(s) within a package. This will help build understanding of the failures within the device and within the package. This work can also lead to future work designing in-situ prognostic circuits to calculate the remaining useful lifetime of TO-247 packaged SiC MOSFETs.

5 Acknowledgments

The authors acknowledge the financial support provided by the U.S. Department of Energy Advanced Manufacturing Office through the Wide Bandgap Generation (WBGen) Fellowship at the Center for Power Electronics Systems (CPES) at Virginia Tech www.eng.vt.edu/WBGen.

6 References

[1] H. Di, J. Noppakunkajorn, and B. Sarlioglu, "Efficiency comparison of SiC and Si-based bidirectional DC-DC converters," in *Transportation Electrification Conference and Expo (ITEC), 2013 IEEE*, 2013, pp. 1-7.

[2] W. Gangyao, W. Fei, G. Magai, L. Yang, A. Huang, and M. Das, "Performance comparison of 1200V 100A SiC MOSFET and 1200V 100A silicon IGBT," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 3230-3234.

[3] L. D. Stevanovic, K. S. Matocha, P. A. Losee, J. S. Glaser, J. J. Nasadoski, and S. D. Arthur, "Recent advances in silicon carbide MOSFET power devices," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, 2010, pp. 401-407.

[4] L. C. Yu, G. T. Dunne, K. S. Matocha, K. P. Cheung, J. S. Suehle, and K. Sheng, "Reliability Issues of SiC MOSFETs: A Technology for High-Temperature Environments," *IEEE Transactions on Device and Materials Reliability,* vol. 10, pp. 418-426, 2010.

[5] S. Dusmez, S. H. Ali, M. Heydarzadeh, A. S. Kamath, H. Duran, and B. Akin, "Aging Precursor Identification and Lifetime Estimation for Thermally Aged Discrete Package Silicon Power Switches," *IEEE Transactions on Industry Applications,* vol. 53, pp. 251-260, 2017.

[6] M. Beier-Moebius and J. Lutz, "Breakdown of gate oxide of 1.2 kV SiC-MOSFETs under high temperature and high gate voltage," in *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2016, pp. 1-8.

[7] J. O. Gonzalez, O. Alatise, J. Hu, L. Ran, and P. A. Mawby, "An Investigation of Temperature-Sensitive Electrical Parameters for SiC Power MOSFETs," *IEEE Transactions on Power Electronics,* vol. 32, pp. 7954-7966, 2017.

[8] S. Liu, W. Sun, Q. Qian, C. Gu, Y. Huang, S. Bai, *et al.*, "Investigations on degradation and optimization of 1.2kV 4H-SiC MOSFET under repetitive unclamped inductive switching stress," in *2015 IEEE 27th International Symposium on*

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications

Power Semiconductor Devices & IC's (ISPSD), 2015, pp. 205-208.
[9] Z. Chen, Y. Yao, M. Danilovic, and D. Boroyevich, "Performance evaluation of SiC power MOSFETs for high-temperature applications," in *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, 2012, pp. DS1a.8-1-DS1a.8-9.
[10] R. M. Kaplar, Matthew; Brock, Reinhard; King, Michael; Smith, Mark A.; Atcitty, Stanley, "Stress Testing on Silicon Carbide Electronic Devices for Prognostics and Health Management," Sandia National Laboratory 2011.
[11] A. O. Ibrahim, J. P.; Lallemand, R.; Khatir, Z., "Power Cycling Tests in High Temperature Conditions of SiC MOSFET Power Modules and Ageing Assessment," presented at the 9th International Conference on Integrated Power Electronics Systems, Nurnberg, Germany, 2016.
[12] A. Ibrahim, J. P. Ousten, R. Lallemand, and Z. Khatir, "Power Cycling Tests in High Temperature Conditions of SiC-MOSFET Power Modules and Ageing Assessment," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, 2016, pp. 1-6.
[13] R. Ouaida, M. Berthou, J. León, X. Perpiñà, S. Oge, P. Brosselard*, et al.*, "Gate Oxide Degradation of SiC MOSFET in Switching Conditions," *IEEE Electron Device Letters,* vol. 35, pp. 1284-1286, 2014.
[14] S. Dusmez and B. Akin, "Remaining useful lifetime estimation for degraded power MOSFETs under cyclic thermal stress," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 3846-3851.
[15] A. J. Lelis, R. Green, and D. B. Habersat, "SiC MOSFET reliability and implications for qualification testing," in *2017 IEEE International Reliability Physics Symposium (IRPS)*, 2017, pp. 2A-4.1-2A-4.4.
[16] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic Mechanisms of Threshold-Voltage Instability and Implications for Reliability Testing of SiC MOSFETs," *IEEE Transactions on Electron Devices,* vol. 62, pp. 316-323, 2015.
[17] R. A. Wood and T. E. Salem, "Long-term operation and reliability study of a 1200-V, 880-A all-SiC dual module," in *International Symposium on Power Electronics Power Electronics, Electrical Drives, Automation and Motion*, 2012, pp. 1520-1525.
[18] Wolfspeed, "C2M0280120D Datasheet," ed. https://www.wolfspeed.com/media/downloads/171/C2M0280120D.pdf
[19] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectronics Reliability,* vol. 42, pp. 653-667, 2002/04/01/ 2002.
[20] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition Monitoring for Device Reliability in Power Electronic Converters: A Review," *IEEE Transactions on Power Electronics,* vol. 25, pp. 2734-2752, 2010.
[21] W. Lai, M. Chen, L. Ran, S. Xu, N. Jiang, X. Wang*, et al.*, "Experimental Investigation on the Effects of Narrow Junction Temperature Cycles on Die-Attach Solder Layer in an IGBT Module," *IEEE Transactions on Power Electronics,* vol. 32, pp. 1431-1441, 2017.
[22] D. C. Katsis and J. D. v. Wyk, "Void-induced thermal impedance in power semiconductor modules: some transient temperature effects," *IEEE Transactions on Industry Applications,* vol. 39, pp. 1239-1246, 2003.
[23] H. Cui, "Accelerated temperature cycle test and Coffin-Manson model for electronic packaging," in *Annual Reliability and Maintainability Symposium, 2005. Proceedings.*, 2005, pp. 556-560.

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications