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Finally, the authors express their great appreciation to Mike Ropp of NPPT for his valuable technical inputs and background material.

List of Acronyms

AC	Alternating current
DOE	Department of Energy
DER	Distributed energy resource
EERE	Office of Energy Efficiency and Renewable Energy (DOE)
EPS	Electric power system
EUT	Equipment under test
FRT	Frequency ride-through
FWC	Frequency-Watt control
GSF	Grid support function
IEEE	Institute of Electrical and Electronic Engineers
NREL	National Renewable Energy Laboratory
PCC	Point of common coupling
PHIL	Power hardware-in-the-loop
PV	Photovoltaic
RL	Resistive-inductive
RLC	Resistive-inductive-capacitive
RMS	Root mean squared
ROT	Run-on time (of an electrical island)
UL	Underwriters Laboratories
VRT	Voltage ride-through
VVC	Volt-VAr control
Volt-VAr	Voltage-reactive power
X/R	Reactance-to-resistance ratio

Executive Summary

It has long been required that distributed energy resources (DERs) such as photovoltaic (PV) systems disconnect from the electric grid when an electrical island is formed. Typically PV inverters perform the islanding detection function autonomously using one or more of a variety of methods. As PV and other DER systems are connected to the grid at increased penetration levels, island detection may become more challenging for two reasons:

1. In islands containing many DERs, active inverter-based anti-islanding methods may have more difficulty detecting islands because each individual inverter's efforts to detect the island may be interfered with by the other inverters in the island.

2. The increasing numbers of DERs are leading to new requirements that DERs ride through grid disturbances and even actively try to regulate grid voltage and frequency back towards nominal operating conditions. These new grid support requirements may directly or indirectly interfere with anti-islanding controls.

This report describes a series of tests designed to examine the impacts of both grid support functions and multi-inverter islands on anti-islanding effectiveness. Crucially, the multi-inverter anti-islanding tests described in this report examine scenarios with multiple inverters connected to multiple different points on the grid. While this so-called "solar subdivision" scenario has been examined to some extent through simulation, this is the first known work to test it using hardware inverters. This was accomplished through the use of power hardware-in-the-loop (PHIL) simulation, which allows the hardware inverters to be connected to a real-time transient simulation of an electric power system that can be easily reconfigured to test various distribution circuit scenarios. The anti-islanding test design was a modified version of the unintentional islanding test in IEEE Standard 1547.1, which creates a balanced, resonant island with the intent of creating a highly challenging condition for island detection. Three common, commercially available single-phase PV inverters from three different manufacturers were tested.

The first part of this work examined each inverter individually using a series of pure hardware resistive-inductive-capacitive (RLC) resonant load based anti-islanding tests to determine the worst-case configuration of grid support functions for each inverter. A grid support function is a function an inverter performs to help stabilize the grid or drive the grid back towards its nominal operating point. The four grid support functions examined here were voltage ride-through, frequency ride-through, Volt-VAr control, and frequency-Watt control. The worst-case grid support configuration was defined as the configuration that led to the maximum island duration (or run-on time, ROT) out of 50 tests of each inverter. For each of the three inverters, it was observed that maximum ROT increased when voltage and frequency ride-through were activated. No conclusive evidence was found that Volt-VAr control or frequency-Watt control increased maximum ROT. Over all single-inverter test cases, the maximum ROT was 711 ms, well below the two-second limit currently imposed by IEEE Standard 1547-2003.

A subsequent series of 244 experiments tested all three inverters simultaneously in the same island. These tests again used a procedure based on the IEEE 1547.1 unintentional islanding test to create a difficult-to-detect island condition. For these tests, which used the two worst-case grid support function configurations from the single-inverter tests, the inverters were connected to a

variety of island circuit topologies designed to represent the variety of multiple-inverter islands that may occur on real distribution circuits. The interconnecting circuits and the resonant island load itself were represented in the real-time PHIL model. PHIL techniques similar to those employed here have been previously used and validated for anti-islanding tests, and the PHIL resonant load model used in this test was successfully validated by comparing single-inverter PHIL tests to conventional tests using an RLC load bank.

The multi-inverter tests varied the following parameters to search for worst-case ROTs:

- Island circuit topology and interconnecting impedances
- Load location relative to the inverter connection points
- Grid impedance at the point of island disconnection
- The placement of each inverter on the circuit
- The timing of the island disconnection relative to inverter output

In all multi-inverter island tests, the maximum island duration was 632 ms, again well within the allowed two-second window.

There have been some concerns expressed about the possibility of load rejection overvoltage during islanding events. While such overvoltage can be seen in unbalanced islands, as seen in previous work, it is not particularly expected in the very well-balanced islands used for anti-islanding tests. Nevertheless, the island waveforms recorded here were examined for overvoltage, and no overvoltage exceeding 110% of nominal was observed.

In summary, for the islanding detection philosophies represented in the inverters tested, this report found evidence that performing voltage and frequency ride-through prolongs island duration for single inverters, but did not find evidence that multi-inverter islands necessarily increase that duration further. Future research can focus on determining whether this conclusion extends to islands with more than three inverters. Nevertheless, it is encouraging that in all tested cases of multi-inverter, multi-point islands with grid support functions active, island ROTs were well below the two-second limit currently imposed by IEEE Standard 1547-2003.

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1 Introduction

A long-standing requirement for distributed energy resources (DERs), such as photovoltaic (PV) systems, connected to the electric power system (EPS) is that they must disconnect from the EPS when an electrical island is formed. As used here, the term *island* refers to a portion of the EPS that remains energized by one or more DERs following disconnection from the remainder of the EPS. Intentional islands, also known as microgrids, are not in the scope of this report. This report is concerned with *unintentional* islands, which form when a breaker or other protective device opens, isolating a part of the EPS containing at least one DER. Unintentional island detection helps prevent potential hazardous conditions such as unexpected contact with energized lines within an island, and closing of a breaker between an EPS and an island with out-of-phase voltages.

In the IEEE 1547-2003 Standard for Interconnecting Distributed Resources with Electric Power Systems, inverters paired with DERs are required to disconnect from the EPS within two seconds of the formation of an electrical island [1]. For inverter-based DERs, such as PV systems and most energy storage systems, this is often achieved through autonomous island detection controls resident in the inverter that connects the DER to the EPS. Such controls use one or more of a wide variety of active or passive methods to detect an island [2]. Many such methods rely at least partially on the EPS voltage or frequency either going outside normal operating regions or changing faster than would occur in a non-islanded situation to detect an island.

In addition to requiring DERs to disconnect during unintentional islands, standards such as IEEE 1547-2003 have also required DERs to quickly disconnect when EPS conditions migrated outside of relatively narrow operating regions and have typically prohibited DERs from attempting to regulate grid voltage or frequency [1]. This was a feasible solution with only a small number of DERs interconnected to the EPS. However, as the number and aggregate power output of DERs – especially PV systems – increase, many utilities, regulators, and standards-setting organizations are considering or imposing new requirements that DERs remain connected during (or ride through) various abnormal grid conditions and even help stabilize the grid in abnormal conditions [3], [4]. These ride-through new requirements are set in place to help stabilize the grid in abnormal conditions and potentially bring the grid back to normal operation faster. However, such requirements make many island detection methods more difficult because DERs must now be able to distinguish between abnormal conditions due to the grid itself and abnormal conditions due to island formation [5].

Simulations have shown that island detection can become more difficult when performing grid support functions (GSFs) [6]. This has also been verified experimentally in [7], [8], which examined one PV inverter in a small number of islanding tests and found a small increase in island run-on time (ROT) with grid support functions active, though all ROTs remained below one second, in compliance with IEEE 1547-2003.

In addition to the impact of GSFs on island detection, the presence of many DERs on the same grid further increases the difficulty of detecting islands and disconnecting. When an island forms containing many DERs, it becomes harder for any individual DER to actively perturb the grid to detect an island. Some past work has examined the ability of inverters to detect multi-inverter islands both through simulation [9], and through laboratory experiment [10]–[12]. However, past

published experimental work on multi-inverter anti-islanding has been limited to cases where all inverters are connected to the EPS at the same point of common coupling (PCC), sometimes called the "AC array" scenario, and has often focused on testing multiple inverters from the same manufacturer. Past testing has not covered the "solar subdivision" scenario of multiple inverters connected at multiple different PCCs on the same circuit, and it has been suggested that such cases may indeed increase island durations [13]. The lack of experimental testing of solar subdivision scenarios is partly due to the onerousness of creating multiple PCCs in a laboratory and adjusting the impedances between those PCCs to test a variety of conditions that may occur in the field. An additional difficulty arises in accounting for the real and reactive power in those interconnecting impedances when tuning the quality factor of the island circuit (a necessary step in conducting controlled islanding experiments, as described later in this report).

This report presents the results of a detailed series of laboratory experiments designed to quantify the effects of the two scenarios described above that make inverter-based anti-islanding more difficult, which are:

- Islands with inverters performing grid support functions (e.g. voltage and frequency event ride-through, Volt-VAr control, and frequency-Watt control)

- Multi-inverter island scenarios with inverters connected at multiple PCCs (the solar subdivision scenario).

This report examines the effects of both of the above conditions on island duration (ROT) using three commercially available, single-phase, residential-scale PV inverters from three different manufacturers. The experiments described here were completed in two phases:

1. The first phase of testing examined each inverter individually with GSF functions active. Each inverter was tested in a condition considered to be the most difficult single-DER island detection condition that may occur in the field: a load tuned to match the real and reactive power of the inverter and to resonate at 60 Hz with a unity quality factor. These tests were performed using varying combinations of GSFs and GSF parameters. Worst-case GSF settings were determined for each inverter based on the resulting island ROTs. The results of this first set of tests are summarized in [14] and are presented in Section 2 of this report.

2. The second phase of testing built on the first phase by testing all three inverters simultaneously while connected to different PCCs in the same circuit. Each inverter was set to one of the two worst-case GSF configurations determined in the first set of tests. These tests were repeated for a wide variety of interconnecting circuit topologies designed to represent the range of such topologies that would be observed in the field. These tests again used the matched resonant load condition. The details of the various multi-inverter tests run and their results are presented in Section 3.

The first phase of testing used a parallel resistive-inductive-capacitive (RLC) load bank, as is conventional for anti-islanding tests. The second set of tests took advantage of power hardware-in-the-loop (PHIL) simulation to emulate both the distribution circuit to which the inverters were connected and the resonant load itself. The PHIL tests are a hybrid of simulation and hardware

test in which some components of the test setup exist in hardware and others are implemented in a real-time simulation, as in [15], [16]. The impedances between the inverter PCCs are implemented in simulation to overcome the obstacle of creating multiple PCCs with easily adjustable interconnecting impedances. This also allows the quality factor of the island circuit to be computed continuously during testing while accounting for real and reactive power in all of the circuit elements. PHIL has previously been used for single-inverter anti-islanding tests [15], [17], but it is not known to previously have been employed for multi-inverter, multi-PCC island tests. An overview of the PHIL test method details is given in Section 3, and a detailed description of the PHIL method for multiple-inverter, multiple-PCC anti-islanding tests will appear in an upcoming publication [18].

The matched resonant load condition used in both phases of testing is described in the unintentional islanding test provided in IEEE Standard 1547.1-2005 [19]. This same test is referred to in UL 1741 [20], the standard test procedure used in the United States to verify the ability of DERs to appropriately interconnect with the EPS. It is worth noting that this unintentional islanding test was specifically designed through a broad, consensus-based process to create conditions believed by stakeholders to be the worst-case island detection condition a single DER would encounter in the field that is repeatable in a laboratory. This test, which is described in Section 2, uses an RLC load that is tuned so that its real and reactive powers are equal (or nearly equal) to those of the of the inverter under test, so that when the island is created, the current coming from the EPS is nearly zero. In addition, the circuit is tuned to resonate at 60 Hz with a quality factor of 1.0, such that the load itself tends to maintain its own voltage on sub-line cycle time scales. Previous studies suggest that such a well-tuned load condition has a low but non-negligible probability of occurring in the field [21]–[23]. These studies generally have considered only the probability of islands with matched real and reactive power, without considering the addition of a resonant load condition, which further increases the difficulty of island detection and further decreases the likelihood of such a condition occurring in the field. Thus, it is expected that the results presented here represent worst-case island durations for the scenarios tested. Other conditions that can further complicate island detection, such as islands with larger numbers of inverters or with combinations of inverters and machine-based generators, are not considered in this report.

2 Single-Inverter Anti-Islanding Testing

This section presents anti-islanding test results for three common single-phase PV inverters with various combinations of grid support functions enabled. These commercially available, residential-scale inverters came from three different vendors. The tests described here are based on the unintentional islanding test described in IEEE 1547.1 [19] and referenced in UL 1741 [20], the widely accepted inverter interconnection safety test standards in North America. The soon-to-be-published UL 1741 Supplement SA includes anti-islanding tests based on those in IEEE 1547.1, but calls for the test to be repeated with certain combinations of GSFs enabled. Specifically, Supplement SA calls for testing with voltage and frequency ride-through enabled, and separately with the worst-case combinations of GSFs (as specified by the inverter manufacturer) enabled. The test procedures used in this report are similar in that they include some tests with just ride-through enabled, but more thorough in that they investigate various combinations of additional GSFs, and different configurations of each GSF, rather than just those the manufacturer believes to be the worst-case condition. The authors are not necessarily suggesting that UL 1741 SA should take a similar approach; instead, the intent is to independently investigate a wider range of GSF configurations to shed light on their impacts on anti-islanding. The test procedures were also modified from standardized anti-islanding tests in other ways described below. Much of the information presented in this section is also available in [14].

Basic power ratings of three inverters tested are shown in Table 1. All inverters were configured for a nominal voltage of 240/120 V, split-phase.

Table 1. Inverters tested

Inverter	kW rating	Max kVAr, absorbing	Max kVAr, producing
1	5.0	3.3	3.3
2	6.0	3.6	3.6
3	4.2	2.0	2.0

2.1 Grid Support Functions

The four grid support functions whose impacts on anti-islanding were investigated are:

1. *Low- and high-voltage ride-through (VRT)*: The inverter must remain connected during certain defined excursions of voltage away from nominal.

2. *Low- and high-frequency ride-through (FRT)*: The inverter must remain connected during certain defined excursions of frequency away from nominal.

3. *Volt-VAr control (VVC)*: The inverter controls its reactive power output following a predefined curve based on the AC voltage at its terminals.

4. *Frequency-Watt control (FWC)*: The inverter controls its real power output following a predefined curve based on the AC frequency at its terminals.

For the three inverters tested, VRT and FRT are implemented by adjusting the voltage and frequency trip times and magnitudes. For tests with ride through disabled, voltage and frequency disconnection settings were programmed to the default values from IEEE 1547-2003. For tests with ride-through enabled, VRT and FRT parameters were selected from the default ride-through specifications for California Rule 21 listed in the draft version of UL 1741 Supplement SA because Rule 21 was the most well-developed set of advanced inverter requirements in North America at the time this work started (Summer 2015). Table 2 and Table 3 show the voltage trip time and magnitude requirements with ride-through disabled and enabled. Note that there is allowed adjustability to ride through limits; the values shown in Table 2 and Table 3 represent the settings used in this study. For each ride-through setting, the desired behavior is that the inverter trips when the voltage or frequency has exceeded the magnitude threshold for a time greater than the corresponding ride-through time threshold. Note that the times in Table 2 and Table 3 are actually trip times; the inverter rides through excursions until just before the time threshold (within 5%), then trips.

Table 2. Voltage ride-through settings for islanding detection tests

	VRT Disabled		VRT Enabled	
Trip Setting	Voltage (% of nominal)	Trip time (ms)	Voltage (% of nominal)	Trip time (ms)
High Overvoltage	120	160	120	160
Low Overvoltage	110	1000	110	13,000
Minor Undervoltage	88	2000	88	21,000
Medium Undervoltage	50	160	70	11,000
Major Undervoltage	-	-	50	1500

Table 3. Frequency ride-through settings for islanding detection tests

	FRT Disabled		FRT Enabled	
Trip Setting	Frequency (Hz)	Trip time (ms)	Frequency (Hz)	Trip time (ms)
High Overfrequency	-	-	62.0	160
Low Overfrequency	60.5	160	60.5	300,00
Minor Underfrequency	59.8	300,000	58.5	300,000
Major Underfrequency	57.0	160	57.0	160

Two different curves were programmed for VVC and FWC, one steep and one low-slope ("shallow"). Figure 1 shows the VVC and FWC curves used for the 6.0 kW inverter (Inverter 2).

For the other inverters, the same VVC and FWC slopes were maintained, though the maximum and minimum reactive power output varied between inverters depending on inverter's reactive power capability, given in Table 1. When programmed for the shallow VVC curve, the inverters operated between maximum positive reactive power and maximum negative reactive power for voltage changes between 88% and 110% of nominal; when programmed for the steep curve they inverters operated between the reactive power extremes for changes between 97% and 103% of nominal voltage. No dead band around nominal voltage was used in these tests to ensure that the Volt-VAr function was actively providing reactive power at all voltage ranges. Under the shallow FWC curve, the inverters produced full power up to 60.1 Hz and then linearly curtailed to zero power by 63.1 Hz (a curtailment slope of 33%/Hz); under the steep FWC curve, power was curtailed to zero by 61.1 Hz (100%/Hz).

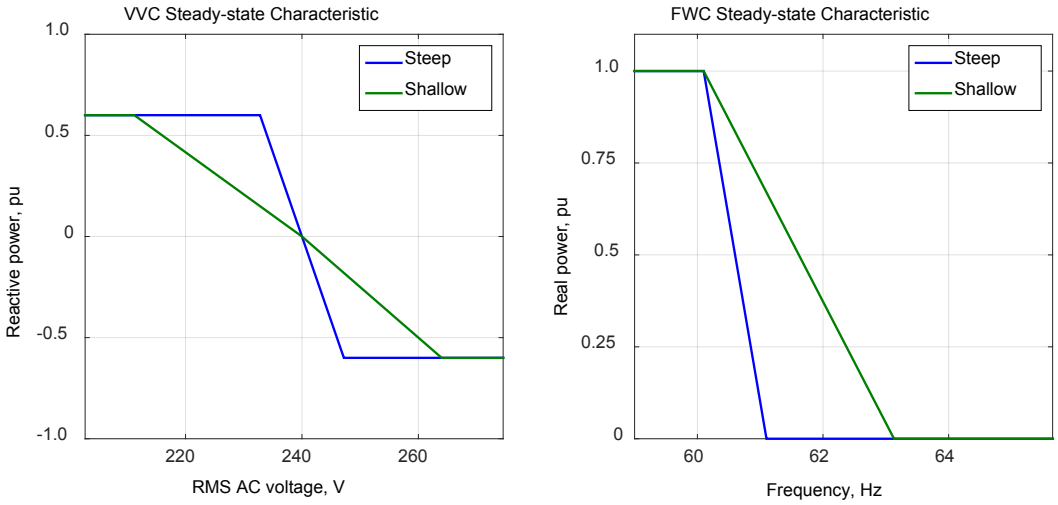

Figure 1. Volt-VAr control curves (left) and frequency-Watt control curves (right).

All inverters were tested for anti-islanding with all four grid support functions disabled to establish a baseline, and then ride-through settings were enabled. FWC and VVC were either disabled, set to the shallow slope, or set to the steep slope; each combination of these settings was tested, creating a total of 10 test cases, as shown in Table 4. Each test was repeated using four different load tunings and a fifth time to repeat the worst case of the previous four tests, following the test procedure outlined in the next subsection. Hence a total of 50 tests were run per inverter.

Table 4. Grid support function test cases

Test Case	Inverter Function Settings			
	VRT	FRT	FWC	VVC
1	OFF	OFF	OFF	OFF
2	ON	ON	OFF	OFF
3	ON	ON	OFF	SHALLOW
4	ON	ON	OFF	STEEP
5	ON	ON	SHALLOW	OFF
6	ON	ON	SHALLOW	SHALLOW
7	ON	ON	SHALLOW	STEEP
8	ON	ON	STEEP	OFF
9	ON	ON	STEEP	SHALLOW
10	ON	ON	STEEP	STEEP

Before initiating anti-islanding tests, initial tests were run to verify the correct operation of each GSF for each inverter. Note that each inverter had a 240:120/240 isolation transformer at its output to derive a split-phase connection from an individual line-neutral grid simulator output phase.

Test results for Inverter 1 were produced using updated firmware that accounted for impacts of FRT on islanding detection; tests also verified that this firmware was capable of riding through fast frequency changes, up to 1 Hz per second.

2.2 Anti-Islanding Test Procedure

The unintentional islanding test followed the procedures described in IEEE 1547.1, Section 5.7, with some modifications discussed in this section. The equipment under test (EUT) was connected to a parallel RLC tank circuit and simulated EPS, as seen in Figure 2. The circuit was tuned to minimize the real and reactive 60 Hz component of the exported EPS current when the inverter operated at full rated power. The quality factor of the load circuit was tuned to be near unity, defined as

$$Quality\ Factor = \frac{\sqrt{Q_L \times Q_C}}{P_R},$$

where P_R, Q_L, and Q_C are the resistive, inductive and capacitive powers of the load, respectively. As mentioned above, the intent of this purposefully-tuned resonant circuit is to create a loading scenario that is challenging for islanding detection.

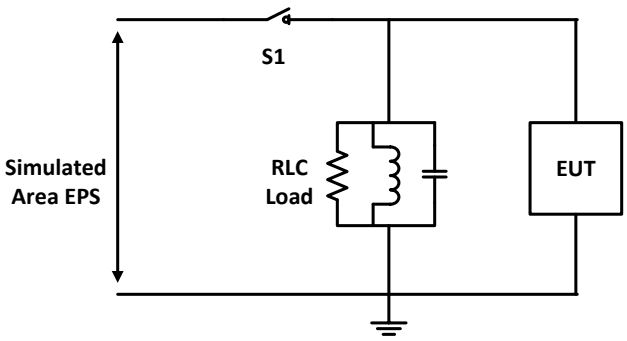

Figure 2. Unintentional islanding test circuit with resonant RLC load.

For each inverter and each combination of grid support functions (described above), four unintentional islanding tests were conducted with varying load tunings, and the test with the longest ROT was repeated once. This varies from IEEE 1547-2003, which calls for eleven variations of load tuning. This allowed for greater coverage of other test parameters (GSF settings) within the project budget and schedule

The simulated EPS was realized using an Ametek MX-45 programmable AC power supply, and the load was a Simplex Trident RLC load bank with 75 VAr resolution on reactive power and 100 W resolution on real power at its rated voltage of 277 V line-neutral. For these tests, a single phase of the load bank was used, connected line-neutral. The Ametek MX-45 was commanded to open its output contactor in order to create the island situation.

Once the inverter under test was operating at full power, the RLC circuit was tuned to create a balanced island. The balance of island condition was determined by viewing the waveform of the current flowing through switch S1 and tuning the load to minimize the 60 Hz component of that current while also ensuring a load quality factor of 1.0 within 2% accuracy or better, most often within 1% accuracy. Once the load was tuned, switch S1 was opened to create the island and the inverter voltage and current waveforms were recorded using a Yokogawa DL750 power analyzer.

Figure 3 shows a sample test waveform plot demonstrating how ROT was measured. As in all waveforms shown in this paper, measured currents are shown magnified five times for better visibility. It took the simulated EPS about 2.5 AC line cycles to create the island by opening its output contactor (switch S1) after the island command was issued (*Aux* signal). The time of island formation was determined by the disappearance of harmonic current output from the grid simulator (I_{grid}, red trace). The time when the inverter ceased to produce current was determined by directly measuring that current (I_{inv}, green trace). The ROT is the time between when the grid simulator current goes to zero and when the inverter current goes to zero. Note that the load continues to resonate for about one line cycle following the trip of the inverter, so the system voltage (V_{inv}) drops to zero about one line cycle after the inverter current does, as expected for a circuit with a quality factor of unity.

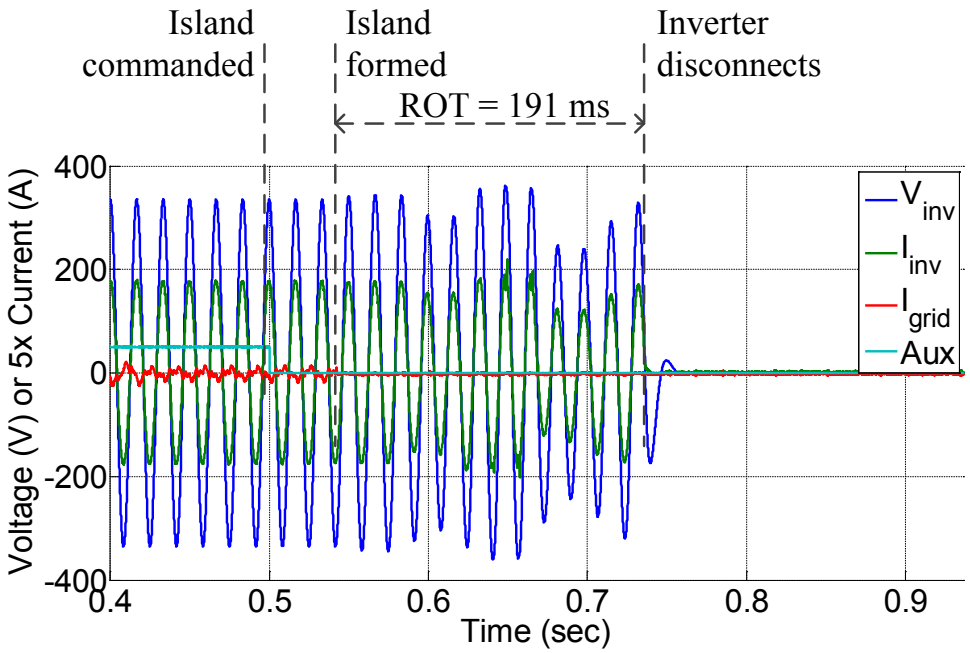

Figure 3. Representative graph depicting run-on time measurement method for a typical unintentional islanding test.

2.3 Single-Inverter Anti-Islanding Test Results

Table 5 summarizes all 150 single-inverter anti-islanding tests by presenting the maximum and mean ROTs for each inverter for each test case in Table 4. Figure 4 presents the data graphically in a whisker plot that includes the maximum, mean, and minimum ROT for each test case. As seen in the data, the maximum ROTs in any test for Inverters 1-3 were 502 ms, 668 ms, and 711 ms, respectively; all ROTs were well below the two second limit required by IEEE 1547-2003. A table of all single-inverter test results can be found in the Appendix.

Table 5. Mean and maximum run-on times for each inverter with each grid support function combination

Test Case	Inverter 1		Inverter 2		Inverter 3	
	Mean (ms)	Maximum (ms)	Mean (ms)	Maximum (ms)	Mean (ms)	Maximum (ms)
1	133	160	167[a]	301[a]	147	312
2	221	421	220	319	205	286
3	139	183	194	410	438	711
4	177	502	200	282	121	134
5	111	161	206[a]	285[a]	326	394
6	211	460	311[a]	399[a]	202	423
7	169	476	201[a]	364[a]	397	615
8	98	138	284[a]	427[a]	179	230
9	149	432	291	668	382	669
10	218	406	188[a]	383[a]	221	291

[a] Based on six tests rather than five; these tests were run first before completely standardizing the number of tests.

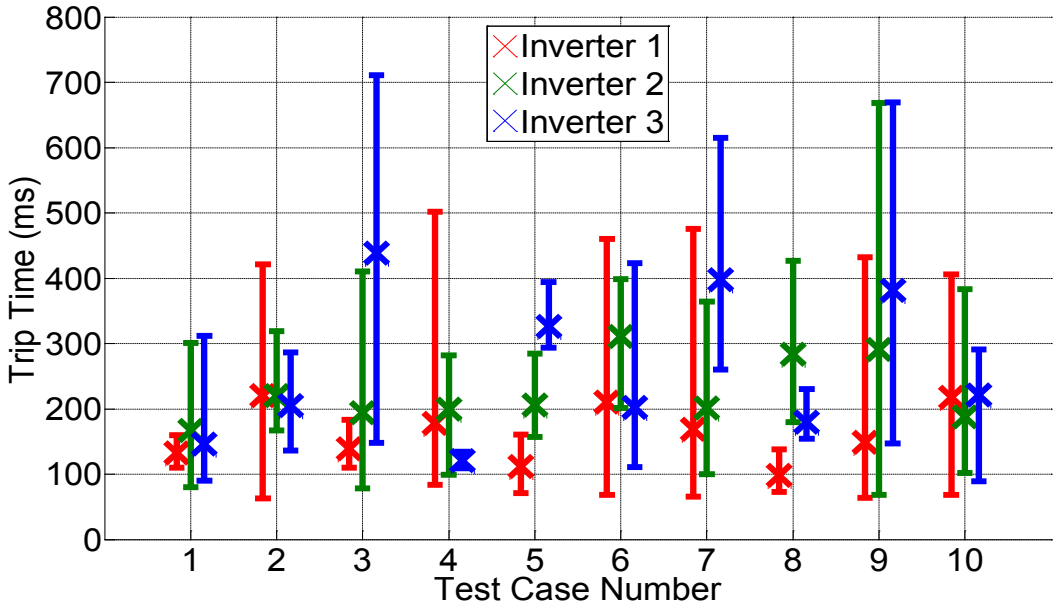

Figure 4. Maximum, mean, and minimum run-on time for each inverter under each test case.

As seen in Figure 4, the baseline case with no grid support functions enabled (Case 1) had among the lowest ROTs, but was not significantly lower than many other test cases. The largest mean and maximum ROTs occurred with Inverter 3 under Case 3. There was no obvious pattern of change in ROT for a given GSF, and most often the variation in ROT within a given test case was greater than the variations between test cases. Regression analysis presented in the next subsection will expand on these qualitative conclusions.

Table 6 and Table 7 summarize the maximum and mean ROT across all tests for each individual grid support function, broken down by inverter. Enabling ride-through functions more than doubled the maximum ROTs and also increased the mean ROTs for all inverters. Enabling FWC only increased the maximum ROT for one of the three inverters. Enabling VVC increased the maximum ROT for all three inverters, but not by particularly large margins. There was no clear effect on the mean ROT with either FWC or VVC enabled. Hence these results support the conclusion that ride-through functions increase maximum island ROTs, but they did not find particularly strong evidence that adding FWC or VVC further increases ROTs. The next subsection applies statistical analysis to quantify these conclusions.

Table 6. Maximum run-on times for each inverter for each individual grid support function

	Ride-through		FWC		VVC	
Inverter	ON	OFF	ON	OFF	ON	OFF
1	502	160	476	502	502	421
2	668	301	668	410	668	427
3	711	312	669	711	711	394

Table 7. Mean run-on times for each inverter for each individual grid support function

	Ride-through		FWC		VVC	
Inverter	ON	OFF	ON	OFF	ON	OFF
1	166	133	159	168	177	220
2	233	167	246	194	231	219
3	275	147	285	228	294	306

2.4 Regression analysis

In an attempt to better quantify the effect of each GSF on island ROT, linear regression was performed on the set of tests for each inverter. The predictor variables considered for the regression analysis were ride-through status, FWC curve status, and VVC curve status. Because VRT and FRT were either both enabled or both disabled, they were considered a single binary predictor variable, denoted *VFRT*, where *VFRT*=0 indicates both ride-through functions were disabled and *VFRT*=1 indicates both ride-through functions were enabled. FWC and VVC were both considered categorical (i.e. non-numerical) variables with three possible states: On, Steep, and Shallow.

For each of the three inverters, regression analysis using linear terms in all three predictor variables plus a constant term resulted in models with p-values of at least 0.16. This indicates that either the models are not valid or more data is needed to draw a conclusion.

Linear regression analysis of the data on Inverter 1 using a model with just the predictor *VFRT* and a constant term resulted in the model $ROT = 133 + 33 \cdot VFRT + \varepsilon$ [ms], with an RMS error of 129 ms. Here ε represents the error in the ROT prediction due to unmodeled effects and stochasticity. This model would indicate that enabling VRT and FRT for Inverter 1 tended to increase ROT by 33 ms, and that the non-modeled variation in ROT (as captured in the RMS

error) is much larger than that accounted for by voltage and frequency ride-through. However, the model p-value was 0.58, which is much too high to draw a conclusion; more data would be needed to draw a conclusion.

Similar regression analysis was performed on the data for Inverter 2. The model with just *VFRT* and a constant term resulted in the model $ROT = 167 + 67 \cdot VFRT + \varepsilon$ [ms] with RMS error of 115 ms and p-value of 0.19. This p-value is still too high to draw conclusions, but it does begin to suggest that for this inverter, ride-through functions tend to increase ROT. As with Inverter 1, this model would also indicate that non-modeled effects account for more variation than modeled effects.

The data for Inverter 3 was analyzed in the same fashion. The model with *VFRT* and the constant term resulted in the equation $ROT = 147 + 128 \cdot VFRT + \varepsilon$ [ms] with an RMS error of 156 ms and a p-value of 0.089. Thus for Inverter 3, the data strongly suggest that VRT and FRT increase island ROT, though more data would be needed to make that conclusion with a high degree of confidence. And as with the other two inverters, the RMS error was larger than the variation accounted for in the regression model.

Thus, when analyzing each of the three inverters independently, regression analysis tended to indicate (with varying degrees of confidence) that having ride-through enabled increases island ROT, but the evidence was not strong enough to state that with confidence for all inverters. However, by combining the data from all three inverters into a single dataset and adding inverter number as a fourth categorical predictor variable, a new ROT-predictive model shown in Equation (1) was developed with p-value of 0.0005, indicating strong confidence that the model accurately captures the true physical system.

$$\boldsymbol{ROT = 95 + 75 \cdot VFRT + 64 \cdot Inv2 + 99 \cdot Inv3} + \varepsilon \text{ [ms]} \qquad (1)$$

Here *Inv2* and *Inv3* are binary variables indicating that the test inverter is Inverter 2 and Inverter 3, respectively. If both *Inv2* and *Inv3* are equal to zero, the test inverter is Inverter 1. Thus this model indicates that when considering data from all three inverters, enabling VRT and FRT tended to increase ROT by 75 ms after accounting for variation between inverters. It also indicates that Inverters 2 and 3 tended to take 64 and 99 ms longer than Inverter 1 to trip following an island, respectively. The RMS error of the model given in Equation (1) was 133 ms, which is larger than any of the terms in the model, indicating that unmodeled effects account for more test-to-test variation than modeled effects.

A second regression model of the data from all three inverters using all four predictors (inverter number, *VFRT*, VVC status, and FWC status) resulted in a model with high p-values associated with several terms. Hence no quantitative conclusions regarding the effects of VVC and FWC were drawn from the statistical analysis.

It is important to note that when considering unintentional islanding, the mean ROT is not as important as the *maximum* ROT since a single islanding event over a threshold is potentially consequential. Thus it would also be of interest to analyze the maximum ROTs for each test case. However, only 30 data points are available when looking at maximum ROTs, so no statistically significant conclusions can be drawn. Nevertheless, it is visually apparent in Figure 4 that

maximum and mean ROT are correlated, so it is expected that an analysis of maximum ROTs on a larger data set would find qualitatively similar results.

2.5 Test waveforms

Typical anti-islanding test voltage and current waveforms for Inverter 1 are shown in Figure 5 (top). Recall that all current waveforms in this report are magnified five times for visibility. Note that some small 60 Hz component of the grid current is visible before the island is created. This is because this inverter modifies the phase angle of its output current periodically (with a period on the order of four seconds), such that the load tuning always leaves some fundamental current flowing to or from the AC supply at certain parts of the inverter output phase angle cycle.

For all tests of this inverter, there was no noticeable distortion in the voltage or current waveforms prior to ceasing to energize. There was no distinctive difference in output waveforms for different GSF settings. Figure 5 (bottom) shows the waveforms for the worst-case ROT of 502 ms for this inverter, which occurred during Test Case 4 (ride-through enabled, FWC disabled, VVC steep).

Some concerns have been raised that inverters may produce transient overvoltage conditions during islanding events. It is expected that in these balanced-island tests, no load rejection overvoltage should result [24], [25]. Test waveforms were examined for overvoltage conditions exceeding 110% of nominal, and none were found, confirming the expectations.

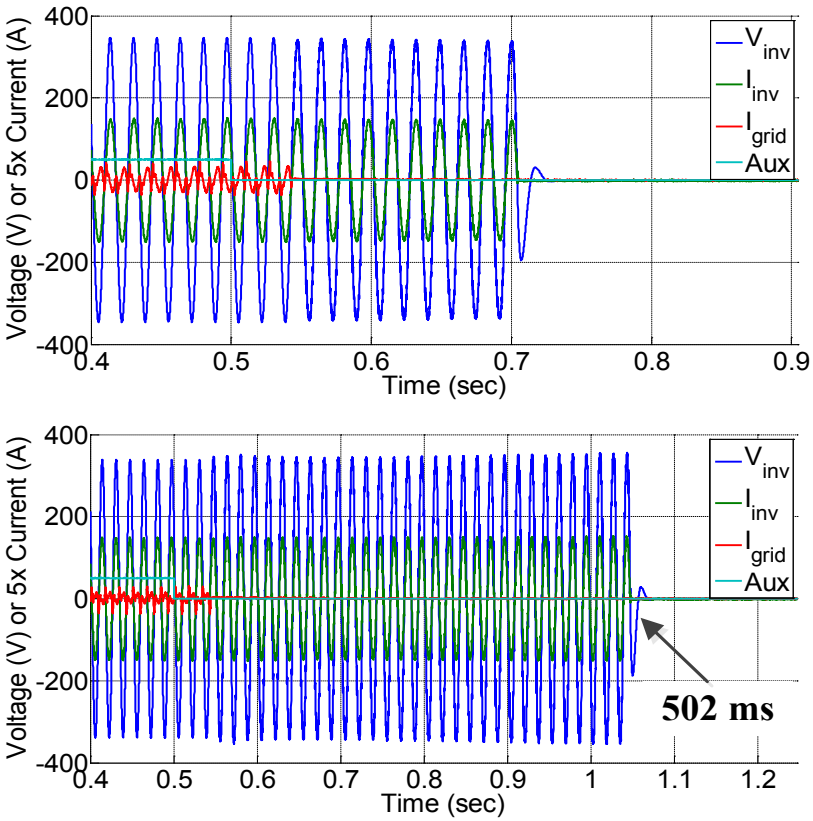

Figure 5. Typical (top) and worst case (bottom) islanding test waveforms for Inverter 1.

Typical test waveforms for Inverter 2 are shown in Figure 6 (top), as well as the worst-case test result (bottom). The longest ROT was 668 ms and occurred during Case 9 (ride-through enabled, FWC steep, VVC shallow). As seen in these figures, the voltage and current waveforms were sinusoidal with no added distortion, but had fluctuating amplitudes in many test cases including those shown in Figure 6. No significant transient overvoltages were observed, and there was no pattern in output waveform dependent on grid support function settings. This inverter did not produce any voltages above 110% of nominal during these tests.

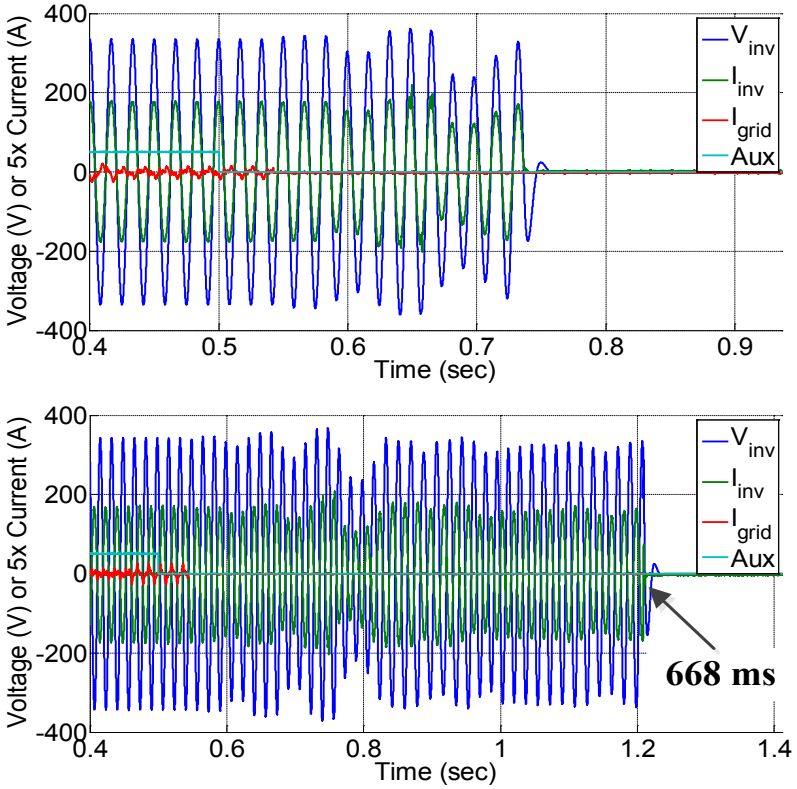

Figure 6. Typical (top) and worst case (bottom) islanding test waveforms for Inverter 2.

A typical test waveform for Inverter 3 is shown in Figure 7 (top). The characteristic output waveform was very repeatable for all tests of this inverter: nominal voltage and current were maintained following island creation for some time before a two-to-three AC cycle decay in amplitude prior to de-energization. The island duration did vary however, as is clear from Figure 4. There was no distinctive difference in output waveforms for different GSF settings. Figure 7 (bottom) shows the worst case ROT of 711 ms for this inverter, which occurred during Case 4 (ride-through enabled, FWC disabled, VVC steep). As with the other two inverters, this inverter did not produce any voltages above 110% of nominal during island tests.

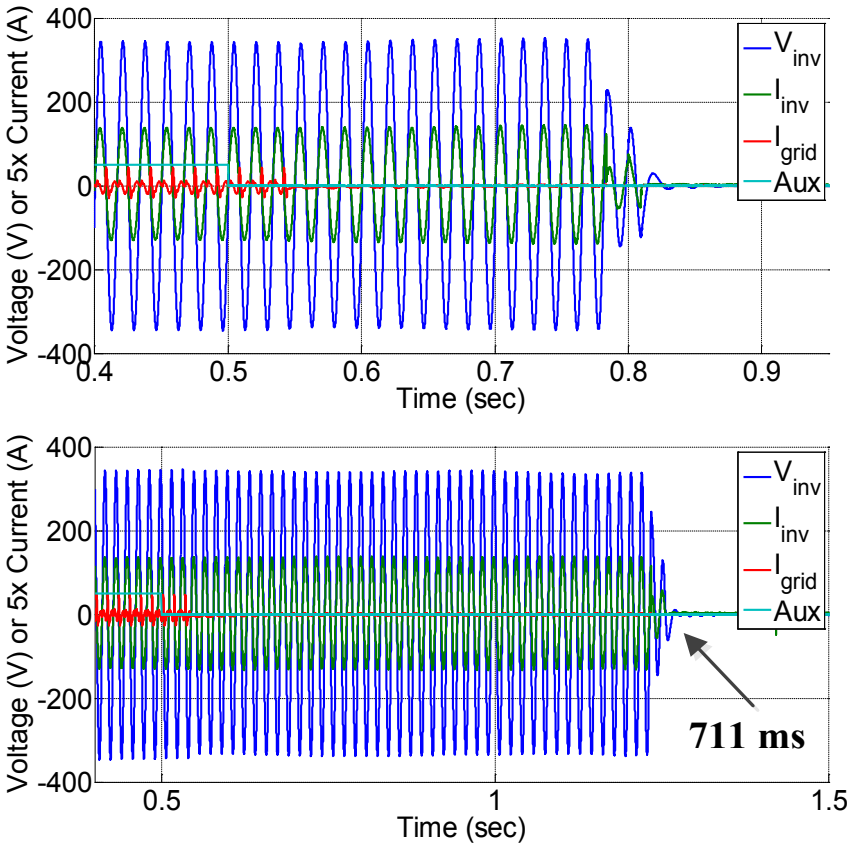

Figure 7. Typical (top) and worst case (bottom) islanding test waveforms for Inverter 3.

2.6 Selection of Worst-Case Grid Support Configurations

A second goal of the single-inverter tests (in addition to verifying that the inverters could pass anti-islanding tests with GSFs enabled) was to identify worst-case GSF configurations for further testing in multiple-inverter, multiple-PCC scenarios. At least two possible criteria for selecting worst-case settings exist: One would be to select the GSF configuration that led to the longest mean ROT. The second would be to select the configuration that led to the test with the single longest ROT. The latter criterion was given priority because the potential consequences of a rare but prolonged island event would be greater than those of frequency shorter events, and because in certification testing the pass/fail criterion is based on the maximum ROT, such that a single failure of an unintentional islanding test results in a complete failure of the test series, whereas an average island duration that is high but not above two seconds is not penalized [19]. The worst-case GSF configuration for each of the three inverters based on the criterion of maximum measured ROT is shown in Table 8.

Table 8. Worst-case Grid Support Functions from Single-Inverter Tests

Inverter	Voltage ride-through	Frequency ride-through	Frequency-Watt	Volt-VAr
1	ON	ON	OFF	HIGH
2	ON	ON	HIGH	LOW
3	ON	ON	OFF	LOW

A second-worst-case GSF configuration was also selected for each inverter, shown in Table 9. This configuration was used in some multi-inverter tests as well, as described below. The GSF configuration that gave the longest *average* ROT was selected as the second-worst-case because in multi-inverter cases a GSF configuration that tends to run on longer on average may allow more opportunity for other inverters in the island to operate undisturbed.

Table 9. Second-worst-case Grid Support Functions from Single-Inverter Tests

Inverter	Voltage ride-through	Frequency ride-through	Frequency-Watt	Volt-VAr
1	ON	ON	OFF	OFF
2	ON	ON	LOW	LOW
3	ON	ON	HIGH	LOW

The one common feature of all six worst- and second-worst-case GSF configurations for the three inverters is that both voltage and frequency ride-through were enabled in all cases. This experimental result confirms the expectation that the requirement to ride-through voltage and frequency disturbances makes island detection more difficult, at least for these three inverters. Nevertheless, all three inverters passed all single-inverter tests within a comfortable margin.

3 Multiple-Inverter Anti-Islanding Testing

The multiple-inverter anti-islanding tests utilized the worst-case GSF configurations for each inverter that were determined in Section 2. Each of the three inverters was connected to a different PCC on the same single-phase section of a simulated distribution circuit.

3.1 Multi-Inverter Test Scenario Overview

This subsection provides an overview of the multi-inverter anti-islanding tests. Further test details are presented in subsequent sections.

The multiple-inverter tests considered variations in circuit topology, load location, interconnecting impedances, and inverter locations. Considering all possible combinations of these variables would have resulted in an intractable number of tests, so a four-step plan was created in which each step considered a subset of the possible test parameters. The purpose of the first three steps was to select sets of worst-case parameters for more detailed testing in Step 4. The four steps are summarized in Table 10 and described below.

Table 10. Multi-Inverter Test Steps

Step	Parameters Varied	Number of Tests	Number of Worst-Case Conditions Selected
1	Circuit topology and impedances	50	3
2	Load location relative to inverters	15	1
3	Short-circuit impedance of grid at island breaker	15	1
4	Inverter locations and GSF settings	144	NA

The first three steps were formulated to use a relatively smaller number of tests to select worst-case conditions of the parameter under test. Each of the first three steps identified one or more worst-case conditions for its parameters under test to be used in subsequent steps. Step 1 was completed first to find the single worst-case condition of circuit topology and impedance. The worst-case circuit from Step 1 was used in in Steps 2 and 3. In Step 2, a single worst-case load location was selected for use in Steps 3 and 4. And in Step 3, one worst-case grid impedance was selected for use in Step 4.

After Steps 1-3 were complete, to preserve some variation in circuit topology and impedance, *three* worst-case conditions were selected from Step 1 for more detailed testing in Step 4.

Each of Steps 1-3 used the worst-case GSF settings from the single inverter tests. Step 4 used both of the two worst-case GSF settings.

Step 1 simultaneously varied circuit topology and impedances, rather than being divided into two steps with one step varying topology and the other varying impedance, because the circuit topology and typical circuit impedances are inherently linked. The chosen combinations of

topology and impedance were intended to represent a range of typical configurations seen in real distribution feeders.

Each unique set of test parameters in Steps 1-3 was tested four times with varying load tunings to increase the chances of finding a load tuning that leads to a longer ROT. Each load tuning adjusts real power or reactive power of one or more load elements by 1%-3%. After the first four repetitions of each test, the load tuning that produced the longest ROT was repeated once, for a total of five repetitions of each set of parameters. Thus the 50 tests in Step 1 were comprised of five repetitions of ten different test cases (described below). Likewise, the 15 tests in each of Steps 2 and 3 were comprised of five repetitions of three different cases.

Step 4 was designed to conduct a more detailed investigation of island ROTs for the combined worst-case conditions observed in Steps 1-3, as well as the worst-case GSF settings for each of the three inverters identified in the single-inverter tests. During Step 4, all combinations of the following variables were tested:

- The *two* worst-case inverter settings from the single-inverter tests
- The *three* worst-case combinations of topology and impedances from Step 1
- The single worst case load location from Step 2
- The single worst-case grid impedance from Step 3
- All *six* permutations (3!) of inverter locations on the three PCCs in each test circuit.

More details on each of these items are provided in the next two sections.

During Step 4, each unique set of test parameters was repeated three times with varying load tunings (i.e. one or more load powers adjusted by 1%-3%). The load tuning that produced the longest ROT was repeated once more, for a total of four repetitions at each setting and an overall total of 144 tests. (The number of repetitions under Step 4 was one less than under Steps 1-3 due to time and budget constraints, not for any technical reason.)

3.2 Circuit Topologies

Various single-phase topologies were considered, and typical impedances were estimated for each circuit element as described below. The circuit topologies used for multi-inverter tests were selected to represent the range of circuit topologies that are found in the field. Because all three inverters tested are single-phase inverters, and inverters on different phases would be unlikely to impact each other's anti-islanding performance, all topologies used were single-phase.

The circuit elements that were considered as island test parameters were those that lie on paths connecting inverters or connecting the inverters to the island load. Additionally, the short-circuit impedance of the grid at the island breaker was modeled because as it may impact some island detection methods. Considering the location of the three inverters relative to low voltage distribution transformers, there are three possibilities, shown in Figure 8:

1. All three inverters at different PCCs on the same transformer
2. Three inverters on three different transformers, connected by medium voltage lines
3. Two inverters on one transformer and one inverter on a second transformer connected to the first by a medium voltage line.

Figure 8 shows loads at the location of each inverter. As noted above and described further in the next section, tests were also run with the load centralized at other locations in the island.

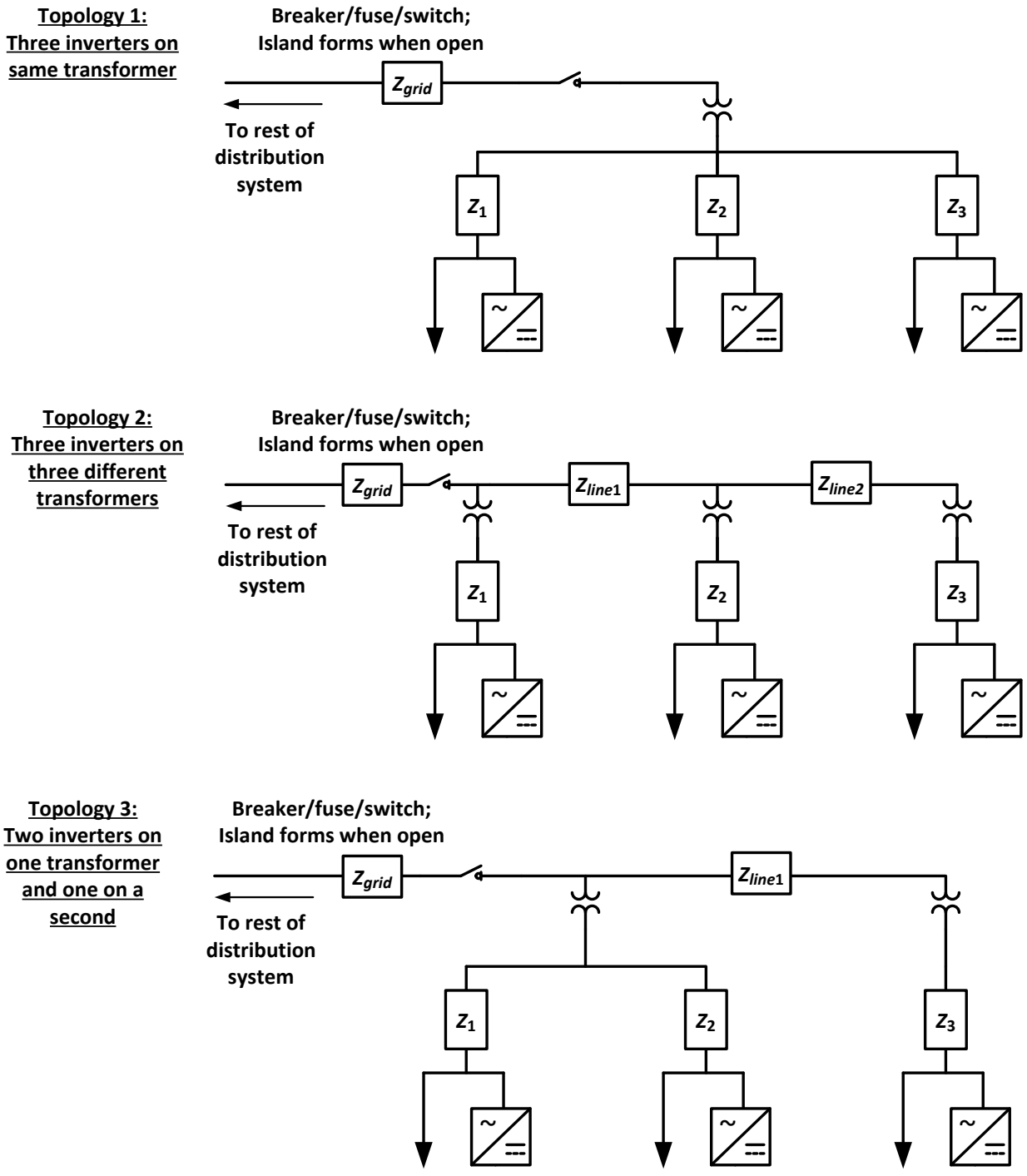

Figure 8. The three basic island circuit topologies considered

For lines on the secondary side of distribution transformers, both underground and overhead lines were considered. Additionally, three different line lengths were considered: 100 feet, 200 feet, and 300 feet. In cases where inverters were on the same transformer, it was assumed either that all secondary lines coming from that transformer were overhead, or all were underground. In

cases of inverters on different transformers, the tested cases covered combinations of overhead and underground lines. Table 11 summarizes the ten island circuit topologies tested in Step 1.

Table 11. Island circuit topologies

Test Case	Description	# of Transformers	# of Overhead Lines	# of Underground Lines
1	Three inverters on one transformer connected via underground lines	1	0	3
2	Three inverters on one transformer connected via overhead lines	1	3	0
3	Three inverters on three different transformers, connected via underground lines	3	0	3
4	Three inverters on three different transformers, connected via overhead lines	3	3	0
5	Two inverters connected to two different transformers via underground lines and one inverter connected to a third transformer via overhead lines	3	1	2
6	Two inverters connected to two different transformers via overhead lines and one inverter connected to a third transformer via underground lines	3	2	1
7	Three inverters connected to two different transformers via underground lines	2	0	3
8	Three inverters connected to two different transformers via overhead lines	2	3	0
9	Two inverters connected to one transformer via underground lines and one inverter connected to a second transformer via overhead lines	2	1	2
10	Two inverters connected to one transformer via overhead lines and one inverter connected to a second transformer via underground lines	2	2	1

Overhead secondary triplex lines were taken to consist of one 4/0 AWG aluminum conductor for each line of the split-phase connection, with a one-way impedance of 0.059 + j0.026 Ω/kft [26], [27]. Underground secondaries were taken to consist of two direct-buried 4/0 AWG aluminum conductors with a one-way impedance of 0.093 + j0.028 Ω/kft [28].

Distribution transformer impedances were taken to be those of a typical 50 kVA, 7200:240/120 V, oil-filled transformer with an impedance of 1.5% and a reactance:resistance (X/R) ratio of 2.0 [29], as would often be found on a 12.47 kV system. Medium voltage lines were represented by a one-mile segment of a 7.2 kV overhead line with an impedance of 0.08∠60° Ω/mile [30], again typical for a 12.47 kV system. The estimated impedances of the various elements that make up the three basic circuits in Figure 8 are shown in Table 12. The six 240 V line segments in Table 12 were used as half of Z_1, Z_2, and Z_3 in Figure 8 in various combinations, and the 7200 V line segment was used as Z_{line1} and Z_{line2}. All of the per-unit line segment impedances in Table 12 are on a 100 MVA base, but the transformer impedance is on the transformer's 50 kVA base.

Table 12. Interconnecting Circuit Element Impedances

Impedance	R (Ω)	X (Ω)	R (pu)	X (pu)
100' 240 V overhead line	0.0059	0.0026	10	4.5
200' 240 V overhead line	0.012	0.0052	21	9.0
300' 240 V overhead line	0.018	0.0078	31	14
100' 240 V underground line	0.0093	0.0028	16	4.8
200' 240 V underground line	0.019	0.0055	32	9.6
300' 240 V underground line	0.028	0.0083	48	14
50 kVA 7200:240 V transformer	0.0077	0.015	0.0067	0.013
1 mile 7200 V line segment	0.040	0.069	0.049	0.084

Because some inverters use anti-islanding methods that rely at least partially on changes in grid impedance to detect islands, the impedance from the grid source to the breaker that created the island (Z_{grid} in Figure 8) was also varied across a range of values (Step 3). The values used were the minimum, median, and maximum short-circuit impedances at all distribution transformer primary nodes of the IEEE 8500-node test feeder [31], shown in Table 13. The per-unit values in Table 13 are again on a 100 MVA base.

Table 13. Grid Impedances

Impedance	R (Ω)	X (Ω)	R (pu)	X (pu)
Minimum	0.00195	0.00334	0.0013	0.0022
Median	0.0198	0.0249	0.013	0.016
Maximum	0.0747	0.105	0.048	0.067

Various combinations of the impedances listed in Table 12 and Table 13 were used to form the test circuits described in Section 3.3.

Note that it is not claimed that the circuit topologies and impedances tested cover the entire range of possible real-world circuits. Testing all such circuits would be prohibitively costly and time-consuming, if not impossible. Instead, the goal is to test a range of plausible topologies and impedances to investigate the effects of varying topologies and impedances on island duration.

3.3 PHIL Test Setup

The PHIL test setup used for the multi-inverter tests is shown in Figure 9. It consists of a computer model running in real-time coupled to a hardware test setup. The model runs on a 30 microsecond discrete time step on an Opal-RT target computer, so there are 555.6 discrete time steps in each 60 Hz AC line cycle. At each time step, the model receives measured inverter currents from the hardware setup and sends computed voltages to the three voltage amplifiers. The three voltage amplifiers are comprised of a single three-phase Ametek MX-45 voltage source with each line-neutral voltage controlled independently. The net effect of this real-time

simulation with hardware inverters in the simulation loop is a hybrid simulation-experiment allowing the inverters to be tested in an environment that closely mimics that of the simulated circuit. At the same time, the simulated circuit reacts as if the hardware inverters were part of the simulation. There are of course limitations and non-idealities in such a setup, including processing delays and discretization effects, so the potential for artifacts or instability in the closed-loop system must be addressed [32]. PHIL systems similar to the one used here have been successfully used in the past to test anti-islanding scenarios [15], [17]; inverters with advanced grid support functions [16]; and scenarios involving multi-inverter dynamics on simulated distribution systems [33], [34]. This report describes the first known use of PHIL to test multi-inverter island scenarios.

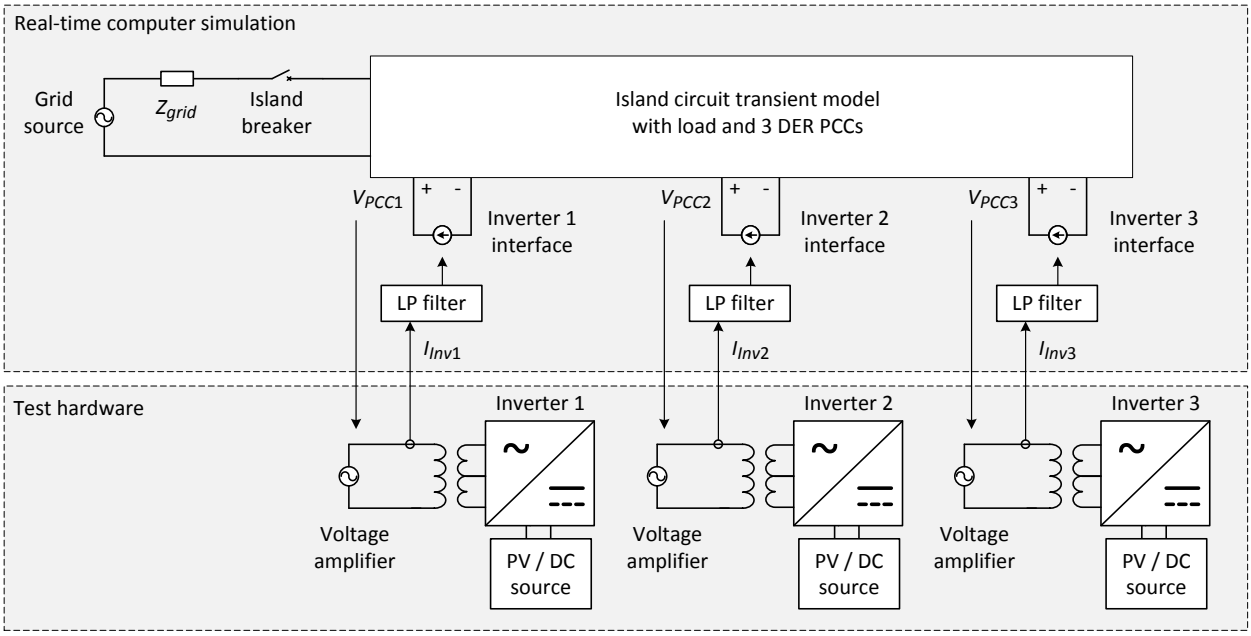

Figure 9. Multi-inverter anti-islanding PHIL test setup overview

Each of the three inverters was connected via a 10 kVA 240:240/120 split-phase transformer to a voltage amplifier. The purpose of the transformers was to derive neutral connections for the inverters with each inverter connected to one phase of a three-phase voltage amplifier. Each measured inverter current after the transformer was fed into the PHIL real-time computer model. In the model, the currents were filtered through a single-pole low-pass filter with a 1.2 kHz cutoff frequency. The purpose of the low pass filter is to attenuate higher frequency components including measurement noise, and to stabilize the closed-loop PHIL system. For more information on the stabilization of PHIL models, see [35]–[37]. The filtered inverter currents each were used to drive a current source, thus reproducing the output of the three PV inverters inside the model.

For each test, the generalized island circuit model shown in Figure 9 was populated with a transient Simulink/SimPowerSystems model (adapted for real-time operation using RT-LAB) representing one of the three circuit topologies shown in Figure 8. The RLC load was also

implemented inside the SimPowerSystems model. In Step 1, the load was concentrated near the island circuit breaker. In Step 2, three load locations were examined:

1. Load distributed across the three inverter locations, with one RLC load modeled at each inverter PCC

2. Load concentrated near the island breaker

3. Load concentrated far from the island breaker.

Figure 10 shows an example of an island circuit transient model including the resonant RLC load. This example shows circuit topology 3 (three inverters connected to three different transformers via underground lines) with the load concentrated near the island breaker. Circuit topology 4 also follows this circuit diagram, but with overhead lines. The transient models for the remaining scenarios were modified from that shown in Figure 10 to reflect the appropriate circuit topology and load location. For the case of a load concentrated far from the island breaker, the load was placed across the primary of the farthest transformer from the island breaker. For the case of a distributed load, smaller loads were placed at the PCCs of all three inverters.

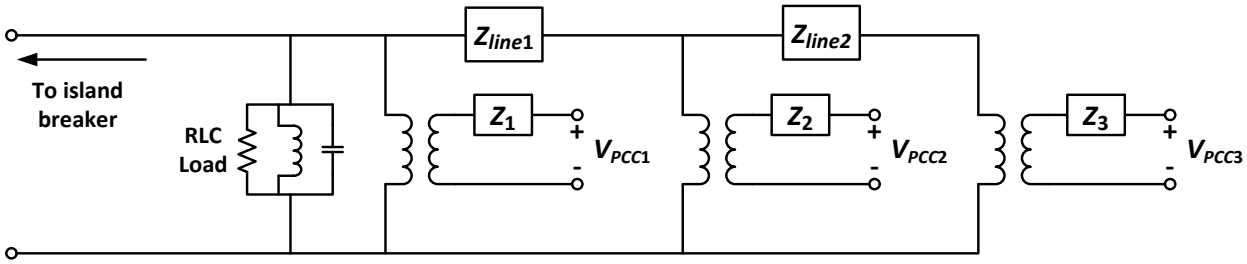

Figure 10. Example island circuit transient model. This model is for the case where each inverter is on a different transformer and the load is located near the island breaker.

This circuit diagram was modified as necessary to create the remaining combinations of load location with circuit topology and impedance.

Physical currents and voltages on both sides of the transformer were recorded during each test. In addition, currents in each modeled circuit element and voltages at each modeled node were recorded. Modeled and simulated voltages and currents were used to calculate the circuit quality factor during each test. Effects of transformer shunt impedances (equivalent core resistance and magnetizing inductance) were neglected in the quality factor calculations because simulations showed that the impacts of estimated shunt impedances on total circuit quality factor was negligible [18]. Series impedances for both modeled and hardware transformers were accounted for in the quality factor calculation [18].

A series of anti-islanding tests were run to validate the PHIL model described above by comparing PHIL anti-islanding test results and waveforms to those of similar pure-hardware anti-islanding tests. Those tests, to be presented in [18], found that island ROTs fell in the same range for both the PHIL tests and the hardware-only tests, and that observed voltage and current

waveforms were qualitatively similar between the two kinds of tests. The variation between pure hardware tests and PHIL tests was no greater than the variation *among* pure hardware tests. Thus the PHIL apparatus presented above does not introduce artifacts or errors that would impact the validity of the test results presented below. This is consistent with the work presented in references [15] and [17], which used a very similar test setup and were also able to validate PHIL anti-islanding test results against conventional hardware anti-islanding tests.

In contrast to conventional IEEE 1547.1 unintentional islanding tests, these tests include segments of distribution circuits. The elements of those circuits (lines and transformers) have their own significant real and reactive power impacts. The tuning of the RLC load must take all elements into account. This is best achieved by monitoring the real and reactive power flowing through the island breaker and bringing it as close to zero as possible by tuning the load. An overall circuit quality factor very near to 1.0 should also be maintained while tuning the load. In the real-time PHIL model used here, the test engineer was able to observe continuously-updated plots of the measured fundamental-frequency real and reactive power flowing through the modeled island breaker as well as a continuously updated display of the total circuit quality factor. Examples plots of real and reactive power flowing through the island breaker are shown in Figure 25 and Figure 27 in Section 3.4.5. Both the quality factor calculation and the real and reactive power calculations accounted for all simulated and physical circuit elements. This enabled the test engineer to accurately tune the RLC load before each test.

In contrast to hardware anti-islanding tests, in PHIL tests the island breaker exists only in simulation, as shown in Figure 9. For each test, once the simulated load was balanced and tuned so that the fundamental real and reactive power flowing through the simulated breaker were nearly zero, the island was created by commanding the simulated breaker to open. The grid simulator (voltage amplifier) output remained enabled during the island test and continued to reproduce the PCC voltages. The test ended when the inverters recognized the island condition and tripped offline, causing the PCC voltages to drop to zero.

3.4 Multi-Inverter Anti-Islanding Test Results

The models and methods described above were used to run the 224 anti-islanding tests summarized in Table 10. An additional 20 anti-islanding tests described at the end of this section were run to check island ROTs in other scenarios not covered in Steps 1-4. Recall that Steps 1-3 used the worst-case configuration of GSFs for each inverter (as shown in Table 8), while Step 4 examined both of the two worst-case GSF configurations (from Table 8 and Table 9). A table presenting the results of all multi-inverter tests can be found in the Appendix.

3.4.1 Step 1: Circuit topology and impedance

The 50 tests in Step 1 examined the impacts of different island circuit topologies on island ROT (also called trip time or clearing time). The maximum and average (mean) measured ROTs for each inverter are summarized in Table 14. The ten test case numbers identify the ten circuit topologies tested (described in Section 2). Recall that each test scenario was repeated five times, with the first four tests varying the load tuning and the fifth test repeating the worst-case load tuning. The last two columns of Table 14 show the averages and maxima across all inverters for each test. Figure 11 presents the maximum, minimum, and mean ROT for each inverter for each case.

Table 14. Step 1: Island ROT summary for varying circuit topologies

Test Case	Circuit Topology and Impedances			Inverter 1		Inverter 2		Inverter 3		ALL INVERTERS	
	# Transformers	# Overhead Lines	# Underground Lines	Avg (ms)	Max (ms)	Avg (ms)	Max (ms)	Avg (ms)	Max (ms)	Avg (ms)	Max (ms)
1	1	0	3	147	187	289	555	221	310	**219**	**555**
2	1	3	0	269	356	227	312	277	365	257	365
3	3	0	3	212	383	290	411	244	380	249	411
4	3	3	0	208	281	221	417	241	350	223	417
5	3	1	2	202	300	297	494	234	403	**244**	**494**
6	3	2	1	196	255	255	448	228	326	227	448
7	2	0	3	285	347	312	394	314	365	**304**	**394**
8	2	3	0	164	245	219	374	192	279	191	374
9	2	1	2	217	371	245	345	243	386	235	386
10	2	2	1	232	374	314	402	255	361	267	402

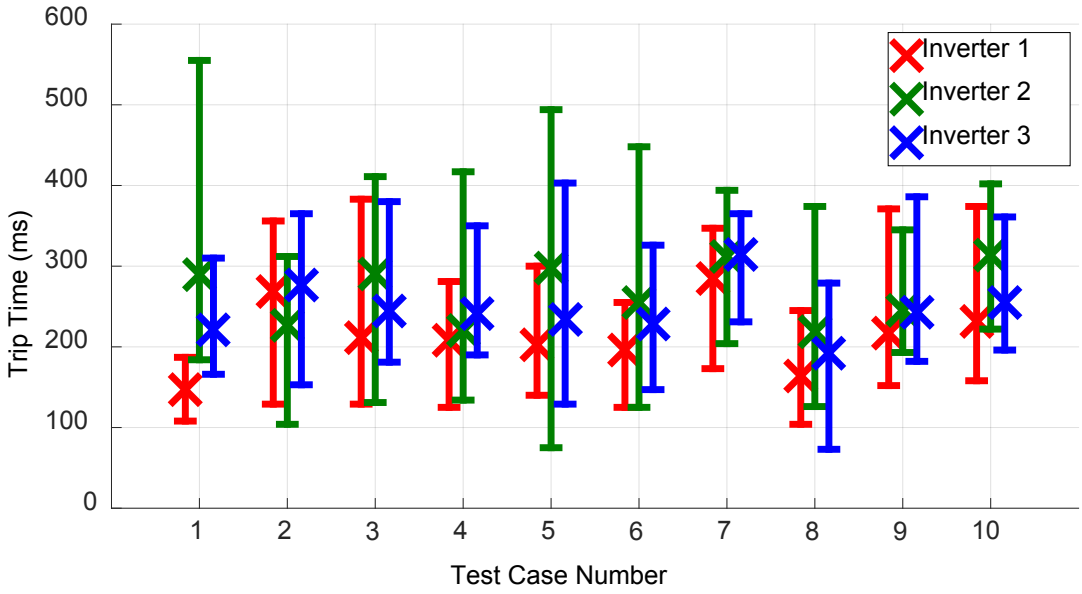

Figure 11. Maximum, mean, and minimum run-on time for each inverter for each case under Step 1.

The three worst-case tests scenarios selected for use in Step 4 are shown in red; two of the worst-case scenarios selected were the two topologies that gave the longest individual ROTs (cases 1 and 5). The third worst-case was selected as the topology that gave the longest average ROT (case 7) because that case had a noticeably longer average ROT than the other cases. Notably, while three nominally worst-case topologies were selected, the ROTs are actually fairly consistent across cases; no single topology stands out as producing remarkably longer ROTs that the others. In addition, of the three worst-case topologies, one has all inverters on the same transformer, one has each inverter on a different transformer, and one has two inverters on one transformer and one on another. Hence no topology stood out as particularly problematic.

Finally, in this test series, Inverter 2 recorded all three of the selected worst-case ROTs, but it always tripped in less than 600 ms, or less than one third of the allowed two seconds. The other two inverters tripped in less than 403 ms in all test cases. In subsequent steps, Inverter 2 did not always produce the worst-case ROTs. Figure 12 shows the measured inverter current and voltage waveforms for the test with the longest single ROT. Note that, as in all waveforms, the currents are magnified five times for improved visibility. Voltage at Inverter 1 is shown for reference; the other voltages are nearly identical on this scale, as expected. The currents and voltage shown here were measured on the inverter side of the physical transformer, as with all waveforms reported here, unless otherwise indicated. The grid breaker is opened at 0.5 seconds in the real-time model, as indicated by the Aux signal going to zero. Inverter 1 disconnects just before 0.7 seconds, and Inverter 3 disconnects just after 0.7 seconds. The island voltage drops significantly after the first two inverters drop offline, and Inverter 2 runs on alone for roughly an additional 350 ms, disconnecting 555 ms after the creation of the island. Notice that Inverter 3 appears to maintain its output contactor open for roughly 200 ms after controlling its power to near zero – the small current, likely flowing in the inverter's output filter, is not problematic. This behavior was typical of Inverter 3.

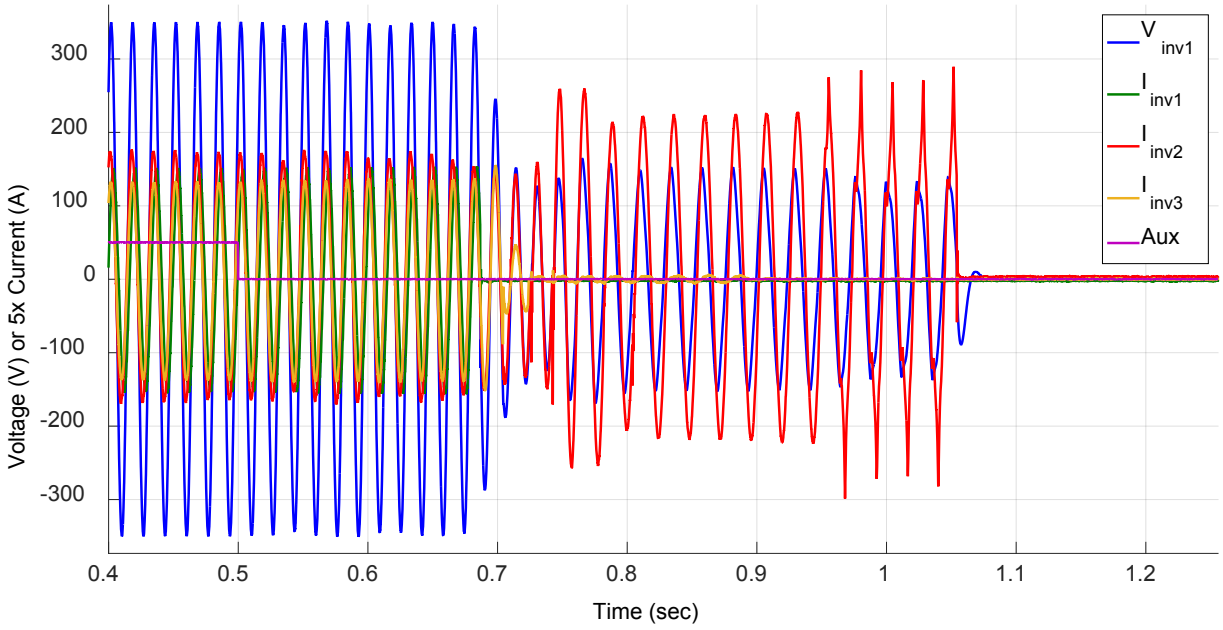

Figure 12. Inverter current and voltage waveforms for the Step 1 test with the longest maximum run-on time of 555 ms. The Aux signal goes to zero at the time the island is created. Only Inverter 1's voltage is shown for clarity; all three voltages are nearly identical on this scale. As in all test waveforms shown in this report, the currents are magnified five times for visibility.

Other test waveforms were qualitatively similar in that they remained largely sinusoidal with some variations in magnitude after the island formed. The order in which the inverters tripped varied from test to test. In general not all tests had two inverters trip at nearly the same time – in many tests the three inverters tripped at a three distinct times. A waveform with a more typical ROT of 221 ms is shown in Figure 13. Here, as in all tests, the island is formed at time 0.5

seconds. Inverter 2 trips first just after time 0.65, followed by Inverter 3 just after time 0.7, and Inverter 1 trips last at time 0.72, or 221 ms after the island was created.

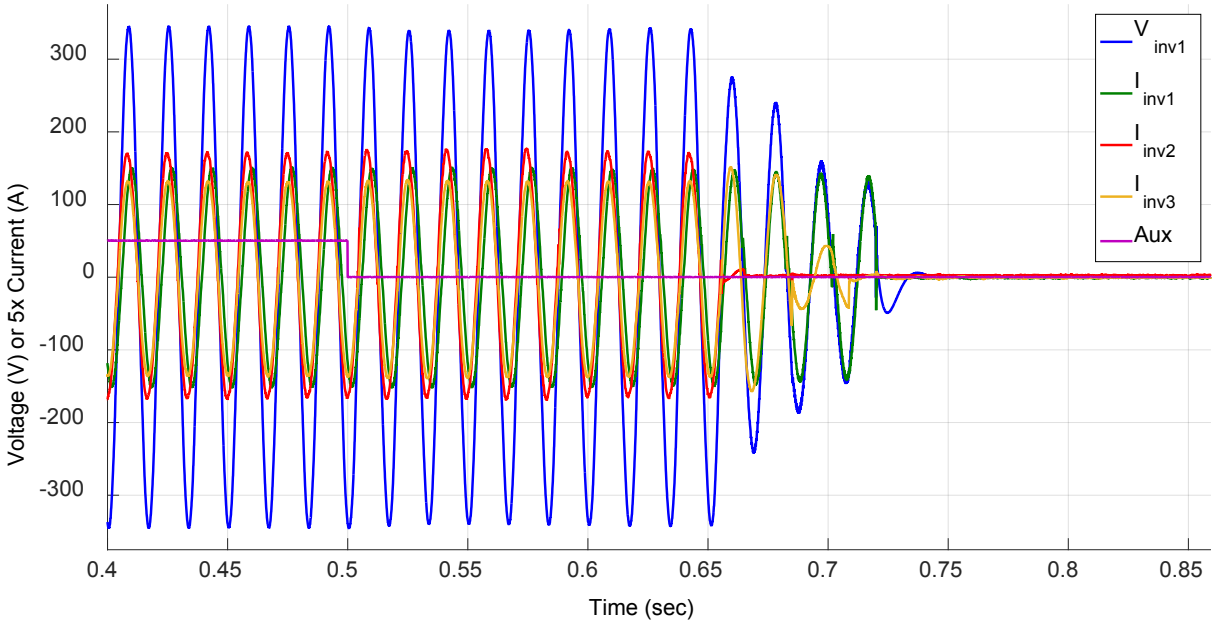

Figure 13. Inverter current and voltage waveforms for a Step 1 test with a typical run-on time of 221 ms.

3.4.2 Step 2: Load location

The 15 tests in Step 2 examined the impacts on island ROT of different resonant load locations relative to the inverters under test. As described in Section 3.3, three RLC load location scenarios were tested: 1. load distributed across the three inverter PCCs, 2. load located near the island breaker, and 3. load located far from the island breaker. These tests used the worst-case circuit topology from Step 1, which was Test Case 1 in Table 14. The maximum and average measured ROTs for each inverter are summarized in Table 15. Again each test scenario was repeated five times, with the first four tests varying the load tuning and the fifth test repeating the worst-case load tuning. The last two columns of Table 15 show the averages and maxima across all inverters for each test. Figure 14 presents the maximum, minimum, and mean ROT for each inverter for each case.

Table 15. Step 2: Island ROT summary for varying load locations

Test Case	Load Location	Inverter 1		Inverter 2		Inverter 3		ALL INVERTERS	
		Avg (ms)	Max (ms)	Avg (ms)	Max (ms)	Avg (ms)	Max (ms)	Avg (ms)	Max (ms)
1	Load distributed	218	249	211	350	243	344	224	350
2	Load near island breaker	188	241	169	280	201	311	186	311
3	Load far from island breaker	202	382	252	459	254	475	**236**	**475**

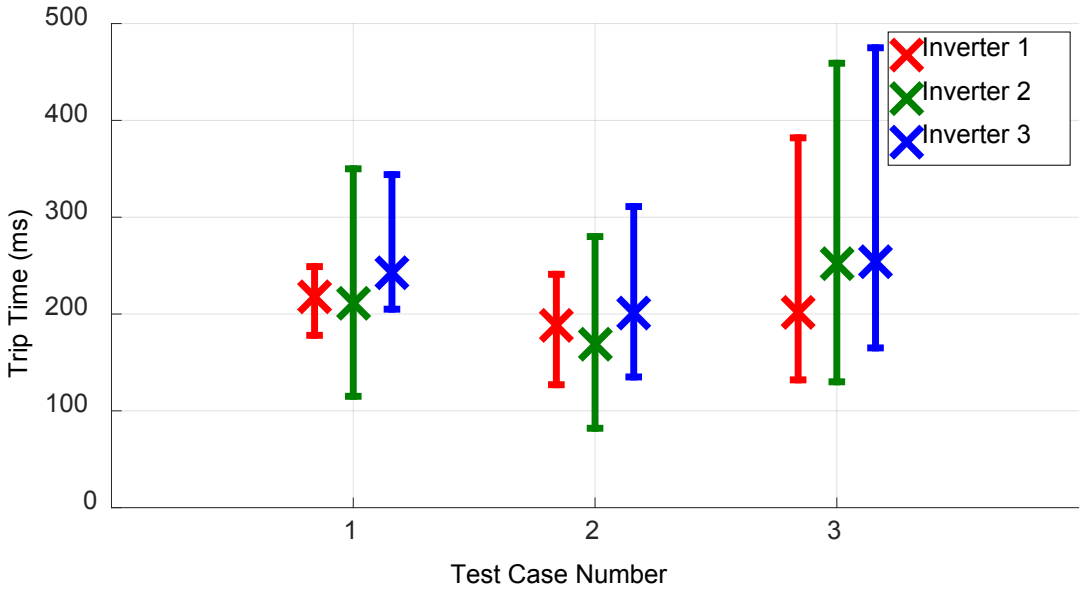

Figure 14. Maximum, mean, and minimum run-on time for each inverter for each case under Step 2.

In this step, the longest single ROT occurred in case 3, with the load aggregated into a single location far from the island breaker, and was produced by Inverter 3. However, no single load location scenario stood out as inducing consistently longer islands compared to other load location scenarios.

Figure 15 shows the inverter voltage and current waveforms for the Step 2 test with the longest ROT, 475 ms. Inverter 1 trips just before time 0.9; its current it difficult to see behind the other traces, but the trip time is clearly indicated by the abrupt drop in voltage magnitude. The other two inverters trip within six additional line cycles. Figure 16 shows a test from Step 2 with a more typical ROT of 241 ms.

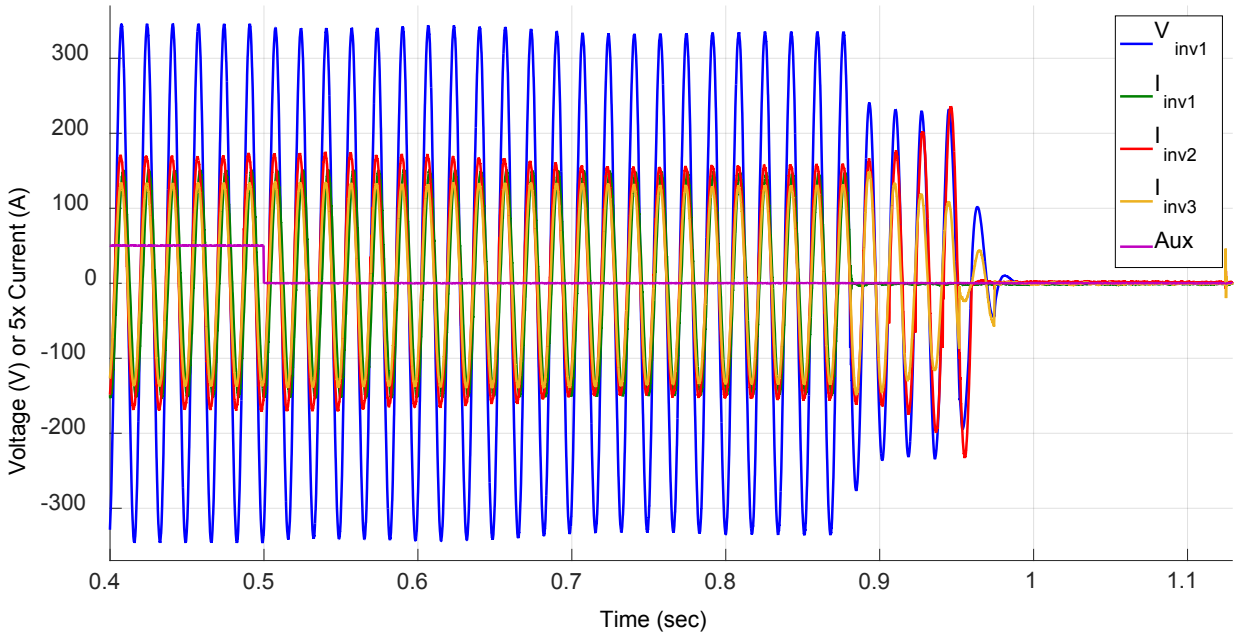

Figure 15. Inverter current and voltage waveforms for the Step 2 test with the longest maximum run-on time of 475 ms.

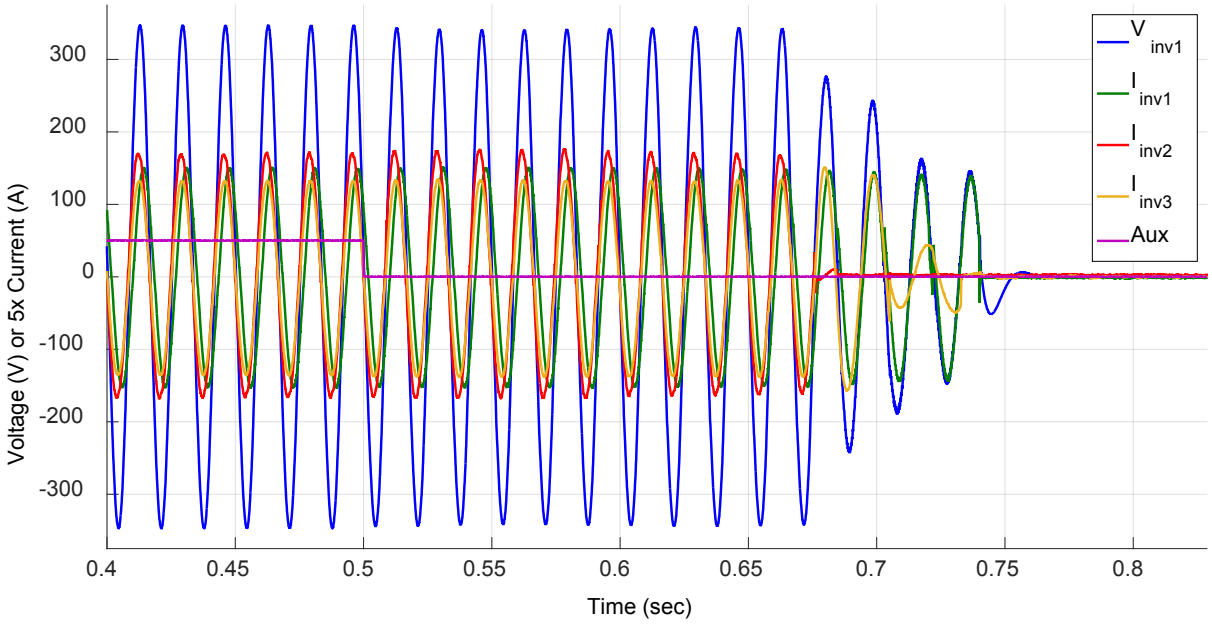

Figure 16. Inverter current and voltage waveforms for a Step 2 test with a typical run-on time of 241 ms.

3.4.3 Step 3: Grid impedance

The 15 tests in Step 3 examined the impacts on island ROT of different grid short-circuit impedances at the point of island disconnection (Z_{grid} in Figure 9). These tests used the worst-case circuit topology from Step 1 (Test Case 1, Table 14) and the worst-case load location from Step 2 (Test Case 3, Table 15, load near inverters). The maximum and average measured ROTs for each inverter are summarized in Table 16. As before, each test scenario was repeated five times, with the first four tests varying the load tuning and the fifth test repeating the worst-case load tuning. Figure 17 shows the maximum, minimum, and mean ROT for each inverter for each case.

Table 16. Step 3: Island ROT summary for varying short-circuit impedances

Test Case	Grid Impedance	Inverter 1		Inverter 2		Inverter 3		ALL INVERTERS	
		Avg (ms)	Max (ms)	Avg (ms)	Max (ms)	Avg (ms)	Max (ms)	Avg (ms)	Max (ms)
1	Minimum	257	379	306	430	307	390	290	430
2	Median	173	218	218	366	198	234	196	366
3	Maximum	220	280	324	438	271	324	**271**	**438**

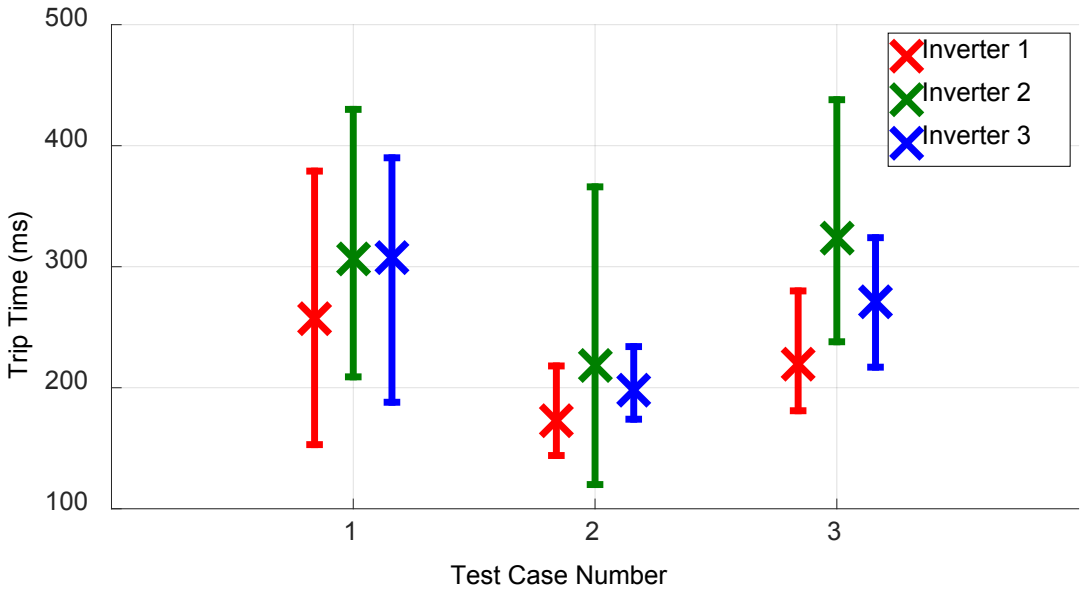

Figure 17. Maximum, mean, and minimum run-on time for each inverter for each case under Step 3.

In this step, the longest single ROT occurred in case 3, with the maximum grid short-circuit impedance. However, no grid impedance stood out as inducing consistently longer islands compared to others. As in Step 1, the longest ROT was due to Inverter 2.

Figure 18 shows the inverter voltage and current waveforms for the Step 3 test with the longest ROT. Inverter 1 trips first, followed a few cycles later by Inverter 3, and Inverter 2 trips last.

Figure 19 shows a test from Step 3 with a more typical ROT of 268 ms.

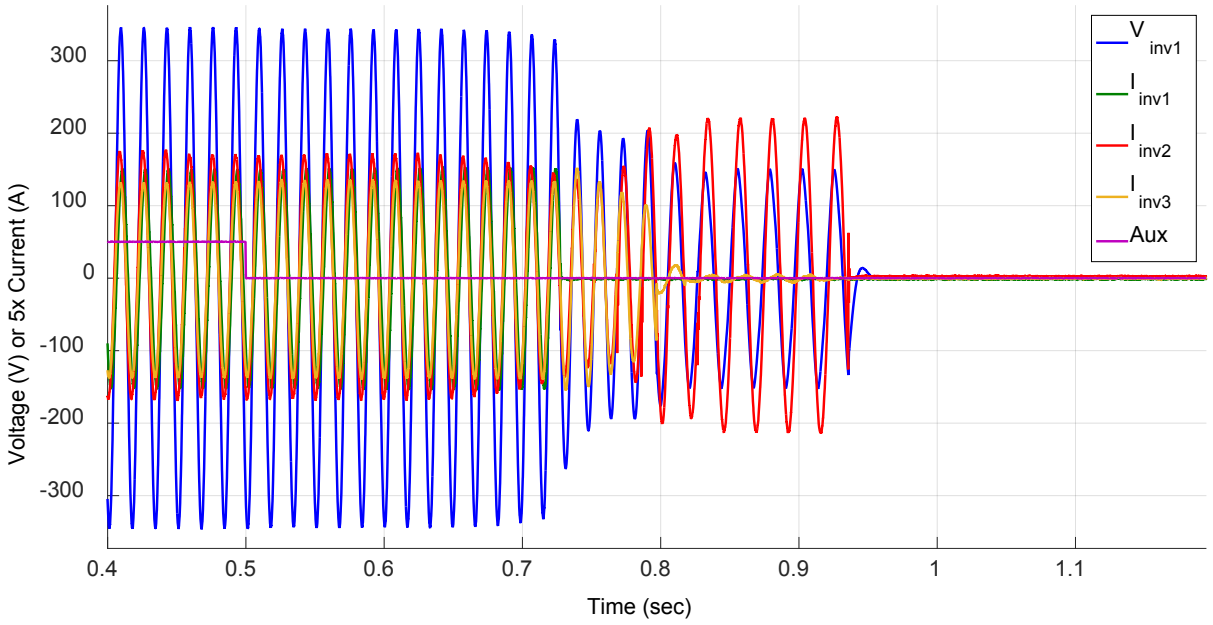

Figure 18. Inverter current and voltage waveforms for the Step 3 test with the longest maximum run-on time, 438 ms.

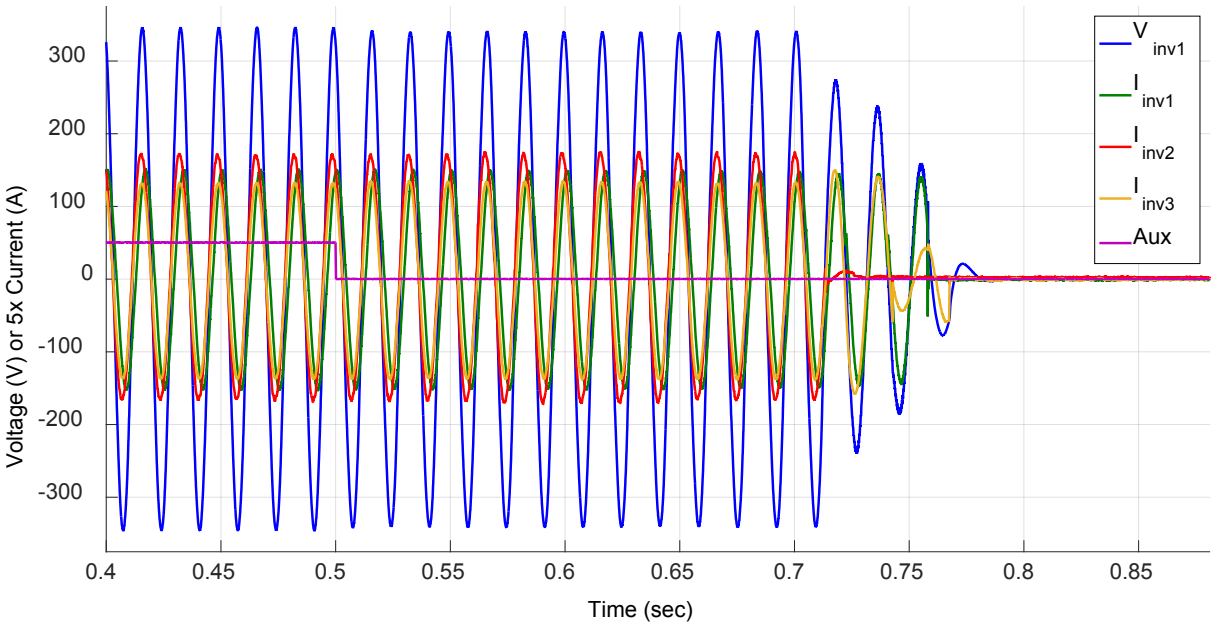

Figure 19. Inverter current and voltage waveforms for a Step 3 test with a typical run-on time of 268 ms.

3.4.4 Step 4: Detailed study of combined worst cases

The 144 tests in Step 4 combined the parameters that resulted in worst-case island ROTs in Steps 1-3 as well as the single-inverter tests. Step 4 examined all permutations of the two worst-case sets of inverter settings, the three worst-case circuit topologies (with associated impedances), and the six unique inverter location scenarios, creating 36 unique test cases. All tests were completed with loads aggregated at the far end of the circuit from the island breaker and with the maximum grid short circuit impedance, the worst-case conditions identified in Steps 2 and 3 respectively. Inverter GSF configurations 1 and 2 used were those shown in Table 8 and Table 9, respectively. Circuits 1, 2, and 3 were identified in Step 1 as cases 1, 5, and 7 respectively, per Table 14. Finally, the six inverter location scenarios were generated simply by rotating inverters between the three PCCs in each test circuit. Recall that, unlike in Steps 1-3, in Step 4 each test case was repeated four times: three times with varying load tunings and one time repeating the load tuning that resulted in the longest ROT.

Table 17 shows the maximum and mean ROTs for each inverter for each of the 36 test cases in Step 4. All ROT's fell below 630 ms, with most being well below that; no test came close to violating the IEEE 1547-2003 limit of two seconds.

Table 17. Step 4: Island ROT summary for detailed check of combined worst-case scenarios

Test Case	Test Settings			Inverter 1		Inverter 2		Inverter 3		ALL INVERTERS	
	Inverter GSF Configuration	Circuit #	Location Map	Avg (ms)	Max (ms)	Avg (ms)	Max (ms)	Avg (ms)	Max (ms)	Avg (ms)	Max (ms)
1	1	1	1	263	358	304	483	298	443	288	483
2	1	1	2	266	389	279	416	285	398	277	416
3	1	1	3	229	294	204	248	234	305	222	305
4	1	1	4	239	342	308	373	279	313	275	373
5	1	1	5	223	287	307	410	252	300	261	410
6	1	1	6	257	349	285	422	280	346	274	422
7	1	2	1	280	330	288	432	280	344	283	432
8	1	2	2	171	227	209	282	212	240	197	282
9	1	2	3	313	444	315	434	357	470	328	470
10	1	2	4	253	393	224	368	261	390	246	393
11	1	2	5	277	455	276	411	301	474	285	474
12	1	2	6	307	403	256	374	310	414	291	414
13	1	3	1	201	264	348	405	251	287	267	405
14	1	3	2	252	319	285	409	292	338	277	409
15	1	3	3	203	284	252	336	234	298	230	336
16	1	3	4	243	404	278	417	259	413	260	417
17	1	3	5	213	239	217	415	238	302	223	415
18	1	3	6	236	350	215	304	249	337	233	350
19	2	1	1	306	605	292	560	336	611	311	611
20	2	1	2	301	411	310	348	299	395	303	411
21	2	1	3	237	425	268	362	256	417	254	425
22	2	1	4	212	275	216	342	237	265	221	342
23	2	1	5	220	304	255	357	261	315	245	357
24	2	1	6	308	397	255	353	303	400	289	400
25	2	2	1	418	616	368	572	419	627	**402**	**627**
26	2	2	2	209	262	281	396	236	300	242	396
27	2	2	3	195	254	268	370	253	286	238	370
28	2	2	4	281	355	217	291	270	347	256	355
29	2	2	5	178	202	223	331	214	263	205	331
30	2	2	6	256	439	248	374	276	428	260	439
31	2	3	1	187	303	295	356	247	284	243	356
32	2	3	2	426	530	448	516	458	538	444	538
33	2	3	3	281	412	309	404	292	429	294	429
34	2	3	4	364	558	340	533	378	581	361	581
35	2	3	5	270	365	198	303	257	343	241	365
36	2	3	6	165	240	300	352	246	272	237	352

Figure 20 shows the maximum, mean, and minimum ROTs over the four iterations of each test case. Unlike in Steps 1-3, this whisker plot has the ROTs for all three inverters combined for each test. This was done simply to fit all results on one plot. A few ROTs fall above 500 ms, and two fall above 600 ms, but the majority fall in the 100-400 ms range. The overall maximum of 627 ms came on case 25, which used inverter GSF configuration 2 (see Table 9). This case used circuit 2, which had the three inverters on three different transformers, with two inverters connected via underground lines and one connected via an overhead line. However, it would not

be appropriate to conclude that this particular circuit topology and GSF configuration are likely to lead to longer island durations in the field based on the four tests of case 25. Also note that even in this worst case, all inverters disconnected in less than one third of the allowed two seconds.

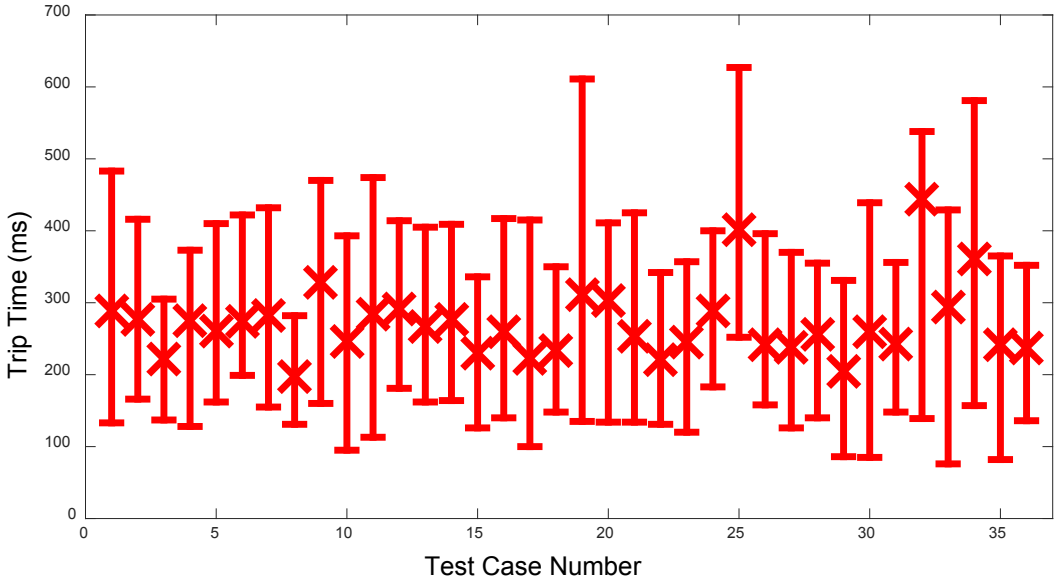

Figure 20. Maximum, mean, and minimum run-on time for each case under Step 4.

Figure 21 shows the inverter voltage and current waveforms for the test of case 25 with the single longest ROT. Notably, all three inverters run on for longer than typical, disconnecting within three cycles of each other. In this case Inverter 2 trips first, in contrast to many other tests where Inverter 2 often tripped last.

Figure 22 shows a test from Step 4 with a more typical ROT of 300 ms.

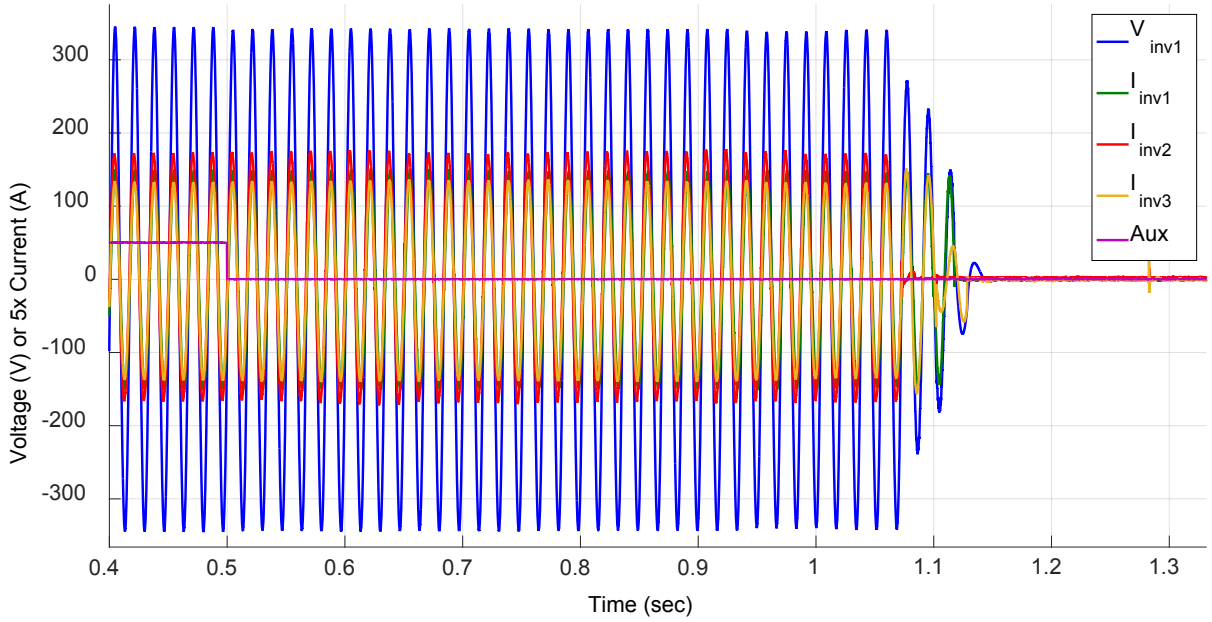

Figure 21. Inverter current and voltage waveforms for the Step 4 test with the longest maximum run-on time, 627 ms.

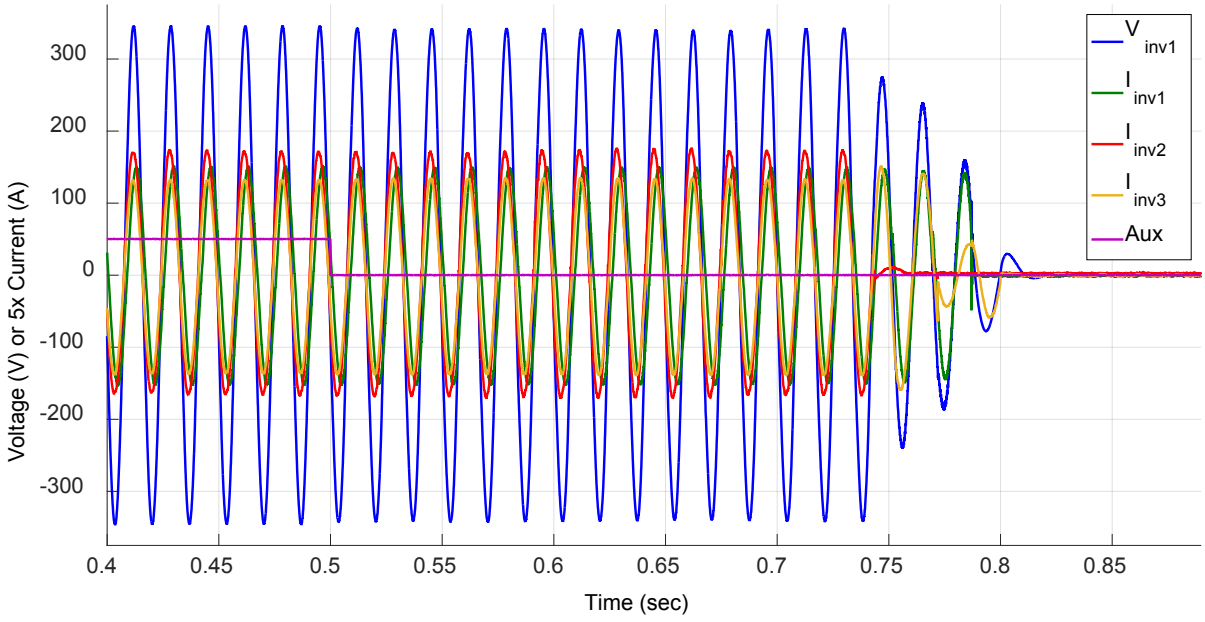

Figure 22. Inverter current and voltage waveforms for a Step 4 test with a typical run-on time of 300 ms.

3.4.5 Additional Tests: Timing of the Island

It is apparent from testing that one of the tested inverters (Inverter 1) attempts to shift grid frequency as part of its anti-islanding algorithm by introducing small periodic variations in the phase angle of its output current. If it is able to shift grid frequency, it concludes that it is in an island and disconnects. The period of the variations in phase angle is on the order of four seconds. This has the effect of creating small variations in the inverter's reactive power output. Because the reactive power draw of the rest of the circuit is nearly constant, a nearly equal-and-opposite variation in the reactive power flowing through the island breaker was observed. The variations in reactive power also induce changes in real power with the same regular period, which were also clearly observed in the PHIL model. For these reasons, a load tuning that is nearly perfect at one moment is off by several percentage points one second later, and then nearly perfect again after another second (this is in fact the mechanism by which this islanding detection method works). To account for this behavior, in Steps 1-4 above the opening of the island breaker was timed to coincide as nearly as possible with the zero-crossing of real and reactive power flowing through the island breaker.

To investigate the possibility that other timings of island creation relative to the periodic variations in power could actually lead to longer ROTs, an additional series of ten tests was run using the test case that led to the worst-case overall ROT in Step 4 (case 25). In five of the tests, the island ROT was timed to minimize power flowing through the breaker as usual. In the other five, the island disconnection time was randomized.

Table 18 shows the results of these additional ten tests, and Figure 23 depicts the ROT data graphically. The cases of random disconnection timing led to slightly lower *average* ROT, but higher *maximum* ROT due to one outlier test, which is investigated and explained below. Even this outlier, which at 632 ms was longest overall ROT from all multi-inverter tests, was comfortably below the two-second allowance. Also note that while test case 1 here is nominally the same as test case 25 from Step 4, the two cases were run on different days and had slightly different load tunings due to non-idealities in the test physical setup (e.g. transformer temperature) that result in small variations in load tuning from day to day. This, coupled with stochastic effects inherent to anti-islanding tests, caused the two sets of tests to have different ranges of ROT.

Table 18. Island ROT summary comparing timed island creation to untimed island creation

Test Case	Island disconnection timing	Inverter 1		Inverter 2		Inverter 3		ALL INVERTERS	
		Avg (ms)	Max (ms)	Avg (ms)	Max (ms)	Avg (ms)	Max (ms)	Avg (ms)	Max (ms)
1	Timed Disconnection	283	428	328	455	325	410	312	455
2	Random Disconnection Time	242	632	226	550	247	612	238	632

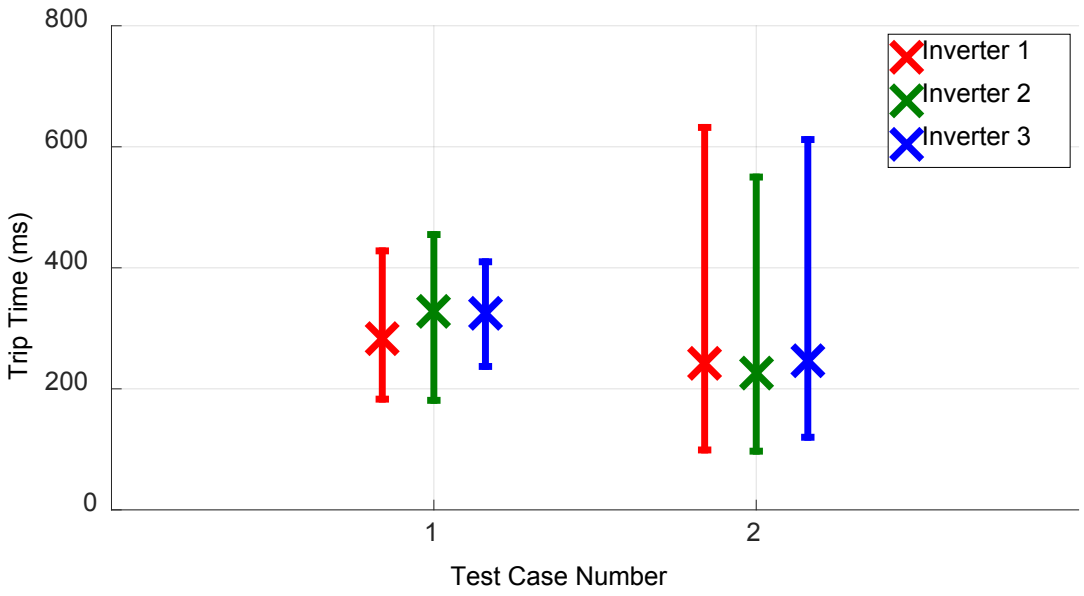

Figure 23. Maximum, mean, and minimum run-on time for each inverter comparing cases of timed disconnection and untimed disconnection.

Figure 24 shows the inverter voltage and current waveforms for the test with the longest ROT (the outlier mentioned above). As in the test shown in Figure 21, the three inverters all trip late in the test. Inverter 2 trips first, followed by Inverter 3 a few cycles later, and then by Inverter 1 about one cycle later.

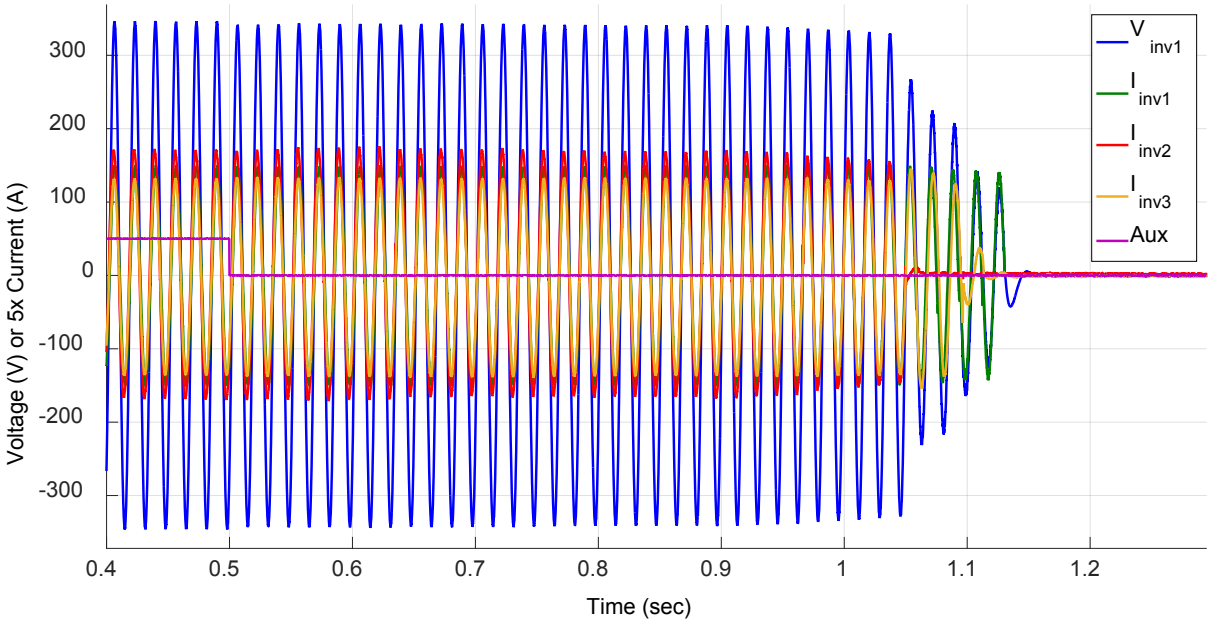

Figure 24. Inverter current and voltage waveforms for the test with the longest overall maximum run-on time, 632 ms.

Simulated PHIL waveforms were examined to investigate this outlier. Figure 25 shows the real and reactive powers flowing through the island breaker before the island was formed, as calculated from the simulated voltage and current in the PHIL model. The island was formed at time 180.7 in PHIL time, as is clearly visible from the fact that the power flows both go to zero at that time. Some of the spikes in reactive power are due to the anti-islanding mechanism of Inverter 2, and others are due to noise and other effects. The real and reactive powers were both averaged over five line cycles. One half-period of the periodic variations in real and reactive power due to Inverter 1 is also visible. Note that while the timing of the island creation was randomized, in this particular test it happened to occur very near the zero-crossings of the periodic variation in real and reactive power flowing through the breaker. Thus this one test is effectively very similar to the tests where the disconnection was intentionally timed to coincide with the zero-crossing of real and reactive power. In other words, the outlier is effectively the same as a timed disconnection test.

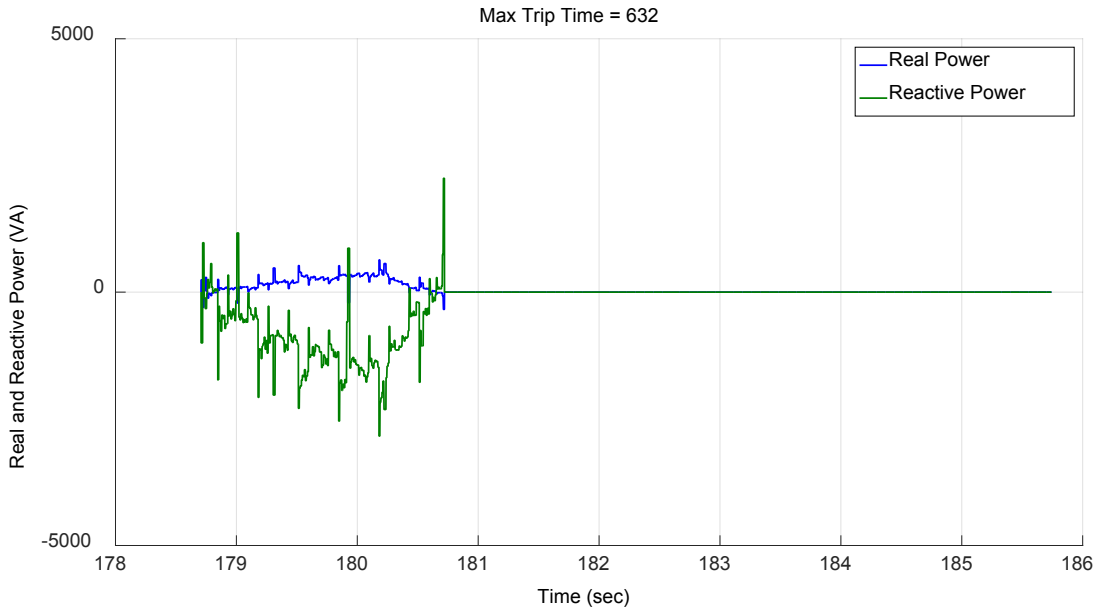

Figure 25. Real and reactive power flowing through the PHIL-simulated island breaker during the test with the longest run-on time.

If the one test shown in Figure 24 and Figure 25 were excluded, the tests with randomized disconnection time would have a maximum ROT of only 200 ms, which is below the *average* ROT of the five comparable tests with targeted disconnection time. This supports the conclusion that intentionally targeting the disconnection time at the zero-crossing of real and reactive power flowing through the island breaker tends to lead to longer island durations. This was the technique used in all tests in Steps 1-4. Thus this comparison of randomized disconnection to targeted disconnection supports the conclusion that Steps 1-4 truly capture worst-case ROTs for the scenarios examined, as designed.

Figure 26 shows the voltage and current waveforms for a test that is typical of those with randomized disconnection time. This test had a maximum ROT of 200 ms. Figure 27 shows the real and reactive power flowing through the island breaker. In this test, more data was captured before the island event, so the periodic variations in power are more evident than in Figure 25. It is evident that in this test, the island disconnection occurred near – but not exactly at – the zero-crossing of real and reactive power.

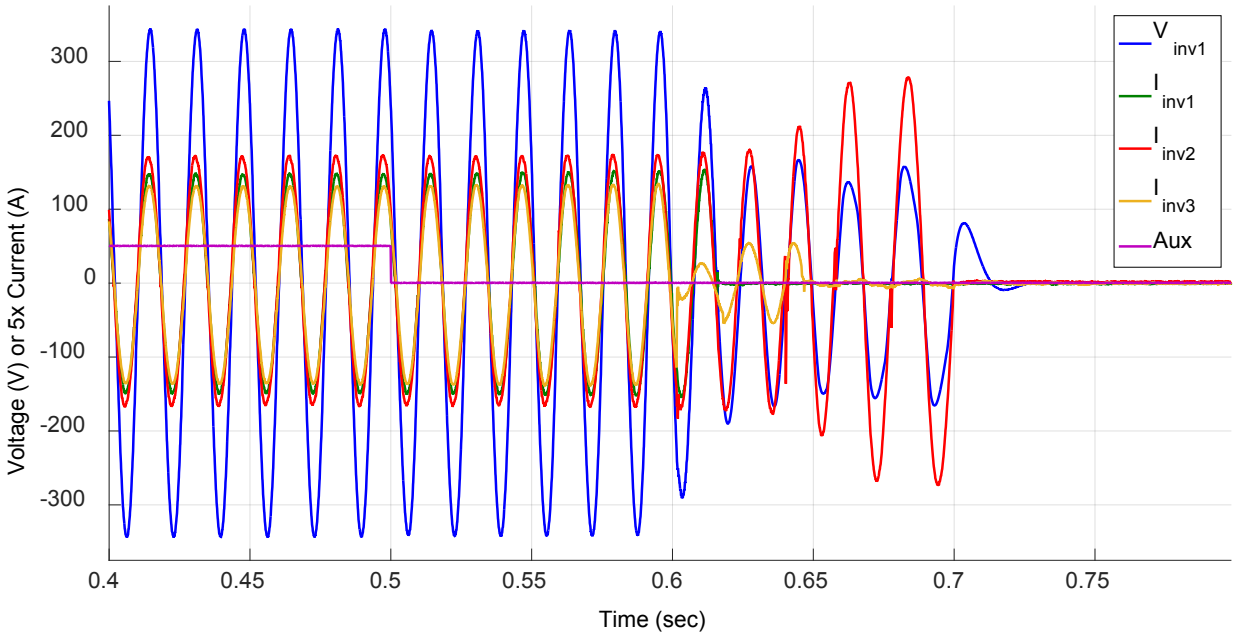

Figure 26. Inverter current and voltage waveforms for a test with randomized island disconnection time and typical run-on time of 200 ms.

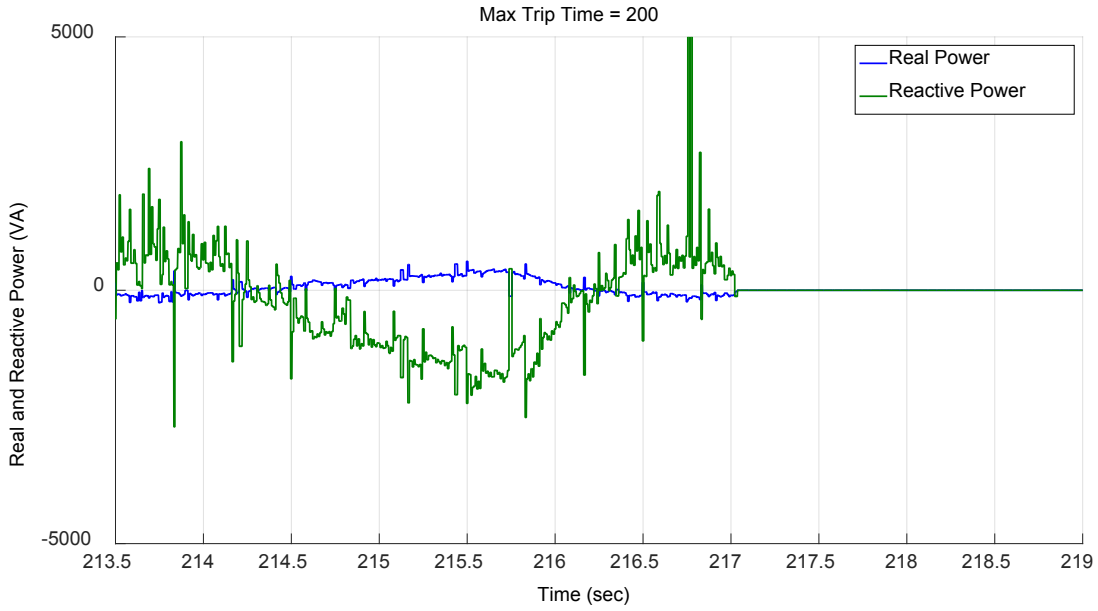

Figure 27. Real and reactive power flowing through the PHIL-simulated island breaker during the test with a typical run-on time shown in Figure 26.

3.4.6 Additional Tests: Other Load Tunings

Realistic distribution circuits rarely contain enough capacitance to replicate the balanced resonant RLC load condition used in anti-islanding tests. For an inverter operating near unity power factor, the load's absorption of VArs must be nearly equal to its sourcing of VArs to meet this condition. Loads that can be approximated by linear circuit elements tend to have some combination of resistive and inductive components. Therefore several additional tests were run using only the resistive and inductive load elements to tune the load. Hence the load quality factor for these tests is much lower than unity.

Two sets of five tests were run using a parallel resistive-inductive (RL) load in the PHIL model: in the first case an RL load was used with the elements tuned so that the entire circuit matched the real and reactive powers of the inverters. To achieve this tuning, the magnitude of the voltage source in the PHIL model was reduced so that inverters with Volt-VAr control active were sourcing VArs. The second set of five tests used the same scenario, but the RL load was de-tuned by approximately 10% to investigate the effect of a somewhat less well-tuned circuit on island duration. Both sets of tests used the worst-case overall scenario from Step 4, which was case 25.

Table 19 summarizes the measured ROTs for the ten RL load tests and Figure 28 presents the results graphically. For comparison, test case 25 from Step 4 is also included as case 1 in the figure and the table. Both sets of RL load tests had mean and maximum ROTs roughly 200 ms below those of the baseline case. These ROTs are on the low end of those measured in Steps 1-4, but are not outside the range of ROTs from the RLC load tests.

Table 19. Island ROT summary using resistive-inductive loads

Test Case	Test Settings	Inverter 1		Inverter 2		Inverter 3		ALL INVERTERS	
		Avg (ms)	Max (ms)	Avg (ms)	Max (ms)	Avg (ms)	Max (ms)	Avg (ms)	Max (ms)
1	Tuned RLC (baseline)	418	616	368	572	419	627	402	627
2	Tuned RL Load	181	342	275	397	200	299	219	397
3	De-Tuned RL Load	167	297	230	372	188	314	195	372

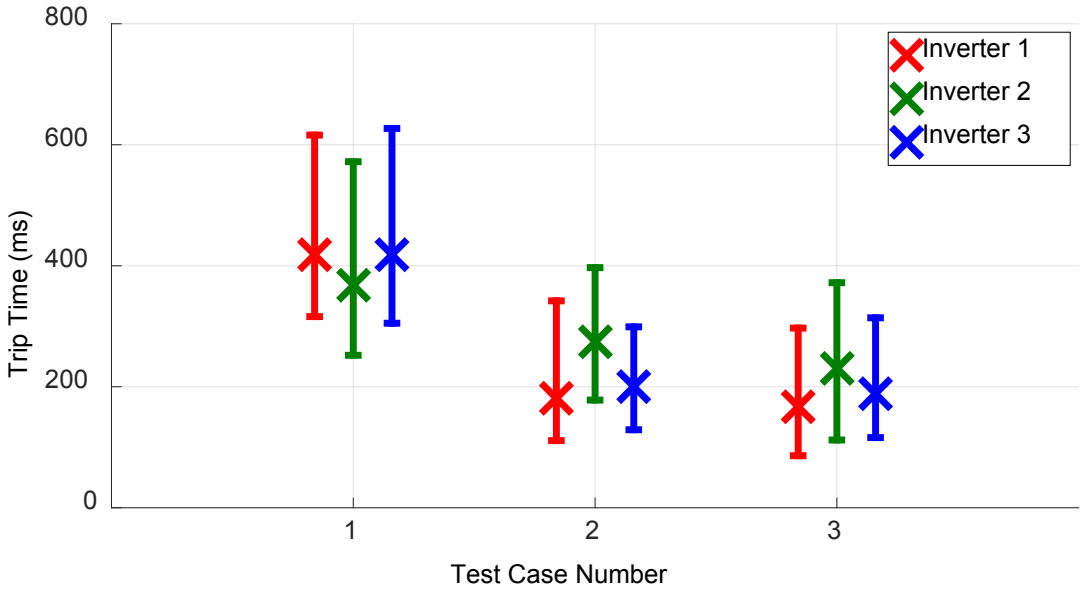

Figure 28. Maximum, mean, and minimum run-on time for each inverter for tests using an RL load.

Figure 29 shows the voltage current waveforms for the de-tuned RL load test with the longest ROT, and Figure 30 shows a more typical test from that set. These waveforms are qualitatively fairly similar to those from the RLC load tests. Note that in these tests, after the last inverter disconnects the load does not resonate as it did in the RLC load tests, as expected.

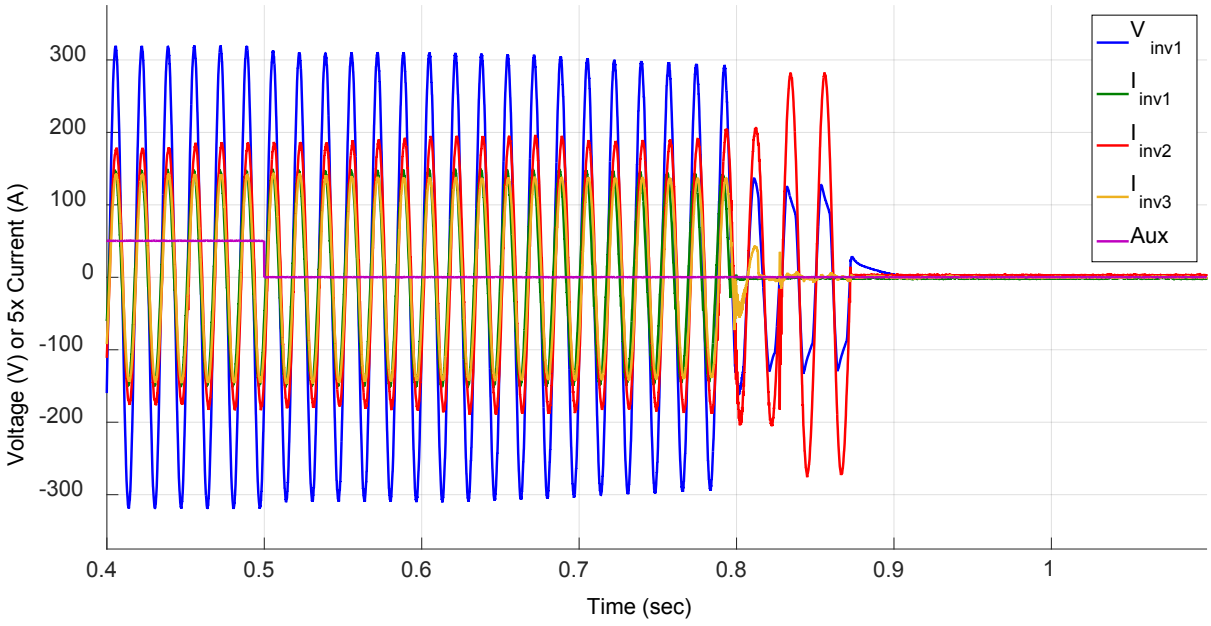

Figure 29. Inverter current and voltage waveforms for the de-tuned RL load test with the longest maximum run-on time, 372 ms.

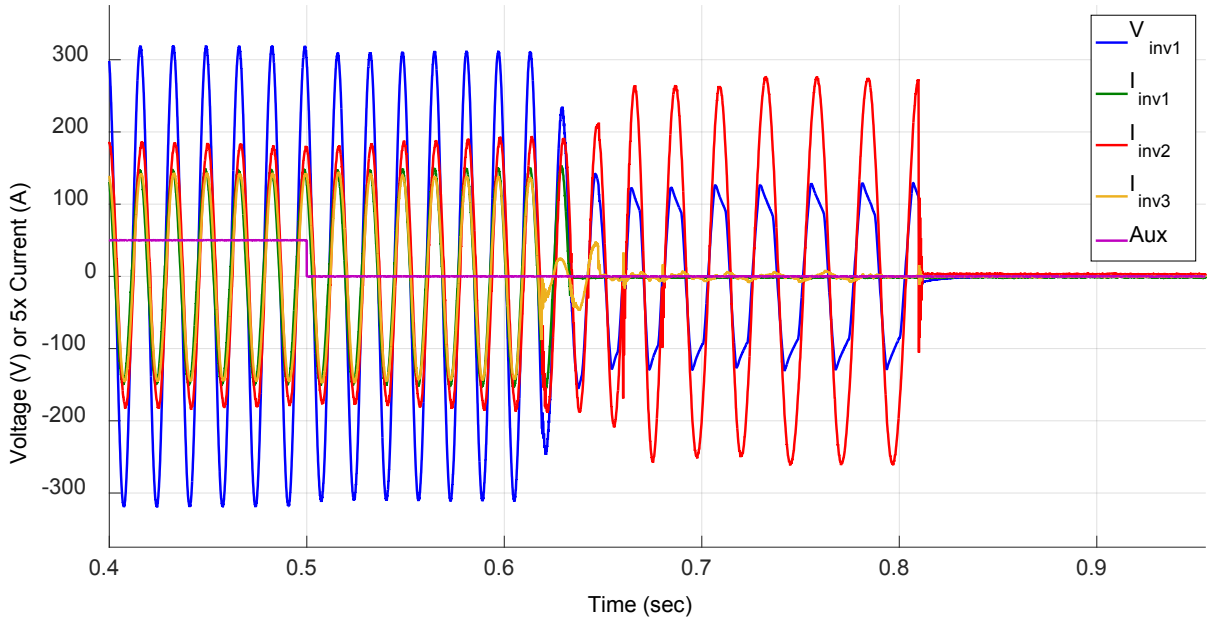

Figure 30. Inverter current and voltage waveforms for a de-tuned RL load test with typical run-on time of 311 ms.

3.4.7 Statistical Analysis

In the multi-inverter tests, no single test parameter seemed to clearly have a large impact on ROT. Regression analysis was performed on the multi-inverter test data in an attempt to quantify this conclusion. Maximum ROT was taken as the dependent variable. The following categorical predictor variables were considered:

- Grid support function configuration
- Island circuit configuration
- Location of load relative to inverters
- Grid short-circuit impedance at the island location
- Inverter location map (i.e. which inverter is connected to which PCC)

A linear regression model considering all predictor variables had a p-value of 0.4, so the model was discarded. Models with other combinations of predictor variables were also generated, and high p-values were found for most. However, linear regression with GSF configuration as the only predictor resulted in Equation (2) with a reasonably low p-value of 0.046 and RMS error of 98 ms.

$$\boldsymbol{ROT} = \mathbf{297} + \mathbf{27} \cdot \boldsymbol{GSF2} + \varepsilon \text{ [ms]} \quad (2)$$

Here *ROT* is the maximum ROT among the three inverters for a given test, and *GSF*2 is a binary variable that is equal to one when GSF configuration 2 is active and equal to zero when GSF configuration 1 is active.

A primary conclusion to be drawn from this analysis is that the stochastic variation between tests is significantly larger than the effect of any single test parameter. In other words, none of the many variables tested had a larger effect of ROT than the random variations that are inherently present in anti-islanding tests.

In addition, the model captured in Equation (2) indicates that the second worst-case GSF configuration from single inverter tests actually resulted in *longer* ROTs in multi-inverter tests than the worst-case GSF configuration did by 27 ms. These two GSF configurations can be found in Table 8 and Table 9.

One significant thing to keep in mind when considering this regression analysis is that it is based on all multi-inverter tests in Steps 1-4, and thus is predictive of the maximum ROT for the three inverters in a single test. However, it is not predictive of the maximum ROT that would result from repeating any single test many times, which is a more important parameter since the goal of anti-islanding is to prevent ROTs beyond some threshold rather than to reduce average ROTs. Much more data would be needed to develop a model to predict maximum ROTs across many tests, since each individual data point going into the model would need to consist of the maximum ROT across many tests.

3.4.8 Transient Overvoltage

Because some members of the energy industry have expressed concern about transient overvoltage associated with islanding, all test waveforms were examined for any overvoltage. Because these are single-phase tests, the overvoltage mechanism of concern is load rejection overvoltage. No instantaneous voltage measurement exceeding 110% of the nominal peak voltage was measured in any test. This is not particularly surprising: the islanding tests were intentionally run at or very near matched generation:load ratios to create a difficult island detection scenario, and little transient overvoltage is expected in such matched-load cases [24], [25].

4 Conclusions

This report has presented the results of a detailed experimental study of the impacts on anti-islanding of inverter-based grid support functions including low- and high-voltage ride-through, low- and high-frequency ride-through, Volt-VAr control, and frequency-Watt control. This study was designed to determine how grid support functions impacted island detection in individual inverters and on a circuit with multiple inverters connected. For this reason, this test examined both single-inverter and multiple-inverter island scenarios.

The multi-inverter island scenarios were tested using a ten realistic distribution circuit topologies with the inverters connected to different points in those circuits. A detailed test plan was used to empirically identify worst-case test scenarios for in-depth anti-island testing. Load locations, grid short-circuit impedances, and combinations of grid support functions were varied, resulting in a total of 49 unique multi-inverter test cases (36 from Step 4, plus an additional 13 unique cases in other steps), each of which was tested at least four times. Three PV inverters from different manufacturers were used in testing. The tests employed an RLC load bank tuned so that the island circuit:

- resonated at 60 Hz with a quality factor of 1.0, and
- matched the real and reactive power of the inverters under test.

This load tuning was designed by the authors of IEEE 1547.1-2005 to make island detection difficult for the purpose of evaluating the effectiveness of anti-islanding algorithms. Additional tests were also run with RL loads which are more representative of typical distribution circuit loads. These tests resulted in significantly lower maximum and average island durations than the RLC load tests.

In all multi-inverter test cases and for all island circuit scenarios, the island run-on time remained below 640 milliseconds, comfortably below the maximum allowed island run-on time specified in IEEE 1547 of two seconds.

In all single-inverter tests, the maximum island run-on time was 711 ms, also well below the requirement. Given the expectation that multiple-inverter islands may persist longer than single-inverter islands, it is perhaps notable that the three longest overall run-on times came in single-inverter tests. This may be because in a balanced multi-inverter island, once one inverter detects the island and disconnects, the island is no longer balanced and it becomes easier for the remaining inverters to detect the island. It is difficult to predict the extent to which these results will apply to islands with larger numbers of inverters, or to inverters using different islanding detection philosophies than those embodied in the test inverters. However, these results are highly encouraging in that they present the first laboratory test of multi-inverter, multi-point islands, and no island durations longer than 640 ms were observed, despite the challenging island-detection conditions that were created.

These test results confirm that it will be important for standards development organizations working on anti-islanding to account for the effects of grid support functions. The soon-to-be published UL 1741 Supplement SA does just that, and thus this report should increase

confidence that inverters certified to UL 1741 Supplement SA may be safely and reliably interconnected with grid support functions activated.

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Appendix

This appendix presents the results of each individual anti-islanding test analyzed in this report.

All individual anti-islanding test results are shown below for Inverters 1, 2, and 3 in Table 20, Table 21, and Table 22, respectively. The GSF configurations for each test cast are as defined in Table 4, and are repeated below for convenience.

Table 23 presents the results of all 244 multi-inverter anti-islanding tests.

Table 20. Run-on times of all single-inverter anti-islanding tests of Inverter 1

GSF Test Case	Inverter	VRT	FRT	FWC	VVC	ROT (ms)
1	1	OFF	OFF	OFF	OFF	132
1	1	OFF	OFF	OFF	OFF	133
1	1	OFF	OFF	OFF	OFF	128
1	1	OFF	OFF	OFF	OFF	110
1	1	OFF	OFF	OFF	OFF	160
2	1	ON	ON	OFF	OFF	66
2	1	ON	ON	OFF	OFF	421
2	1	ON	ON	OFF	OFF	391
2	1	ON	ON	OFF	OFF	63
2	1	ON	ON	OFF	OFF	162
3	1	ON	ON	OFF	SHALLOW	101
3	1	ON	ON	OFF	SHALLOW	71
3	1	ON	ON	OFF	SHALLOW	126
3	1	ON	ON	OFF	SHALLOW	98
3	1	ON	ON	OFF	SHALLOW	161
4	1	ON	ON	OFF	STEEP	92
4	1	ON	ON	OFF	STEEP	138
4	1	ON	ON	OFF	STEEP	98
4	1	ON	ON	OFF	STEEP	90
4	1	ON	ON	OFF	STEEP	73
5	1	ON	ON	SHALLOW	OFF	110
5	1	ON	ON	SHALLOW	OFF	117
5	1	ON	ON	SHALLOW	OFF	167
5	1	ON	ON	SHALLOW	OFF	119
5	1	ON	ON	SHALLOW	OFF	183
6	1	ON	ON	SHALLOW	SHALLOW	167
6	1	ON	ON	SHALLOW	SHALLOW	288
6	1	ON	ON	SHALLOW	SHALLOW	68
6	1	ON	ON	SHALLOW	SHALLOW	70
6	1	ON	ON	SHALLOW	SHALLOW	460
7	1	ON	ON	SHALLOW	STEEP	81
7	1	ON	ON	SHALLOW	STEEP	74
7	1	ON	ON	SHALLOW	STEEP	64
7	1	ON	ON	SHALLOW	STEEP	92
7	1	ON	ON	SHALLOW	STEEP	432
8	1	ON	ON	STEEP	OFF	100
8	1	ON	ON	STEEP	OFF	108
8	1	ON	ON	STEEP	OFF	502
8	1	ON	ON	STEEP	OFF	84
8	1	ON	ON	STEEP	OFF	93
9	1	ON	ON	STEEP	SHALLOW	73
9	1	ON	ON	STEEP	SHALLOW	476
9	1	ON	ON	STEEP	SHALLOW	66
9	1	ON	ON	STEEP	SHALLOW	76
9	1	ON	ON	STEEP	SHALLOW	154
10	1	ON	ON	STEEP	STEEP	107
10	1	ON	ON	STEEP	STEEP	68
10	1	ON	ON	STEEP	STEEP	406
10	1	ON	ON	STEEP	STEEP	115
10	1	ON	ON	STEEP	STEEP	394

Table 21. Run-on times of all single-inverter anti-islanding tests of Inverter 2

GSF Test Case	Inverter	VRT	FRT	FWC	VVC	ROT (ms)
1	2	OFF	OFF	OFF	OFF	80
1	2	OFF	OFF	OFF	OFF	182
1	2	OFF	OFF	OFF	OFF	116
1	2	OFF	OFF	OFF	OFF	301
1	2	OFF	OFF	OFF	OFF	153
1	2	OFF	OFF	OFF	OFF	168
2	2	ON	ON	OFF	OFF	178
2	2	ON	ON	OFF	OFF	206
2	2	ON	ON	OFF	OFF	230
2	2	ON	ON	OFF	OFF	319
2	2	ON	ON	OFF	OFF	167
3	2	ON	ON	OFF	SHALLOW	410
3	2	ON	ON	OFF	SHALLOW	78
3	2	ON	ON	OFF	SHALLOW	92
3	2	ON	ON	OFF	SHALLOW	120
3	2	ON	ON	OFF	SHALLOW	272
4	2	ON	ON	OFF	STEEP	282
4	2	ON	ON	OFF	STEEP	223
4	2	ON	ON	OFF	STEEP	142
4	2	ON	ON	OFF	STEEP	99
4	2	ON	ON	OFF	STEEP	254
5	2	ON	ON	SHALLOW	OFF	285
5	2	ON	ON	SHALLOW	OFF	246
5	2	ON	ON	SHALLOW	OFF	157
5	2	ON	ON	SHALLOW	OFF	181
5	2	ON	ON	SHALLOW	OFF	179
5	2	ON	ON	SHALLOW	OFF	190
6	2	ON	ON	SHALLOW	SHALLOW	382
6	2	ON	ON	SHALLOW	SHALLOW	201
6	2	ON	ON	SHALLOW	SHALLOW	318
6	2	ON	ON	SHALLOW	SHALLOW	399
6	2	ON	ON	SHALLOW	SHALLOW	327
6	2	ON	ON	SHALLOW	SHALLOW	237
7	2	ON	ON	SHALLOW	STEEP	128
7	2	ON	ON	SHALLOW	STEEP	100
7	2	ON	ON	SHALLOW	STEEP	364
7	2	ON	ON	SHALLOW	STEEP	224
7	2	ON	ON	SHALLOW	STEEP	284
7	2	ON	ON	SHALLOW	STEEP	107
8	2	ON	ON	STEEP	OFF	274
8	2	ON	ON	STEEP	OFF	346
8	2	ON	ON	STEEP	OFF	191
8	2	ON	ON	STEEP	OFF	427
8	2	ON	ON	STEEP	OFF	180
8	2	ON	ON	STEEP	OFF	283
9	2	ON	ON	STEEP	SHALLOW	431
9	2	ON	ON	STEEP	SHALLOW	68
9	2	ON	ON	STEEP	SHALLOW	203
9	2	ON	ON	STEEP	SHALLOW	668
9	2	ON	ON	STEEP	SHALLOW	84
10	2	ON	ON	STEEP	STEEP	383
10	2	ON	ON	STEEP	STEEP	196
10	2	ON	ON	STEEP	STEEP	187
10	2	ON	ON	STEEP	STEEP	148
10	2	ON	ON	STEEP	STEEP	102
10	2	ON	ON	STEEP	STEEP	112

Table 22. Run-on times of all single-inverter anti-islanding tests of Inverter 3

GSF Test Case	Inverter	VRT	FRT	FWC	VVC	ROT (ms)
1	3	OFF	OFF	OFF	OFF	130
1	3	OFF	OFF	OFF	OFF	97
1	3	OFF	OFF	OFF	OFF	312
1	3	OFF	OFF	OFF	OFF	90
1	3	OFF	OFF	OFF	OFF	104
2	3	ON	ON	OFF	OFF	238
2	3	ON	ON	OFF	OFF	136
2	3	ON	ON	OFF	OFF	156
2	3	ON	ON	OFF	OFF	207
2	3	ON	ON	OFF	OFF	286
3	3	ON	ON	OFF	SHALLOW	337
3	3	ON	ON	OFF	SHALLOW	407
3	3	ON	ON	OFF	SHALLOW	148
3	3	ON	ON	OFF	SHALLOW	588
3	3	ON	ON	OFF	SHALLOW	711
4	3	ON	ON	OFF	STEEP	120
4	3	ON	ON	OFF	STEEP	118
4	3	ON	ON	OFF	STEEP	109
4	3	ON	ON	OFF	STEEP	123
4	3	ON	ON	OFF	STEEP	134
5	3	ON	ON	SHALLOW	OFF	394
5	3	ON	ON	SHALLOW	OFF	299
5	3	ON	ON	SHALLOW	OFF	327
5	3	ON	ON	SHALLOW	OFF	316
5	3	ON	ON	SHALLOW	OFF	294
6	3	ON	ON	SHALLOW	SHALLOW	111
6	3	ON	ON	SHALLOW	SHALLOW	126
6	3	ON	ON	SHALLOW	SHALLOW	145
6	3	ON	ON	SHALLOW	SHALLOW	205
6	3	ON	ON	SHALLOW	SHALLOW	423
7	3	ON	ON	SHALLOW	STEEP	615
7	3	ON	ON	SHALLOW	STEEP	260
7	3	ON	ON	SHALLOW	STEEP	263
7	3	ON	ON	SHALLOW	STEEP	579
7	3	ON	ON	SHALLOW	STEEP	270
8	3	ON	ON	STEEP	OFF	154
8	3	ON	ON	STEEP	OFF	157
8	3	ON	ON	STEEP	OFF	183
8	3	ON	ON	STEEP	OFF	172
8	3	ON	ON	STEEP	OFF	230
9	3	ON	ON	STEEP	SHALLOW	147
9	3	ON	ON	STEEP	SHALLOW	360
9	3	ON	ON	STEEP	SHALLOW	223
9	3	ON	ON	STEEP	SHALLOW	669
9	3	ON	ON	STEEP	SHALLOW	510
10	3	ON	ON	STEEP	STEEP	89
10	3	ON	ON	STEEP	STEEP	280
10	3	ON	ON	STEEP	STEEP	175
10	3	ON	ON	STEEP	STEEP	272
10	3	ON	ON	STEEP	STEEP	291

Table 23. Run-on times of each inverter in all multi-inverter anti-islanding tests

Step	Description	GSF config.	Circuit	Load location	Grid impedance	Inverter location map	ROT (ms)			
							Inv 1	Inv 2	Inv 3	Max
1	all on same transformer, all UG	1	1	near	median	1	108	229	199	229
1	all on same transformer, all UG	1	1	near	median	1	156	285	310	310
1	all on same transformer, all UG	1	1	near	median	1	157	194	207	207
1	all on same transformer, all UG	1	1	near	median	1	187	555	222	555
1	all on same transformer, all UG	1	1	near	median	1	126	184	166	184
1	all on same transformer, all OH	1	4	near	median	1	129	104	153	153
1	all on same transformer, all OH	1	4	near	median	1	328	281	325	328
1	all on same transformer, all OH	1	4	near	median	1	210	145	200	210
1	all on same transformer, all OH	1	4	near	median	1	356	312	365	365
1	all on same transformer, all OH	1	4	near	median	1	320	291	342	342
1	all on different transformers, all UG	1	5	near	median	1	167	372	224	372
1	all on different transformers, all UG	1	5	near	median	1	176	131	185	185
1	all on different transformers, all UG	1	5	near	median	1	203	411	252	411
1	all on different transformers, all UG	1	5	near	median	1	383	353	380	383
1	all on different transformers, all UG	1	5	near	median	1	129	183	181	183
1	all on different transformers, all OH	1	6	near	median	1	221	156	210	221
1	all on different transformers, all OH	1	6	near	median	1	209	417	350	417
1	all on different transformers, all OH	1	6	near	median	1	125	181	190	190
1	all on different transformers, all OH	1	6	near	median	1	205	134	192	205
1	all on different transformers, all OH	1	6	near	median	1	281	215	263	281
1	all on different transformers, 2 UG + 1 OH	1	2	near	median	1	300	494	403	494
1	all on different transformers, 2 UG + 1 OH	1	2	near	median	1	170	393	217	393
1	all on different transformers, 2 UG + 1 OH	1	2	near	median	1	183	370	218	370
1	all on different transformers, 2 UG + 1 OH	1	2	near	median	1	140	75	129	140
1	all on different transformers, 2 UG + 1 OH	1	2	near	median	1	219	154	202	219
1	all on different transformers, 2 OH + 1 UG	1	7	near	median	1	135	125	156	156
1	all on different transformers, 2 OH + 1 UG	1	7	near	median	1	226	448	311	448
1	all on different transformers, 2 OH + 1 UG	1	7	near	median	1	240	333	326	333
1	all on different transformers, 2 OH + 1 UG	1	7	near	median	1	255	187	147	255
1	all on different transformers, 2 OH + 1 UG	1	7	near	median	1	125	183	201	201
1	2 on 1 transformer, 1 on another, all UG	1	3	near	median	1	339	294	352	352
1	2 on 1 transformer, 1 on another, all UG	1	3	near	median	1	173	394	231	394
1	2 on 1 transformer, 1 on another, all UG	1	3	near	median	1	347	337	365	365
1	2 on 1 transformer, 1 on another, all UG	1	3	near	median	1	295	333	362	362
1	2 on 1 transformer, 1 on another, all UG	1	3	near	median	1	269	204	261	269
1	2 on 1 transformer, 1 on another, all OH	1	8	near	median	1	245	177	237	245
1	2 on 1 transformer, 1 on another, all OH	1	8	near	median	1	104	207	73	207
1	2 on 1 transformer, 1 on another, all OH	1	8	near	median	1	150	126	171	171
1	2 on 1 transformer, 1 on another, all OH	1	8	near	median	1	163	374	279	374
1	2 on 1 transformer, 1 on another, all OH	1	8	near	median	1	156	211	199	211
1	2 UG on 1 transformer, 1 OH on another	1	9	near	median	1	152	229	184	229
1	2 UG on 1 transformer, 1 OH on another	1	9	near	median	1	158	253	182	253
1	2 UG on 1 transformer, 1 OH on another	1	9	near	median	1	371	345	386	386
1	2 UG on 1 transformer, 1 OH on another	1	9	near	median	1	167	206	223	223
1	2 UG on 1 transformer, 1 OH on another	1	9	near	median	1	237	193	240	240
1	2 OH on 1 transformer, 1 UG on another	1	10	near	median	1	165	242	198	242
1	2 OH on 1 transformer, 1 UG on another	1	10	near	median	1	158	380	196	380
1	2 OH on 1 transformer, 1 UG on another	1	10	near	median	1	267	222	276	276
1	2 OH on 1 transformer, 1 UG on another	1	10	near	median	1	194	402	245	402
1	2 OH on 1 transformer, 1 UG on another	1	10	near	median	1	374	324	361	374
2	Load distributed	1	1	dist	median	1	211	115	205	211
2	Load distributed	1	1	dist	median	1	178	234	209	234
2	Load distributed	1	1	dist	median	1	249	186	244	249

Step	Description	GSF config.	Circuit	Load location	Grid impedance	Inverter location map	ROT (ms)			
							Inv 1	Inv 2	Inv 3	Max
2	Load distributed	1	1	dist	median	1	217	350	344	350
2	Load distributed	1	1	dist	median	1	233	170	212	233
2	Load far from inverters	1	1	far	median	1	241	176	232	241
2	Load far from inverters	1	1	far	median	1	206	280	311	311
2	Load far from inverters	1	1	far	median	1	221	105	156	221
2	Load far from inverters	1	1	far	median	1	127	82	135	135
2	Load far from inverters	1	1	far	median	1	146	202	170	202
2	Load near inverters	1	1	near	median	1	382	459	475	475
2	Load near inverters	1	1	near	median	1	139	130	165	165
2	Load near inverters	1	1	near	median	1	193	148	189	193
2	Load near inverters	1	1	near	median	1	132	155	178	178
2	Load near inverters	1	1	near	median	1	163	368	263	368
3	Minimum grid impedance	1	1	near	min	1	271	345	363	363
3	Minimum grid impedance	1	1	near	min	1	259	213	268	268
3	Minimum grid impedance	1	1	near	min	1	379	334	390	390
3	Minimum grid impedance	1	1	near	min	1	223	430	328	430
3	Minimum grid impedance	1	1	near	min	1	153	209	188	209
3	Median grid impedance	1	1	near	median	1	144	202	174	202
3	Median grid impedance	1	1	near	median	1	185	120	175	185
3	Median grid impedance	1	1	near	median	1	161	366	200	366
3	Median grid impedance	1	1	near	median	1	156	211	206	211
3	Median grid impedance	1	1	near	median	1	218	192	234	234
3	Maximum grid impedance	1	1	near	max	1	280	252	298	298
3	Maximum grid impedance	1	1	near	max	1	189	394	220	394
3	Maximum grid impedance	1	1	near	max	1	181	238	217	238
3	Maximum grid impedance	1	1	near	max	1	220	296	324	324
3	Maximum grid impedance	1	1	near	max	1	228	438	297	438
4	GSF setting 1, ckt 1, location map 1	1	1	near	max	1	234	133	198	234
4	GSF setting 1, ckt 1, location map 1	1	1	near	max	1	243	448	344	448
4	GSF setting 1, ckt 1, location map 1	1	1	near	max	1	358	483	443	483
4	GSF setting 1, ckt 1, location map 1	1	1	near	max	1	218	151	207	218
4	GSF setting 1, ckt 1, location map 2	1	1	near	max	2	233	188	230	233
4	GSF setting 1, ckt 1, location map 2	1	1	near	max	2	389	344	398	398
4	GSF setting 1, ckt 1, location map 2	1	1	near	max	2	211	416	296	416
4	GSF setting 1, ckt 1, location map 2	1	1	near	max	2	232	166	216	232
4	GSF setting 1, ckt 1, location map 3	1	1	near	max	3	294	248	305	305
4	GSF setting 1, ckt 1, location map 3	1	1	near	max	3	204	137	200	204
4	GSF setting 1, ckt 1, location map 3	1	1	near	max	3	277	214	268	277
4	GSF setting 1, ckt 1, location map 3	1	1	near	max	3	139	215	161	215
4	GSF setting 1, ckt 1, location map 4	1	1	near	max	4	322	258	313	322
4	GSF setting 1, ckt 1, location map 4	1	1	near	max	4	164	373	279	373
4	GSF setting 1, ckt 1, location map 4	1	1	near	max	4	342	278	311	342
4	GSF setting 1, ckt 1, location map 4	1	1	near	max	4	128	321	211	321
4	GSF setting 1, ckt 1, location map 5	1	1	near	max	5	287	243	300	300
4	GSF setting 1, ckt 1, location map 5	1	1	near	max	5	236	191	233	236
4	GSF setting 1, ckt 1, location map 5	1	1	near	max	5	205	410	262	410
4	GSF setting 1, ckt 1, location map 5	1	1	near	max	5	162	385	214	385
4	GSF setting 1, ckt 1, location map 6	1	1	near	max	6	349	307	346	349
4	GSF setting 1, ckt 1, location map 6	1	1	near	max	6	226	200	246	246
4	GSF setting 1, ckt 1, location map 6	1	1	near	max	6	199	422	262	422
4	GSF setting 1, ckt 1, location map 6	1	1	near	max	6	255	210	264	264
4	GSF setting 1, ckt 2, location map 1	1	2	near	max	1	329	432	344	432
4	GSF setting 1, ckt 2, location map 1	1	2	near	max	1	330	265	316	330
4	GSF setting 1, ckt 2, location map 1	1	2	near	max	1	155	213	179	213

Step	Description	GSF config.	Circuit	Load location	Grid impedance	Inverter location map	ROT (ms)			
							Inv 1	Inv 2	Inv 3	Max
4	GSF setting 1, ckt 2, location map 1	1	2	near	max	1	305	240	282	305
4	GSF setting 1, ckt 2, location map 2	1	2	near	max	2	131	170	163	170
4	GSF setting 1, ckt 2, location map 2	1	2	near	max	2	184	282	230	282
4	GSF setting 1, ckt 2, location map 2	1	2	near	max	2	227	162	213	227
4	GSF setting 1, ckt 2, location map 2	1	2	near	max	2	142	220	240	240
4	GSF setting 1, ckt 2, location map 3	1	2	near	max	3	170	160	196	196
4	GSF setting 1, ckt 2, location map 3	1	2	near	max	3	444	434	470	470
4	GSF setting 1, ckt 2, location map 3	1	2	near	max	3	351	303	368	368
4	GSF setting 1, ckt 2, location map 3	1	2	near	max	3	286	362	392	392
4	GSF setting 1, ckt 2, location map 4	1	2	near	max	4	195	95	161	195
4	GSF setting 1, ckt 2, location map 4	1	2	near	max	4	243	178	226	243
4	GSF setting 1, ckt 2, location map 4	1	2	near	max	4	393	368	390	393
4	GSF setting 1, ckt 2, location map 4	1	2	near	max	4	179	255	267	267
4	GSF setting 1, ckt 2, location map 5	1	2	near	max	5	183	390	304	390
4	GSF setting 1, ckt 2, location map 5	1	2	near	max	5	455	411	474	474
4	GSF setting 1, ckt 2, location map 5	1	2	near	max	5	255	190	246	255
4	GSF setting 1, ckt 2, location map 5	1	2	near	max	5	213	113	180	213
4	GSF setting 1, ckt 2, location map 6	1	2	near	max	6	269	204	256	269
4	GSF setting 1, ckt 2, location map 6	1	2	near	max	6	330	265	326	330
4	GSF setting 1, ckt 2, location map 6	1	2	near	max	6	403	374	414	414
4	GSF setting 1, ckt 2, location map 6	1	2	near	max	6	226	181	245	245
4	GSF setting 1, ckt 3, location map 1	1	3	near	max	1	177	383	199	383
4	GSF setting 1, ckt 3, location map 1	1	3	near	max	1	162	386	248	386
4	GSF setting 1, ckt 3, location map 1	1	3	near	max	1	200	405	287	405
4	GSF setting 1, ckt 3, location map 1	1	3	near	max	1	264	219	269	269
4	GSF setting 1, ckt 3, location map 2	1	3	near	max	2	230	164	212	230
4	GSF setting 1, ckt 3, location map 2	1	3	near	max	2	319	254	305	319
4	GSF setting 1, ckt 3, location map 2	1	3	near	max	2	257	314	338	338
4	GSF setting 1, ckt 3, location map 2	1	3	near	max	2	203	409	313	409
4	GSF setting 1, ckt 3, location map 3	1	3	near	max	3	126	223	157	223
4	GSF setting 1, ckt 3, location map 3	1	3	near	max	3	226	336	298	336
4	GSF setting 1, ckt 3, location map 3	1	3	near	max	3	284	219	274	284
4	GSF setting 1, ckt 3, location map 3	1	3	near	max	3	175	230	207	230
4	GSF setting 1, ckt 3, location map 4	1	3	near	max	4	140	163	172	172
4	GSF setting 1, ckt 3, location map 4	1	3	near	max	4	193	417	232	417
4	GSF setting 1, ckt 3, location map 4	1	3	near	max	4	235	170	220	235
4	GSF setting 1, ckt 3, location map 4	1	3	near	max	4	404	360	413	413
4	GSF setting 1, ckt 3, location map 5	1	3	near	max	5	239	194	258	258
4	GSF setting 1, ckt 3, location map 5	1	3	near	max	5	208	415	302	415
4	GSF setting 1, ckt 3, location map 5	1	3	near	max	5	200	100	175	200
4	GSF setting 1, ckt 3, location map 5	1	3	near	max	5	205	159	217	217
4	GSF setting 1, ckt 3, location map 6	1	3	near	max	6	350	304	337	350
4	GSF setting 1, ckt 3, location map 6	1	3	near	max	6	213	168	217	217
4	GSF setting 1, ckt 3, location map 6	1	3	near	max	6	148	203	193	203
4	GSF setting 1, ckt 3, location map 6	1	3	near	max	6	231	186	248	248
4	GSF setting 2, ckt 1, location map 1	2	1	near	max	1	282	238	289	289
4	GSF setting 2, ckt 1, location map 1	2	1	near	max	1	156	235	255	255
4	GSF setting 2, ckt 1, location map 1	**2**	1	**near**	max	1	**605**	**560**	**611**	611
4	GSF setting 2, ckt 1, location map 1	2	1	near	max	1	180	135	190	190
4	GSF setting 2, ckt 1, location map 2	2	1	near	max	2	286	223	270	286
4	GSF setting 2, ckt 1, location map 2	**2**	1	**near**	max	2	**134**	**342**	**159**	342
4	GSF setting 2, ckt 1, location map 2	2	1	near	max	2	411	348	395	411
4	GSF setting 2, ckt 1, location map 2	2	1	near	max	2	372	326	370	372
4	GSF setting 2, ckt 1, location map 3	**2**	1	**near**	max	3	**134**	**326**	**159**	326

Step	Description	GSF config.	Circuit	Load location	Grid impedance	Inverter location map	ROT (ms)			
							Inv 1	Inv 2	Inv 3	Max
4	GSF setting 2, ckt 1, location map 3	2	1	near	max	3	145	188	199	199
4	GSF setting 2, ckt 1, location map 3	2	1	near	max	3	242	197	250	250
4	GSF setting 2, ckt 1, location map 3	2	1	near	max	3	425	362	417	425
4	GSF setting 2, ckt 1, location map 4	2	1	near	max	4	275	212	264	275
4	GSF setting 2, ckt 1, location map 4	2	1	near	max	4	196	131	188	196
4	GSF setting 2, ckt 1, location map 4	2	1	near	max	4	135	342	265	342
4	GSF setting 2, ckt 1, location map 4	2	1	near	max	4	240	177	229	240
4	GSF setting 2, ckt 1, location map 5	2	1	near	max	5	304	239	281	304
4	GSF setting 2, ckt 1, location map 5	2	1	near	max	5	120	163	173	173
4	GSF setting 2, ckt 1, location map 5	2	1	near	max	5	150	357	273	357
4	GSF setting 2, ckt 1, location map 5	2	1	near	max	5	304	260	315	315
4	GSF setting 2, ckt 1, location map 6	2	1	near	max	6	342	298	345	345
4	GSF setting 2, ckt 1, location map 6	2	1	near	max	6	397	353	400	400
4	GSF setting 2, ckt 1, location map 6	2	1	near	max	6	247	184	227	247
4	GSF setting 2, ckt 1, location map 6	2	1	near	max	6	247	183	239	247
4	GSF setting 2, ckt 2, location map 1	2	2	near	max	1	616	572	627	627
4	GSF setting 2, ckt 2, location map 1	2	2	near	max	1	316	252	305	316
4	GSF setting 2, ckt 2, location map 1	2	2	near	max	1	404	359	405	405
4	GSF setting 2, ckt 2, location map 1	2	2	near	max	1	336	290	338	338
4	GSF setting 2, ckt 2, location map 2	2	2	near	max	2	190	396	300	396
4	GSF setting 2, ckt 2, location map 2	2	2	near	max	2	226	163	205	226
4	GSF setting 2, ckt 2, location map 2	2	2	near	max	2	262	200	251	262
4	GSF setting 2, ckt 2, location map 2	2	2	near	max	2	158	366	187	366
4	GSF setting 2, ckt 2, location map 3	2	2	near	max	3	126	333	260	333
4	GSF setting 2, ckt 2, location map 3	2	2	near	max	3	254	190	237	254
4	GSF setting 2, ckt 2, location map 3	2	2	near	max	3	241	177	227	241
4	GSF setting 2, ckt 2, location map 3	2	2	near	max	3	160	370	286	370
4	GSF setting 2, ckt 2, location map 4	2	2	near	max	4	346	282	338	346
4	GSF setting 2, ckt 2, location map 4	2	2	near	max	4	217	154	210	217
4	GSF setting 2, ckt 2, location map 4	2	2	near	max	4	355	291	347	355
4	GSF setting 2, ckt 2, location map 4	2	2	near	max	4	205	140	185	205
4	GSF setting 2, ckt 2, location map 5	2	2	near	max	5	140	331	165	331
4	GSF setting 2, ckt 2, location map 5	2	2	near	max	5	202	246	263	263
4	GSF setting 2, ckt 2, location map 5	2	2	near	max	5	184	86	174	184
4	GSF setting 2, ckt 2, location map 5	2	2	near	max	5	184	227	253	253
4	GSF setting 2, ckt 2, location map 6	2	2	near	max	6	151	360	267	360
4	GSF setting 2, ckt 2, location map 6	2	2	near	max	6	439	374	428	439
4	GSF setting 2, ckt 2, location map 6	2	2	near	max	6	199	85	179	199
4	GSF setting 2, ckt 2, location map 6	2	2	near	max	6	233	171	228	233
4	GSF setting 2, ckt 3, location map 1	**2**	3	**near**	max	1	**148**	**356**	**274**	356
4	GSF setting 2, ckt 3, location map 1	**2**	3	**near**	max	1	**148**	**355**	**258**	355
4	GSF setting 2, ckt 3, location map 1	2	3	near	max	1	148	230	171	230
4	GSF setting 2, ckt 3, location map 1	2	3	near	max	1	303	239	284	303
4	GSF setting 2, ckt 3, location map 2	2	3	near	max	2	139	346	264	346
4	GSF setting 2, ckt 3, location map 2	**2**	3	**near**	max	2	**506**	**516**	**538**	538
4	GSF setting 2, ckt 3, location map 2	**2**	3	**near**	max	2	**529**	**464**	**511**	529
4	GSF setting 2, ckt 3, location map 2	**2**	3	**near**	max	2	**530**	**467**	**518**	530
4	GSF setting 2, ckt 3, location map 3	2	3	near	max	3	150	356	184	356
4	GSF setting 2, ckt 3, location map 3	2	3	near	max	3	172	76	151	172
4	GSF setting 2, ckt 3, location map 3	2	3	near	max	3	412	404	429	429
4	GSF setting 2, ckt 3, location map 3	2	3	near	max	3	390	401	405	405
4	GSF setting 2, ckt 3, location map 4	2	3	near	max	4	478	414	464	478
4	GSF setting 2, ckt 3, location map 4	2	3	near	max	4	261	197	241	261
4	GSF setting 2, ckt 3, location map 4	2	3	near	max	4	157	217	225	225

Step	Description	GSF config.	Circuit	Load location	Grid impedance	Inverter location map	ROT (ms)			
							Inv 1	Inv 2	Inv 3	Max
4	GSF setting 2, ckt 3, location map 4	**2**	3	**near**	max	4	**558**	**533**	**581**	581
4	GSF setting 2, ckt 3, location map 5	2	3	near	max	5	269	205	247	269
4	GSF setting 2, ckt 3, location map 5	2	3	near	max	5	197	82	178	197
4	GSF setting 2, ckt 3, location map 5	2	3	near	max	5	365	303	343	365
4	GSF setting 2, ckt 3, location map 5	2	3	near	max	5	247	202	259	259
4	GSF setting 2, ckt 3, location map 6	2	3	near	max	6	137	344	272	344
4	GSF setting 2, ckt 3, location map 6	2	3	near	max	6	136	327	218	327
4	GSF setting 2, ckt 3, location map 6	2	3	near	max	6	145	352	264	352
4	GSF setting 2, ckt 3, location map 6	2	3	near	max	6	240	176	231	240
Extra	GSF setting 2, ckt 2, loc 1, timed disconnect	2	2	near	max	1	183	392	306	392
Extra	GSF setting 2, ckt 2, loc 1, timed disconnect	2	2	near	max	1	244	181	237	244
Extra	GSF setting 2, ckt 2, loc 1, timed disconnect	2	2	near	max	1	428	365	410	428
Extra	GSF setting 2, ckt 2, loc 1, timed disconnect	2	2	near	max	1	248	455	379	455
Extra	GSF setting 2, ckt 2, loc 1, timed disconnect	2	2	near	max	1	311	246	294	311
Extra	GSF setting 2, ckt 2, loc 1, random disconnect	2	2	near	max	1	196	97	171	196
Extra	GSF setting 2, ckt 2, loc 1, random disconnect	2	2	near	max	1	167	140	184	184
Extra	GSF setting 2, ckt 2, loc 1, random disconnect	2	2	near	max	1	116	200	146	200
Extra	GSF setting 2, ckt 2, loc 1, random disconnect	2	2	near	max	1	632	550	612	632
Extra	GSF setting 2, ckt 2, loc 1, random disconnect	2	2	near	max	1	99	144	120	144
RL load	GSF setting 2, ckt 2, loc 1, tuned RL load	2	2	near	max	1	342	230	299	342
RL load	GSF setting 2, ckt 2, loc 1, tuned RL load	2	2	near	max	1	221	397	269	397
RL load	GSF setting 2, ckt 2, loc 1, tuned RL load	2	2	near	max	1	119	277	163	277
RL load	GSF setting 2, ckt 2, loc 1, tuned RL load	2	2	near	max	1	111	178	129	178
RL load	GSF setting 2, ckt 2, loc 1, tuned RL load	2	2	near	max	1	113	291	139	291
RL load	GSF setting 2, ckt 2, loc 1, de-tuned RL load	2	2	near	max	1	159	187	187	187
RL load	GSF setting 2, ckt 2, loc 1, de-tuned RL load	2	2	near	max	1	86	112	116	116
RL load	GSF setting 2, ckt 2, loc 1, de-tuned RL load	2	2	near	max	1	134	311	148	311
RL load	GSF setting 2, ckt 2, loc 1, de-tuned RL load	2	2	near	max	1	160	167	175	175
RL load	GSF setting 2, ckt 2, loc 1, de-tuned RL load	2	2	near	max	1	297	372	314	372