Stress Intensity of Delamination in a Sintered-Silver Interconnection

Preprint

D. J. DeVoto and P. P. Paret
National Renewable Energy Laboratory

A. A. Wereszczak
Oak Ridge National Laboratory

Presented at IMAPS/HiTEC
Albuquerque, New Mexico
May 13–15, 2014

NREL is a national laboratory of the U.S. Department of Energy
Office of Energy Efficiency & Renewable Energy
Operated by the Alliance for Sustainable Energy, LLC

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications.

Conference Paper
NREL/CP-5400-61598
August 2014

Contract No. DE-AC36-08GO28308

NOTICE

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications.

Available electronically at http://www.osti.gov/scitech

Available for a processing fee to U.S. Department of Energy and its contractors, in paper, from:

U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831-0062
phone: 865.576.8401
fax: 865.576.5728
email: mailto:reports@adonis.osti.gov

Available for sale to the public, in paper, from:

U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Road
Springfield, VA 22161
phone: 800.553.6847
fax: 703.605.6900
email: orders@ntis.fedworld.gov
online ordering: http://www.ntis.gov/help/ordermethods.aspx

Cover Photos: (left to right) photo by Pat Corkery, NREL 16416, photo from SunEdison, NREL 17423, photo by Pat Corkery, NREL 16560, photo by Dennis Schroeder, NREL 17613, photo by Dean Armstrong, NREL 17436, photo by Pat Corkery, NREL 17721.

Stress Intensity of Delamination in a Sintered-Silver Interconnection

D. J. DeVoto,[*] P. P. Paret,[*] and A. A. Wereszczak[§]

[*] Transportation and Hydrogen Systems Center, Phone: 303-275-4256, Email: Douglas.DeVoto@nrel.gov
National Renewable Energy Laboratory, Golden, CO 80401
[§] Materials and Science Technology Division, Oak Ridge National Laboratory, Oak Ridge, TN 37831

Abstract

In automotive power electronics packages, conventional thermal interface materials such as greases, gels, and phase-change materials pose bottlenecks to heat removal and are also associated with reliability concerns. The industry trend is toward high thermal performance bonded interfaces for large-area attachments. However, because of coefficient of thermal expansion mismatches between materials/layers and resultant thermomechanical stresses, adhesive and cohesive fractures could occur, posing a reliability problem. These defects manifest themselves in increased thermal resistance. This research aims to investigate and improve the thermal performance and reliability of sintered-silver for power electronics packaging applications. This has been experimentally accomplished by the synthesis of large-area bonded interfaces between metalized substrates and copper base plates that have subsequently been subjected to thermal cycles. A finite element model of crack initiation and propagation in these bonded interfaces will allow for the interpretation of degradation rates by a crack-velocity (V)-stress intensity factor (K) analysis. A description of the experiment and the modeling approach are discussed.

Key words: bonded interfaces, sintered-silver, reliability, delamination, stress intensity

Introduction

In a power electronics module, a semiconductor chip/die is typically attached by a bonded interface material (BIM), such as solder, to a metalized substrate. Beneath this die attach layer, the substrate is commonly composed of a ceramic bounded by Cu layers on either side and provides electrical isolation. This substrate is then mounted onto a base plate or directly to a heat exchanger, typically made of Cu or Al, via a large-area BIM. A cross-section of a typical power electronics package is shown in Fig. 1.

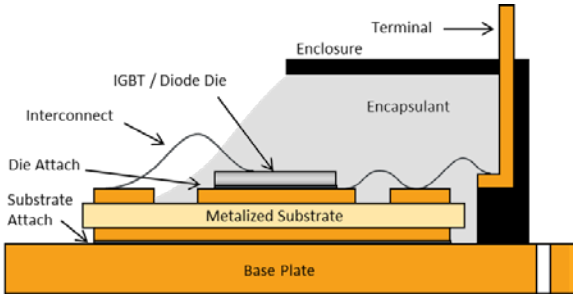

Figure 1. Traditional power electronics package.

A coefficient of thermal expansion (CTE) mismatch between the ceramic substrate and the Cu base plate, when paired with any temperature change, will impose stress that can cause defect initiation and propagation in the joining solder layer if the magnitude of that stress is sufficiently high. Lead-based solders had predominantly been used in the electronics packaging industry; however, the Restriction of Hazardous Substances Directive [1] mandated lead-free solutions. Initially, the industry focused on various Sn, Ag, and Cu (SAC) compositions as a suitable lead-free alternative, with Innolot ($SnAg_{3.8}Cu_{0.7}Bi_{3.0}Sb_{1.4}Ni_{0.2}$) proving to be a promising solution [2–3]. Research found that varying the composition of the Ag and Cu content in the SAC solders would help minimize creep strain. Despite these advances, the reliability under temperature cycling continues to be a concern with lead-free solders. The transition to wide-bandgap devices and higher junction temperatures also places packaging constraints on power electronics designs where temperatures would exceed reflow temperatures of many commonly used solder alloys.

To provide greater thermomechanical reliability under temperature cycling and to allow for higher temperature applications, sintered-silver material has been proposed as an alternative solution in power electronics packages [4–8]. However, to reduce synthesis temperatures to below 300°C, the concurrent application of pressure up to 40 MPa onto the package or sintered-silver BIM was originally advocated. However, this caused a higher complexity in the production process and more

stringent flatness specifications for the substrates. Recently, several manufacturers have developed sintered-silver materials that require lower or even no bonding pressures.

Because large-area BIMs are promising [9–12], work has focused on assessing their thermal performance and reliability. Conclusions on thermal performance and reliability from the present effort are intended to directly assist incorporation of these materials into automotive power electronics designs. This paper focuses on sintered-silver based on micrometer-sized Ag particles, and $Sn_{63}Pb_{37}$ solder as a baseline. The sample synthesis, characterization plan, experimental results, and interface modeling are described below.

Sample Synthesis

The assembly consisted of a 5-mm-thick Cu base plate attached to a 0.72-mm-thick active metal bonded substrate (0.32-mm-thick silicon nitride [Si_3N_4] with 0.2-mm-thick Cu foil on either side of Si_3N_4, 50.8 mm × 50.8 mm cross-sectional area footprint) via the bonding material. The Cu metallization layers were inset 1 mm from the perimeter of the Si_3N_4, for a 48.8 mm × 48.8 mm footprint, and the corners were given a radius of 2 mm to minimize stress intensities. Before assembly, the Cu metallization layers in the substrate were plated with 4 µm of electroless Ni-P, 1 µm of Pd, and 0.3 µm of Ag to improve adhesion with the bonding material. The Cu base plate was electroplated with 5 µm of Ag. An assembled sample is shown in Fig. 2.

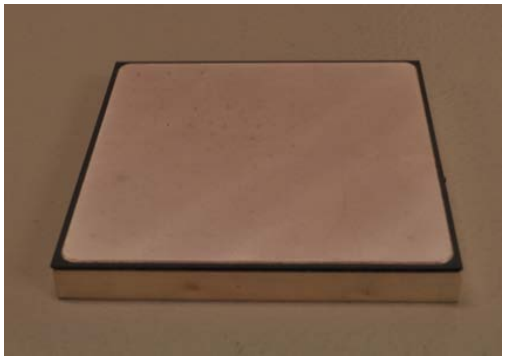

Figure 2. Representative metalized substrate/base plate assembly for sintered-silver and $Sn_{63}Pb_{37}$ solder.

Bonded interfaces based on sintered-silver particles were synthesized by Semikron (Nürnberg, Germany). Corners of the Si_3N_4 substrate were rounded off to match the 2-mm radius of the Cu metallization layers. The sample assembly was placed in a hot press and raised to its processing temperature, after which pressure was applied. Specifics of the sintering temperature and schedule and bonding pressure were not provided by Semikron.

As a baseline, a $Sn_{63}Pb_{37}$ bond was also synthesized between the substrate/base plate assembly. A 127-µm-thick stainless steel stencil with a five-by-five opening array (9-mm × 9-mm square openings with 1-mm separation) was used to apply solder evenly to the substrate and base plate surfaces. After the solder was applied, the assembled sample was placed in a vacuum solder reflow oven. The reflow profile ensured that flux was removed from the bond and that voiding remained less than 2%.

Initial Material Characterization

Degradation (e.g., cracks, voids, and delaminations) of the bonded interface can be non-destructively detected by scanning acoustic microscopy. After defect initiation, the thermal and electrical performance of the sample assembly degrades. A C-mode scanning acoustic microscope (C-SAM) measured the initial bonding condition of the samples and then subsequently tested their interfaces every 100 thermal cycles. Images showing the bonded interface within samples before accelerated thermal testing are shown in Fig. 3. The circular bands visible in each sample are artifacts of the C-SAM representing top surface curvatures as 2-D images and are not indicators of bond quality. The $Sn_{63}Pb_{37}$ solder and sintered-silver both exhibited uniform bonds between the base plate and substrate samples.

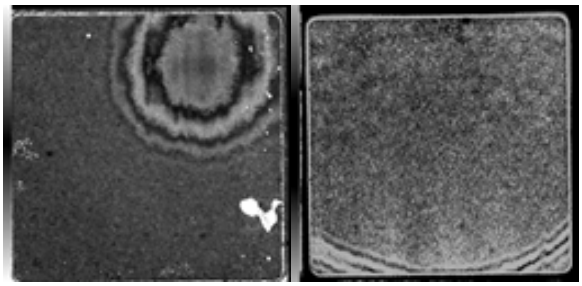

Figure 3. C-SAM images showing initial bond quality in $Sn_{63}Pb_{37}$ solder (left) and sintered-silver (right).

In addition to acoustic microscopy, the electrical resistance of the Si_3N_4 insulation layer was measured. In a high potential (hipot) test, a high

voltage is applied to an electronic device's current-carrying components. The quality of the insulation in the device is determined by measuring the presence of a leakage current. Leakage current indicates that dielectric breakdown in the insulation layer has occurred [13]. A dielectric resistance tester was previously constructed based on the hipot testing process to detect when a crack in the Si_3N_4 has developed. A custom fixture contacts the top and bottom sides of a test sample, and a test voltage of 2.0 kV is applied for 20 seconds, which is sufficient voltage to cause an arc in the air through a defect or crack in the 0.32-mm-thick Si_3N_4 layer. Measurement of the leakage current from an arc indicates that damage occurred within the Si_3N_4 layer in the sample. The sample successfully passes the test if no current was measured over the analysis period. The results correlated with acoustic microscopy images, indicating that all initial samples exhibited no defects within the Si_3N_4 layer.

Deformation of the samples occurred as a consequence of their elevated temperature processing. Residual stresses, which arose due to CTE mismatches of the bonded constituents, combined with the sample's geometry, and their cool-down to ambient temperature caused this deformation. These stresses can be sufficient to cause crack initiation and propagation within the Si_3N_4, leading to failure of the layer's electrical insulating properties. Representative CTE parameters for materials common within a power electronics package and examples of package deformation conditions are shown in Fig. 4. As a package cools from its strain-free temperature, the Cu base plate's higher CTE relative to the substrate and silicon die causes it to contract more and induce a bow into the package.

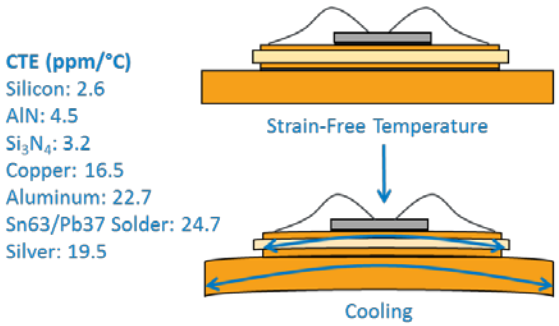

Figure 4. Power electronics package deformation caused by CTE mismatch under cooling and heating conditions.

The high pressure and temperature synthesis requirements for sintered-silver did not cause crack initiation within the Si_3N_4 substrate; however, package deformation was evident when samples were at room temperature. A laser profilometer was used to scan the top and bottom surfaces of sintered-silver samples for accurate measurements of these deformations. Fig. 5 shows the top surface profile of one sintered-silver sample as well as a cross-section profile between two of the sample's corners. The maximum height variation across the sample was 166 µm. Surface profile measurements were also taken for $Sn_{63}Pb_{37}$ solder samples, but no significant permanent deflection was found.

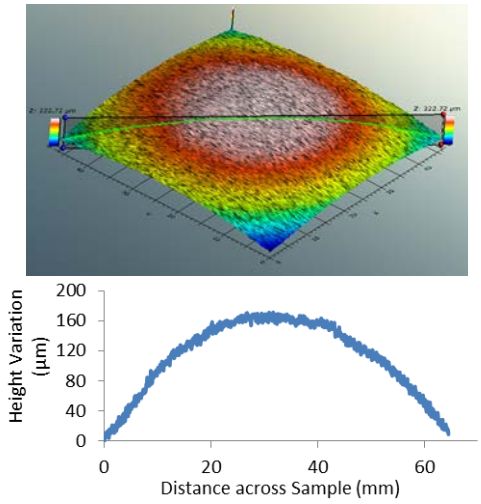

Figure 5. Surface profile of sintered-silver sample at room temperature.

Thermal Cycling

After initial characterization of the test samples, conditions were applied to create thermally induced stresses, leading to cracking, voiding, or delamination failures. Samples were cycled between –40°C and 150°C, a common temperature range for electronics testing, to evaluate the quality of the bonded interfaces [14–17]. A dwell period of 10 minutes at the maximum and minimum temperatures was chosen to promote solder fatigue and creep [17]. Ramp rates for thermal cycling must be sufficiently low to avoid transient thermal gradients in the test samples; therefore, ramp rates were in the 5°C/min range. Each sample was planned to be cycled up to 2,500 thermal cycles, or until degradation propagated to sufficient levels to separate the substrate from the base plate.

BIM Response to Thermal Cycling

A failure is defined here by any of the following: a crack in the Si_3N_4 substrate, a cohesive fracture within the BIM, or an adhesive/interfacial fracture between the BIM and either the substrate or base plate surface. A crack in the Si_3N_4 substrate could indicate loss of electrical insulation capabilities and the sample would immediately be considered failed. Cohesive or adhesive/interfacial fractures in the BIM would increase the thermal resistance of the power electronics package, eventually creating a thermal bottleneck that would elevate the operating temperature of a die above its maximum limit. For testing purposes, a fracture leading to 20% area delamination of the BIM is defined as a failure.

$Sn_{63}Pb_{37}$ solder samples were subjected to 1,500 thermal cycles. C-SAM images showed progressively increasing delamination up to 1,500 cycles, indicating a relatively poor performance of the large-area BIM (Fig. 6). Light-shaded regions in the acoustic images indicate a void or defect while dark regions denote an intact bond.

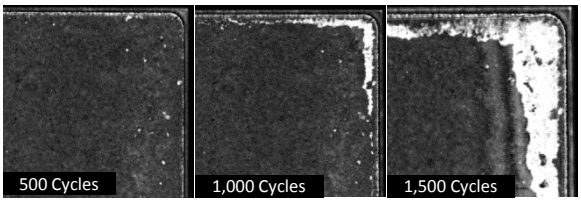

Figure 6. C-SAM images of $Sn_{63}Pb_{37}$ solder material after select number of thermal cycles.

Sintered-silver samples completed 2,500 temperature cycles and delamination rates were comparatively lower than $Sn_{63}Pb_{37}$ solder samples. This is observed in acoustic images of a corner region of the sintered-silver material after 1,000 temperature cycles, 1,500 cycles, and 2,500 cycles, as shown in Fig. 7.

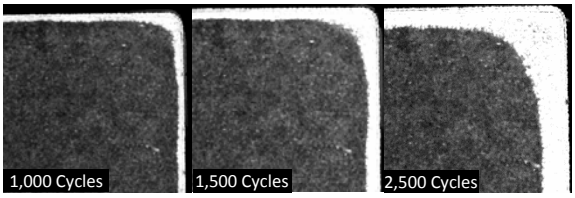

Figure 7. C-SAM images of sintered-silver material after select number of thermal cycles.

Measurements of the delamination percentage within the sintered-silver BIM were taken every 100 cycles from C-SAM imaging. Depending on the sample, this perimeter fracturing increased to 19%–32% of initial 48.8 mm × 48.8 mm bonded area after undergoing 2,500 temperature cycles, as shown in Fig. 8. Under these specific bonding and temperature cycling conditions, the sintered-silver samples remained defect free until approximately 300 cycles. A period of transient rate delamination occurred after defect initiation until approximately 1,000 cycles, after which a constant rate delamination was observed to the conclusion of temperature cycling at 2,500 cycles.

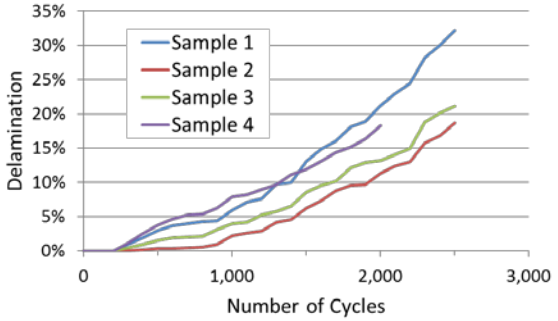

Figure 8. Perimeter delamination of sintered-silver BIM as a function of number of thermal cycles.

The fourth sample was cross-sectioned and the bonded interface layer was imaged after 2,000 temperature cycles. The delamination observed in acoustic microscope images was the result of fracturing (i.e., cohesive failure) within the sintered-silver material. The cohesive fracturing is shown in Fig. 9. After 2,500 cycles, additional cross-sectioning and imaging confirmed that cohesive fracturing occurred in the remaining three sintered-silver samples.

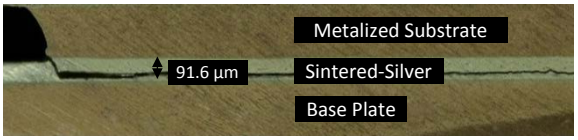

Figure 9. Cohesive fracture of the sintered-silver BIM after 2,000 temperature cycles.

The delamination percentage was calculated for the sintered-silver BIM and compared with the $Sn_{63}Pb_{37}$ solder material. After 1,500 cycles, cohesive fracturing within the solder material reached 21%–24% delamination, and observed delamination rates were higher in the solder samples than in sintered-silver samples. Delamination rates of both interface materials are shown in Fig. 10.

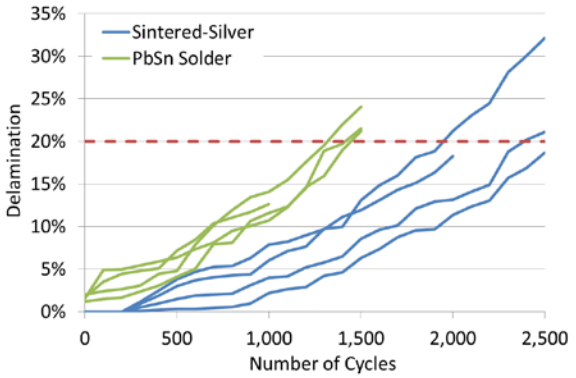

Figure 10. Perimeter delamination of sintered-silver and $Sn_{63}Pb_{37}$ solder as a function of number of thermal cycles.

Crack growth rates within the sintered-silver BIM were also determined as a function of number of thermal cycles. Three characteristic crack growth rate regions were consistently observed, as with the delamination percentage. Delamination distance from the original corner in each quadrant for sample four is shown in Fig. 11. No delamination occurred within the first few hundred cycles in any of the samples. Immediately after initiation, a region of transient increase in percent delaminated area then occurred for the next few hundred cycles. Lastly, a constant or increasing rate of percent delamination occurred for the remainder of the testing.

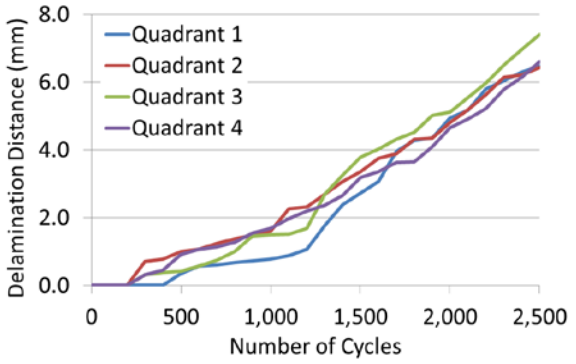

Figure 11. Delamination distance of sintered-silver BIM as a function of number of thermal cycles, or da/dN curves.

The observation of three such regions is consistent with those observed with the damage tolerant criterion (da/dN vs. K or ΔK) for fatigue [18] whose crack initiation and growth behavior is analyzed in context to fracture mechanics. One such technique involves the study of crack growth rates (da/dN) or crack velocity (V) as a function of stress intensity factor (K). K is analytic for simple crack shapes and loading scenarios but can be obtained from three-dimensional finite element analysis (FEA) for more complicated shapes and loadings. Stress intensity factor is a parameter that determines the intensity of the stresses in the crack tip region. Extensive crack initiation and propagation modeling will be conducted to obtain stress intensity factors, which will then be plotted against crack velocities to obtain a V-K curve. A typical V-K curve is shown in Fig. 12.

Another supporting reason to consider such a V-K response for illustrating delamination response of sintered-silver interconnects is the cracking response in Fig. 9 is consistent with cracking in a linearly elastic material. Conversely, delamination in a ductile or plastically deforming material, such as that that can occur in a solder, is better suited for representation by viscoplastic models such as Anand's.

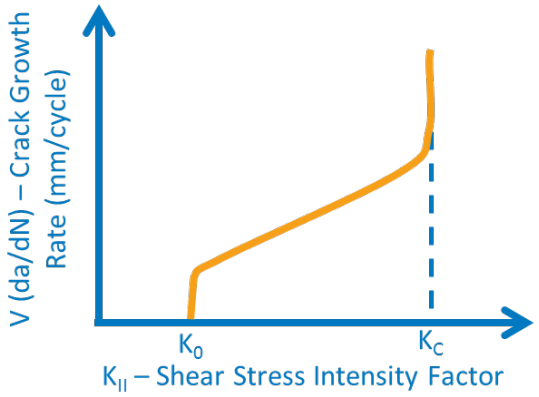

Figure 12. A typical V-K curve.

Modeling

The observation of cohesive fracture within sintered-silver BIM means that the tracked ingress front of the delamination (captured with C-SAM) can be linked to their modeled stress intensity factor (which depends on the size and shape of the interface at any given time instant) to construct and interpret the V-K response of this particular sintered-silver material. While this study's interpretation may be specific to the employed sintered-silver to substrate-baseplate system, this analysis method could provide a logical way to interpret such damage in interfaces whose material has sustained linear elasticity. An identified V-K curve is important because it affords the possibility to pre-determine

what sizes and shapes of sintered-silver interfaces can be used without causing delamination, and this has positive implications for future reliability improvement with power electronic devices where the bonding of a relatively large area is sought.

The main objective of the computational modeling approach in this work is to calculate the values of stress intensity factor using FEA at various points along crack growth in sintered-silver BIMs. Stress intensity factor values will then be correlated with the crack velocities calculated from C-SAM images of delaminated sintered-silver. A three-dimensional linear elastic fracture mechanics based crack initiation and propagation model of the sample shown in Fig. 2 with sintered-silver interface will be developed to get the desired outputs.

An accurate set of material properties for sintered-silver is required for the crack initiation and propagation models. Material characterization tests at various temperatures are being planned on a different set of samples to extract stress-strain curves of sintered-silver from which properties, such as elastic modulus, can be calculated. A parameter of interest is the amount of residual stress on the samples that would undergo material characterization tests. Sintering temperature is usually between 250-300°C depending on the commercial paste used, and as the temperature drops down to room temperature, residual stresses are formed due to the CTE mismatch within the sample.

A parametric study was conducted using FEA to optimize the sintered-silver geometry in the samples so as to keep residual stresses to a minimum. An ANSYS Parametric Design Language (APDL) code was developed that included model pre-processing, solver, and post-processing stages. The model geometry consists of a sintered-silver layer of 10 mm diameter bonded between two 12.7-mm x 12.7-mm DBC alumina substrates. The thickness of substrate was 1.2 mm and for sintered-silver, 25-µm and 50-µm thickness variations were considered. A quarter symmetry of the package was utilized in the modeling to save computational space and time, shown in Fig. 13.

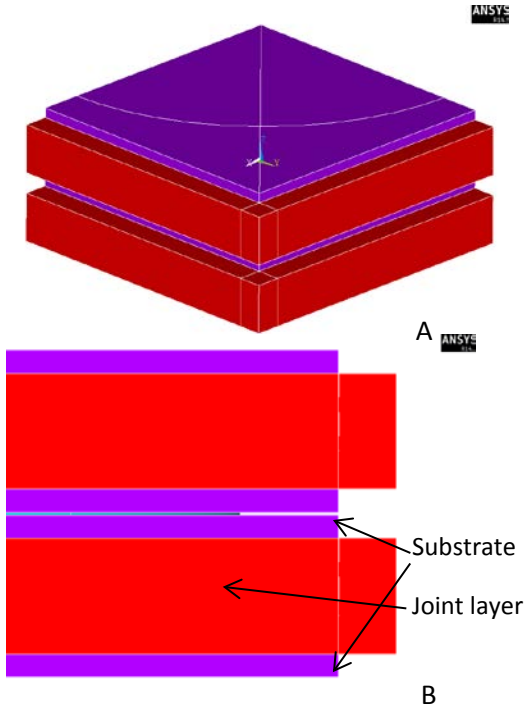

Figure 13. Quarter symmetry model (A) and layers in the sample (B).

Material properties were obtained from literature for the simulation [19] to explore general trends within the sintered-silver interface. After the geometry was constructed and material properties at room temperature applied, the model was meshed using SOLID185 hexahedral elements. Increased mesh density was achieved at the sintered-silver interface layer through meshing operations such as edge sizing and element sizing.

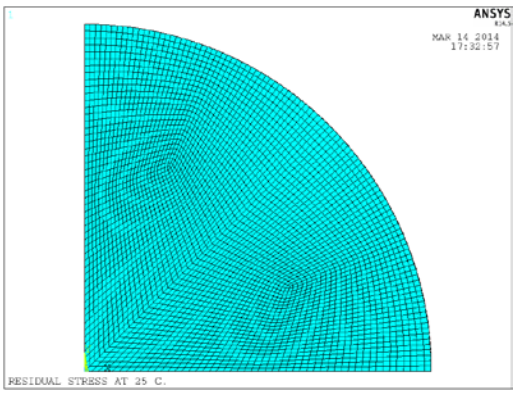

Figure 14. Sintered-silver joint (top-view).

A total of six linear elastic simulations were performed incorporating variations in thickness and diameter of the sintered-silver joint. A contour plot

of the von-Mises stresses in the sintered-silver interface layer is displayed in Fig. 15. Results from the simulations are shown in Table 1.

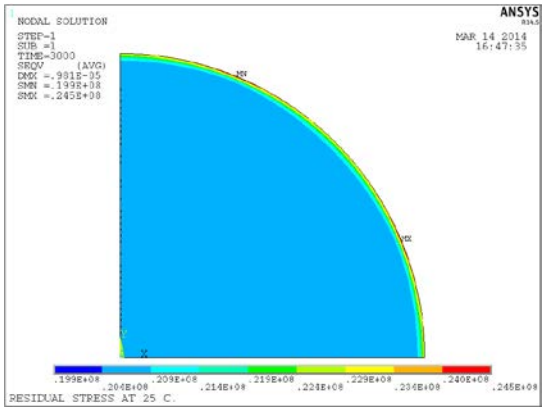

Figure 15. von-Mises stresses in the sintered-silver interconnect layer.

Table 1. von-Mises stress (maximum).

Thickness (µm)	Diameter (mm)	von-Mises Stress (MPa)
25	10	24.5
25	9	24.9
25	8	25.5
25	7	26.1
25	6	26.8
50	10	27.5

From the above results, it becomes clear that stresses increase with decrease in diameter of the sintered-silver joint for the same substrate size. Also, it increases with thickness of the joint. Based on these results, a joint thickness of 25 µm and diameter 10 mm will be chosen for the material characterization test samples.

Conclusion

A consistent framework has been implemented to establish the thermal performance and reliability of large-area bonded interfaces based on sintered-silver materials as compared to $Sn_{63}Pb_{37}$ solder. These large-area attachments are currently being considered in state-of-the-art power electronics packages for electric-drive vehicle applications. Results for bond quality after thermal cycling suggest that sintered-silver could be a promising alternative to solders. Perimeter fracturing within sintered-silver test samples increased to 19%–32% of initial bonded area after undergoing 2,500 temperature cycles. Future work will focus on capturing stress-strain data for the selected sintered-silver material, and developing a crack initiation and propagation model to obtain stress intensity factor values. These values will be plotted against crack velocities to obtain a V-K curve. Additionally, a second round of test samples with sintered-silver BIM of different geometry will be made and subjected to accelerated tests, and crack propagation rates will be analyzed from C-SAM images. Based on this information, techniques to minimize the occurrence of cohesive fracturing by optimizing processing conditions will be evaluated.

Acknowledgments

The authors would like to acknowledge the support provided by Susan Rogers and Steven Boyd, Technology Development Managers for Advanced Power Electronics and Electric Motors Program, Vehicle Technologies Office, U.S. Department of Energy Office of Energy Efficiency and Renewable Energy. The authors would also like to acknowledge Christian Goebl, Semikron, for providing the sintered-silver bonded samples.

References

[1] Official Journal of the European Union, 2003, “Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment.” February 13, 2003.

[2] Dudek, R., Faust, W., Ratchev, R., Roellig, M., Albrecht, H., Michel, B., 2008, “Thermal Test- and Field Cycling Induced Degradation and its FE-based Prediction for Different SAC Solders,” *Proceedings of the ITHERM Conference*, Orlando, FL, May 28–31, 2008, pp. 668–675.

[3] Wang, Q., Johnson, W., Ma, H., Gale, W. F., Lindahl, D., 2005, “Properties of Lead Free Solder Alloys as a Function of Composition Variation,” *Electronic Circuits World Convention (ECWC 10),* Anaheim, CA, February 22–24, 2005.

[4] Klaka, S., Sittig, R., 1994, “Reduction of Thermomechanical Stress by Applying a Low Temperature Joining Technique,” *Proceedings of the 6th International Symposium Power Semiconductor Devices & ICs,* Davos, Switzerland, 1994, pp. 259-264.

[5] Schulze, E., Mertens, C., Lindemann, A., 2009, "Low Temperature Joining Technique – a Solution for Automotive Power Electronics,"

Power Conversion, Intelligent Motion (PCIM), Nuremberg, Germany, May 12–14, 2009.

[6] Lu, G-Q., Zhao, M., Lei, G., Calata, J. N., Chen, X., Luo, S., 2009, "Emerging Lead-Free, High-Temperature Die-Attach Technology Enabled by Low-Temperature Sintering of Nanoscale Silver Pastes," *International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP)*, Beijing, China, August 10–13, 2009, pp. 461–466.

[7] Schulze, E., Mertens, C., Lindemann, A., 2010, "Pure Low Temperature Joining Technique Power Module for Automotive Production Needs*," 6th International Conference on Integrated Power Electronics Systems (CIPS),* Nuremberg, Germany, March 16–18, 2010.

[8] Wereszczak, A. A., Liang, Z., Ferber, M. K., Marlino, L. D., 2014, "Uniqueness and Challenges of Sintered Silver as a Bonded Interface Material," International Conference on High Temperature Electronics (HiTEC), Albuquerque, NM, 2014.

[9] Chuang, R. W., Lee, C. C., 2002, "Silver-Indium Joints Produced at Low Temperature for High Temperature Devices," *IEEE Transactions on Components and Packaging Technologies*, Vol. 25, No. 3, pp. 453–458.

[10] McCluskey, P., Quintero, P. O., 2007, "High Temperature Lead-Free Attach Reliability," *Proceedings of InterPACK, IPACK2007-33457*, Vancouver, British Columbia, Canada, July 8–12, 2007.

[11] Wu, R., McCluskey, F. P., 2007, "Reliability of Indium Solder for Cold Temperature Packaging," *Proceedings of InterPACK, IPACK2007-31456,* Vancouver, British Columbia, Canada, July 8–12, 2007.

[12] Lei, T. G., Calata, J. N., Lu, G-Q., Chen, X., Luo, S., 2010, "Low-Temperature Sintering of Nanoscale Silver Paste for Attaching Large-Area (>100 mm^2) Chips," *IEEE Transactions on Components and Packaging Technology*, Vol. 33, No. 1, pp. 98–104.

[13] Associated Research, Inc., 2011, "Exploring the Necessity of the Hot Hipot Test," http://www.asresearch.com/events-training/pdfs/HotHipot.pdf, Accessed May 2011.

[14] JEDEC Solid State Technology Association, 2009, "JESD22-A104D Temperature Cycling."

[15] Vandevelde, B., Gonzalez, M., Limaye, P., Ratchev, P., Beyne, E., 2007, "Thermal Cycling Reliability of SnAgCu and SnPb Solder Joints: A Comparison for Several IC-Packages," *Microelectronics Reliability*, Vol. 47, pp. 259–265.

[16] Aoki, Y., Tsujie, I., Nagai, T., 2007, "The Effect of Ramp Rate on Temperature Cycle Fatigue in Solder Joints," *Espec Technology Report,* pp. 4–13.

[17] Lu, G-Q., Calata, J. N., Lei, G., Chen, X., 2007, "Low-Temperature and Pressureless Sintering Technology for High-Performance and High-Temperature Interconnection of Semiconductor Devices," *International Conference on Thermal, Mechanical and Multi-Physics Simulation Experiments in Microelectronics and Micro-Systems (EuroSime),* London, Great Britain, April 16–18, 2007, pp. 1–5.

[18] Cameron, D. W., Hoeppner, D. W., "ASM Handbook Volume 19, Fatigue and Fracture," ASM International, Materials Park, OH, pp. 15-26, 1996

[19] Chen, Xu., Li, Rong., Qi, Kun., Lu, Guo-Quan., 2008, "Tensile Behaviors and Ratcheting Effects of Partially Sintered-Chip Attachment Films of a Nanoscale Silver Paste," *Journal of Electronic Materials,* Vol. 37, No. 10.