

Performance and Reliability of Bonded Interfaces for High-Temperature Packaging



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Annual Merit Review and Peer Evaluation Meeting

June 17, 2014

Washington, D.C.
PR-5400-61357

Project ID: APE063

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Overview

Timeline

- **Project Start Date:** FY14
- **Project End Date:** FY16
- **Percent Complete:** 10%

Budget

- **Total Project Funding:**
 - DOE Share: \$500K
- **Funding for FY14:** \$500K

Barriers and Targets

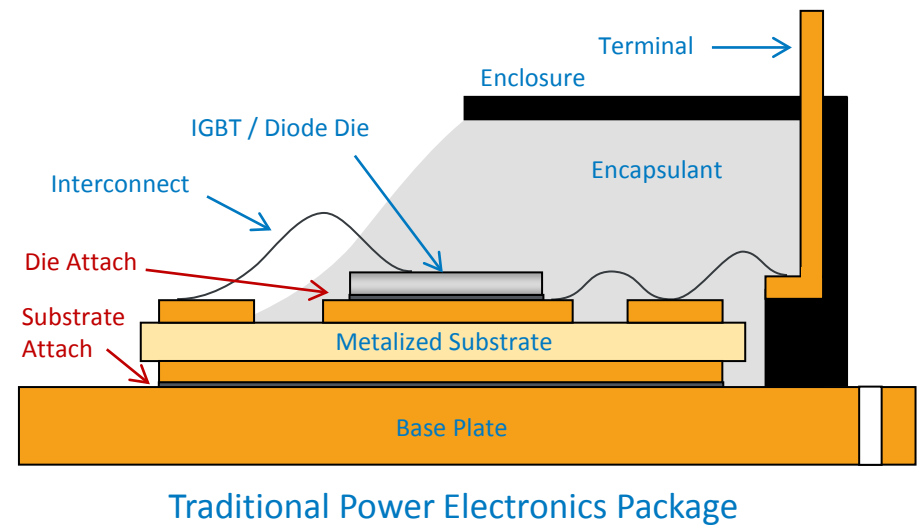
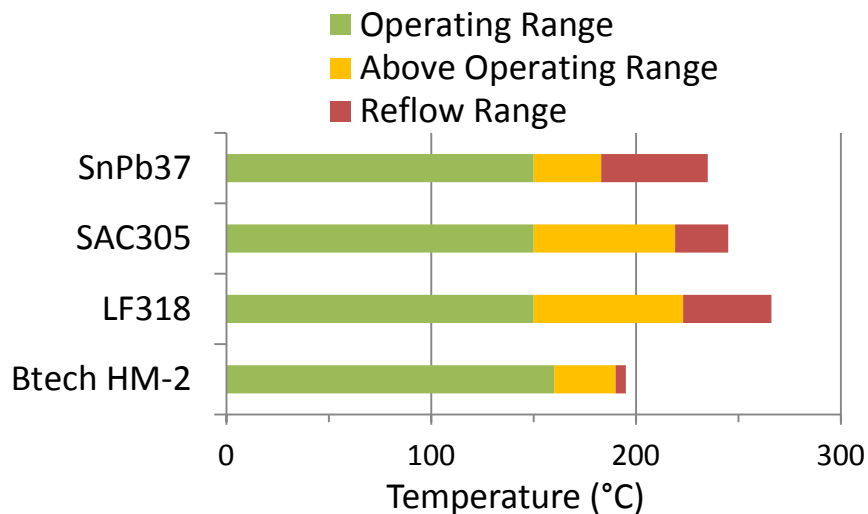
- Cost
- Weight
- Performance and Lifetime

Partners

- Interactions / Collaborations
 - Heraeus, Henkel, General Motors, Oak Ridge National Laboratory (ORNL) (Andrew Wereszczak)
- Project Lead
 - National Renewable Energy Laboratory (NREL)

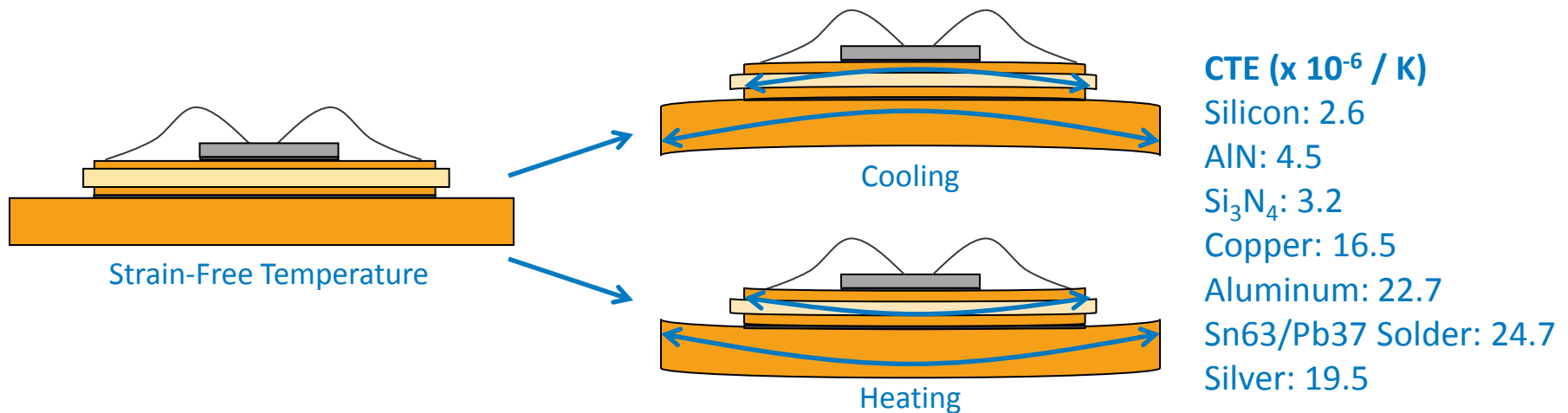
Relevance

- Current automotive power electronics are transitioning from silicon to wide bandgap (WBG) devices to meet cost, volume, and weight targets.
- Packaging designs must improve to take advantage of WBG devices' higher junction temperatures (>200°C).
- Current bonded interface materials (BIMs) do not meet packaging requirements:
 - Continuously operate above 200°C
 - Meet RoHS standards (lead-free)
 - Exhibit thermal fatigue resistance
 - Provide high thermal conductivity.



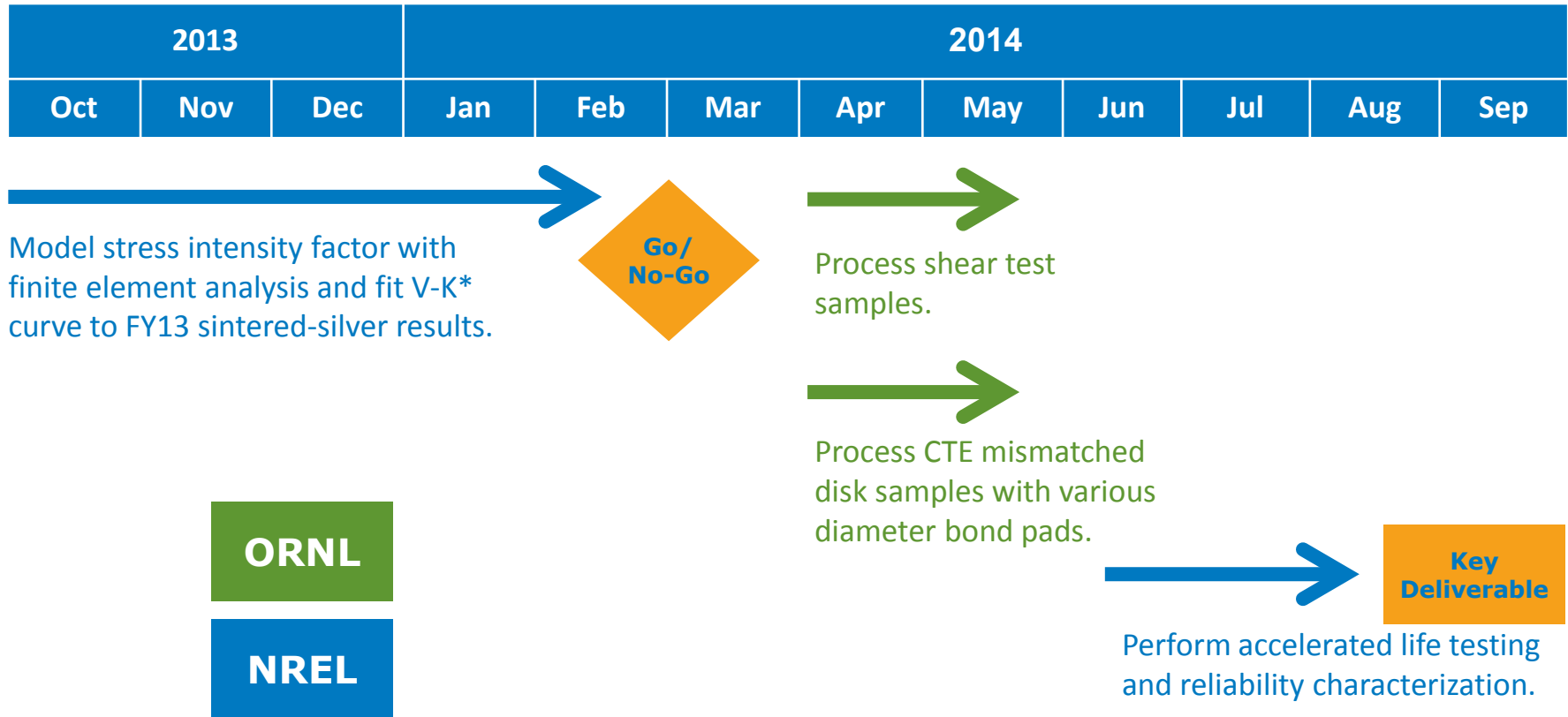
Relevance

- As operating temperatures increase, the coefficient of thermal expansion (CTE) mismatch between the substrate and the base plate causes delamination initiation and propagation in the joining layer.



- Sintered-silver reliability has not been documented at 200°C conditions for the substrate attach layer.
 - ORNL and NREL's prior experience with sintered-silver processing will generate recommended practices for synthesis of reliable interfaces.

Milestones



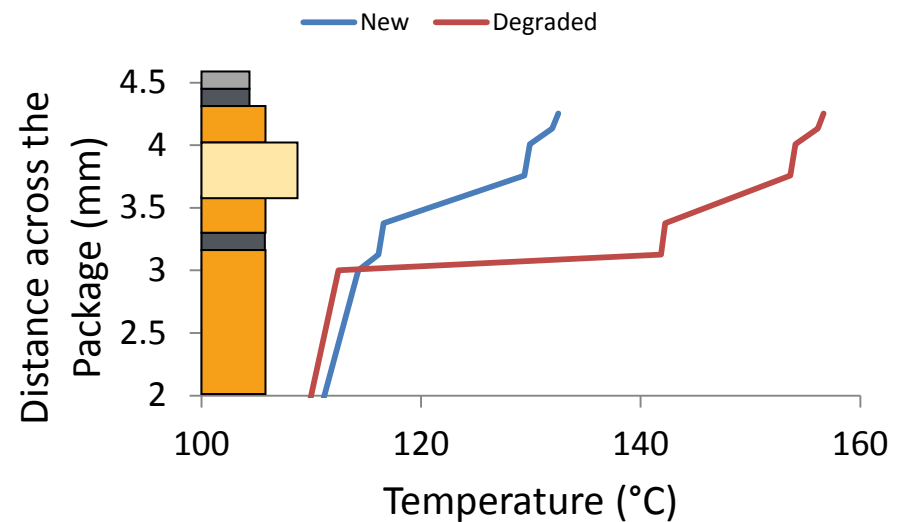
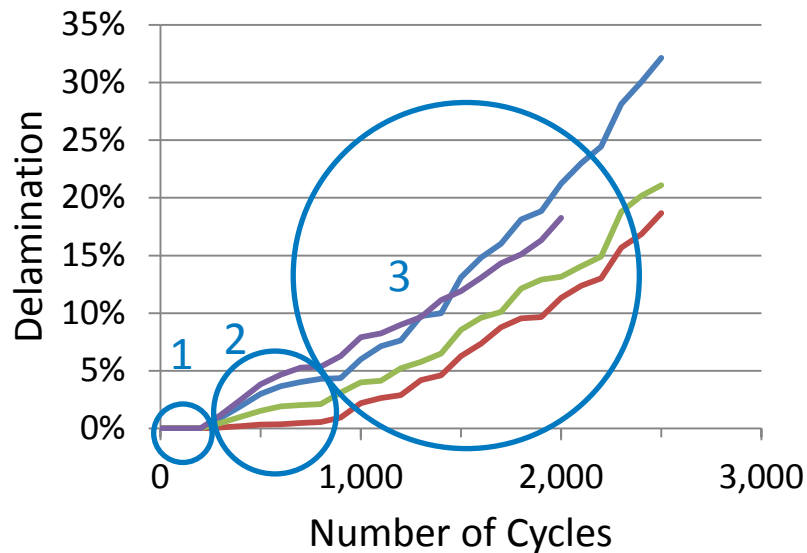
Go/No-Go: Can threshold before delamination initiates be defined?

Key Deliverable: Publish delamination initiation findings for sintered-silver.

*V= da/dN, Crack Growth Rate, (mm/cycle) – K = Stress Intensity Factor

Strategy

- Subject samples to shear tests for development of stress-strain curves.
- Focus on optimizing and understanding key synthesis parameters for sintered-silver.
 1. Identify threshold at which stress intensity factors are sufficient to cause delamination initiation.
 2. Evaluate the crack region where a transient delamination rate occurs.
 3. Evaluate the crack region where a constant-slope delamination rate occurs.
- Develop stronger experimental correlation between interface patterning/ degradation and junction temperature rise.



Strategy

- Synthesize and shear test initial samples for mechanical characterization of sintered-silver.
 - Attempt to measure residual stress at room temperature.
 - Estimate stress-strain curves.
 - Use information to model plastic deformation.
- Sintered-silver is bonded between two direct bond copper substrates.

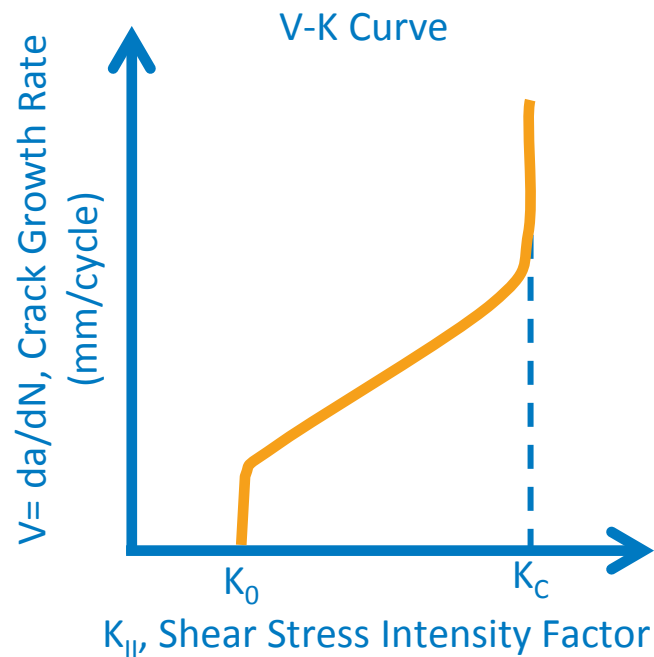


- Process CTE-mismatched disk samples with various diameter bond pads to validate stress intensity factor relationship with delamination initiation.
 - The stress intensity factor is a function of the loading amount, deformation mode, and the region of interest relative to the crack tip deformation.
 - Crack tip deformation can propagate through three modes:
 - Tension
 - Shear
 - Tearing.



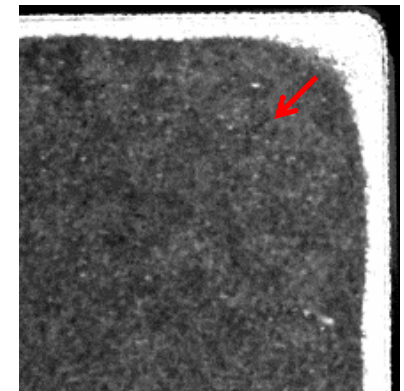
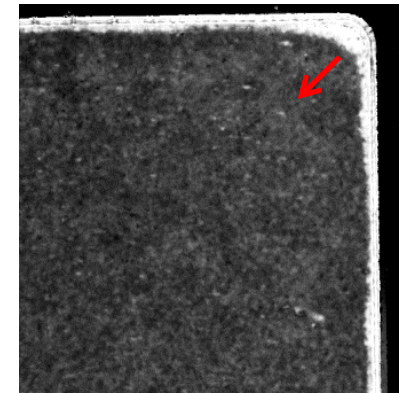
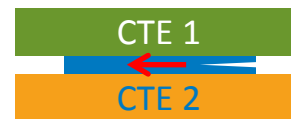
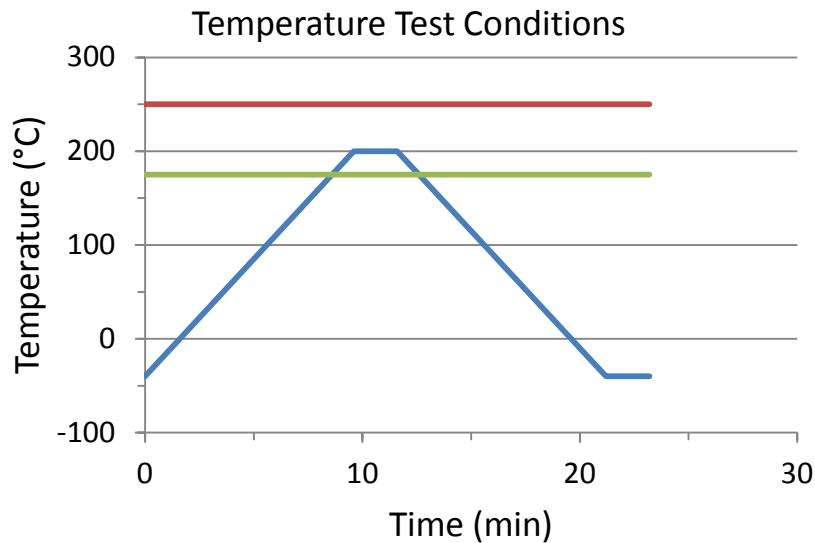
Strategy

- Identify threshold at which stress intensity factor is sufficient to cause delamination initiation.
 - Model stress intensity factor with finite element analysis and correlate with FY13 sintered-silver results.
 - Fit V-K curve to FY13 sintered-silver results.



Strategy

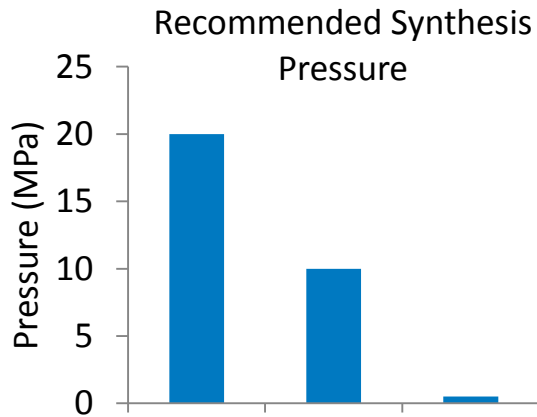
- Subject samples to accelerated temperature testing:
 - -40°C to 200°C thermal shock
 - 175°C and 250°C temperature elevation.
- Monitor delamination rates through acoustic microscopy.



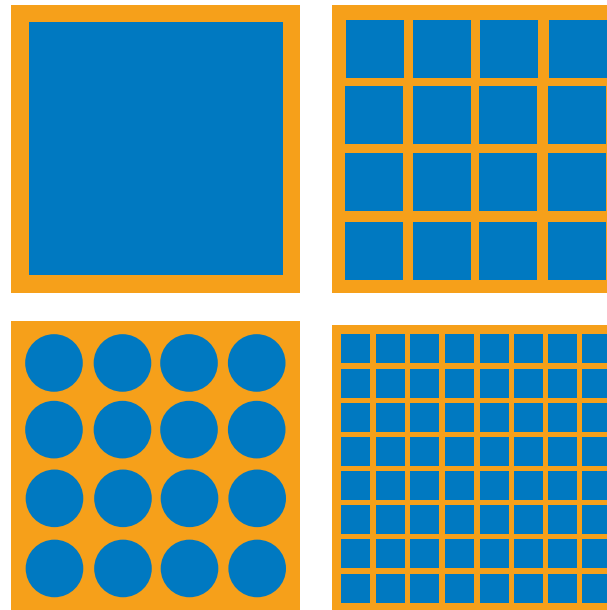
Strategy

- Evaluate the delamination rate of sintered-silver test coupons under various pressure requirements, bond areas, pad geometries, and surface-plating materials.

Evaluate low- and no-pressure sintered-silver materials.

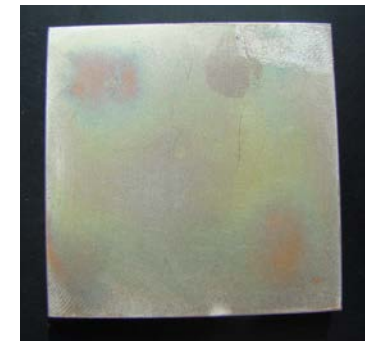


Optimize pad geometries for a large-area bond pad.



Recommend industry standard practices for plating.

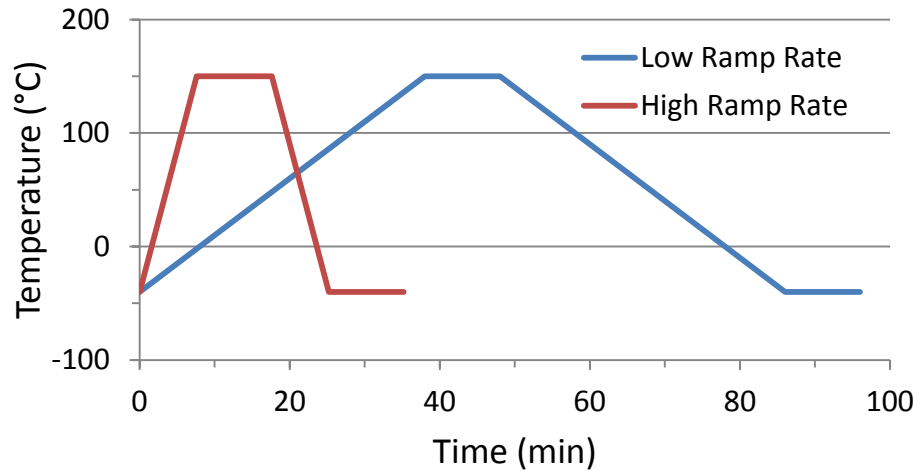
Plating Material	Ag, Au
Cleaning	None, substrate cleaning, pre-oxidation



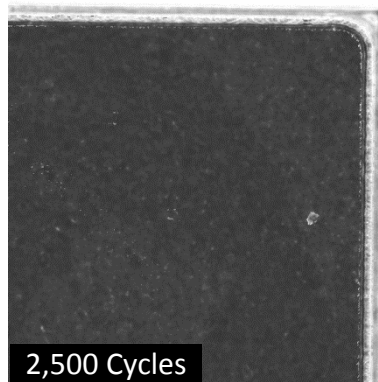
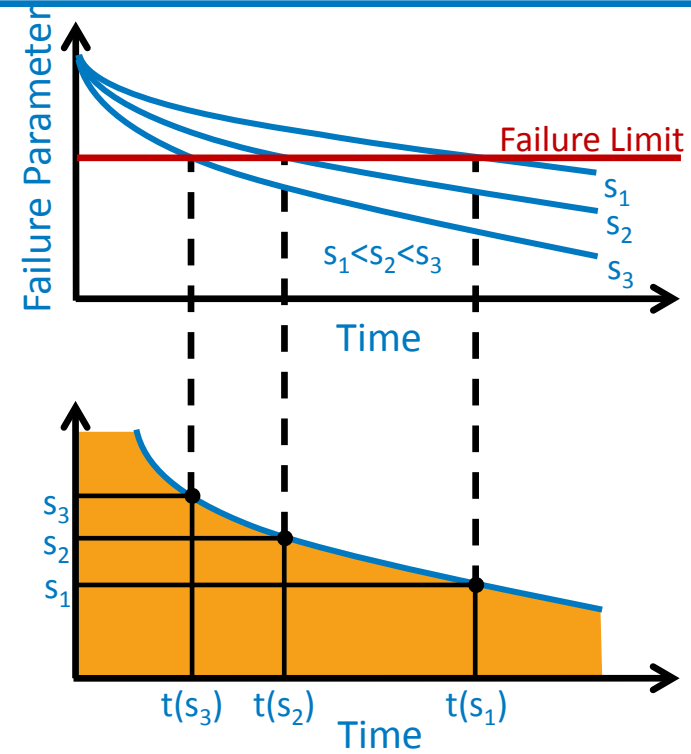
Poor Ag Plating

Prior Temperature Cycling

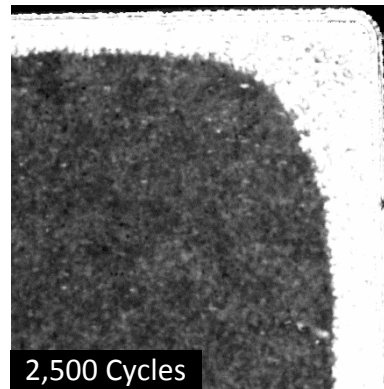
Temperature Test Conditions



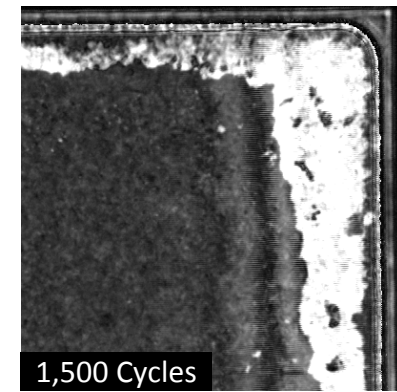
- Thermoplastic film embedded with carbon fibers, sintered-silver, and Sn63/Pb37 solder were subjected to accelerated thermal cycling.



Thermoplastic



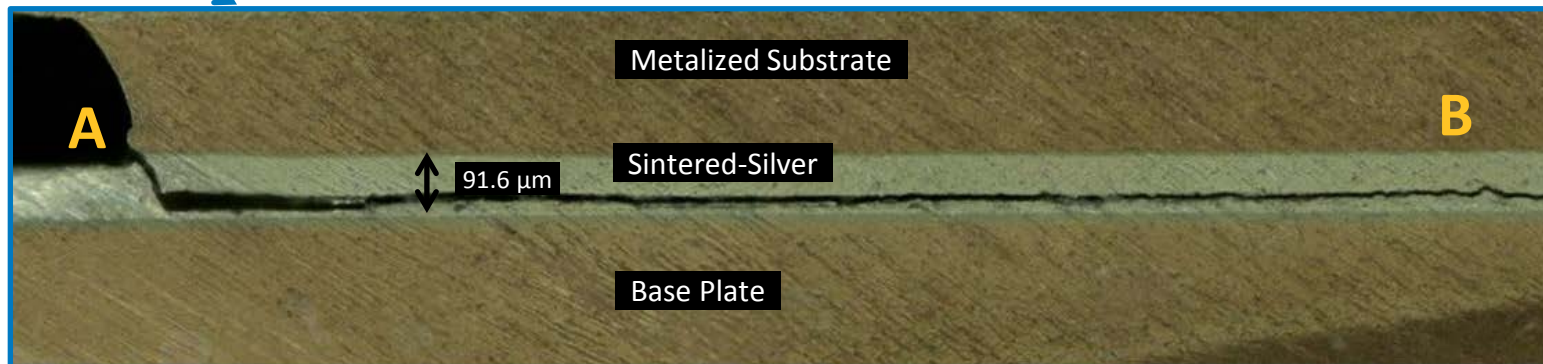
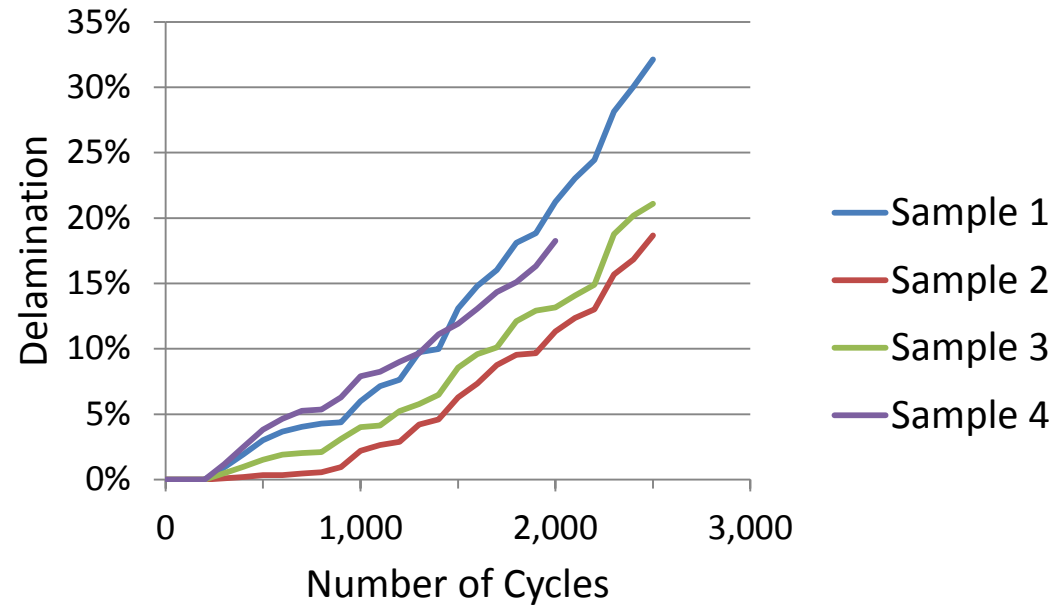
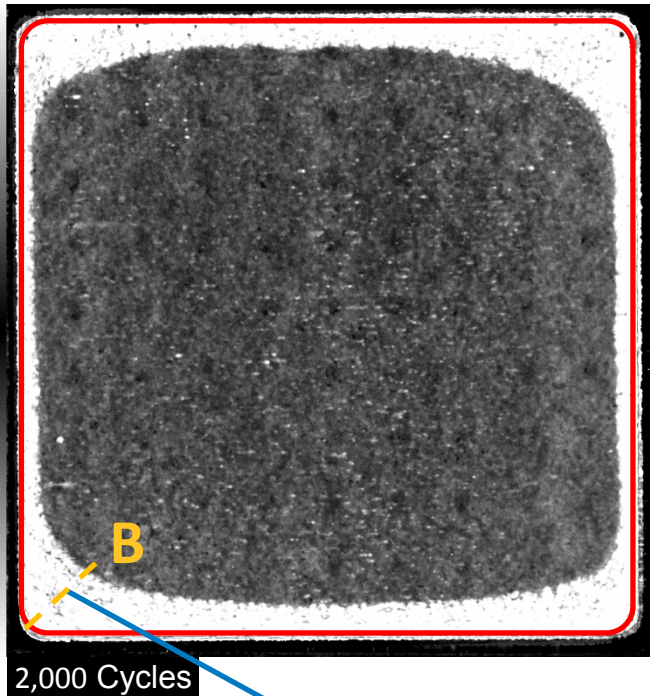
Sintered-Silver



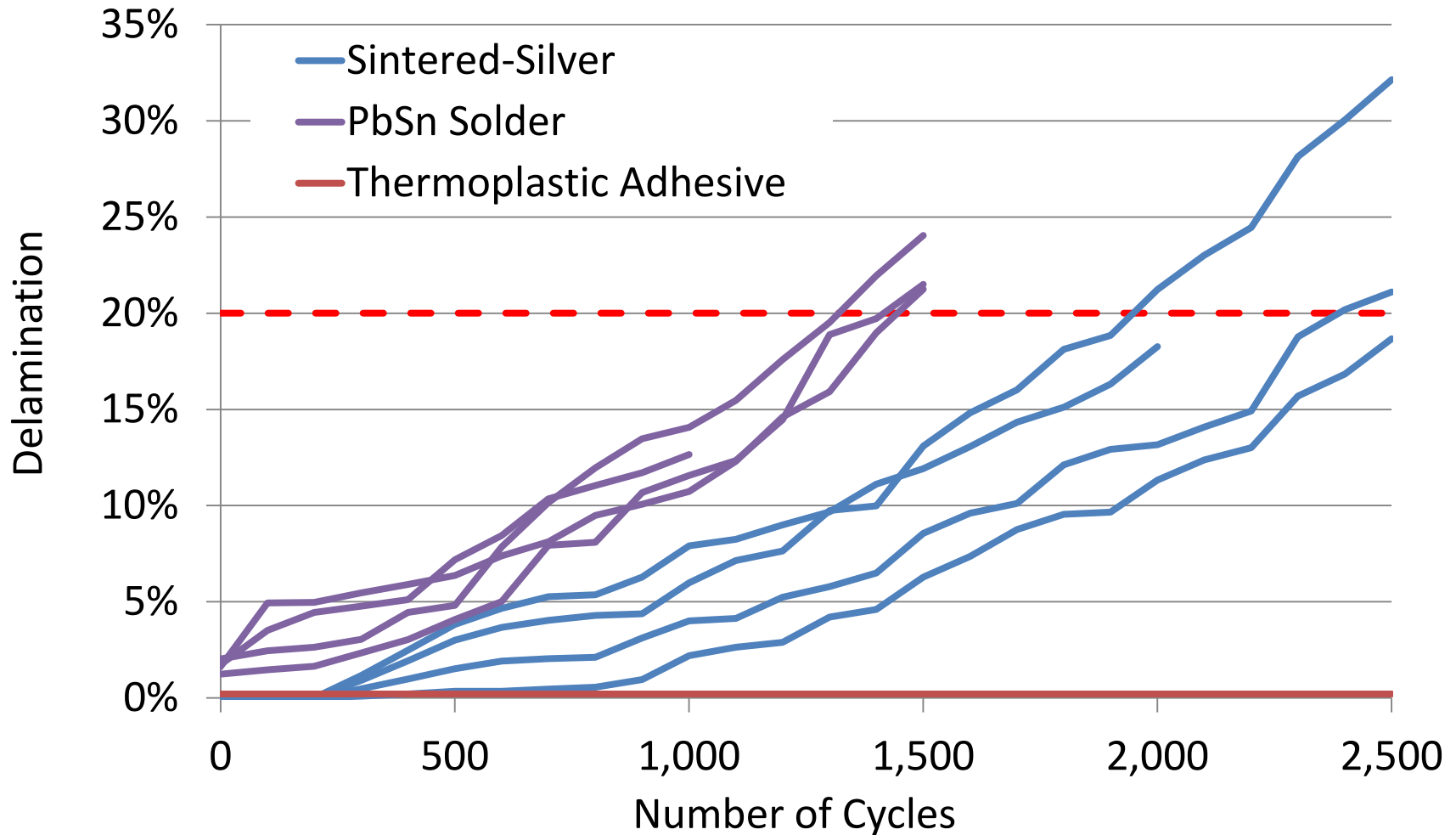
Solder

Sintered-Silver Evaluation

- After 2,500 thermal cycles, perimeter fracturing reached 19% to 32%.



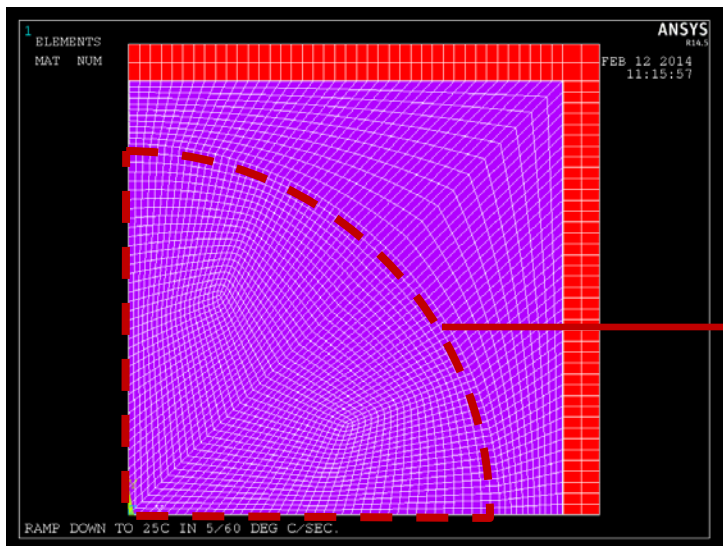
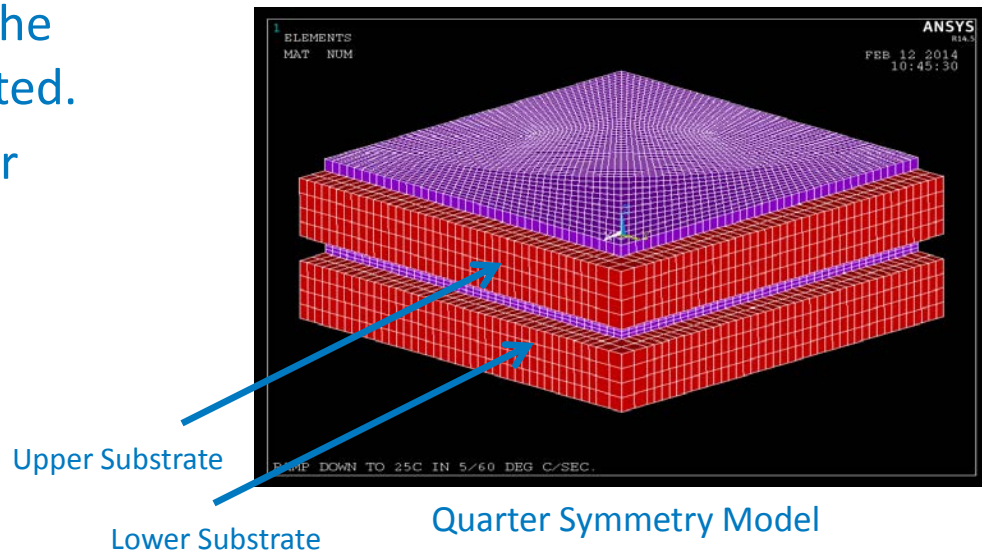
BIM Degradation Summary



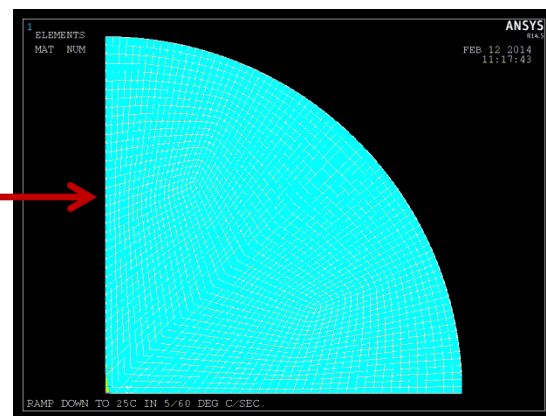
DeVoto, D., Paret, P., Narumanchi, S., Mihalic, M., 2013, "Reliability of Bonded Interfaces for Automotive Power Electronics," InterPACK2013-73143, Proceedings of the 2013 InterPACK Conference, July 2013, Burlingame, CA.

Interface Modeling

- A quarter symmetry model of the substrate test sample was created.
- Material parameters for a linear elastic analysis were applied to various layers of the model.
- Temperature is first raised to 275°C, then lowered to room temperature.



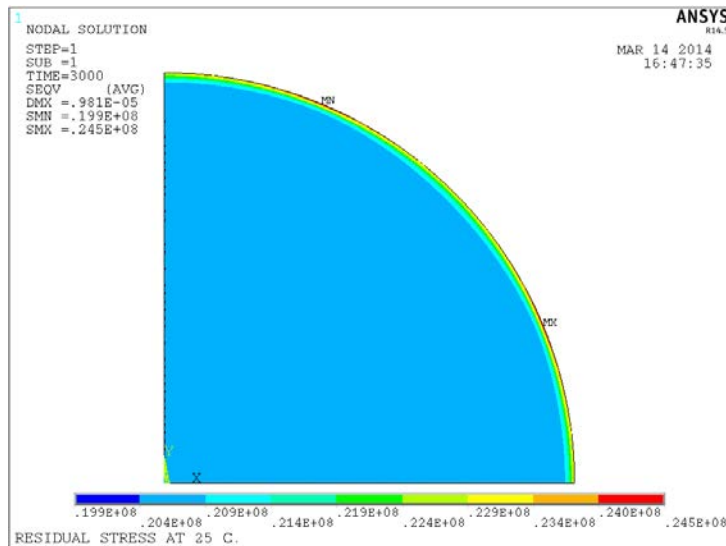
Model – Top View



Sintered-Silver Layer – 5 mm Radius

Interface Modeling

- Six linear elastic simulations were performed and incorporated variations in thickness and diameter of the sintered-silver joint.



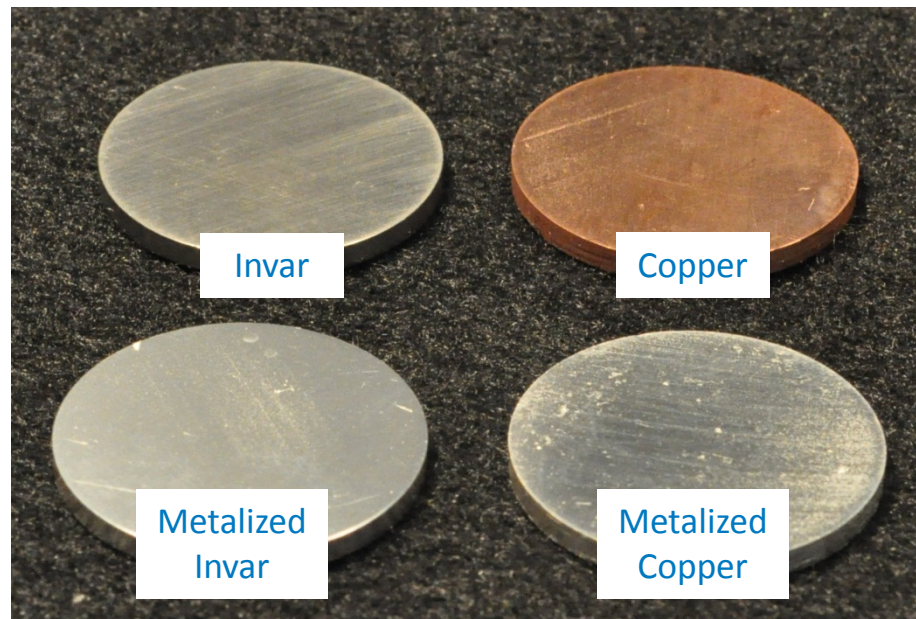
von-Mises Stresses in Sintered-Silver Layer

Thickness (μm)	Diameter (mm)	von-Mises Stress (MPa)
25	10	24.5
25	9	24.9
25	8	25.5
25	7	26.1
25	6	26.8
50	10	27.5

- Stress increased with decrease in diameter of the sintered-silver joint for the same substrate size.
- Stress increased as thickness was increased from 25 μm to 50 μm.

Coupon Synthesis

- Invar and copper were selected for round test coupons.
 - Coupon dimensions are 25.4 mm in diameter, 2 mm in thickness.
 - Materials were chosen for CTE mismatch.
 - Surfaces were blanchard ground and metalized with silver.



Invar and Copper Test Coupons

Responses to Previous Year Reviewers' Comments

- This is a new start for FY14.

Collaboration and Coordination

- Partners
 - **ORNL** (Federal): technical partner on sintered-silver samples
 - **Heraeus** (Industry): sintered-silver material guidance
 - **Henkel** (Industry): sintered-silver material guidance
 - **General Motors** (Industry): technical guidance

Proposed Future Work (FY14)

- Synthesize and shear test initial samples for mechanical characterization of sintered-silver.
- Process CTE-mismatched disk samples with various diameter bond pads to validate stress intensity factor relationship with delamination initiation.
- Focus on optimizing and understanding key synthesis parameters for sintered-silver.
- Develop stronger experimental correlation between interface patterning/ degradation and junction temperature rise.

Proposed Future Work (FY15)

- Evaluate the delamination rate of sintered-silver test coupons under various pressure requirements, bond areas, pad geometries, and surface plating materials.
 - Evaluate low- and no-pressure sintered-silvers.
 - Optimize pad geometries for a large-area bond pad.
 - Recommend industry standard practices for plating.

Summary

- **DOE Mission Support:**
 - BIMs are a key enabling technology for compact, lightweight, low-cost, reliable packaging and for high-temperature coolant and air-cooling technical pathways.
- **Approach:**
 - Synthesis of sintered-silver bonds, thermal temperature cycling, bond inspection (acoustic microscope), and stress intensity factor versus cycles-to-failure models.
- **Accomplishments:**
 - Established a procedure for the material and degradation characterization of sintered-silver.

Summary

- **Collaborations**

- ORNL, Heraeus, Henkel, GM

- **Future Work**

- Synthesize and shear test initial samples for mechanical characterization of sintered-silver.
- Process CTE-mismatched disk samples with various diameter bond pads to validate stress intensity factor relationship with delamination initiation.
- Focus on optimizing and understanding key synthesis parameters for sintered-silver.
- Develop stronger experimental correlation between interface patterning/degradation and junction temperature rise.

Acknowledgments:

Susan Rogers and Steven Boyd
U.S. Department of Energy

Team Members:

Paul Paret (NREL)
Andrew Wereszczak (ORNL)

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