Designing Safe Lithium-Ion Battery Packs Using Thermal Abuse Models

Ahmad A. Pesaran, Gi-Heon Kim, Kandler Smith

(ahmad_pesaran@nrel.gov)
National Renewable Energy Laboratory

Eric C. Darcy
NASA Johnson Space Center

NREL/PR-540-45388
Background

- For powering spacesuits, NASA is considering using a battery pack consisting of arrays (16P-5S) of 18650 Li-ion cells.
- These cells are equipped with a positive temperature coefficient (PTC) device proven effective for control of overcurrent hazards at the Li-ion cell and small battery level.
- However, PTC devices are not as effective in high-voltage battery designs.
- A fire in a 2004 Memphis FedEx facility suspected to be due to a PTC device failure in a large-capacity (66p-2s) battery shorted while at 50% SOC.
PTC Device: Background

- Commercial lithium-ion 18650 cells typically have a current-limiting PTC (positive temperature coefficient) device installed in the cell cap to limit external currents in the event of an external short to the cell.
- The PTC device consists of a matrix of a crystalline polyethylene containing dispersed conductive particles, usually carbon black.* The resistance of the PTC device increases with temperature.
- The PTC resistance increases sharply with temperature. When a short is applied to a cell, the elevated currents cause the PTC to self-heat and move to a high-resistance state in which most of the cell voltage is across the PTC but the current is significantly reduced.
- As long as the short is maintained, the PTC device produces enough heat to keep itself in this tripped state (lower current is offset by greater voltage drop across PTC).

Cell Design Features for Abuse Tolerance

- Scored Disk Vent
- Gasket Seal
- Crimped Can
- CID Button
- CID ring
- PTC ring
- Top Cover
- + Tag mounting disk
- + Tag mounting disk
Motivation for this Work

• Can NASA’s spacesuit battery design (16p-5s) array depend on cell PTC devices to tolerate an external 16p short?

• Is there a range of smart shorts that can be hazardous?
Objectives

• Create an engineering model to guide the design and to verify the safety margin of a battery using high specific energy COTS cells

• Use the model to provide input for designing a NASA 16p-5s 18650 spacesuit battery
  – Cell model must include the electrical and thermal behavior of the cell PTC device
  – Use cell model as building block to model multi-cell battery behavior under short-circuit conditions
  – Assess the range of smart short conditions that push cells close to the onset of thermal runaway temperature
Utilizing NREL’s Multi-physics Battery Modeling

- Electrical Performance Modeling
  - Cells & multi-string modules
- Thermal Modeling
  - Cells & modules
- Thermal/Electrochemical Modeling
  - Cells
- Thermal/Chemical Abuse Modeling*
  - Cells and modules

Overview

• Modeling
  – Approach
  – PTC device
  – Cell
    • Electrical
    • Thermal (5-node)
  – Module
    • Electrical (multi-node network)
    • Thermal (multi-node network)

• Validation with experiments from SRI
  – 16P module with 10 mΩ external short

• Parametric study
  – Resistance of external short
  – Heat rejection rate to ambient

• Conclusions
Modeling Approach

Previous Work:
• Design module to prevent thermal runaway propagation

Present Work:
• Verify module design tolerant to external electrical short

Chemical Reaction Model + Thermal Network Model

Electrical Model + Thermal Network Model

Photo: Symmetry Resources Inc.
PTC Resistance versus Temperature;
Moli ICR-18650J

Cell header removed from cell without disturbing closure configuration
Resistance measurements taken from rupture disk surface to positive button

![Graph showing PTC resistance versus temperature](image_url)

- **Phase Transition**

- **Legend:**
  - PTC 71A06 virgin
  - PTC 71A07 virgin
  - PTC 71A08 virgin
  - PTC 71A09 tripped
Behavior Principles of PTC Devices

Cell can be in 40°C range with two possible PTC device states
- Low-resistance current conducting state (<50 mΩ)
- Current-limiting state with high resistance (>1 kΩ)

Minimum and maximum base resistance (given ambient T)
- Minimum is for virgin (never been tripped) devices
- Maximum is for once (or more) tripped devices

Ultimate trip current, \(I_u\), is the highest equilibrium current possible in the low-resistance state of the device for a given temperature
- It’s the maximum current achieved in an I vs. V curve for a given ambient temperature, for example, at 45°C
  - Moli J’s \(I_u = 7\) A
  - LV’s \(I_u = 9\) A

Power generated in device = power dissipated in device
- The trip time depends on size of the overcurrent, ambient T, thermal mass of the device, its specific heat, its heat dissipation coefficient, and its base resistance
- Steady-state trip current is inversely proportional to voltage applied and ambient temperature
Model needs to capture important physics happening during an experiment

16P Bundle External Short Test
- Performed by Symmetry Resources, Inc.
- Moli ICR18650J cells
- 16 parallel
- 10 mΩ external short

Photos: SRI

- PTC device behavior
  - $R_{PTC}(T)$
  - Thermal connection with the cell
- Cell electrical behavior
  - Current/voltage/temperature relationship
- Cell-to-cell heat transfer
  - Conduction
    - air gaps
    - electrical tabs
  - Radiation
- Cell-to-ambient heat transfer
  - Convection to air
  - Conduction through wire leads
Model Development Approach

Integrated Thermal and Electrical Network Model of a Multi-Cell Battery for Safety Evaluation of Module Design with PTC Devices during External Short
Unit Cell Model: Electrical Performance Model

\[ V(t) = V_{OCV}(SOC) + V_1 - (R_s + R_{PTC}) \times I(t) \]

\[ \frac{d}{dt} \begin{bmatrix} SOC \\ V_1 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \lambda_1 \end{bmatrix} \begin{bmatrix} SOC \\ V_1 \end{bmatrix} + \begin{bmatrix} 1/Q \\ \lambda_1 R_1 \end{bmatrix} I(t) \]

\[ \lambda_1 = \frac{-1}{R_1 C_1} \]

\[ Q = 2.345 \text{ A-h} \]

\[ R_1(SOC, T_{JR}) \]

\[ R_s(SOC, T_{JR}) \]

\[ R_{PTC}(T_{PTC}) \]

\[ C_1(SOC, T_{JR}) \]

\[ V_{OCV}(SOC) \]

\[ I(t) \]

\[ V(t) \]

Jellyroll

PTC

Equivalent Circuit Model and Relevant Parameters
Unit Cell Electrical Model Agrees Well with Data

Validation of Equivalent Circuit Model

- Model compared with constant current discharge data from manufacturer (21C)

- Model compared with mission power profile data from NASA (25C and 65C)
Unit Cell Model: Thermal Model

Developed detailed cell model based on cell cross-cut measurements…

…and validated it with data from PTC device withstanding voltage test. (NASA/SRI)

Detailed Cell Thermal Model

- Finite Volume Method
- 41,250 computational grid
Unit Cell Model: 5-node Thermal Model Validated

Detailed Cell Thermal Model
- Large computational requirement
- Not suitable for multi-cell modeling

5-Node Cell Thermal Model
- Low order dynamic model
- Suitable for multi-cell modeling

Comparison of Detailed and 5–Node Models
For Different Heat Generation Conditions

Steady Form
\[ Q_i = \sum_j K_{ij} (T_i - T_j) \]

Unsteady Form
\[ Q_i = \sum_j K_{ij} (T_i - T_j) + MCp_i \frac{dT_i}{dt} \]

5. Jelly Bottom
4. Jelly Middle
3. Jelly Top
2. PTC
1. Top Button

Ambient

K_{5a} K_{4a} K_{3a} K_{1a} K_{23} K_{12} K_{34} K_{45}
Multi-Cell Network Model

Electrical Network Model

PTC Resistance as a function of PTC temperature

Data: SRI

Jellyroll Resistance as a function of cell temperature

R_{ptc} = 6.172e-5 \exp(2178/T)

R_{jr} = 1.04e-2 \exp(651/T)

Open-Circuit Voltage as a function of cell SOC

V_0 = 6.172e-5 \exp(2178/T)

V_{meas} = 1.04e-2 \exp(651/T)

The Model Solves Voltage and Current Interactions among the Components in a Multi-Cell Circuit
Multi-Cell Network Model

Thermal Network Model

**Thermal Mass:** Identifying thermal mass at each node

**Heat Generation:** PTC heat, charge transfer heat (future: abuse reaction heat)

**Heat Transfer:** Quantifying heat exchange among the nodes

\[ Q_{\text{transport},i} = \sum_{j=1, j \neq i} -Q_{ij}, \quad Q_{ij} = Q_{ij,\text{radiation}} + Q_{ij,\text{connector\_conduction}} + Q_{ij,\text{convection}} \cdots \]

Radiation Heat Transfer

\[ Q_{ij,\text{radiation}} = \varepsilon F_{ij} A (T_i^4 - T_j^4) \]
Multi-Cell Network Model

Thermal Network Model

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\]

**Heat Transfer to Ambient**

\[
Q_{i-a} = hA_{i-a} (T_i - T_\infty)
\]

**Conduction Through Bus**

\[
R_{\text{connector },i-j} = \frac{L_{i-j}}{k_{i-j} A_{i-j}}
\]

**Heat Rejection Through Wires**

\[
Q_{\text{heat}} = k_A \frac{dT}{dx} \bigg|_{x=b} = hA \left(T_i - T_\infty\right)
\]

**Heat Conduction Through Air-Gap**

\[
T - T_a = Ae^{-\alpha x} + Be^{-\beta x}, \quad 0 \leq x < x_i
\]

\[
T - T_a = Ce^{-\gamma x}, \quad x \geq x_i
\]
Experimental Model Validation

10 mΩ External Short

1) $t = 0$ sec: Circuit closed

2) $t \approx 12$ sec: PTC devices trip
   - $T_{PTC} \approx 130^\circ C$

3) $t \approx 1$ hr: Steady state reached
   - $\sim C/5$ discharge
Model Validation – Current & Voltage

1. Peak inrush current readily predicted with knowledge of cell & short resistances.

2. PTC device trip time affected by
   - PTC thermal mass
   - PTC conductive path to jellyroll & can.

3. Steady-state behavior affected by jellyroll and PTC device temperature, indirectly
   - PTC conductive path to jellyroll & can
   - Thermal boundary conditions to ambient.
Model Prediction – Heat Generation

- Pre-trip: Jellyroll heat generation dominates.
- Post-trip: PTC device heat generation dominates.

PTC devices at steady-state 1.35 to 1.86 W
Is this design safe under other short conditions?

- **Max Temperature**
  - PTC-limited
  - Adequate thermal dissipation required
  - SOC-limited

- **$R_{\text{short}}$**
  - small
  - large
Simulation Results at Various Values of $R_{\text{short}}$

- $R_{\text{short}} \leq 40 \, \text{m\Omega}$: PTC-limited
- $R_{\text{short}} \geq 50 \, \text{m\Omega}$: SOC-limited

- Tripped PTC device serves as thermal regulator
  
  \[ [dR_{\text{PTC}}/dT]_{130^\circ\text{C}} = 3\,\Omega/\text{C} \]
  
  (5 orders of magnitude > than at 25°C)

- Large pre-trip heat rates are safe provided they are of
  - short duration
  - sufficient thermal mass
  - sufficient heat dissipation
How much heat rejection is required for safety?

Additional simulations run with various values of $h$ (convective heat transfer coefficient to ambient).

Red lines: $h = \frac{h_{\text{nominal}}}{2}$
Black lines: $h = h_{\text{nominal}}$

- PTC device trip time decreases only slightly with less heat rejection from cells.
- Less rejection leads to hotter PTC device (higher resistance) and slower discharge of cell.
How much heat rejection is required for safety?

- Less rejection causes an increase in jellyroll temperature.
- Pre-trip heat generation rate is largely unaffected by thermal boundary conditions.
- Post-trip, the PTC device reduces heat generation rate as heat rejection decreases.

Red lines: \( h = \frac{h_{\text{nominal}}}{2} \)
Black lines: \( h = h_{\text{nominal}} \)
Conclusions

- Created & validated a new multi-cell math model capturing electrical and thermal interactions of cells with PTC devices during abuse. Suitable for
  - Assessing battery safety design margins
  - Supplementing and guiding verification tests

- Moli ICR18650J cell design has promise to be tolerant to a wide range of external shorts for the 16p configuration of a spacesuit battery, as long as
  - No damage occurs due to the in-rush current transient
  - Nominal tripping of cell PTC devices and steady-state conditions occur
  - External short does not excessively heat battery.

- PTC device is an effective thermal regulator. Maximum cell temperature (final state) is very similar for a variety of initial and boundary conditions.
Acknowledgements

**NASA Johnson Space Center**

- Funding for this work was provided by NASA JSC under Inter-Agency Government Agreement NNJ08HC04I
- Technical Guidance: Frank Davies

**Symmetry Resources Inc.**

- Brad Strangways