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VEHICLE TECHNOLOGIES OFFICE

V.3. Reliability of Bonded Interfaces

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Objectives

- Investigate and improve the thermal performance and reliability of emerging bonded interface materials for power electronics packaging applications.
- Identify failure modes in emerging bonded interface materials, experimentally characterize their lives under known conditions, and develop lifetime estimation models.

Technical Barriers

In automotive power electronics packages, conventional thermal interface materials such as greases, gels, and phase-change materials pose bottlenecks to heat removal and are also associated with reliability concerns. The industry trend is toward high thermal performance bonded interfaces. However, because of coefficient of thermal expansion mismatches between materials/layers and resultant thermomechanical stresses, adhesive and cohesive fractures could occur, posing a reliability problem. These defects manifest themselves in increased thermal resistance.

Technical Targets

Improved package reliability is an enabler to achieve the U.S. Department of Energy (DOE) Advanced Power Electronics and Electric Motors (APEEM) Program power electronics targets for improved efficiency, performance, and lifetime.

Accomplishments

We present results for thermal performance and reliability of bonded interfaces based on thermoplastic (polyamide) adhesive, with embedded near-vertical aligned carbon fibers, as well as sintered silver material. The results for these two materials are compared to conventional lead-based ($Sn_{63}Pb_{37}$) bonded interfaces. These materials were bonded between 50.8-mm × 50.8-mm cross-sectional footprint silicon nitride substrates and Cu base plate samples. Samples of the substrate/base plate bonded assembly underwent thermal cycling from –40°C to 150°C according to Joint Electron Devices Engineering Council standard Number 22-A104D for up to 2,500 cycles. The dwell time of the cycle was 10 minutes, and the ramp rate was 5°C/minute. Damage was monitored every 100 cycles by acoustic microscopy as an indicator of an increase in thermal resistance of the interface layer. The acoustic microscopic images of the bonded interfaces after 2,500 thermal cycles showed that thermoplastics with embedded carbon fibers performed quite well with no defects, whereas interface delamination occurred in the case of the sintered silver material. Both these materials showed a superior bond quality compared to the $Sn_{63}Pb_{37}$ solder interface after 1,500 thermal cycles. The delamination percentage was calculated and compared between the three interface materials. Strain energy density values of $Sn_{63}Pb_{37}$ solder were obtained as an output from ANSYS simulations for lifetime estimation of the interface material.

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Introduction

In a power electronics module, a semiconductor chip/die is typically attached by a bonded interface material (BIM) such as solder to a metalized substrate. The substrate is composed of a ceramic bounded by Cu layers on either side and provides electrical isolation. This substrate is then mounted onto a base plate or directly to a heat exchanger, typically made of Cu or Al, via another BIM. A cross-section of a typical power electronics package is shown in Figure V-34.

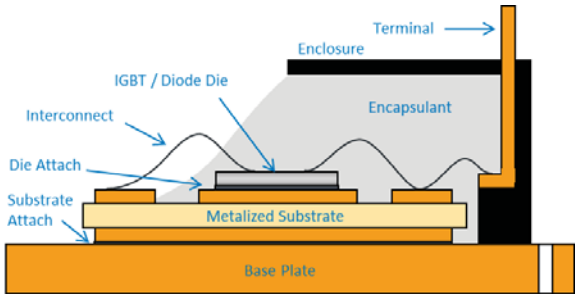

Figure V-34: Traditional power electronics package.

A coefficient of thermal expansion (CTE) mismatch between the ceramic substrate and the Cu base plate can cause defect initiation and propagation in the joining solder layer. Lead-based solders had predominantly been used in the electronics packaging industry; however, the Restriction of Hazardous Substances Directive [1] mandated lead-free solutions. Initially, the industry focused on various Sn, Ag, and

Cu (SAC) compositions as a suitable lead-free alternative, with Innolot ($SnAg_{3.8}Cu_{0.7}Bi_{3.0}Sb_{1.4}Ni_{0.2}$) proving to be a promising solution [2–3]. Research found that varying the composition of the Ag and Cu content in the SAC solders would help minimize creep strain. Overall, reliability under temperature cycling continues to be a concern with lead-free solders. To provide greater thermomechanical reliability under temperature cycling and to allow for higher temperature applications, sintered silver material has also emerged as a promising bonding solution in power electronics packages [4–5]. However, to reduce synthesis temperatures to below 300°C, up to 40 MPa of pressure must be applied to the package, causing a higher complexity in the production process and more stringent flatness specifications for the substrates. Hence, alternative bonding techniques are being developed to increase the thermomechanical reliability of this interface through the use of newer materials, such as thermoplastics with embedded micrometer-sized carbon fibers. Little information is available on the thermal performance and reliability of large-area attaches based on the more recently developed thermoplastic materials.

Prior work at the National Renewable Energy Laboratory (NREL) [6–7] focused on establishing a consistent and high-accuracy database, via the American Society for Testing and Materials steady-state approach [8], on the thermal performance of conventional as well as emerging thermal interface materials (TIMs). The conventional materials included greases, gels, phase-change materials, and filler pads. It was concluded that the tested conventional materials could not meet the thermal performance target of 5-mm^2K/W thermal resistance for a 100-µm bond line thickness. For a number of power electronics packaging stack-ups, the TIM stops being a bottleneck to heat removal when its resistance is on the order of 5 mm^2K/W; thus, it is a target. In addition, practical power electronics packaging configurations and manufacturing constraints dictate that the TIM has to fill gaps on the order of 100 µm.

Because BIMs are promising [9–13], work at NREL has focused on assessing their thermal performance and reliability. Conclusions on thermal performance and reliability from the present effort are intended to directly assist incorporation of these materials into automotive power electronics designs. This report focuses on thermoplastic (polyamide) adhesive with embedded near-vertical–aligned carbon fibers (8- to 10-µm diameter), sintered silver based on micrometer-sized Ag particles, and $Sn_{63}Pb_{37}$ solder as a baseline. The sample synthesis, characterization plan, and results are described below.

Approach

Materials and Sample Synthesis

The assembly consists of a 5-mm-thick Cu base plate attached to a 0.72-mm-thick active metal bonded substrate (0.32-mm-thick silicon nitride [Si_3N_4] with 0.2-mm-thick Cu foil on either side of Si_3N_4, 50.8 mm × 50.8 mm cross-sectional area footprint) via the bonding material. Before assembly, the Cu metallization layers in the substrate were plated with 4 µm of electroless Ni-P, 1 µm of Pd, and 0.3 µm of Ag to improve adhesion with the bonding material. The Cu base plate was electroplated with 5 µm of Ag. An assembled sample is shown in Figure V-35.

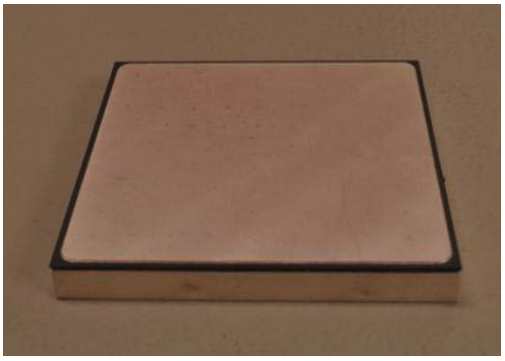

Figure V-35: Representative metalized substrate/base plate assembly.

A tabletop hot press was developed for synthesizing test samples requiring both temperature and pressure bonding parameters. Two hot plates were positioned, one on either side of the sample to be bonded, and were embedded with five 250-W cartridge heaters. Three heaters were inserted in the top hot plate and two in the bottom hot plate. A temperature controller adjusted the power of the heaters based on the temperature measurement by a thermocouple located in the bottom hot plate. The test sample and hot plates were placed between layers of mica and cold plates, and then inserted into an arbor press [14]. Glycol-water (50%–50% mixture by volume) coolant was circulated within the cold plates to isolate the high bonding temperatures from the hydraulic piston and the fluid. A screw jack was also placed between the hydraulic piston and top cold plate to provide fine adjustment to the applied bonding pressure. The pressure of the hydraulic fluid was electronically monitored to determine the force applied to the sample under bonding.

The HM-2 material, manufactured by Btech Corporation, is a composite structure consisting of 8- to 10-µm-diameter carbon fibers embedded in a polyamide/thermoplastic adhesive at approximately 40% fill factor by volume. The HM-2 was placed between the substrate/base plate assembly and subjected to a pressure of 689.5 kPa and a temperature of 190°C. Once the temperature was reached, the assembly was allowed to cool to room temperature while the pressure was maintained.

Bonded interfaces based on sintered silver particles were synthesized by Semikron. Corners of the Si_3N_4 substrate were rounded off to match the 2-mm radius of the Cu layers. The sample assembly was placed in a hot press and raised to its processing temperature, after which pressure was applied.

As a baseline, a $Sn_{63}Pb_{37}$ bond was also synthesized between the substrate/base plate assembly. A 127-µm-thick stainless steel stencil with 9-mm × 9-mm square openings and 1-mm separation was used to apply solder evenly to the substrate and base plate surfaces. After the solder was applied, the assembled sample was placed in a vacuum solder reflow oven. The reflow profile ensured that

flux was removed from the bond and that voiding remained less than 2%.

Initial BIM Characterization

Degradation (e.g., cracks, voids, and delaminations) of the bonded interface can be non-destructively detected by acoustic microscopy. After defect initiation, the thermal and electrical performance of the sample assembly degrades. A C-mode acoustic microscope (C-SAM) emits ultrasound waves with frequencies ranging from 5 MHz to 400 MHz into a sample suspended in water. The strength of the signal reflected back to the microscope's transducer from an interface within a sample depends on the relationship between the acoustic impedances of the two materials forming the interface. A crack, void, or delamination will create a solid-to-air interface, which will cause a strong reflection to be detected by the microscope's transducer. Samples were measured for their initial bonding condition and then subsequently tested every 100 thermal cycles. Images showing the bonded interface within samples before accelerated thermal testing are shown in Figure V-36. The circular bands visible in each sample are artifacts of the C-SAM representing top surface curvatures as 2-D images and are not indicators of bond quality. The $Sn_{63}Pb_{37}$ solder, Btech HM-2, and sintered silver all exhibited uniform bonds between the base plate and substrate samples.

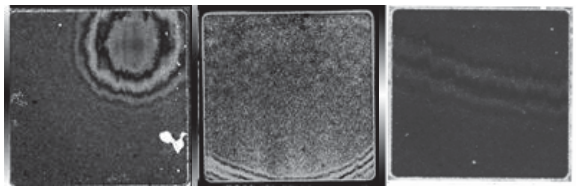

Figure V-36: C-SAM images showing initial bond quality in $Sn_{63}Pb_{37}$ solder (left), sintered silver (center), and Btech HM-2 (right) (Photo credit: Doug DeVoto, NREL).

In addition to acoustic microscopy, the electrical resistance of the Si_3N_4 insulation layer was measured. In a high potential (hipot) test, a high voltage is applied to an electronic device's current-carrying components. The quality of the insulation in the device is determined by measuring the presence of a leakage current. Leakage current indicates that dielectric breakdown in the insulation layer has occurred [15]. A dielectric resistance tester was previously constructed based on the hipot testing process to detect when a crack in the Si_3N_4 has developed. A custom fixture contacts the top and bottom sides of a test sample, and a test voltage of 2.0 kV is applied for 20 seconds, which is sufficient voltage to cause an arc in the air through a defect or crack in the 0.32-mm-thick Si_3N_4 layer. Measurement of the leakage current from an arc indicates that damage occurred within the Si_3N_4 layer in the sample. The sample successfully passes the test if no current was measured over the analysis period. The results correlated with acoustic microscopy images, indicating that all initial samples exhibited no defects within the Si_3N_4 layer.

CTE mismatches within the samples cause package deformation and stresses to build up in the Si_3N_4 layer during the cooldown from the synthesis temperature to room temperature. These stresses can be sufficient to cause crack initiation and propagation within the Si_3N_4, leading to failure of the layer's electrical insulating properties. Representative CTE parameters for materials common within a power electronics package and examples of package deformation conditions are shown in Figure V-37. As a package cools from a stress-free temperature, the Cu base plate's higher CTE relative to the substrate and silicon die causes it to contract more and induce a bow into the package. Heating will conversely cause the base plate to expand more quickly than the rest of the package and create a bow in the opposite direction.

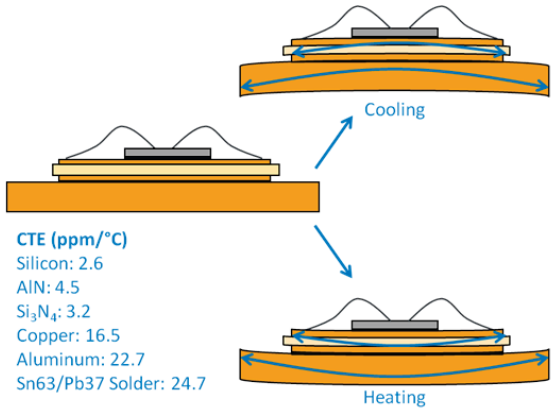

Figure V-37: Power electronics package deformation caused by CTE mismatch under cooling and heating conditions.

The high pressure and temperature synthesis requirements for sintered silver did not cause crack initiation within the Si_3N_4 substrate; however, package deformation was evident when samples were at room temperature. A laser profilometer was used to scan the top and bottom surfaces of sintered silver samples for accurate measurements of these deformations. Figure V-38 shows the top surface profile of one sintered silver sample as well as a cross-section profile between two of the sample's corners. The height variation across the sample was measured to be 166 µm. Surface profile measurements were also taken for $Sn_{63}Pb_{37}$ solder and thermoplastic samples, but no significant package deformations were found.

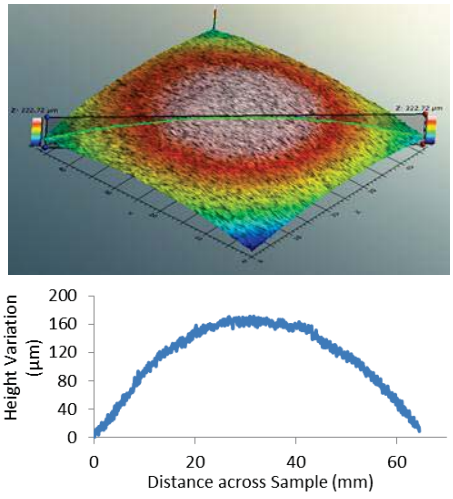

Figure V-38: Surface profile of sintered silver sample at room temperature.

Modeling of Strain Energy Density in $Sn_{63}Pb_{37}$ Solder

The BIM reliability modeling approach involves first calculating the accumulated viscoplastic strain energy density per cycle using finite element analysis. Results are then implemented into a fatigue model to obtain a correlation of the strain energy density with experimentally determined number of thermal cycles to BIM failure. ANSYS Mechanical was selected for the finite element analysis because of its established accuracy in this field [16–20].

An ANSYS Parametric Design Language (APDL) code was developed that included model pre-processing, solver, and post-processing stages. The model geometry matched the experimental test sample geometry and consisted of a stackup of 50.8-mm × 50.8-mm cross-sectional area footprint composed of a Cu base plate, $Sn_{63}Pb_{37}$ solder BIM, and a Si_3N_4 substrate. A quarter symmetry of the package was utilized in the modeling to save computational space and time, shown in Figure V-39.

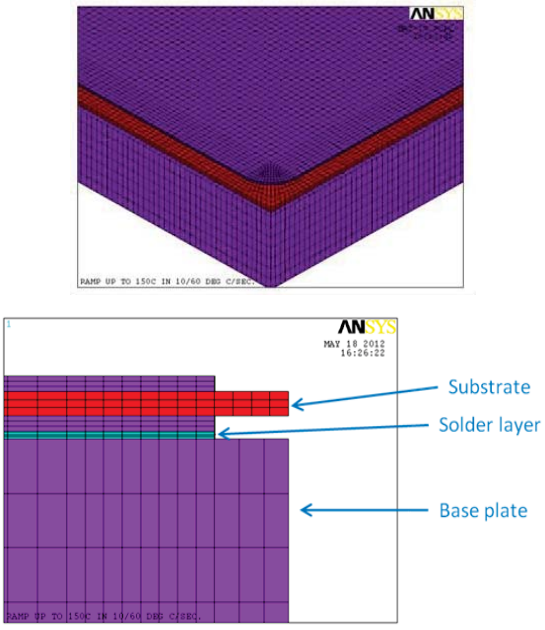

Figure V-39: Quarter symmetry model (top) and layers in the bonded assembly (bottom).

After the geometry was constructed, material properties were assigned to the various layers within the package. The Anand constitutive model was used to define the viscoplastic nature of the solder interface while temperature-dependent, elastic properties were applied to the base plate and substrate layers [21–22]. Nine parameters in the Anand model were obtained from published literature. Various mesh controls, including element sizing, edge sizing, and meshing technique, were then used to create a structured mesh that increased in density at the bonded interface layer. Furthermore, these controls ensured that no mesh mismatch occurred between the model layers. The model was then subjected to a cyclic temperature load with maximum and minimum temperatures of 150°C and –40°C, respectively, a ramp rate of 5°C/min, and a dwell time of 10 minutes. Four such cycles were simulated to study the plastic behavior of the solder interface.

The package design was modified to create a fillet at the corner region to reduce the maximum strain energy distribution. The fillet was created both for the solder layer and for the Cu metallization layers in the substrate. The geometry construction and the meshing sections of the APDL code were significantly modified to incorporate the fillet at the corner region. Separate control over the mesh in the fillet region was achieved in the modified code. This was important for minimizing computational time and mesh size, as mesh density could then be increased in the solder fillet region independently of the solder inner region. An appropriate element size was chosen after conducting a mesh independence study to achieve a balance between computational time and accuracy of the results. Model variations with a fillet radius of 1.5 mm and 2 mm were analyzed as the application of a fillet onto a substrate's metalized layers is a common technique to increase the reliability of the solder layer in the corner region.

Results

BIM Condition after Thermal Cycling

After initial characterization of the test samples, conditions must be applied to create thermally induced stresses, leading to cracking, voiding, or delamination failures. Generally, three types of thermal duty cycles can be used to create thermally induced stresses: a temperature cycle, a thermal shock cycle, and a power cycle. A temperature cycle specifies the temperatures to which a sample under test will be exposed, the durations of exposure, and the rate of temperature change when the sample under test is brought to a new temperature set point. A thermal shock cycle is similar to a temperature cycle, but consists of rapid changes in the ambient temperature. Finally, a power cycle is created by heat dissipation in an actual electronic device to create realistic heat flow patterns and temperature distributions in a sample under test. Because the lifetimes of samples are too long to be tested in real time, an accelerated temperature cycling test procedure is employed to bring testing times down to a reasonable duration.

Samples were cycled between –40°C and 150°C, a common temperature range for electronics testing, to evaluate the quality of the bonded interfaces [23–26]. A soak, or dwell, time of 10 minutes at the maximum and minimum temperatures was chosen to promote solder fatigue and creep [23]. Ramp rates for thermal cycling must be sufficiently low to avoid transient thermal gradients in the test samples; therefore, ramp rates were in the 5°C/min range. Each sample was cycled up to 2,500 thermal cycles, or until degradation propagated to sufficient levels to separate the substrate from the base plate. A failure is defined as a crack in the Si_3N_4 substrate, a cohesive fracture within the BIM, or an adhesive/interfacial fracture between the BIM and either the substrate or base plate surface. A crack in the Si_3N_4 substrate would indicate loss of electrical insulation capabilities and the sample would immediately be considered failed. Cohesive or adhesive/interfacial fractures in the BIM would increase the thermal resistance of the power electronics package,

eventually creating a thermal bottleneck that would elevate the operating temperature of a die above its maximum limit. For testing purposes, a fracture leading to 15% area delamination of the BIM is defined as a failure.

Thermoplastic HM-2 samples have undergone 2,500 temperature cycles and have shown no initiation of defects in the Si_3N_4 substrate or the BIM. Figure V-40 shows C-SAM images highlighting the corner regions of the Btech HM-2 interfaces after 1,000 temperature cycles, 1,500 cycles, and 2,500 cycles.

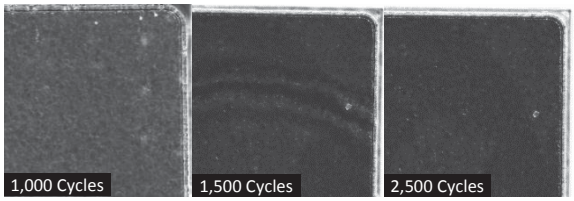

Figure V-40: C-SAM images of Btech HM-2 thermoplastic material after select number of thermal cycles. (Photo credit: Doug DeVoto and Paul Paret, NREL)

Sintered silver samples have also undergone 2,500 temperature cycles but have shown progressively increasing delamination of the BIM. This is observed in acoustic images of a corner region of the sintered silver material after 1,000 temperature cycles, 1,500 cycles, and 2,500 cycles, as shown in Figure V-41.

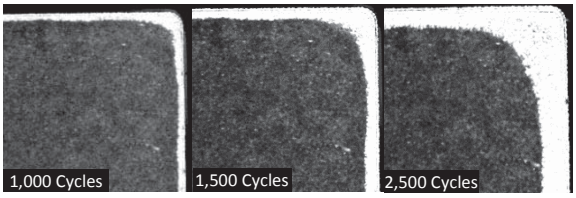

Figure V-41: C-SAM images of sintered silver material after select number of thermal cycles. (Photo credit: Doug DeVoto and Paul Paret, NREL)

Measurements of the delamination percentage within the sintered silver BIM were taken every 100 cycles from C-SAM imaging. Depending on the sample, this perimeter fracturing increased to 19%–32% of initial bonded area after undergoing 2,500 temperature cycles, as shown in Figure V-42. Under these specific bonding and temperature cycling conditions, the sintered silver samples remained defect free until approximately 300 cycles. A period of transient rate delamination occurred after defect initiation until approximately 1,000 cycles, after which a constant rate delamination was observed to the conclusion of temperature cycling at 2,500 cycles.

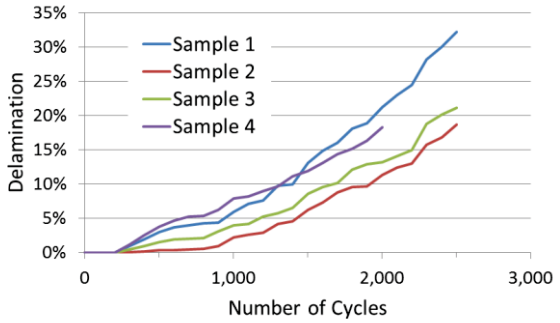

Figure V-42: Perimeter delamination of sintered silver BIM as a function of number of thermal cycles.

The fourth sample was cross-sectioned and the bonded interface layer was imaged after 2,000 temperature cycles. It was determined that the delamination observed in acoustic microscope images was the result of cohesive fracturing within the sintered silver material. The cohesive fracturing is shown in Figure V-43. After 2,500 cycles, additional cross-sectioning and imaging confirmed that cohesive fracturing occurred in the remaining three sintered silver samples.

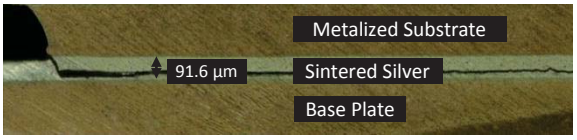

Figure V-43: Cohesive fracture within sintered silver BIM after 2,000 temperature cycles.

$Sn_{63}Pb_{37}$ solder samples have been subjected to 1,500 thermal cycles. C-SAM images show a higher amount of delamination, indicating a relatively poor performance of the BIM (Figure V-44).

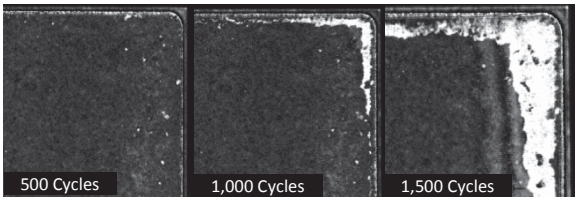

Figure V-44: C-SAM images of $Sn_{63}Pb_{37}$ solder material after select number of thermal cycles. (Photo credit: Doug DeVoto and Paul Paret, NREL)

The delamination percentage was calculated for the $Sn_{63}Pb_{37}$ solder material and compared with the other two interface materials. After 1,500 cycles, cohesive fracturing within the solder material reached 21%–24% delamination, and observed delamination rates were higher in the solder samples than in sintered silver or thermoplastic HM-2 samples. Delamination rates of all three interface materials are shown in Figure V-45.

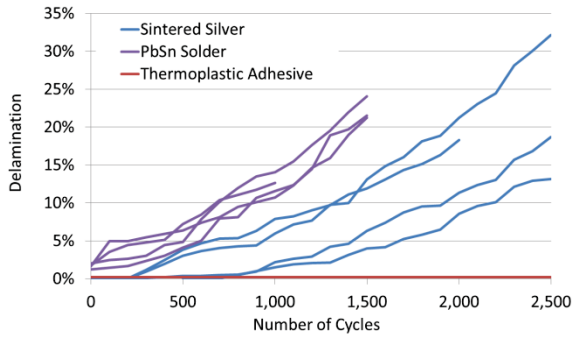

Figure V-45: Perimeter delamination of sintered silver, $Sn_{63}Pb_{37}$ solder, and thermoplastic adhesive as a function of number of thermal cycles.

Modeling Results

Figure V-46 shows the temperature profile and development of shear strain and shear stress within the solder interface's corner region as a function of time. Calculations of strain levels within the solder interface are critical to develop relationships with fatigue failures within the interface material. As the temperature ramps up from room temperature to 150°C, strain within the solder develops and reaches a maximum value at the end of the elevated dwell period. During the subsequent ramp down, the strain decreases and reaches the lowest level at the end of the low-dwell period. A similar pattern is also seen for shear stress, where the stress level first increases with temperature during the ramping up period. Stress relaxation is then observed during the last portion of ramping up and continues to relax through the elevated dwell period. Negative shear stress levels develop during ramp down and reach a minimum at the low dwell, where some stress relaxation is then observed. This model confirms that for $Sn_{63}Pb_{37}$ solder, creep effects accelerate at elevated temperatures.

Analysis of stress-strain hysteresis loops helps to understand the inelastic behavior exhibited by the interface and combines the effect of stress and strain into a single parameter: the strain energy density. On completion of a simulation, the node with the maximum equivalent strain was selected and its stress and strain values as a function of time were obtained through post-processing. Results indicated that the maximum strain energy distribution occurred at the solder's corner region, at the interfacial joint with the Cu base plate. The inelastic behavior of the solder joint under varying thermomechanical loads during a temperature cycle is illustrated in Figure V-47. The temperature cycle is segmented into four different cases, a high dwell at 150°C, a ramp down to –40°C, a low dwell at –40°C, and then a ramp up back to 150°C. Beginning at the 150°C high dwell, shear stress slightly decreases as shear strain increases, with creep strain playing a predominant role. The ramp down segment causes both stress and strain values to decrease until the low dwell at –40°C, at which point stress levels increase slightly while strain values continue to decrease. As the temperature increases during ramp up to 150°C, stress levels increase until approximately room temperature, at which point stress decreases and strain values begin to increase from temperature-dependent creep. At room temperature, the homologous temperature of solder is more than 0.5 and hence stress relaxation begins to occur with the rise in temperature.

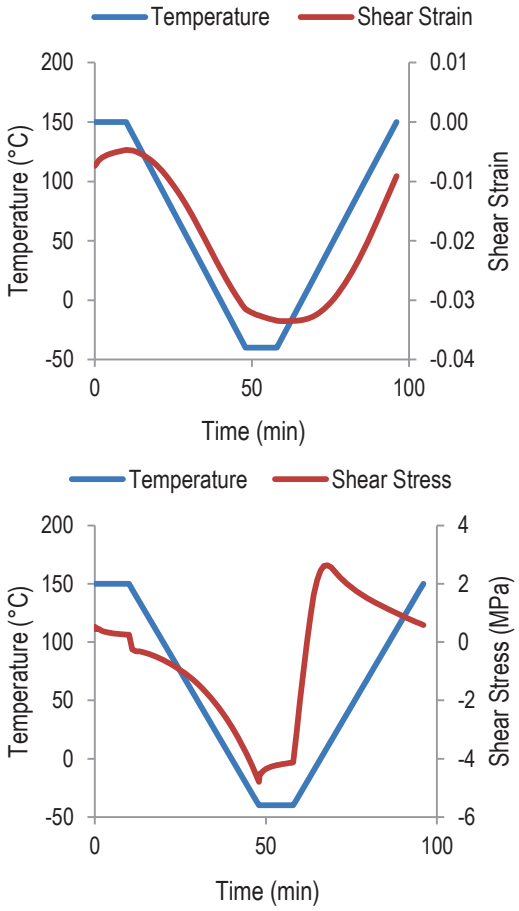

Figure V-46: Temperature and shear strain versus time (top) and temperature and shear stress versus time (bottom).

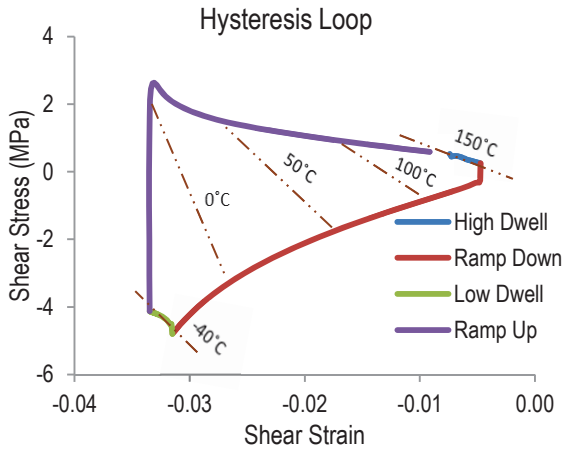

Figure V-47: Hysteresis loop from a solder interface's 2-mm fillet maximum equivalent strain node.

Figure V-48 shows a comparison of stress-strain values between solder interfaces with 1.5-mm and 2-mm fillet corners. Separate simulations were run to obtain the results. The figure shows that under the same temperature loading conditions, an equivalent amount of stress was induced but

the maximum shear strain values were reduced in the 2-mm fillet geometry.

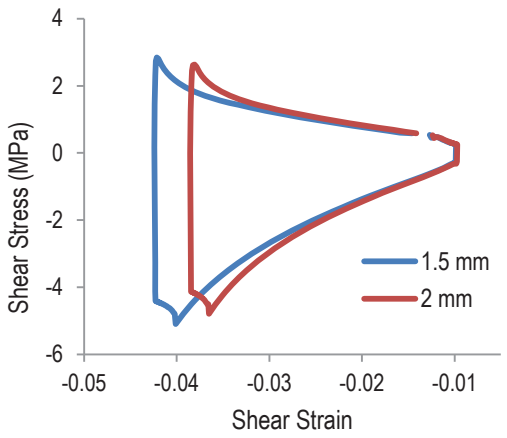

Figure V-48: Stress-strain comparison.

Energy stored in the solder interface region from deformation during the temperature loading conditions is referred to as the strain energy. The strain energy density is the strain energy per unit volume and is determined by calculating the area within the stress-strain hysteresis loop for a given temperature cycle. The strain energy density values calculated over the entire fillet regions for 1.5-mm and 2-mm fillet corners were 9.04 MPa and 8.91 MPa, respectively.

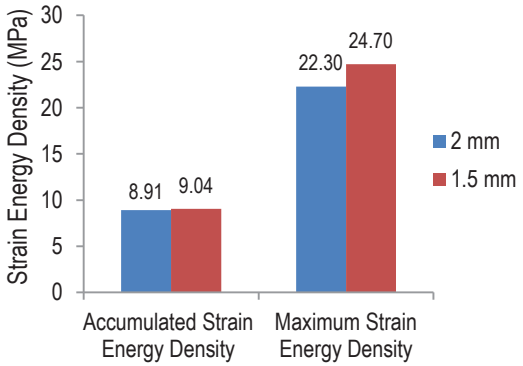

Figure V-49: Strain energy density values.

These strain energy density values will be correlated with an experimentally determined number of thermal cycles to failure for the $Sn_{63}Pb_{37}$ solder BIM.

Conclusions and Future Directions

A consistent framework has been implemented to establish the thermal performance and reliability of large-area bonded interfaces based on novel/emerging materials such as thermoplastics with embedded carbon fibers and sintered silver materials as compared to $Sn_{63}Pb_{37}$ solder. These large-area attachments are currently being considered in state-of-the-art power electronics packages for electric-drive vehicle applications. Results for bond quality after thermal cycling suggest that thermoplastics with embedded fibers could be a promising alternative to solders. Future work with sintered silver material will focus on minimizing the occurrence of cohesive fracturing by optimizing processing conditions.

Modeling of strain energy density for the $Sn_{63}Pb_{37}$ solder BIM bonded between the metalized substrate and Cu base plate was performed using the Anand model parameters for the solder BIM from the literature. The results will be leveraged in the efforts to generate experimental cycles-to-failure versus strain energy density models for BIMs of interest.

FY 2013 Publications/Presentations

1. DeVoto, D., Paret, P., Narumanchi, S., and Mihalic, M., "Reliability of Bonded Interfaces for Automotive Power Electronics," InterPACK2013-73143, *Proceedings of the 2013 InterPACK Conference,* July 2013, Burlingame, CA (Outstanding Paper Award–Second Place, Mechanics).
2. DeVoto, D., Paret, P., and Mihalic, M., "Reliability of Bonded Interfaces," *2013 DOE Vehicle Technologies Office (VTO) Annual Merit Review,* Crystal City, VA, May 2013.
3. DeVoto, D., Paret, P., and Mihalic, M., "Reliability of Bonded Interfaces," *Presentation to the DOE Vehicle Technologies Office Electrical and Electronics Team,* Southfield, MI, April 2013.
4. DeVoto, D., Paret, P., and Mihalic, M., "Reliability of Bonded Interfaces," *Advanced Power Electronics and Electric Motors FY13 Kickoff Meeting, DOE VTO,* Oak Ridge, TN, November 2012.

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