Improvements on PID for c-Si based solar cells

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Abstract

Potential induced degradation (PID) of silicon solar cells has been discussed extensively in the past couple years and PID-resistant cells is becoming a standard in the PV industry. Here we try to identify different ways to further avoid the PID for c-Si based solar cells.

In this work, it is demonstrated that PID resistance of c-Si based solar cells can be improved by several approaches, including the Refraction Index (RI) adjustment of SiNx film, the additional oxidation process, and the modification of wafer surface morphology etc… The oxide film deposited before SiNx deposition can act as a barrier layer between the antireflection coating (ARC) film and the p-n junction. In addition, different oxidation processes made by thermal, plasma, and chemical show different PID resistances. The most promising condition shows a power degradation of less than 1% after PID test, which is stressed under -1000V (PID prone EVA, 60℃, 96hrs, and module covered with aluminum foil). Besides, some potential problems while transferring these technologies into mass production are also discussed.

Introduction

Recently, the studies and solutions for PID issue on silicon solar cells are become more important[1][2]. In the previous study, we have demonstrated the relations between the PID performance and the cross-linking rate of encapsulation material[3]. In this work, we focus on cell level using the standard c-Si solar cell process to improve it and discuss the advantage and disadvantage.

Experiments

PID stress tests of the modules were carried out under -1000V, 60℃ environment during 96 hours. IV test of the modules were measured before and after stress testing at standard test conditions according to IEC60904-1(25°C, 1000 W/m², AM1.5G). The standard processes are including wafer surface texturing; emitter formation by $POCl_3$ diffusion; PSG remove; edge isolation; anti-reflection coating (SiN_x, refraction index=2.06~2.08) and the metallization of font and back contacts by screen printing and co-firing processes.

Results

I. SiNx refraction index adjustment

The following two graphs show the power degradation ongoing PID with refraction index(RI) adjustment and the electrical performance loss. Exp.1 to Exp.6 are SiNx RI modification from 2.08 to 2.20. Exp.6 has the best PID resistant, but the cell efficiency is less 35% than Ref.. Therefore, RI modification is a easy way to enhance PID resistance, but it's definitely not a final solution.

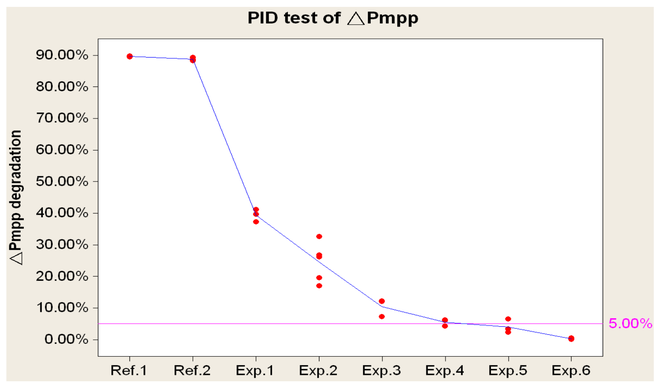

Fig.1 Normalized power degradation of PID test

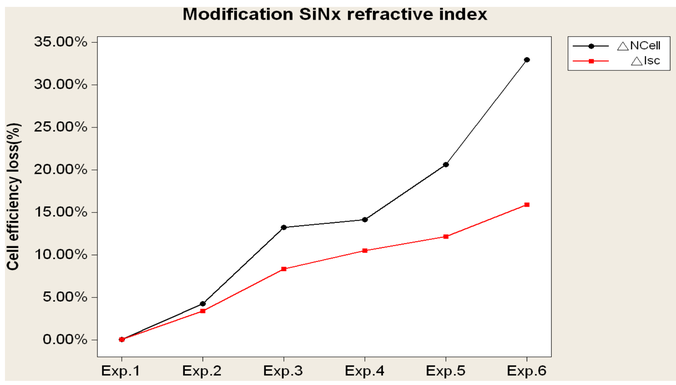

Fig.2 Normalized cell efficiency loss of modification SiNx refractive index

II. Surface treatment

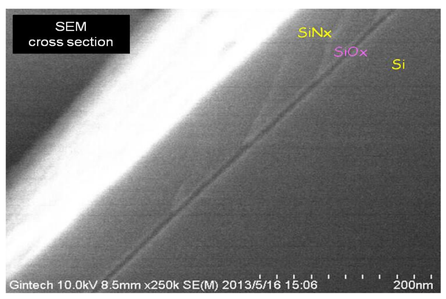

Fig.3 SEM cross-section image

Surface oxidation treatment appears efficient PID improvement and also has good cell performance. The different oxidation ways show results as Table.1. According to our assessment, those ways shows the different mass production possibility.

Comment	oxidation condition	cell performance	process flow	mass production realizable
mono Ref.	none	–	–	–
thermal oxide A	furnace w/Gas A	↑ 0.25%	another process	difficult
thermal oxide B	furnace w/Gas B	↑ 0.25%	another process	difficult
plasma oxide	PECVD	↑ 0.1%	–	realizable
organic oxide	chemical post-treatment	↑ 0.1%	–	realizable

Table.1 The comparison of different surface treatment

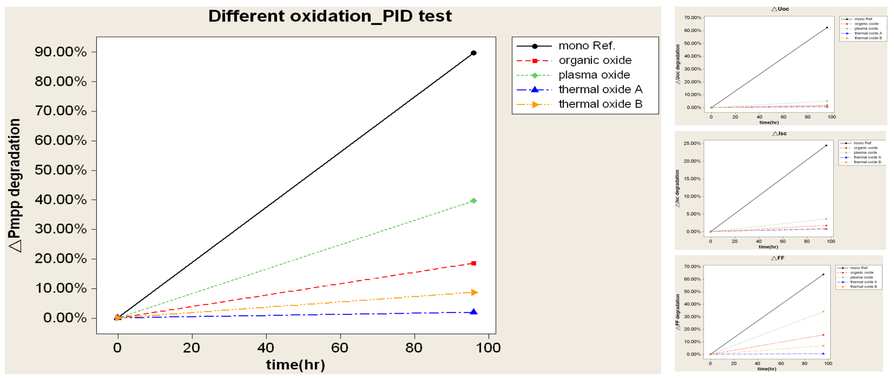

Fig.4 Normalized change of the electrical performance parameters caused by PID

III. Surface morphology effect

When the groove of mono texture become rounding, PID resistant can be improved but not be enough to reach the goal of PID free.

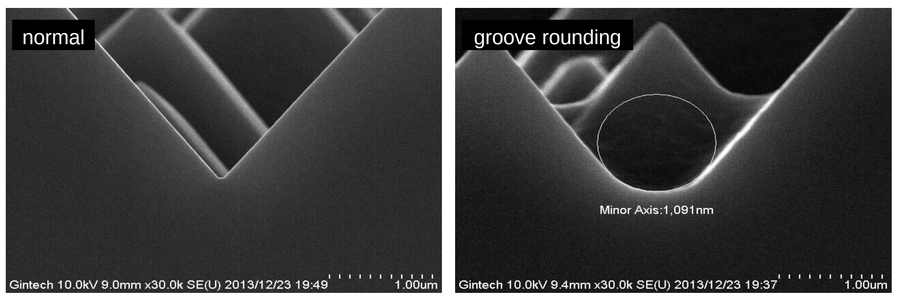

Fig.5 SEM cross-section image by different texture grooving (left:normal ; right:groove rounding)

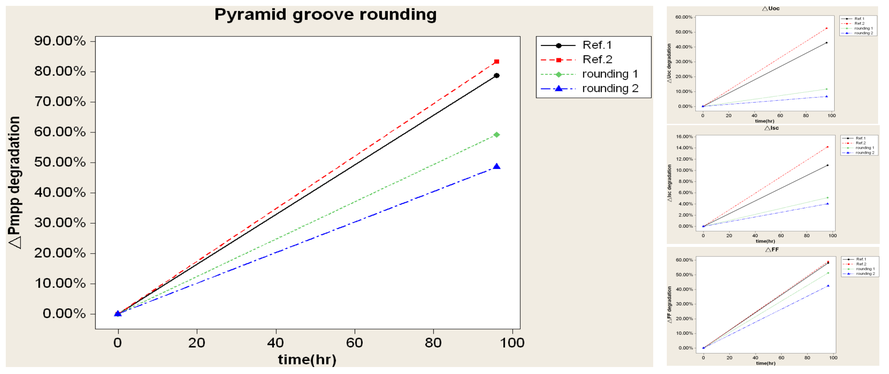

Fig.6 Normalized change of the electrical performance parameters caused by PID

Conclusion

In this article, we have demonstrated that how to improve PID performance for c-Si based solar cells manufacturing by Refraction Index (RI) adjustment of SiNx film, the additional oxidation process, and the modification of wafer surface morphology. The surface treatment is one way to get PID resistant cells without cell performance loss. We continuously improve the PID issue in cell level to reach the goal of PID free. Besides, the selection of module encapsulation material is also a good solution instead of process modification on cell level to resolve PID issue.

Reference

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2. H. Nagel, A. Metz and K. Wabgemann, "Crystalline Si Solar Cells and Modules Featuring Excellent Stability Against Potential-Induced Degradation," 26th European Photovoltaic Solar Energy Conference, p.3107,2011.
3. C.C. Wang, S.H. Yang etc., "The impact of encapsulation material on PID test"