Progress on Power Hardware in the Loop based Anti-Islanding Testing of PV Converters

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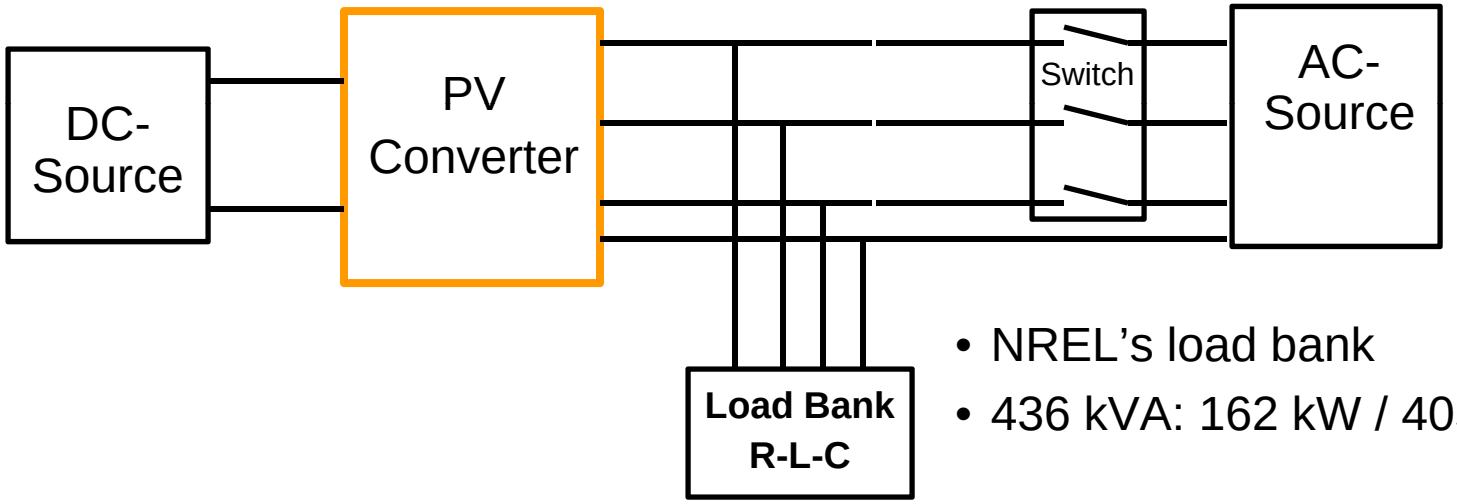
Unintentional Islanding Testing

Current Practice

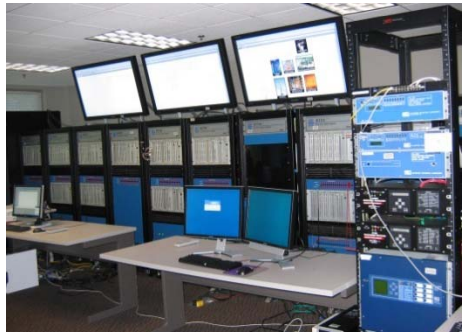
- IEEE Std. 1547.1
  - Dedicated RLC load bank
  - Quality factor of 1 (and steps within ±0.05)
    - Resonant at fundamental frequency
  - Three power levels (100%, 66% and 33%)
  - PV inverter required to disconnect within 2 seconds
  - PV active power matched to resistive load



- NREL's load bank
- 436 kVA: 162 kW / 405 kVAr

Laboratory Facilities

- 7.5 MVA, 4.16kV test and evaluation facility
  - 5 MW variable voltage and variable frequency converter (4x1.25 MW, 180 A)
  - 5 MW dynamometer
- 5 MW MVDC test capability
    - 4 MMC units, 0…6 kV, 0…210A (24 kV)
- Linear amplifier (<400 V, 15 kW)
- Real-time Simulator (RTS)
  - Down to 2 µSec time step
- Integrated
  - Hardware-in-the-Loop (HIL) testbed
  - Testbed(s) + RTS
      - Rest-of-System emulation
      - Custom protection and automated tests
      - Derisking: Model and simulate experiments

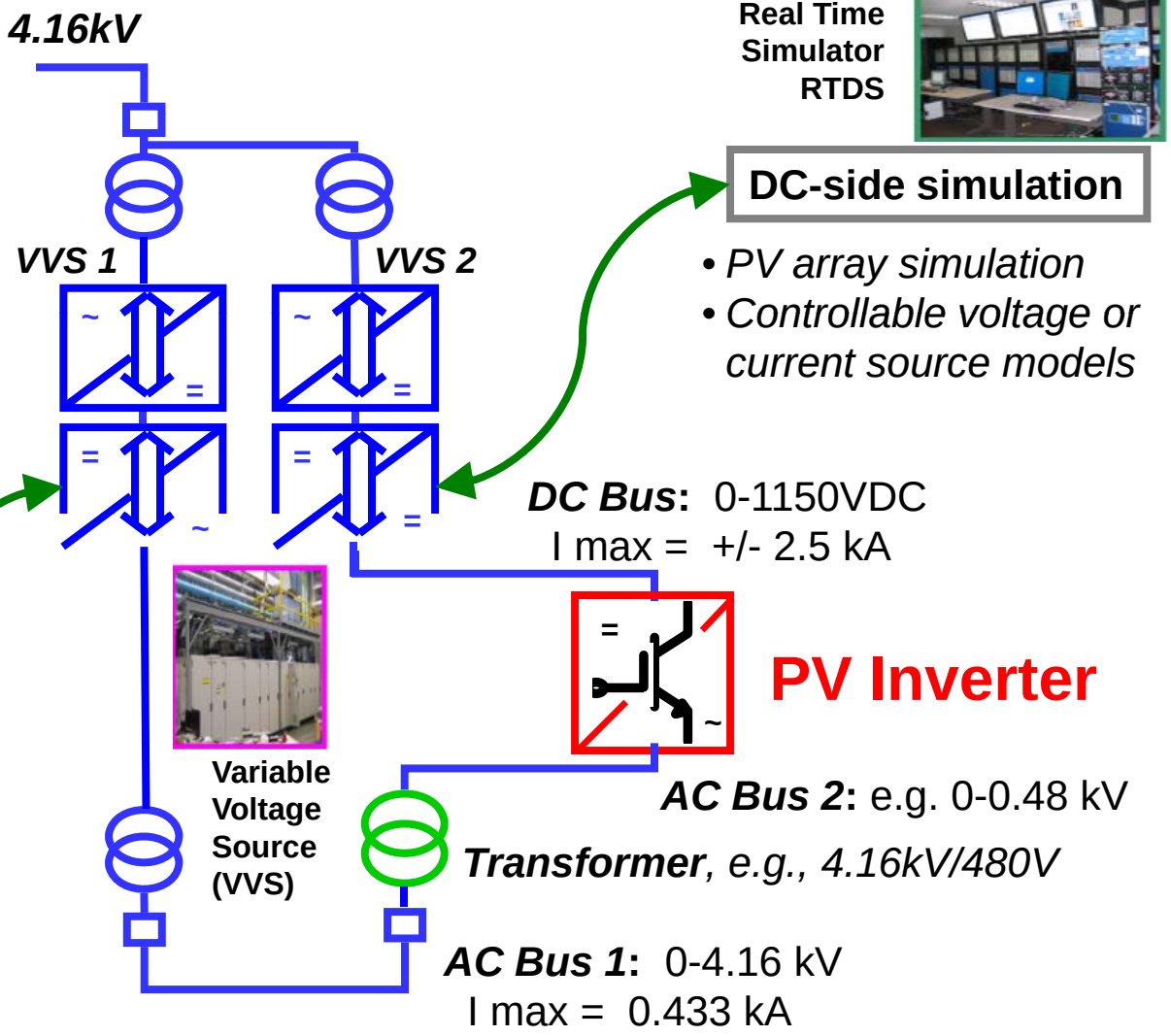


Test Setup for PV Inverter Testing at CAPS

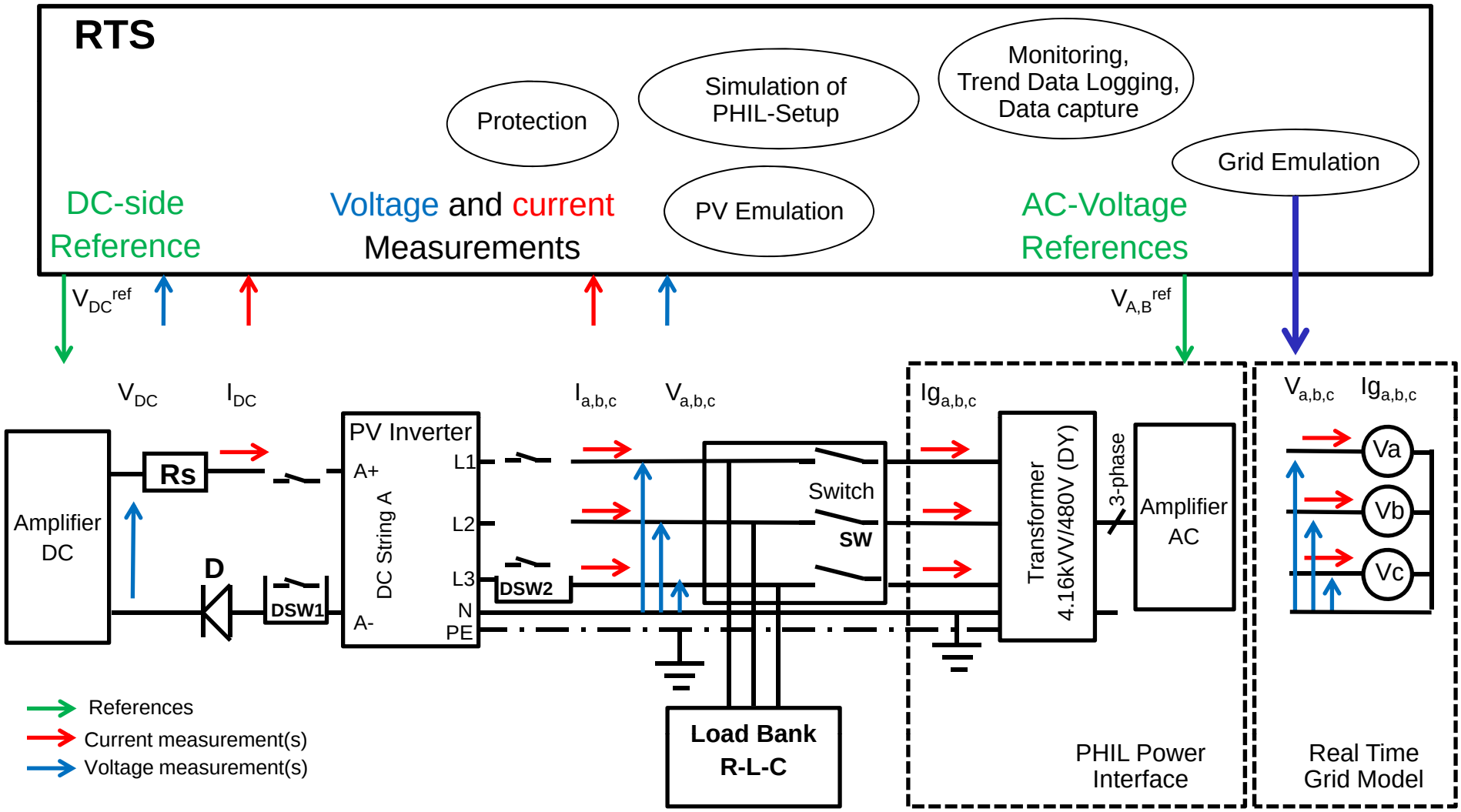
VVS-DC and VVS-AC Arrangement

Real time simulators control AC and DC power interfaces

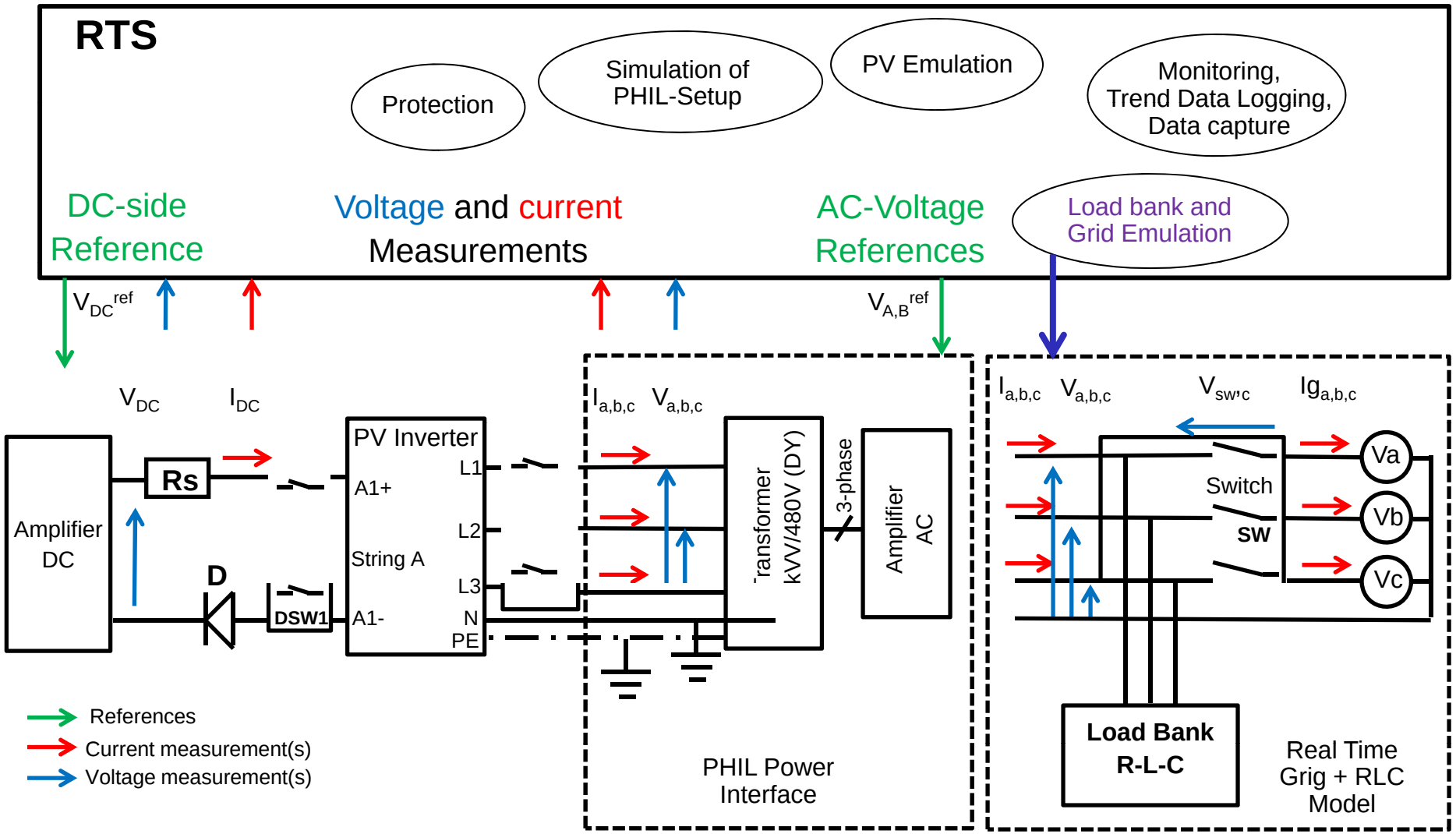
- Up to 2.5 MW_{dc} at 1 kV
- Up to 2.5 MW_{ac} at 4.16 kV



Reference with real Load Bank



PHIL Setup


RTS
Protection
Simulation of PHIL-Setup
PV Emulation
Monitoring, Trend Data Logging, Data capture
DC-side Reference
Voltage and current Measurements
AC-Voltage References
Load bank and Grid Emulation
V_{DC}^{ref}
$V_{A,B}^{ref}$
V_{DC}
I_{DC}
$I_{a,b,c}$ $V_{a,b,c}$
$I_{a,b,c}$ $V_{a,b,c}$ $V_{sw,c}$ $Ig_{a,b,c}$
Amplifier DC
Rs
D
DSW1
PV Inverter
A1+
String A
A1-
L1
L2
L3
N
PE
Transformer kVV/480V (DY)
3-phase
Amplifier AC
Switch
SW
Va
Vb
Vc
Load Bank R-L-C
References
Current measurement(s)
Voltage measurement(s)
PHIL Power Interface
Real Time Grig + RLC Model

PHIL Interface Algorithms

Purpose: Interface simulation through power amplifiers with device under test.

Voltage reference

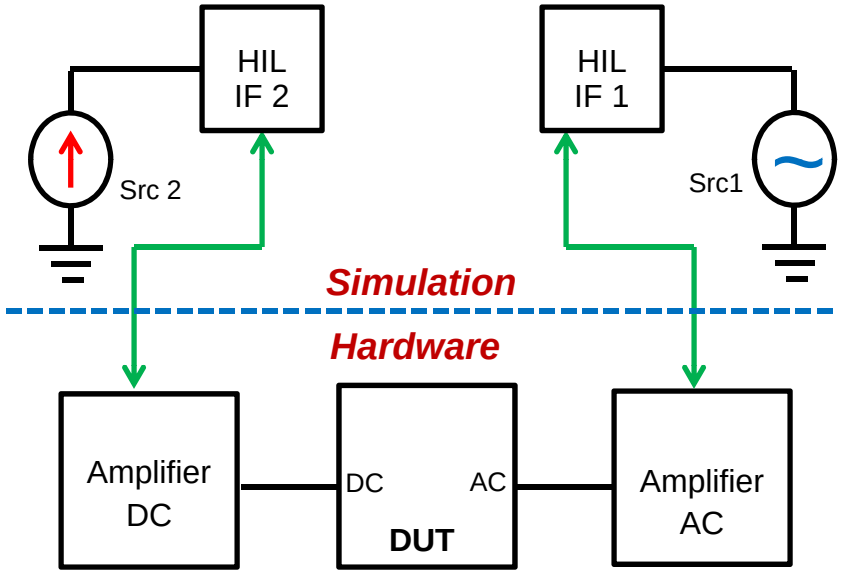
- Voltage commanded (from simulation to amplifier)
- Current measured and fed back into simulated model

Two approaches

dq Reference frame

Ideal Transformer Model

- Proved to be overall more stable and yet dynamic in response

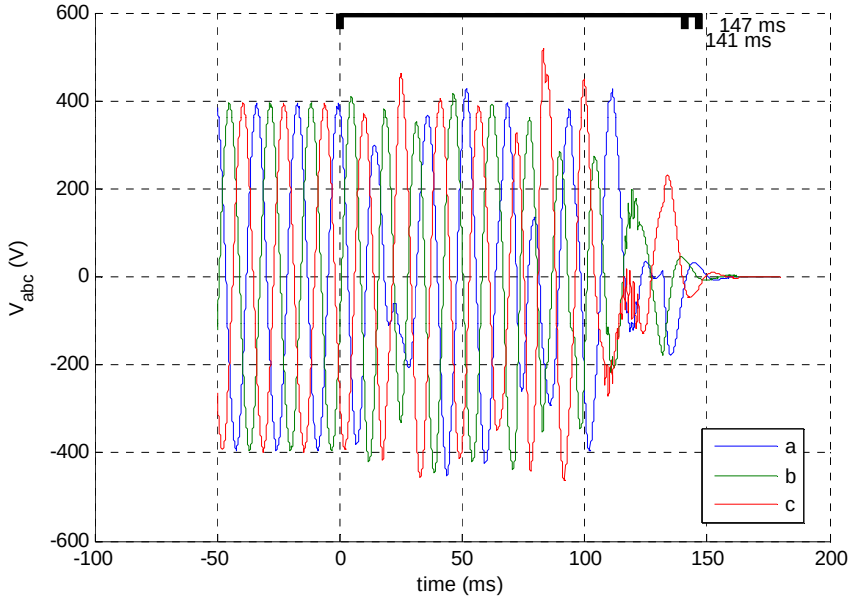


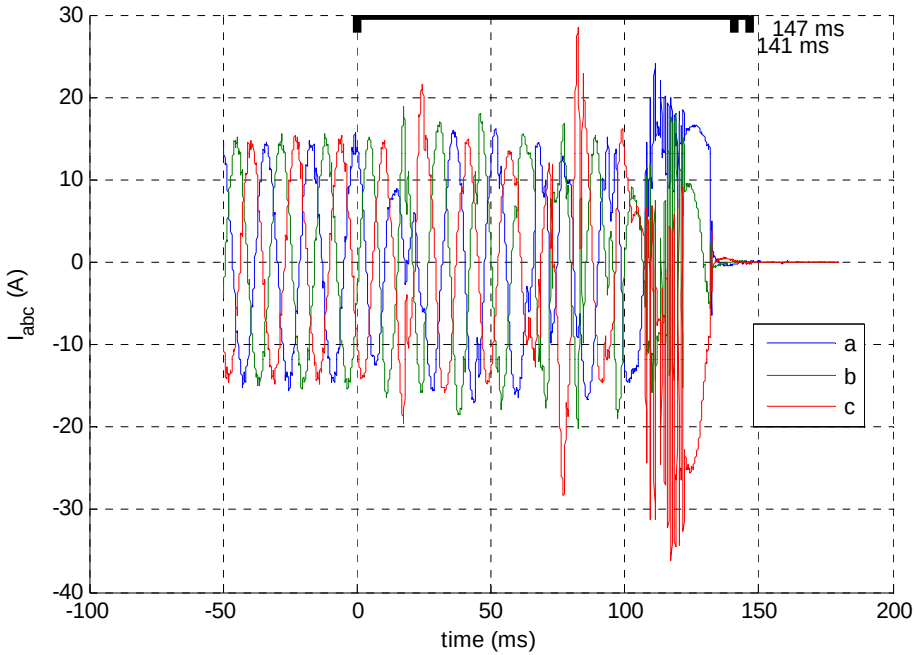
Setup with 20 kW SMA converter

15 kW DC amplifier (ungrounded)

Time Domain Response with real Load Bank

- SMA Sunny TriPower 20 kW
- 8 kW, Qf = 1

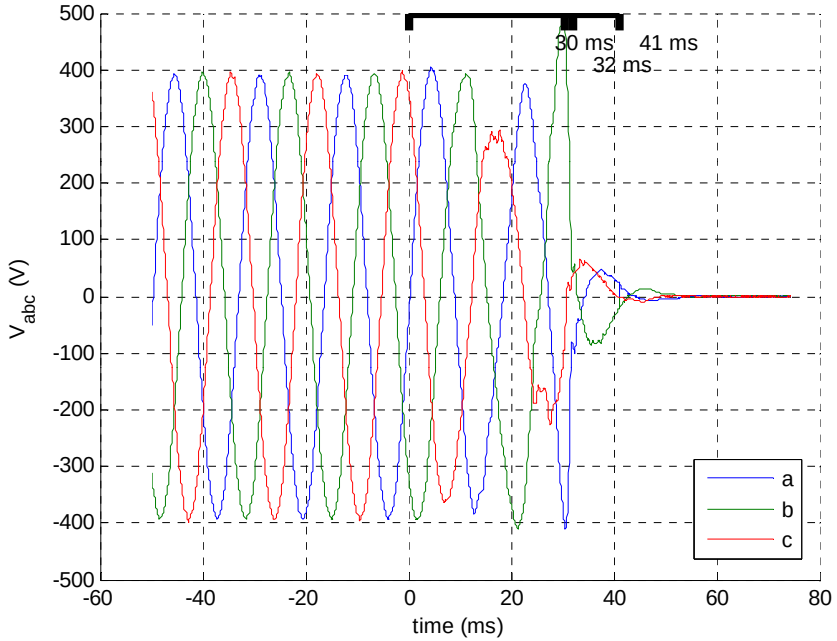


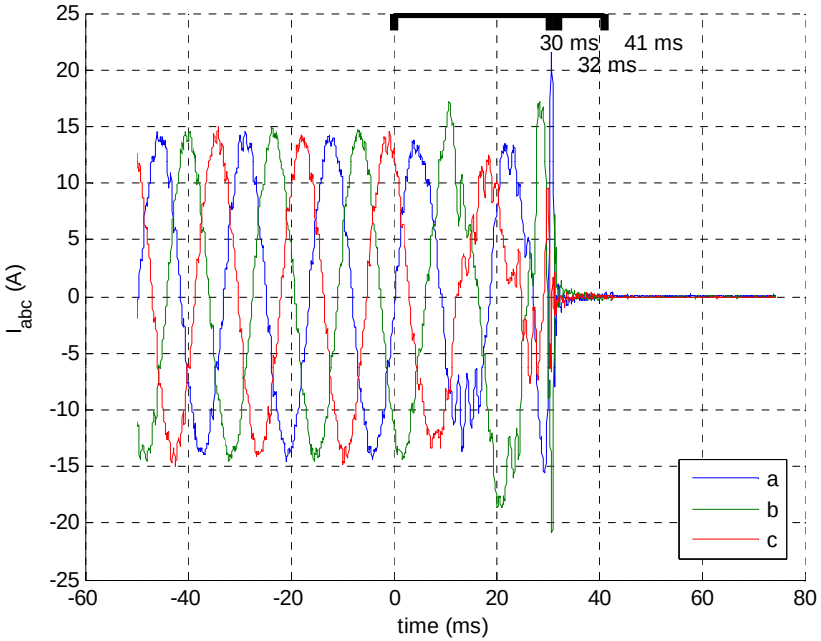


Three detection times shown are based on DC current, AC current, and AC voltage.

Time Domain Response with virtual Load Bank

- SMA Sunny TriPower 20 kW
- 8 kW, Qf = 1

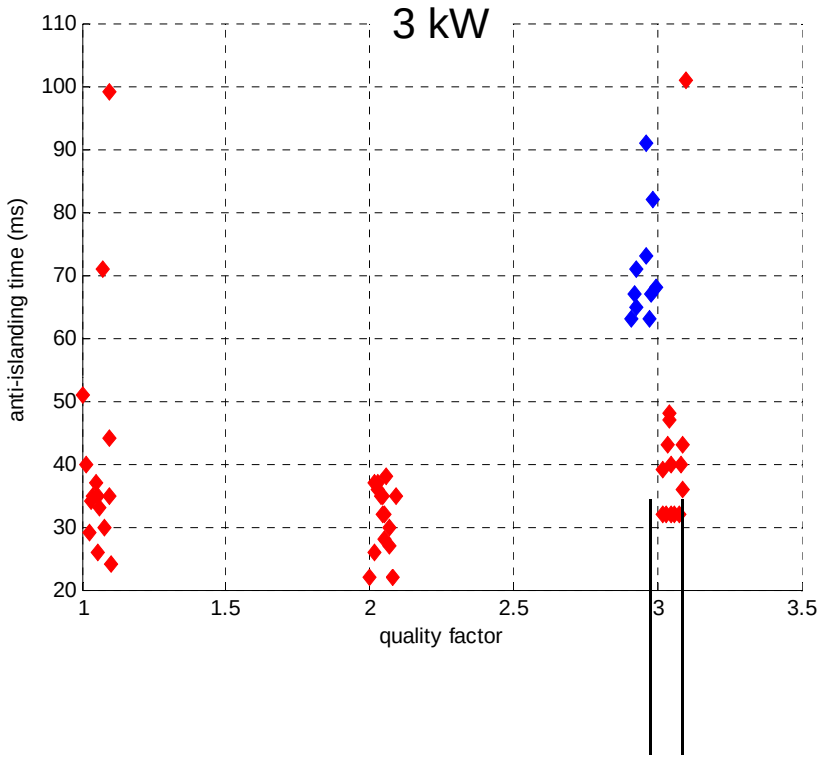




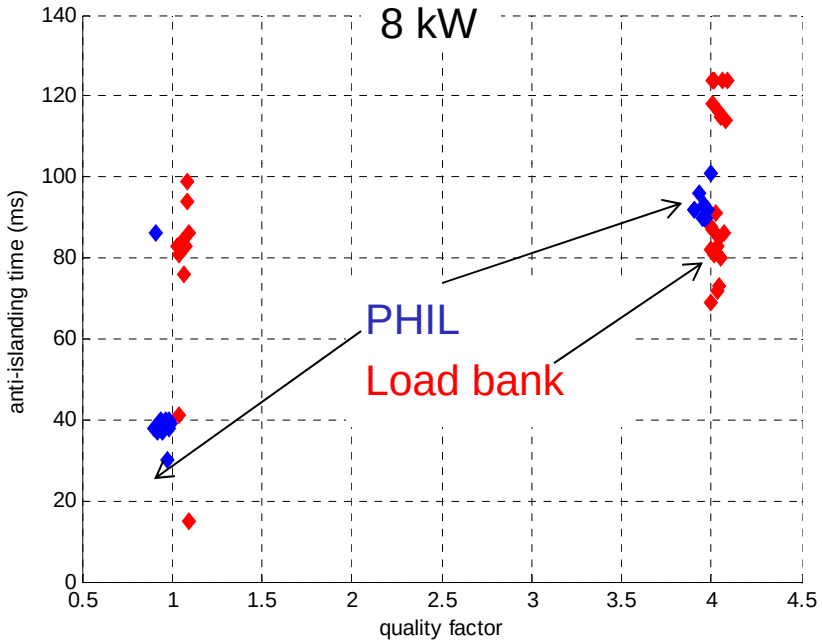
Three detection times shown are based on DC current, AC current, and AC voltage.

Test Results: Detection Times

- 15 tests at quality factors 1, 2, and 3
- Load bank tests vs. PHIL tests

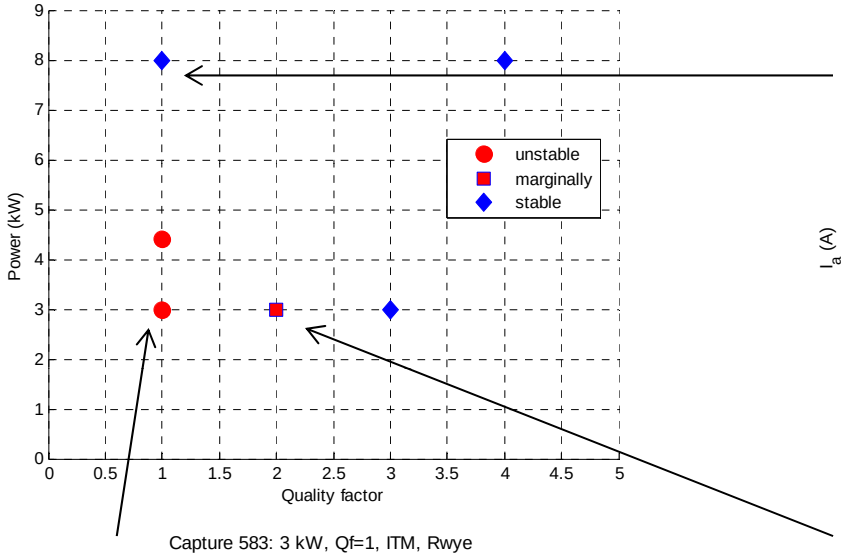


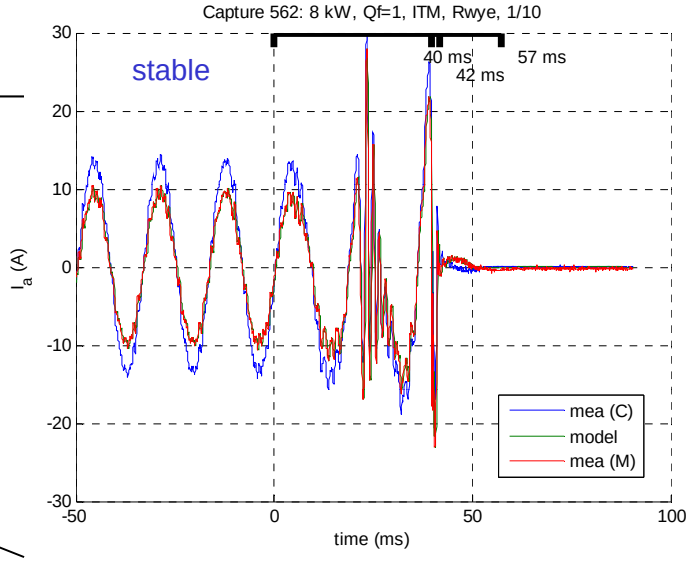
Artificial “spread” for plotting



Test Results: Stability Aspects

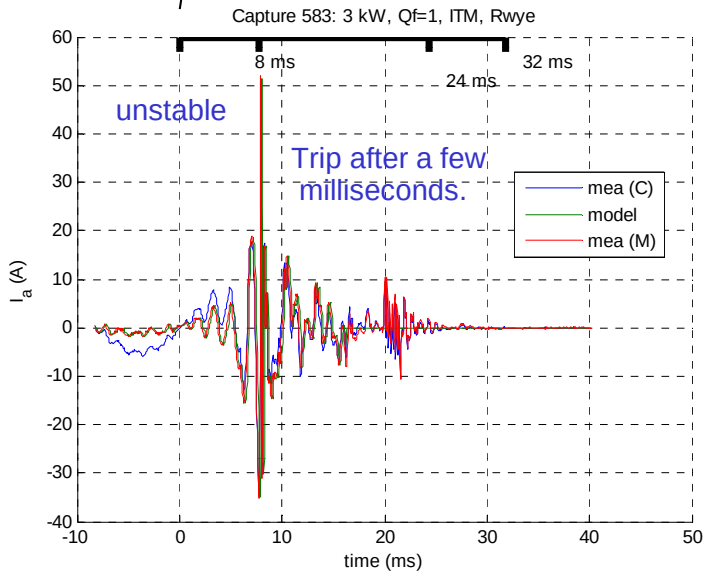
Probing for matching load bank tests

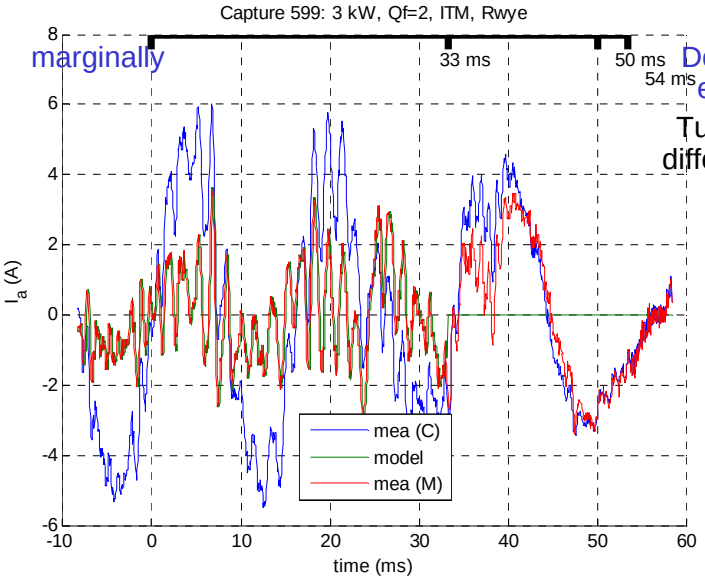




Matches expectations:

Similar to RLC load bank tests





Does not match expectations:

Turn-off too fast, different oscillation pattern

Summary and Outlook

- Feasibility of the PHIL approach demonstrated for anti-islanding with 20 kW unit
- Future: experiment with 60 kW Fronius unit
  - Better quantify accuracy and improve understanding of stability/feasible regions
  - Use alternative PHIL interface algorithms to increase region of stability
- Opportunities: Extend PHIL anti-islanding testing to MW scale power levels
  - Real cost benefit: no RLC load bank required
- Alternate test conditions (Rest-of-System)
  - More challenging and beyond RLC load bank
  - Is RLC load bank based anti-islanding realistic?