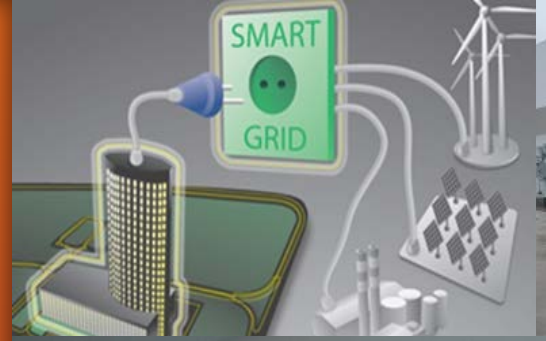






The eGRID Controller

CLEMSON UNIVERSITY
RESTORATION INSTITUTE

Driving economic growth, innovation, and workforce development for South Carolina

What is the Duke Energy eGRID?

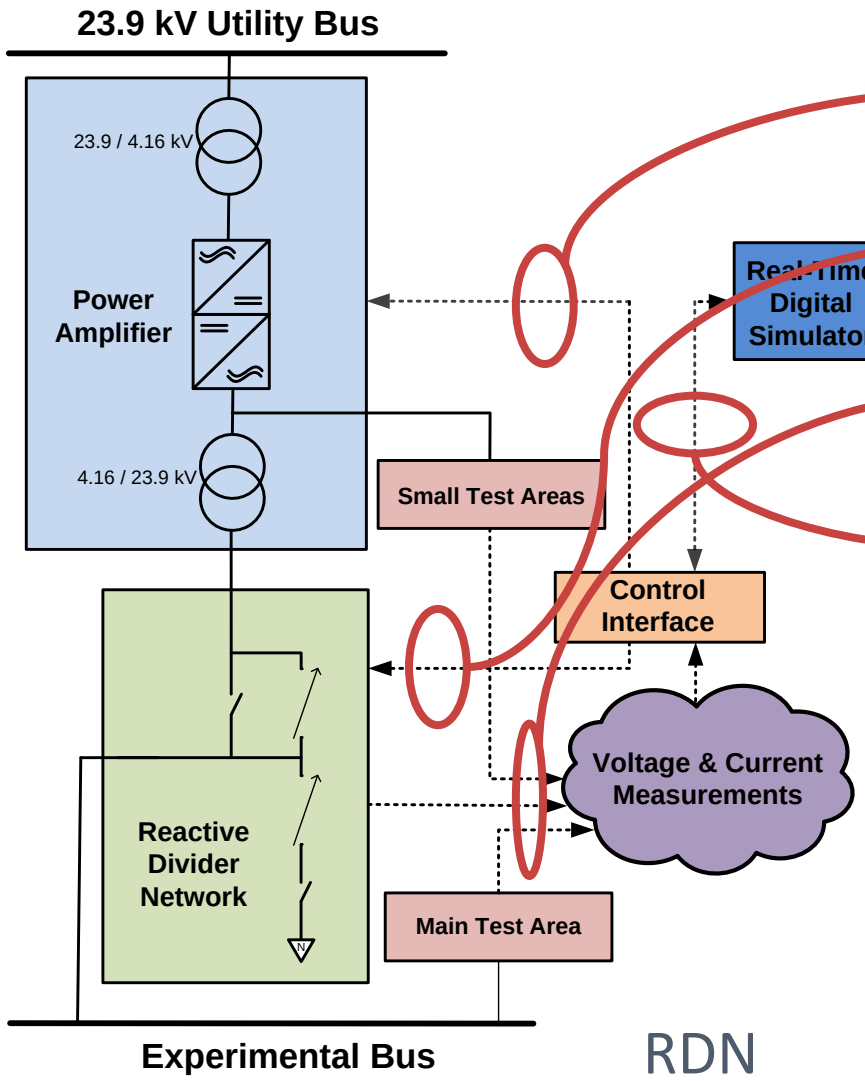
Electric
Grid
Research
Innovation and
Development

"eGRID is a utility-scale electric power laboratory combining real time grid simulation capabilities with a highly configurable, multi-megawatt, medium voltage three phase experimental grid."

The eGRID Center Team Members

Curtiss Fox, PhD	Director of Operations
Randy Collins, PhD, PE	Project Co-PI
Thomas Salem, PhD, PE	Research Scientist
Mark McKinney, PhD	Visiting Research Scientist
Ramtin Hadidi, PhD	Research Scientist
Eric Boessneck	Research Scientist
Benjamin Gislason	Research Engineer
Mark Milcetich	Electrical Technician
Tyler Vasas	Intern

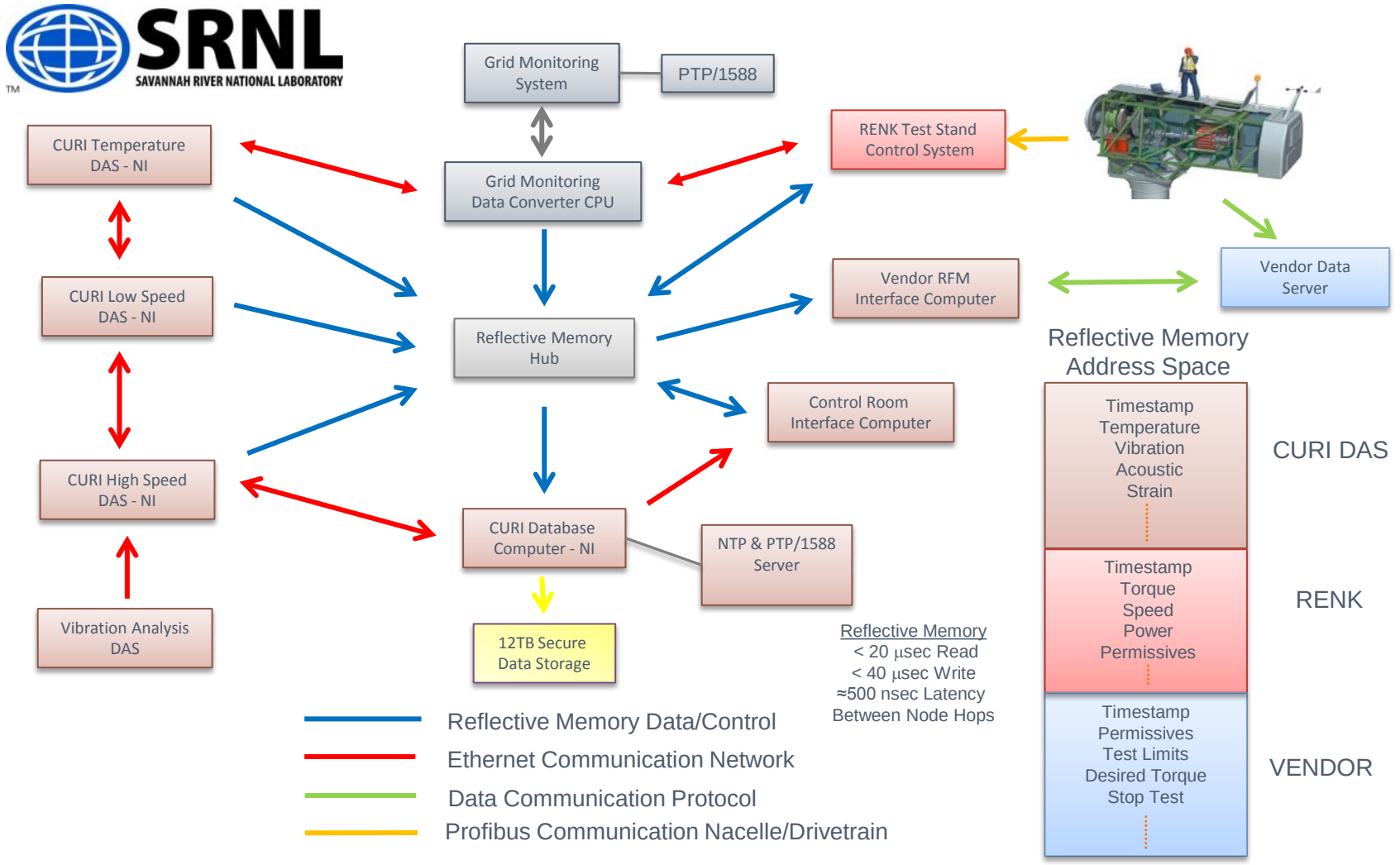
Control Interface of eGRID



RDN

- Send voltage setpoints to Power Amplifier
- Control Configuration of RDN
- Receive measured data from system
- Communicate with RTDS for HIL applications
- Provide a user interface
- Control SCR switches for fault testing
- Stream acquired data to RAID array

Initial Design Based on design of WTDTTF Data Acquisition and Communication System



Design requirements of Control Interface

- Communicate between various protocols such as DNP3 and Modbus in multiple time domains
- High-speed (up to 200kS/S) data acquisition
- Synchronization between multiple data acquisition channels
- GPS-synchronized time-stamped data for later analysis
- Ultra-low latency (<1mS) data for hardware in the loop control
- Easily reconfigurable and expandable to provide for multiple testing scenarios

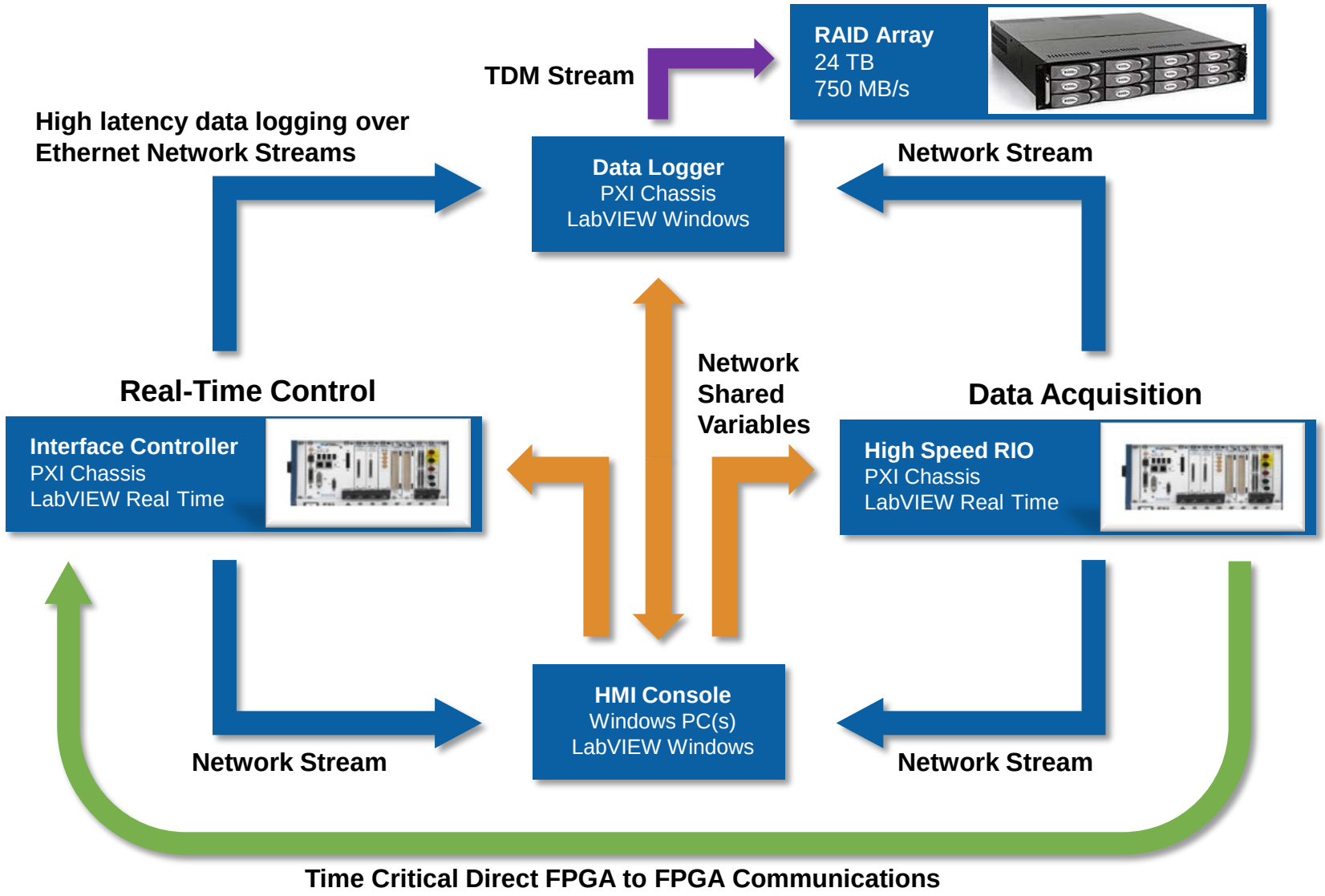
Architecture Selection

- National Instruments hardware
  - Real-time PXI chassis
  - FPGA data acquisition
- LabVIEW development environment
  - LabVIEW RT
  - LabVIEW FPGA
  - Power Analysis toolbox
  - Industrial Communications tools
- Fiber Optic serial communication
  - Custom built fiber system
  - Based on communication protocol for power amplifier

Components of the Control Interface

Chassis	Configuration	Function
HMI PC	Windows PC	• Main User Interface • Low speed control of other chassis • System configuration and monitoring
High Speed RIO	Real Time PXI Chassis	• High Speed data acquisition • Send time-stamped data to Data Logger • Send ultra-low latency data to Interface Controller
Interface Controller	Real Time PXI Chassis	• Send voltage setpoints to power amplifier • Generate waveform setpoints for open loop control • Interface with RTDS
Data Logger	Windows PXI Chassis	• Receive Data from High Speed RIO and Interface Controller Chassis • Write data to RAID array

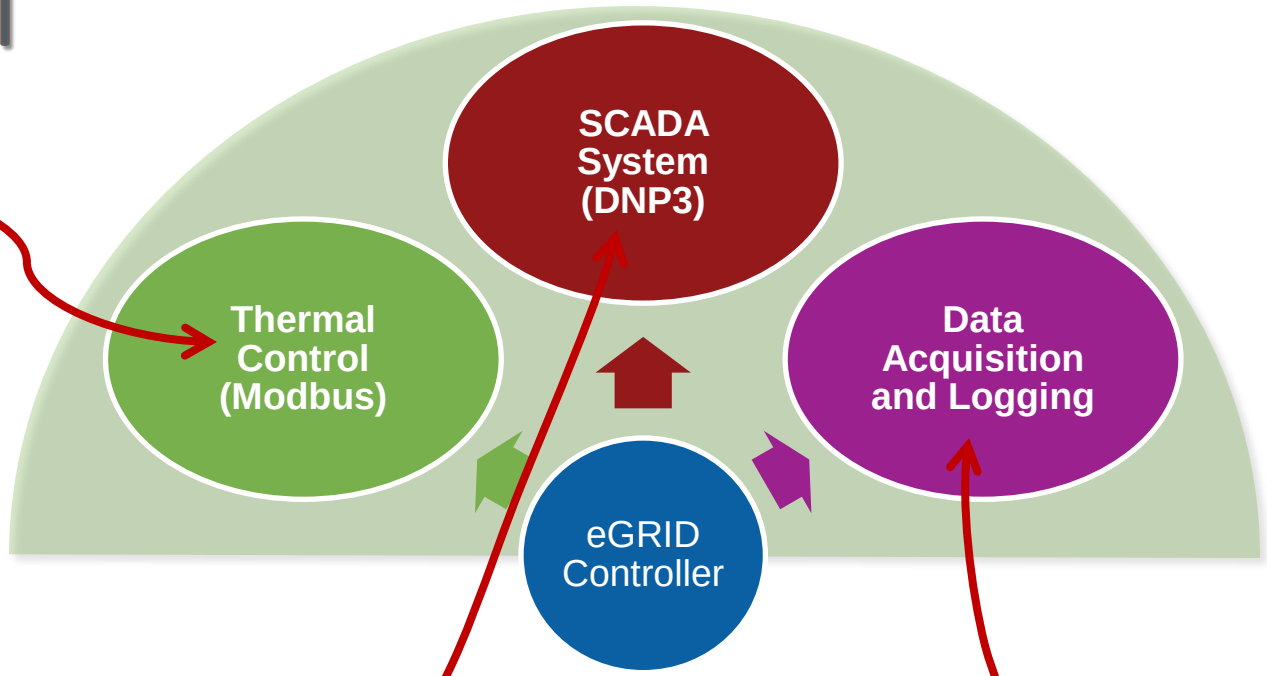
Components of the Control Interface



eGRID Communication

Non-time Critical

SCR and Resistor fan control and temperature monitoring

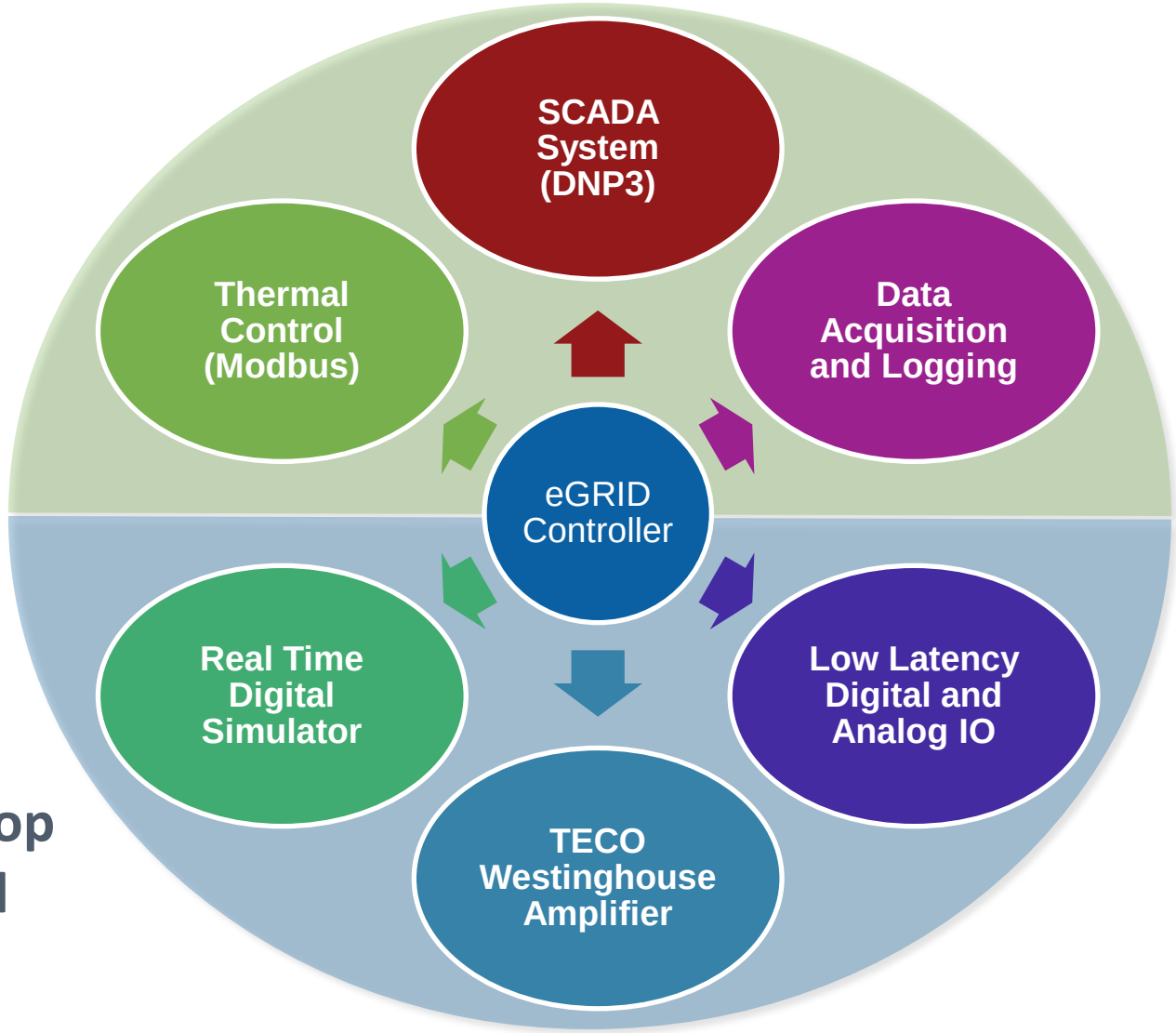


RDN Configuration:
sixteen single phase breakers
& nine motorized tap switches

Streaming of time stamped data to 24TB RAID array for later analysis

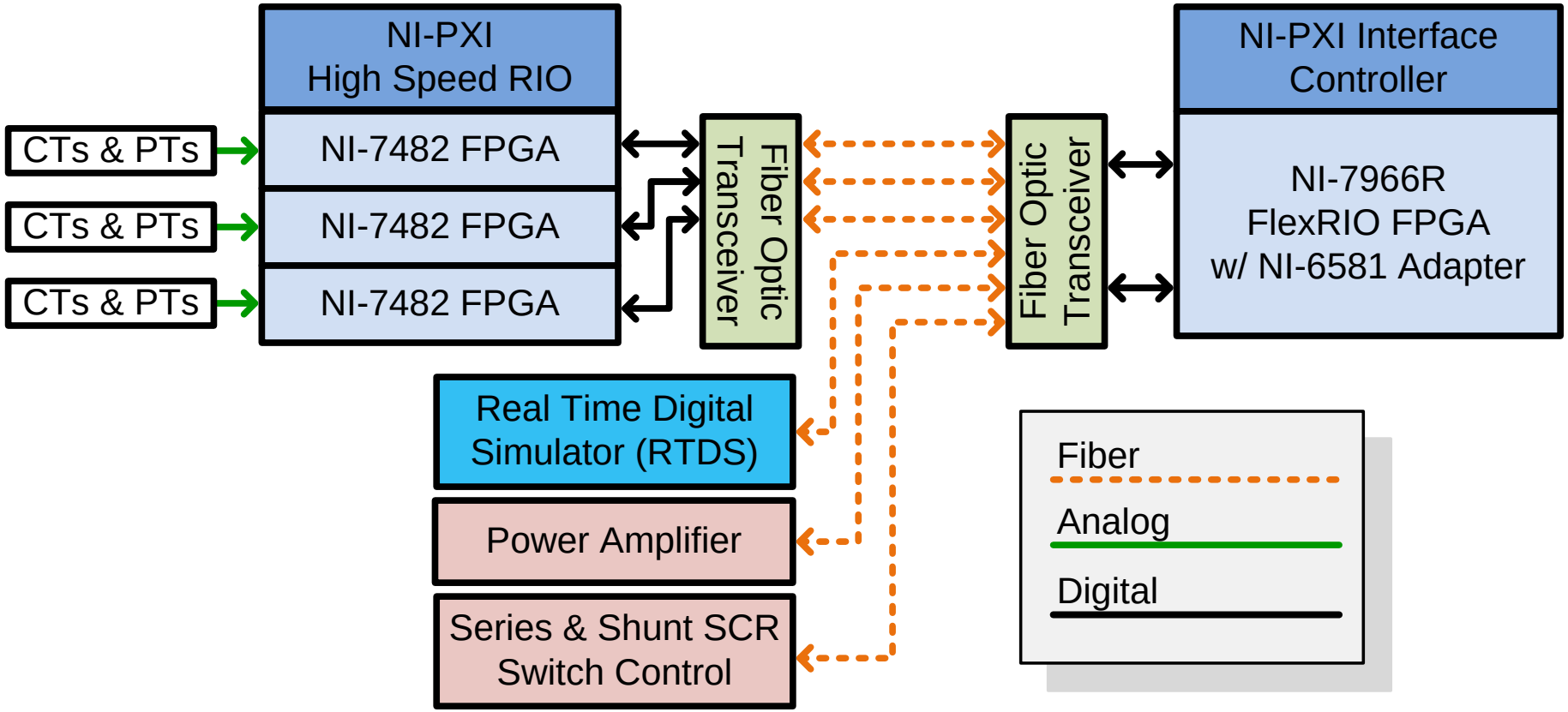
eGRID Communication

Time Critical



Hardware-In-the-Loop
Time Critical Control

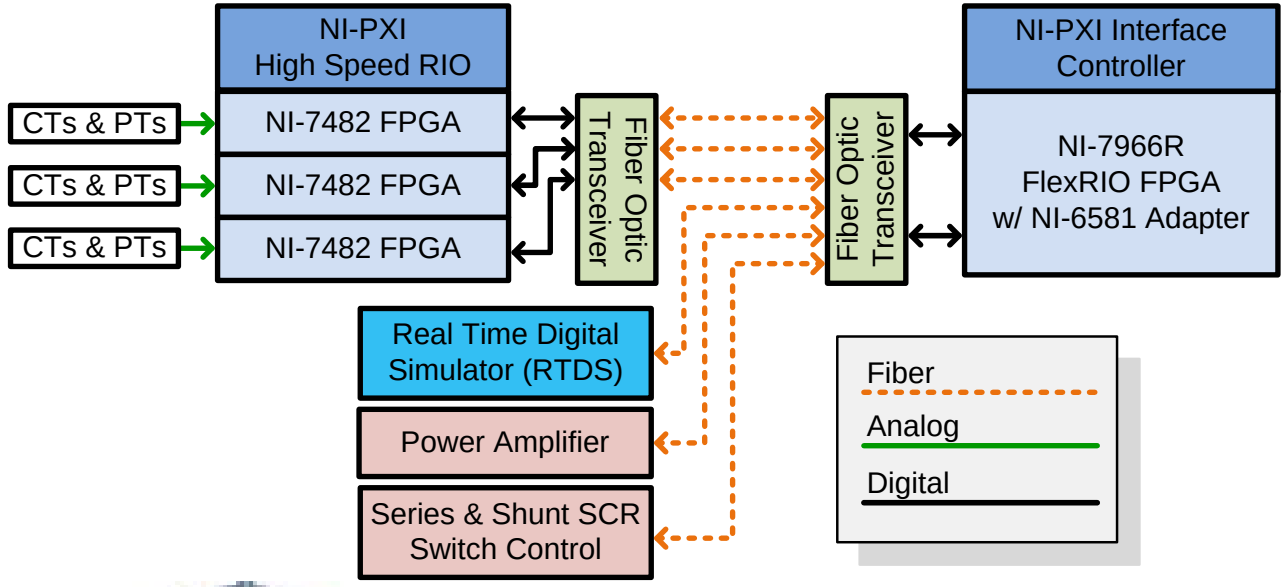
System Interfaces – Time Critical

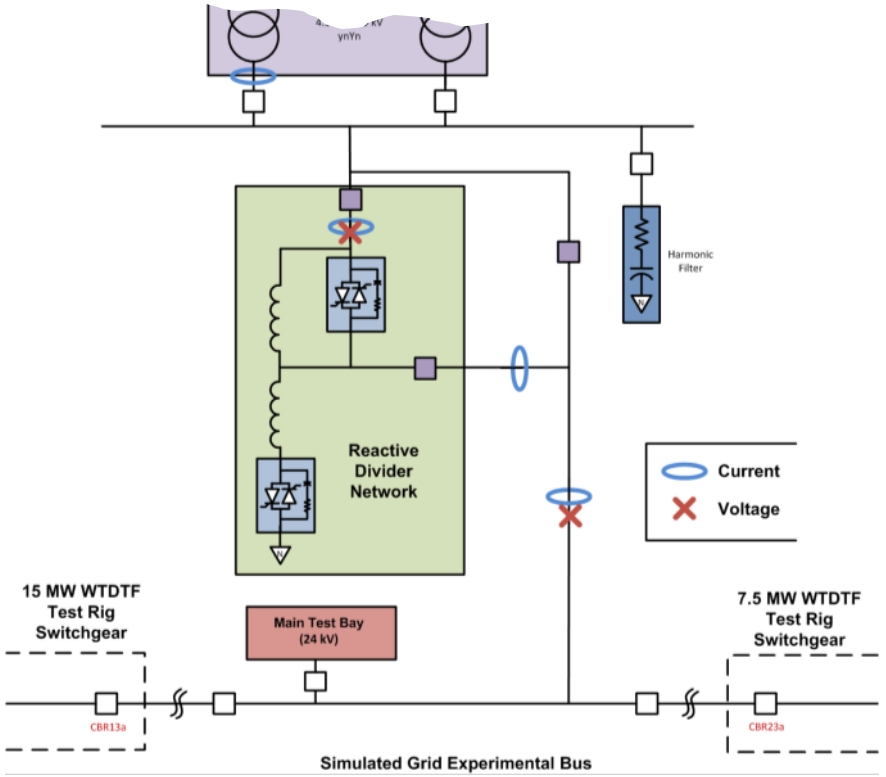


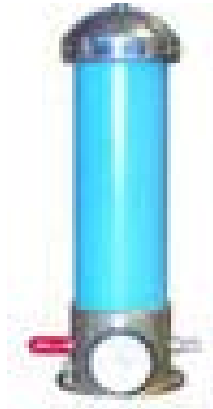
System Interfaces – Time Critical

DAQ System

- Rogowski Coils
- High Precision Voltage Dividers



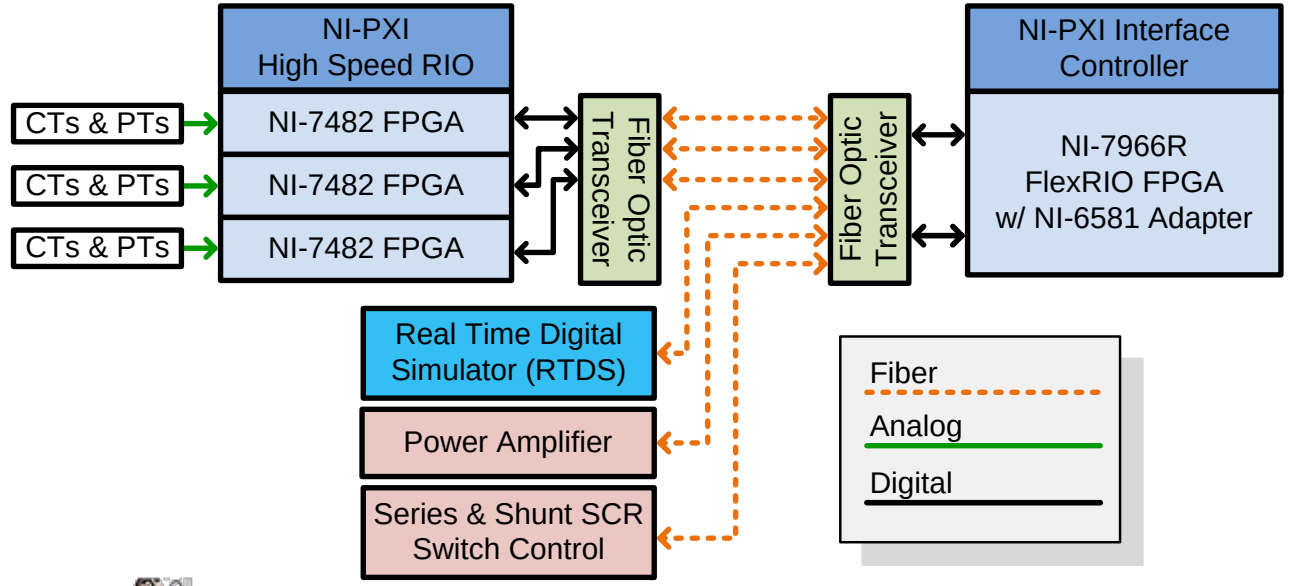




System Interfaces – Time Critical

DAQ System

- Three NI-7842 FPGA Cards
- 8, 16bit, 200kS/S AIs per card
- One card acts as master and asserts backplane PXI trigger
- Other two FPGA cards acquire based on PXI trigger
- <5nS propagation delay



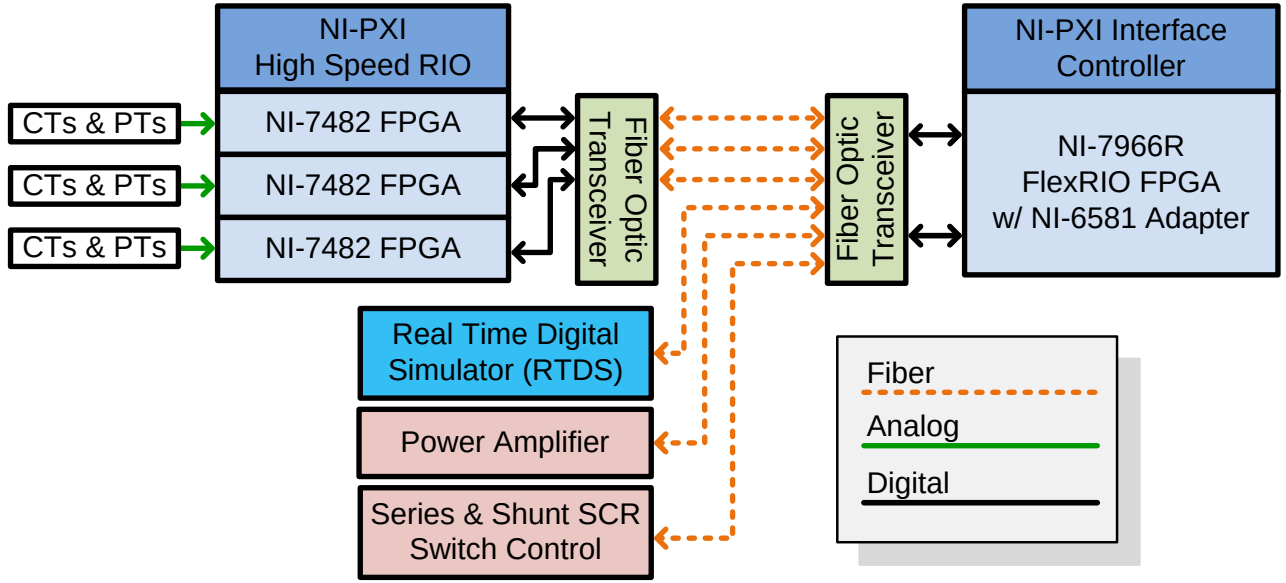
Time Stamp System

- NI-6682 Timing Card
- Disciplined to 1588 GPS grandmaster clock
- Acquires time stamps on PXI trigger
- FPGA FIFOs ensure no lost data and time stamp synchronization

System Interfaces – Time Critical

Fiber Optic Link

- 16 full-duplex plastic optical fiber (POF) channels
- Validated UART at 40 mega baud
- Interface Controller communicates over fiber with with:
  - TWMC Master Controller
  - RTDS
  - High Speed RIO FPGAs
  - Solid state thyristor switches



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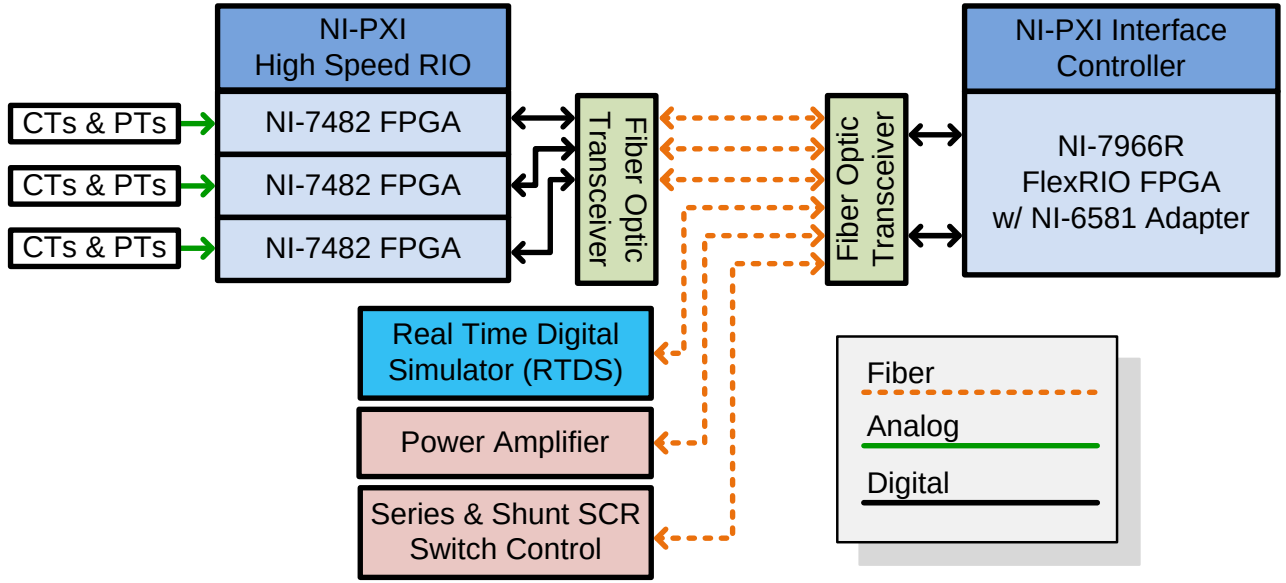
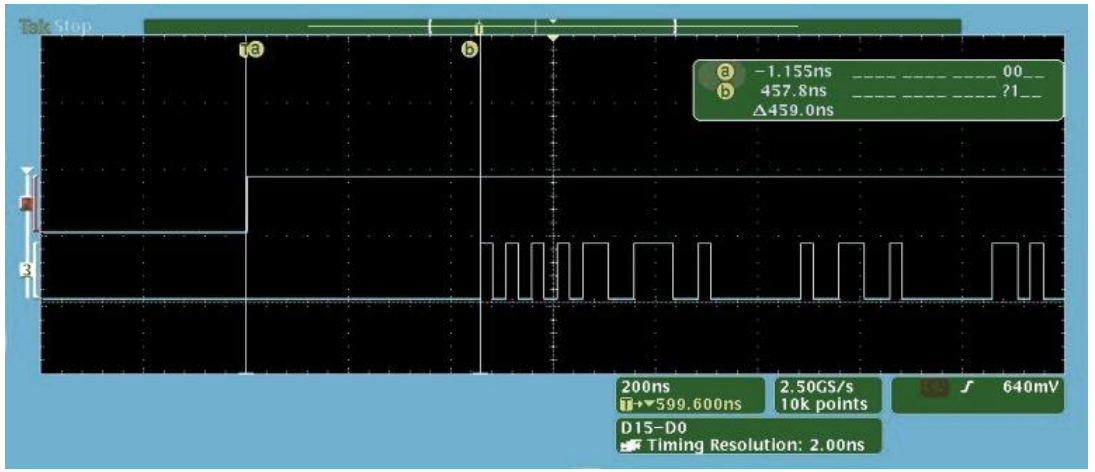
System Interfaces – Time Critical

Fiber Optic Link

- Custom serial communication system based on Power Amplifier protocols for communication between:
  - HS-RIO & Interface Controller
  - Interface Controller & RTDS
  - Interface Controller & Power Amplifier
- Includes error checking and lost packet detection
- Interface Controller sends sync signal and HS-RIO encodes latest data and transmits
- <500nS latency from sync signal to start of packet transmission

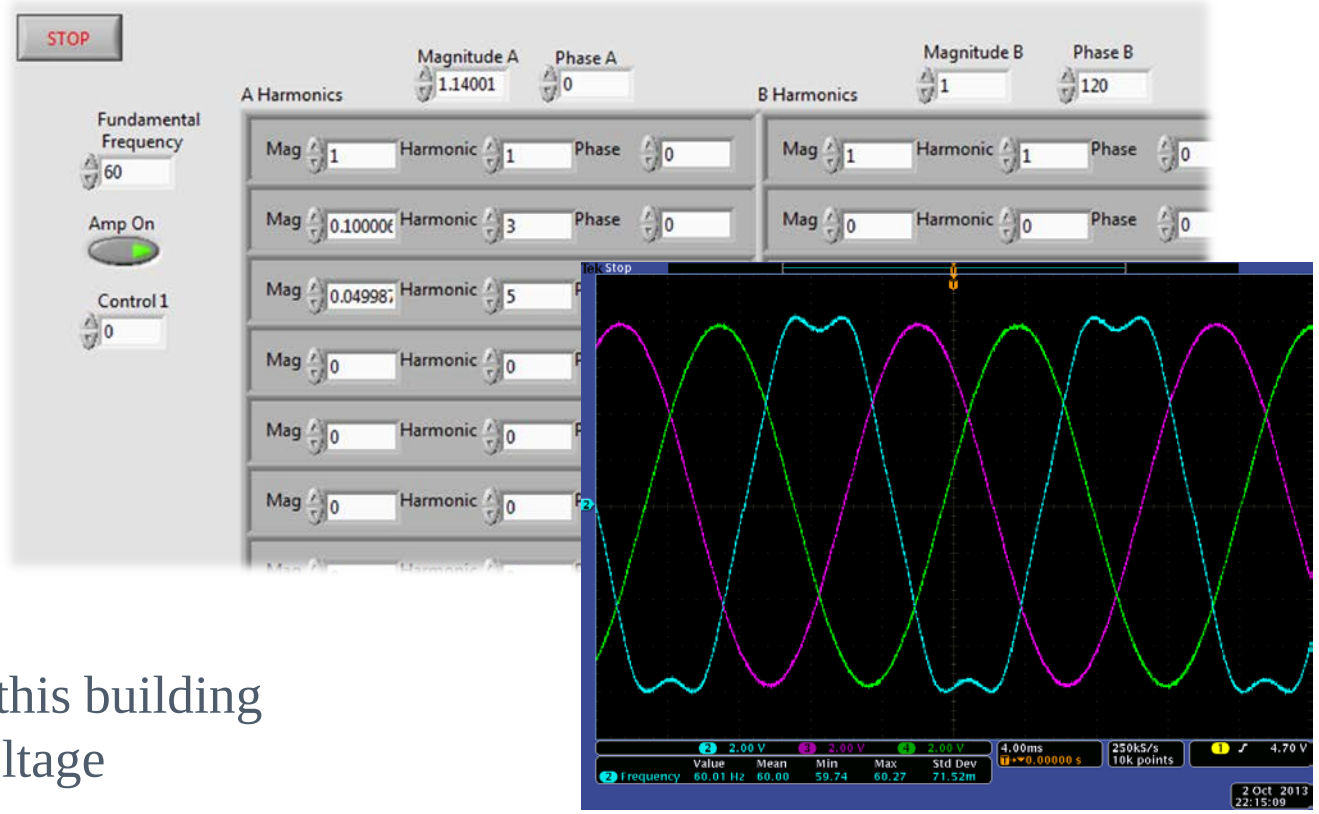




System Interfaces – Time Critical

Open Loop Control

- Power Amplifier sends 12kHz sync signal to Interface Controller
- Interface Controller sends three-phase voltage setpoints to power amplifier
- Fundamental waveform generation block implemented in hardware on Interface Controller
- Independent phase, magnitude, and harmonic control
- Frequency controllable to 1mHz
- HMI-PC will be able to send values to this building block to have dynamically changing voltage waveforms



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System Interfaces – Time Critical

Closed Loop Control

15 MW
TECO-Westinghouse
Power Amplifier

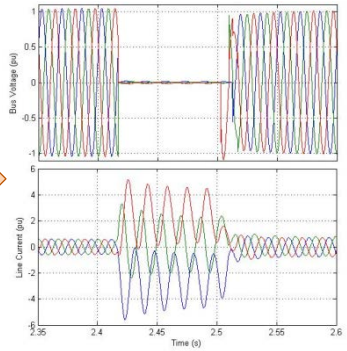
Voltage and Current
Set Point Commands

Interface Controller

BUS #N
Voltage and Current
Information

Real Voltages and Currents
associated with ***BUS #N***

Device Under Test



Real Voltage and
Current Measurements

RTDS®

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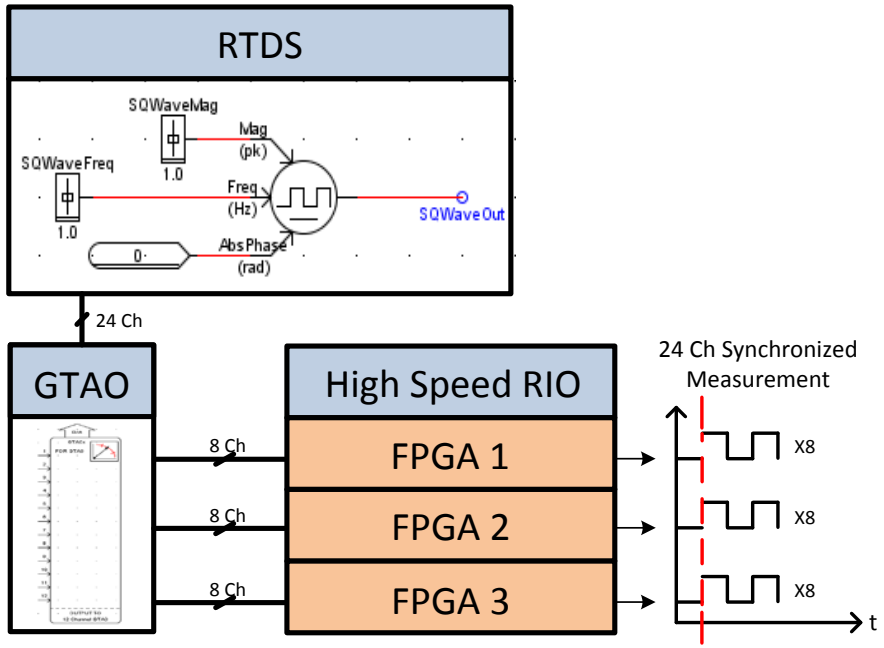
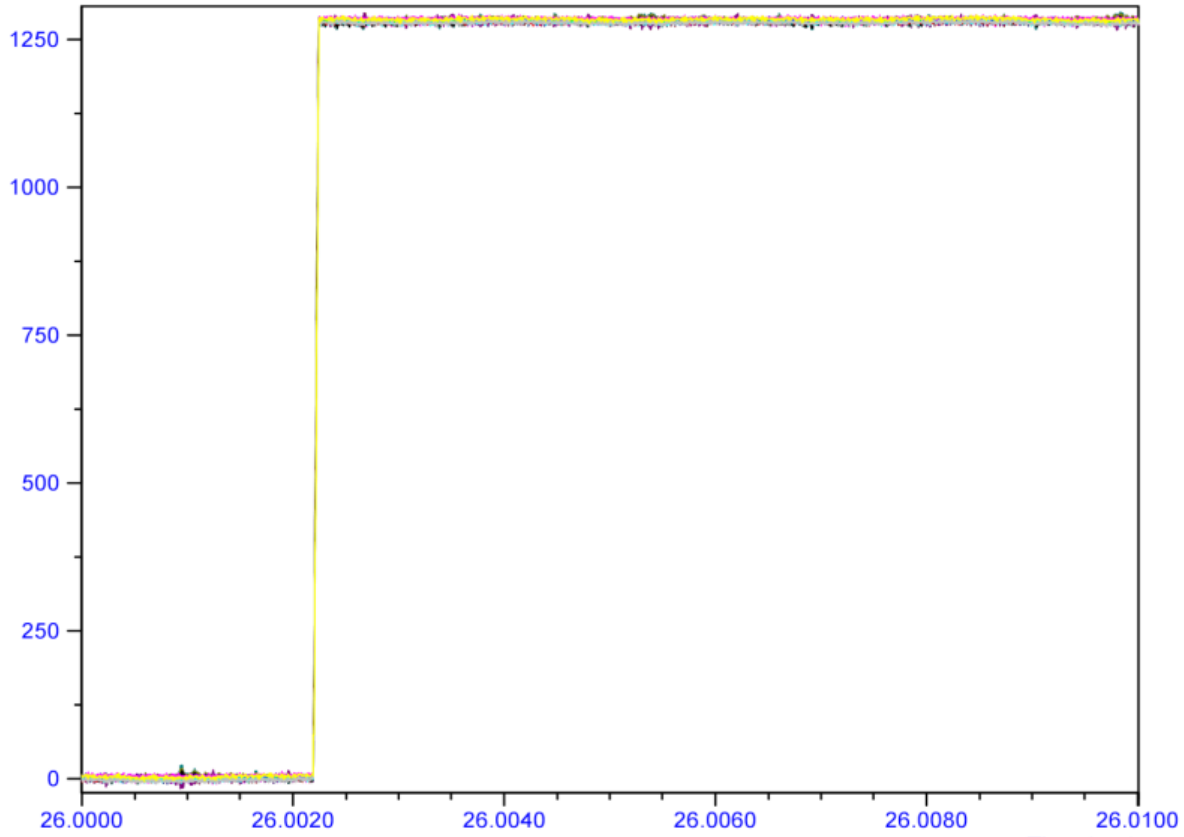
Benchmarking – DAQ Synchronization

- RTDS generates 24 simultaneous square waves, 12 per GTAO card
- All 24 square waves sent to AI inputs on FPGA DAQ cards, 3 cards at 8 inputs per card
- Sampled at 200kS/S, time stamped and sent to the data logger



- All 24 channels plotted
- 10mS of data, sampled every 5uS (200kS/S)
- All 24 channels transition in one time step



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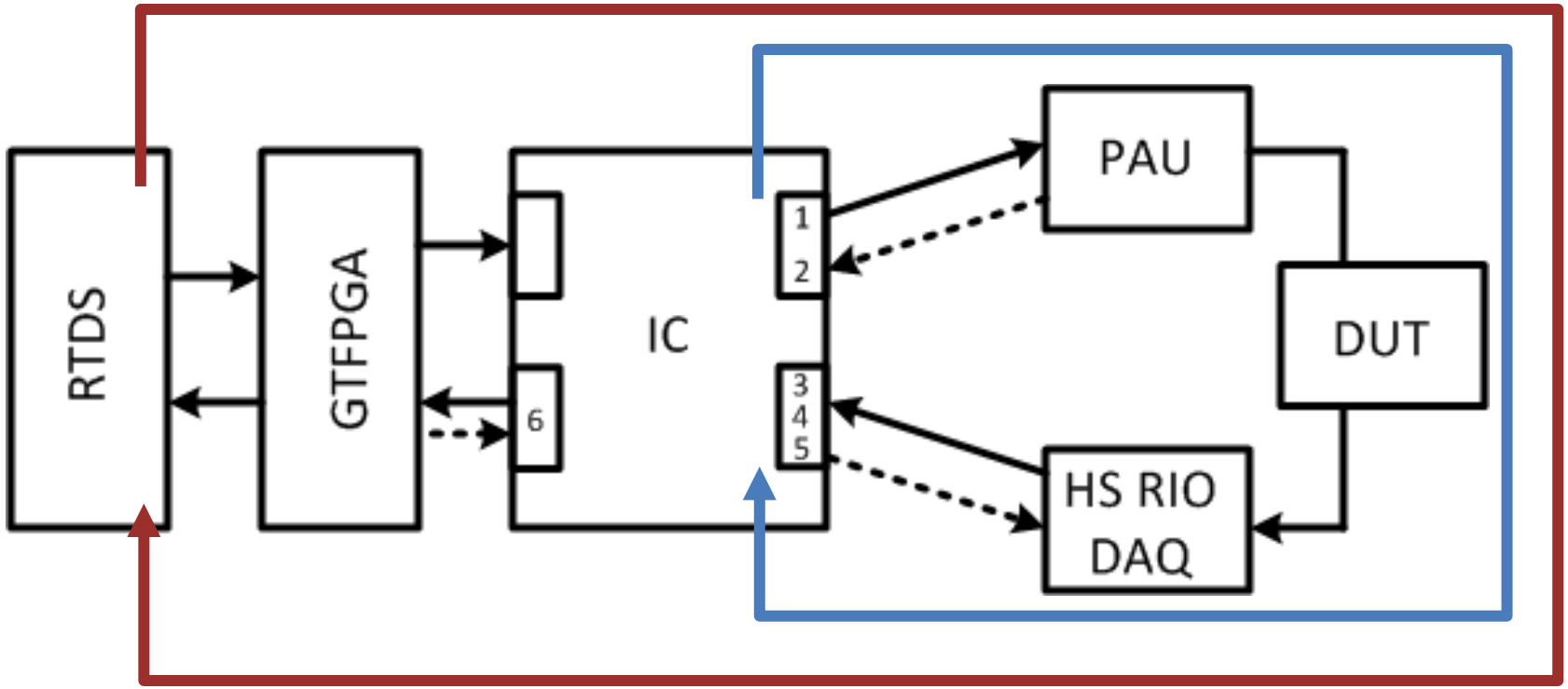
Benchmarking – System Latency

- System latency must be low for hardware in the loop operation

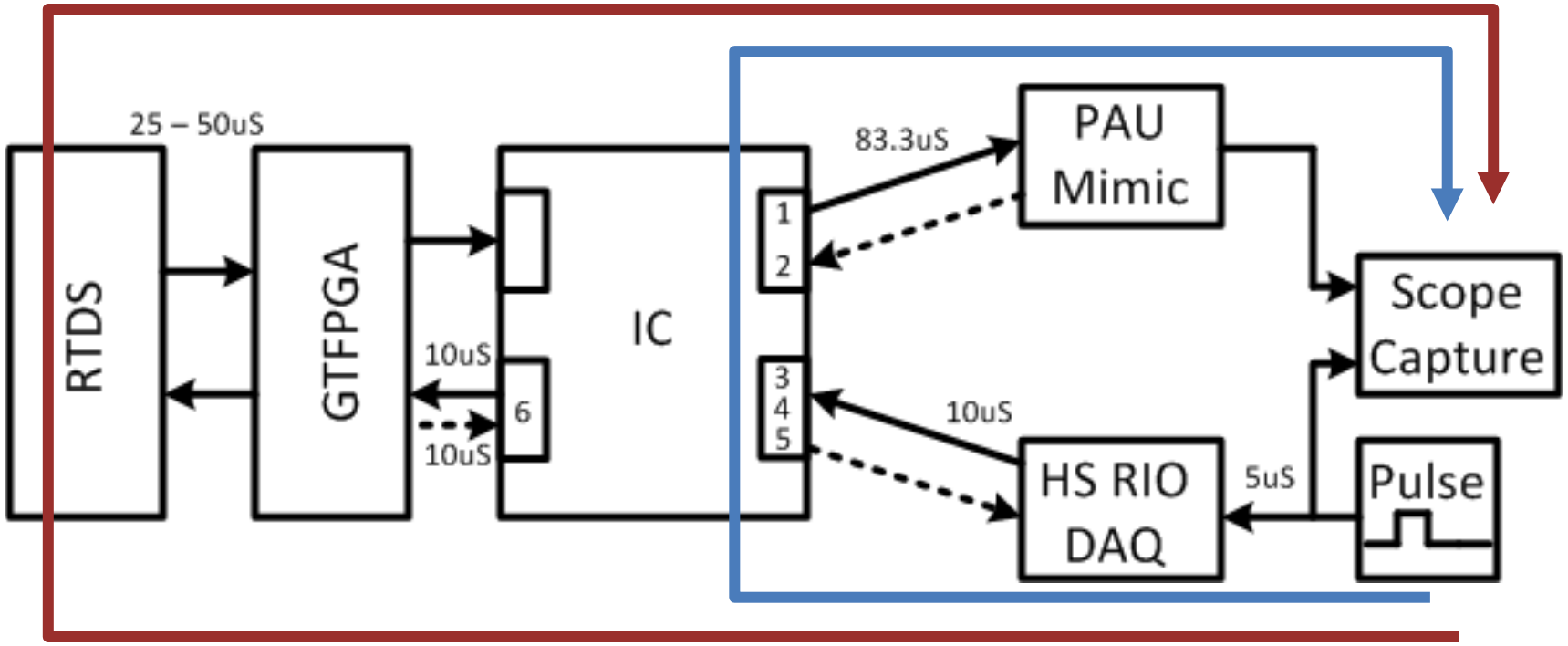
- Test 1: Time from voltage setpoint change to measured output change

- Test 2: Time from RTDS computed voltage to output change detected at RTDS



Benchmarking – System Latency

- PAU latency mimicked in software
  - Decodes packet
  - Asserts DIO line
- Pulse injected at DAQ input of HS-RIO
- Two tests:
  - Looped straight through Interface Controller
  - Routed through RTDS
- Scope capture of loop time



Benchmarking – System Latency

Open Loop Test

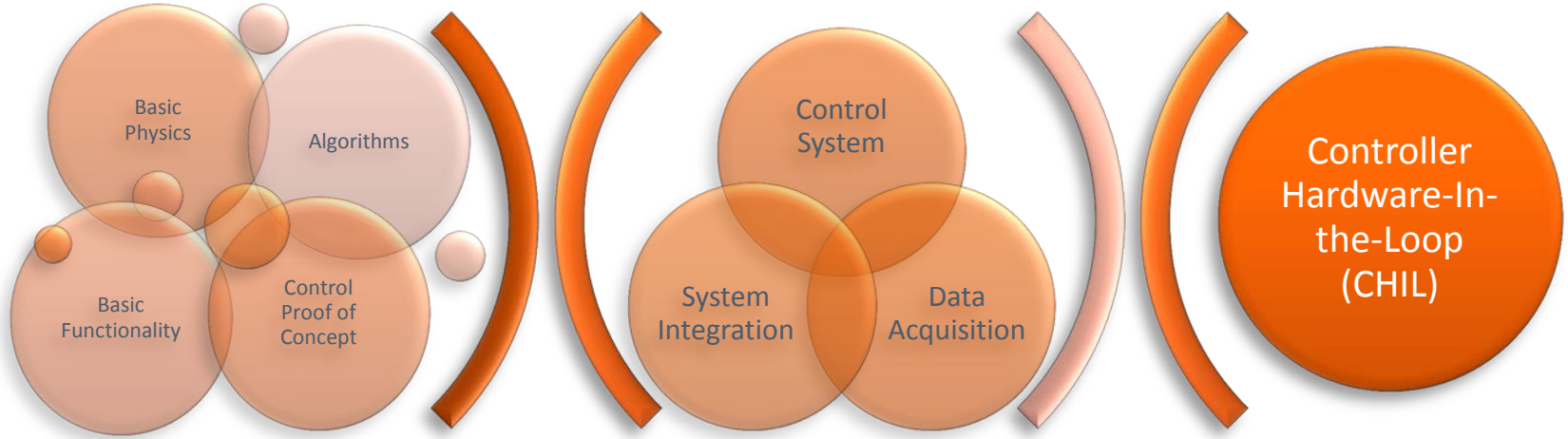
Benchmarking – System Latency

Closed Loop Test

Controller Hardware in the Loop

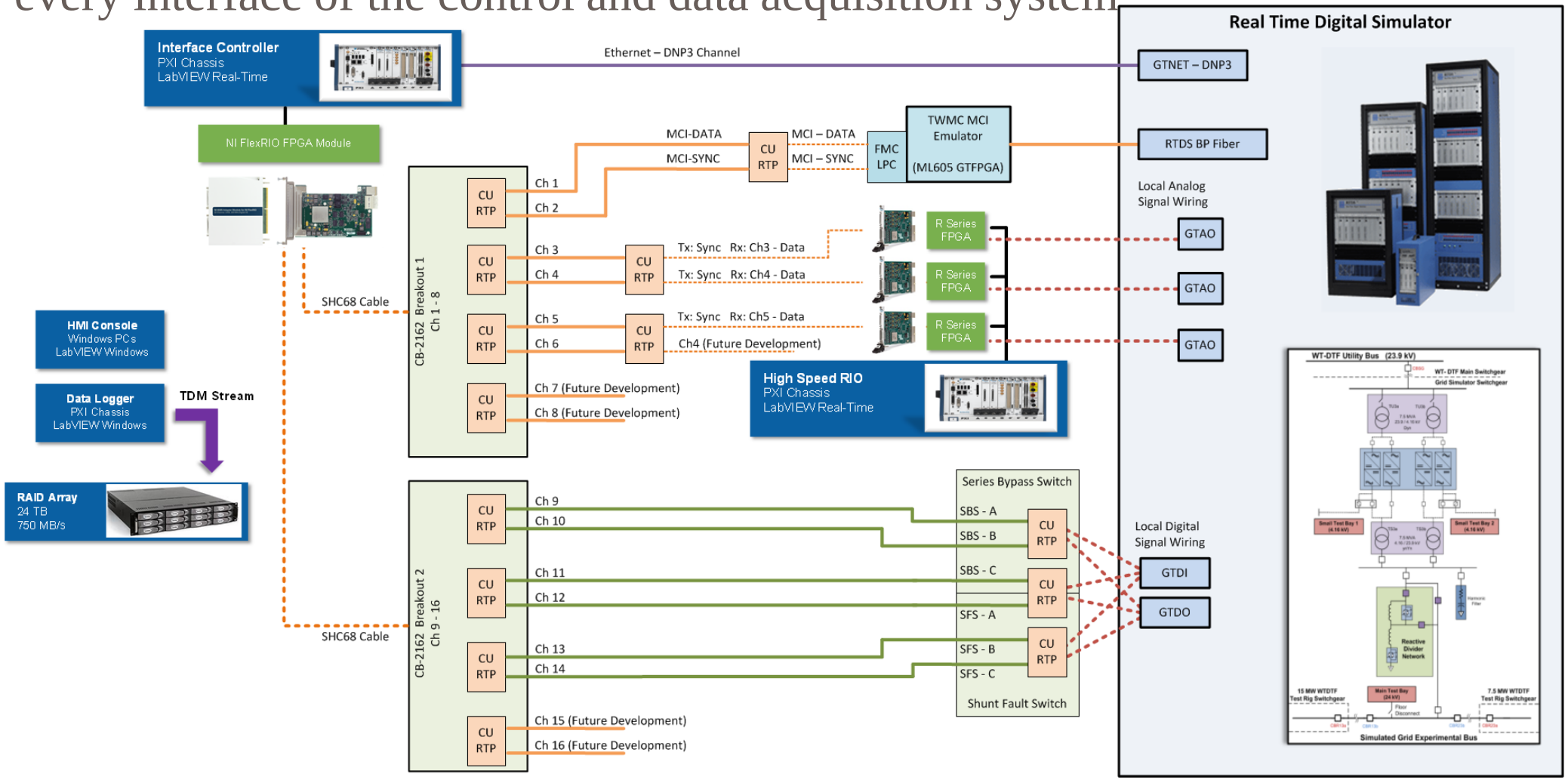
Robust controller and system testing is required for:

- Control algorithm verification and turning
- Startup and operational procedures
- Emergency stop conditions and shutdown methods
- Identifying commissioning activities and protocols
- Development and testing of new testing protocols
- Initial verification of Power Hardware-In-the-Loop (PHIL) experiments and operation
- Human Machine Interface design



Controller Hardware in the Loop

Complete system testing encompasses the simulation
of every interface of the control and data acquisition system



Thank You