Asymmetrical Fault Generation with Clemson Grid Simulator

4th International Grid Simulator Workshop
NREL ESIF
Golden, CO

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TWMC Power Amplifier Units

4 Power Amplifier Units (PAUs)
8 Slices Per PAU

3 Cubes Per Slice
TWMC Power Amplifier Units

Series connecting slices

Cubes isolated to 15 kV
4 series for 3100 V L-N
4.16 kV + 30% overvoltage capability (non-clipped)
Repurposing one PAU for DC leaves others to perform AC grid emulation.

5 MVA PAU (2 x 2.5 MVA)

20 MVA total

PAU1

PAU2 w/ extra stage for DC output (inverter testing)

PAU3

PAU4
Zero-sequence carried through to DUT

- Wye filter
- (3) Single-phase step-up transformers 4160/23.9 kV
PAU Filter Scope Captures

Waveform synthesis

Generating intentional 5th harmonics

DUT @ 1.5MW

Ch3: Phase C
**Waveform Synthesis**

[1] Packets sent every 83us (12 kHz), 200 pts/cycle

[2] Each packet: Dan, Dbn, Dcn directly to modulator (D: duty)

Phase-shifted carrier for SCHB, double-edge PWM sampling [2]

Cases for (a) 600 Hz (b) 1500 Hz (c) 2000 Hz carriers
12 kHz packet timings shown as vertical lines

Recall: 9-level SCHB has 8x $f_{sw}$ effective multiplier

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Test Configuration

- **CB PAU 1**
- **CB PAU 2**
- **PAU 1**
- **PAU 2**

**eGRID DC Supply**

- **7.5 MVA**
- **4160 V**

**0-1000 V_{dc}** configuration:
- 2500 A_{dc} continuous
- Isolated (floating) output
- Grounded within inverter under test.

**Test data is from this bus**
CA Rule 21 Voltage Ride-Throughs

- HV1: within 0.16 s drop to < 10% current
- Nominal: indefinite operation
- HV2: within 0.16 s drop to < 10% current
- LV1: maintain > 80% current
- LV2: maintain > 80% current
- LV3: within 0.16 s drop to < 10% current
**L-L: 2000 kW, 0 Vpu, 2000ms**

SOGI enabled for this test (sat. mitigation).

Still reaches desired voltage within 1 cycle.

IC datalog of commands to PAUs

4160V bus voltages LN

Inverter voltages LL

Vcn channel was moved to different measurement for this test.
Voltage within LV2 region for CA Rule 21: ride through with > 80% pre-disturbance current.

4160V bus
Van, Vbn, Vcn

4160V bus
Ia, Ib, Ic

INV bus
Vab, Vbc, Vca

INV bus
Ia, Ib, Ic
Ideas for Best Practices Development

» Which bus is the PCC? LV (inverter terminals) or MV
  > If LV, need to compensate for MVT or other passives (grid sim topology dependent)
  > If LV, considerations for transformer saturation mitigation without compromising voltage waveform requirements

» SRD’s with VAR requirements for ZVRT
  > Grid simulator method for ZVRT still has passive impedances ex. 5% impedance transformer, inverter required to push 1pu current for ZVRT How strict on “zero volts” is the ZVRT test? Is V < 5% close enough?

» IEEE 1547.1 HIL subgroup
  > Karl Schoder chair, Jesse Leonard co-chair
  > At a minimum, the whole 1547.1 WG needs more insight on grid simulators, HIL work should be on top of that (prevent more tests added with RLC banks)
  > Software/HIL RLC islanding testing: what if the inverter doesn’t pass?