NovaCor™

A revolution in real time.

Advanced PHIL Applications using the RTDS™

RTDS Technologies

Presentation Outline

Introduction

PHIL for a PV Micro Inverter

PHIL Applications by RTDS Users

Key Factors for PHIL Simulation

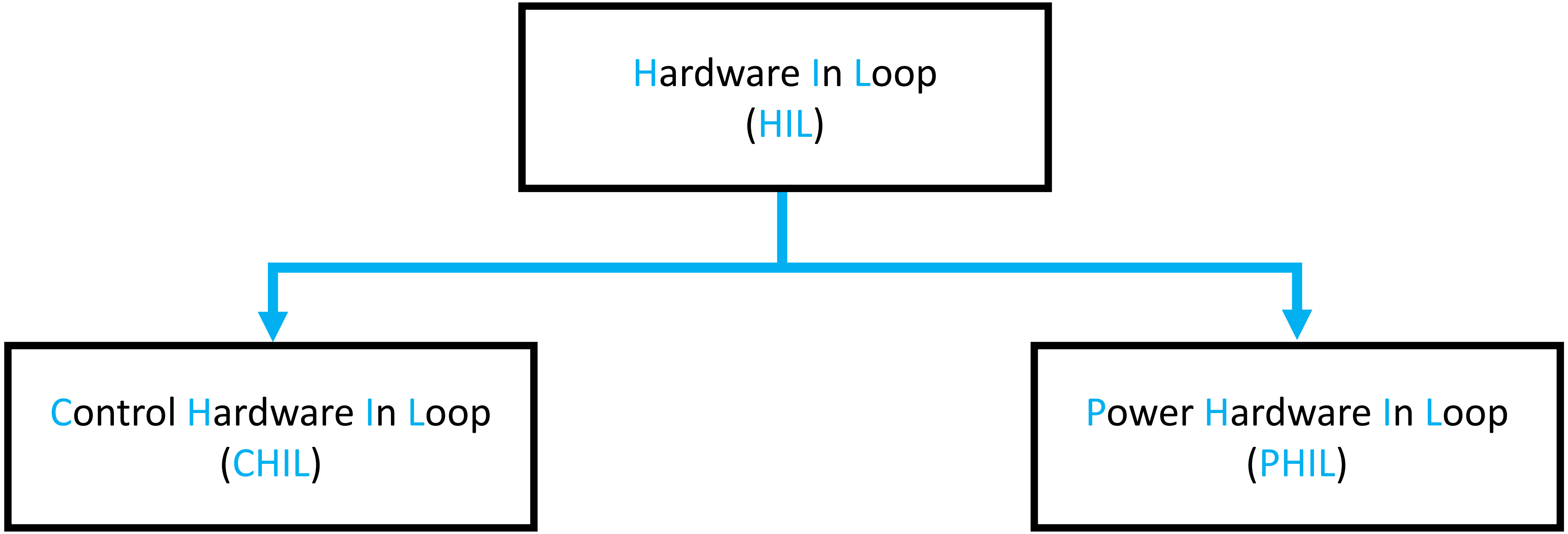
Hardware Developments

Software Developments

Conclusions

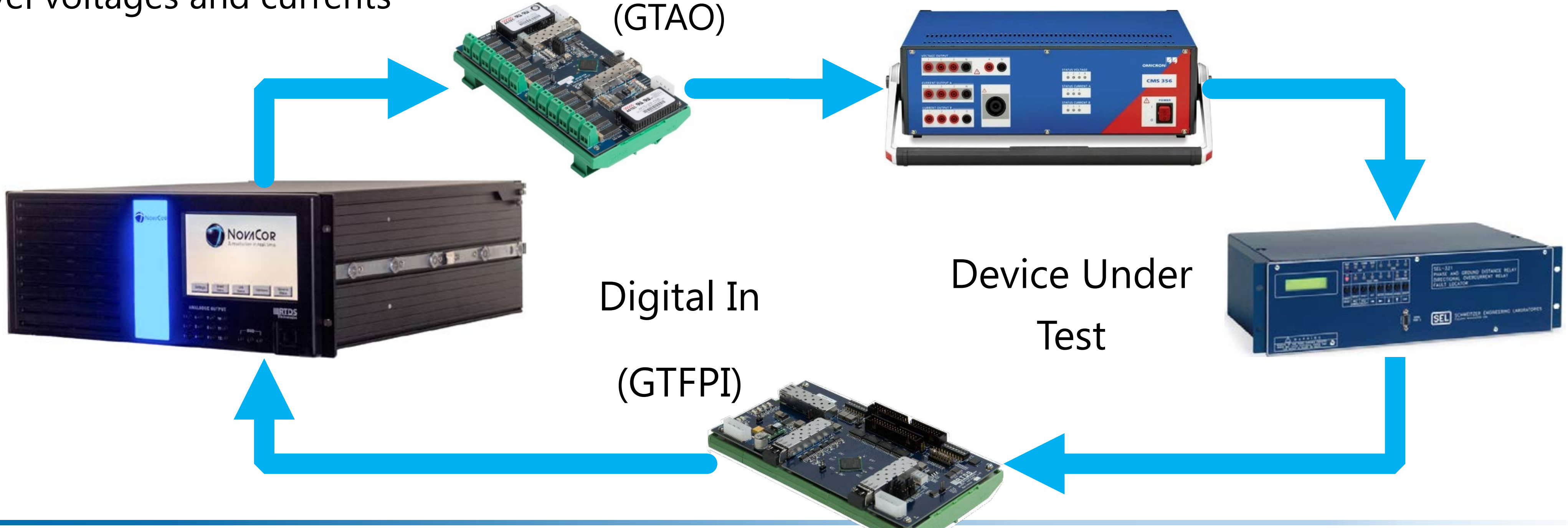
RTDS Technologies

Introduction



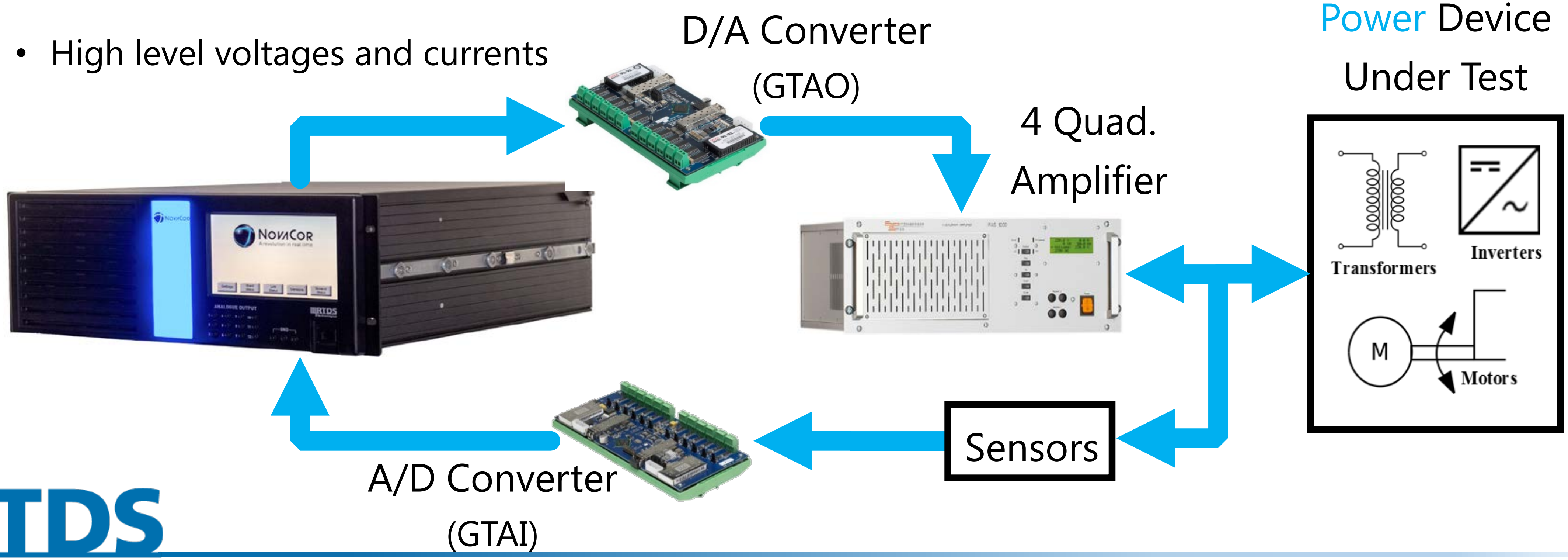
Introduction

- In CHIL,
  - Entire power system is modeled in RTDS
  - No power exchanged over interface
  - Low level voltages and currents



Introduction

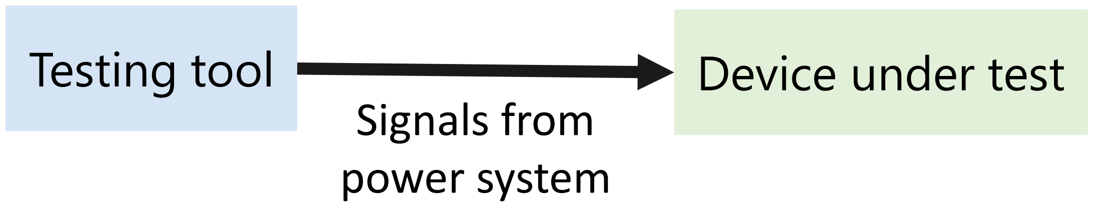
- In PHIL,
  - A portion of the power system is modeled in RTDS
  - Power exchange via 4 quadrant amplifier
  - High level voltages and currents



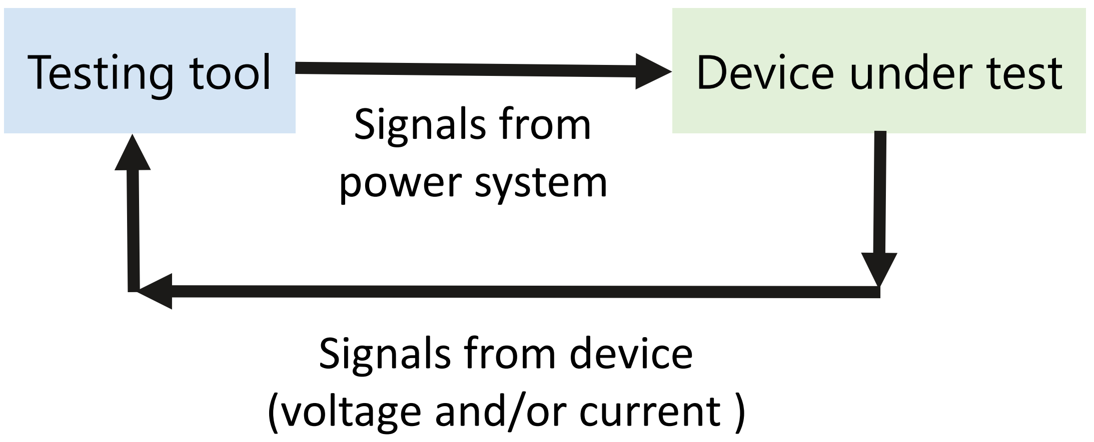
Introduction

- Some applications might consider open loop as PHIL
- Challenges comes from closing the loop for kW to MW range
- All further discussions are referring to Closed Loop PHIL

Open Loop

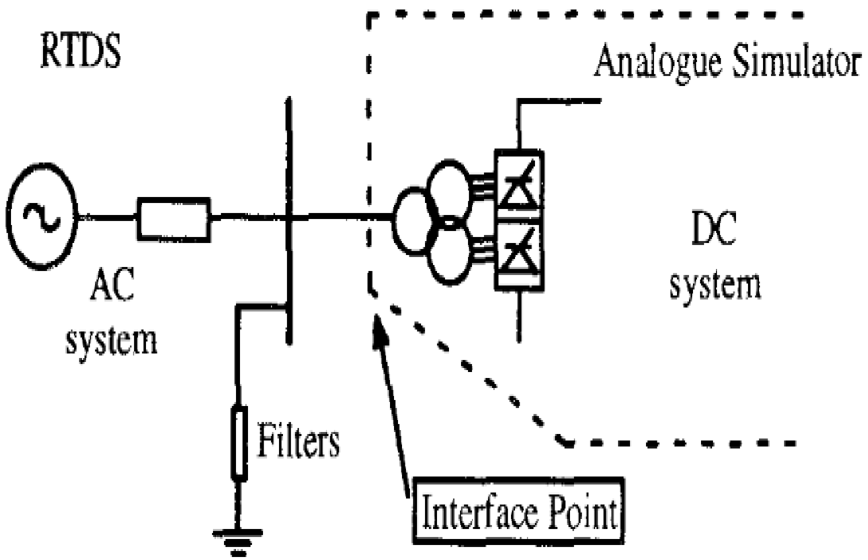


Closed Loop



Introduction

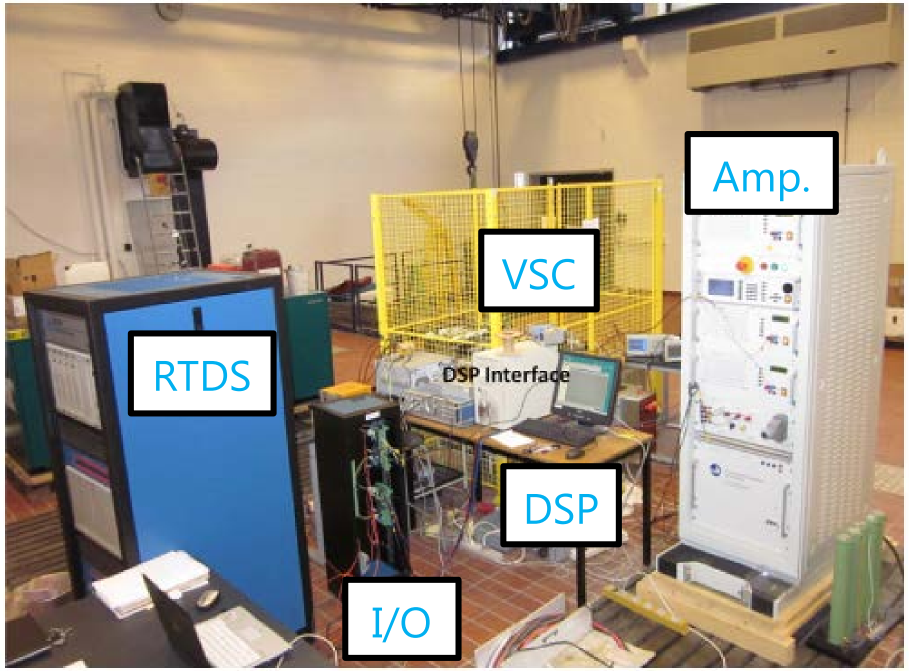
- First RTDS PHIL application used to expand an Analogue HVDC Simulator



Kuffel, R.; Wierckx, R.P.; Duchen, H.; Lagerkvist, M.; Wang, X.; Forsyth, P.; Holmberg, P., "**Expanding an Analogue HVDC Simulator's Modelling Capability Using a Real-Time Digital Simulator (RTDS)**," in *Digital Power System Simulators, 1995, ICDS '95., First International Conference on* , vol., no., pp.199-, 5-7 April 1995.

Introduction

- Motivation behind Power Hardware in Loop Applications
  - Power device under test is a “black box”
  - Difficult to obtain model for the power device under test
  - Testing increasingly complex control circuits
- Current PHIL Applications
  - Power converter testing (VSC, MMC etc.)
  - Distributed and Renewable Energy Integration
  - Micro grids
  - Shipboard Machine Drives



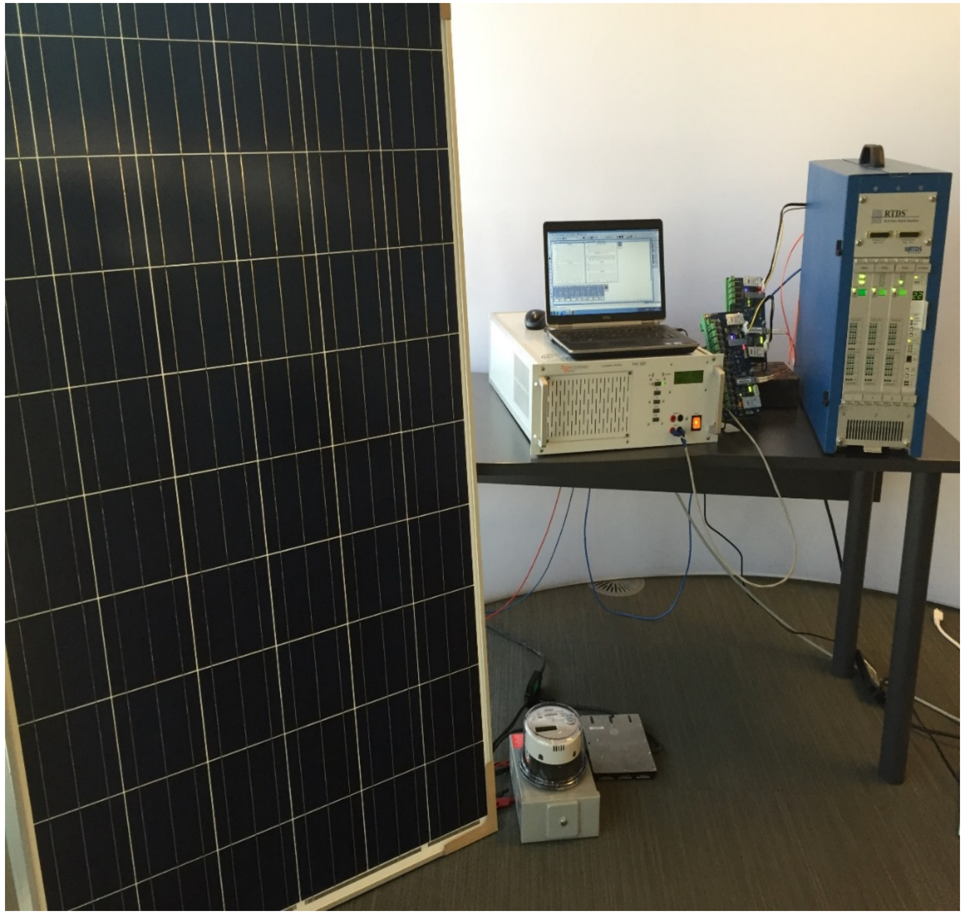
Power hardware in the loop validation of fault ride through of VSC HVDC connected offshore wind power plants
SHARMA, Ranjan ; WU, Qiuwei ; CHA, Seung ; JENSEN, Kim ; RASMUSSEN, Tonny ; ØSTEGAARD, Jacob
Journal of Modern Power Systems and Clean Energy, 2014, Vol.2(1), pp.23-29 [Peer Reviewed Journal]Springer Science & Business Media B.V.

PHIL Applications by RTDS Users

- 500kW PV Array Inverter Testing (J. Langston *et al.*, "Power hardware-in-the-loop testing of a 500 kW photovoltaic array inverter," *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Montreal, QC, 2012, pp. 4797-4802.)
- Fault Ride Through Testing of VSC HVDC Wind Plants (Sharma, R., Wu, Q., Cha, S-T., Jensen, K. H., Rasmussen, T. W., & Østergaard, J. (2014). Power Hardware In The Loop Validation of Fault Ride Through of VSC HVDC Connected Offshore Wind Power Plants. Journal of Modern Power Systems and Clean Energy, 2(1), 23-29.)
- PHIL Virtual Charging Station for V2G Impact Analysis (C. S. Edrington, O. Vodyakho, B. Hacker, S. Azongha, A. Khaligh and O. Onar, "Virtual battery charging station utilizing power-hardware-in-the-loop: Application to V2G impact analysis," 2010 IEEE Vehicle Power and Propulsion Conference, Lille, 2010, pp. 1-6.)
- PHIL Facility for Microgrids (P. Kotsampopoulos, A. Kapetanaki, G. Messinis, V. Kleftakis, N. Hatziargyriou, "A PHIL facility for Microgrids", International Journal of Distributed Energy Resources, Vol. 9, No. 1, pp. 71-86, January-March 2013)
- MW Scale Medium Voltage DC Test Bed on MMC (M. Steurer *et al.*, "Multifunctional megawatt scale medium voltage DC test bed based on modular multilevel converter (MMC) technology," *2015 International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS)*, Aachen, 2015, pp. 1-6.)
- All Electric Ship MVDC Power Distribution System (J. Siegers and E. Santi, "Stability analysis and control design for an all-electric ship MVDC power distribution system using a passivity based stability criterion and power hardware-in-the-loop simulation," *2015 IEEE Electric Ship Technologies Symposium (ESTS)*, Alexandria, VA, 2015, pp. 86-92.)

PHIL for a PV Micro Inverter

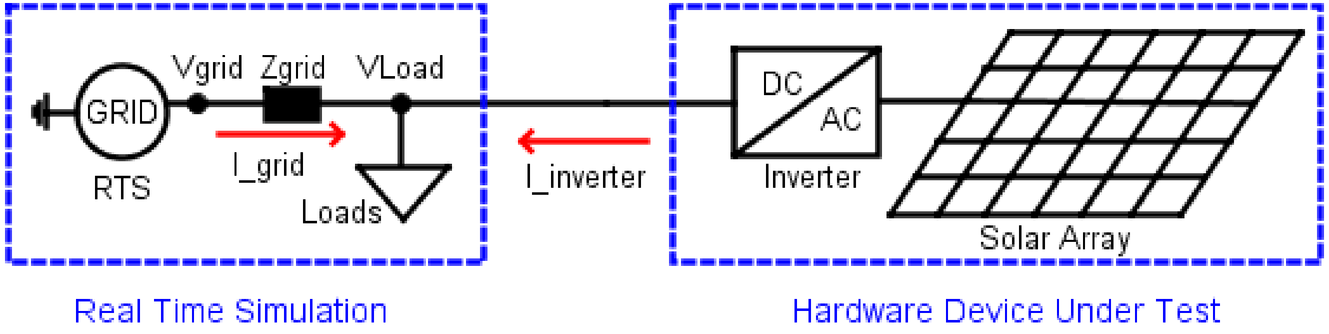
- PHIL Simulation with a 255W PV Panel and 225W Micro Inverter
- Challenges with PHIL Interface (Stability, Accuracy)
- Check out our YouTube video: https://youtu.be/nnKHiEWDXJM
- Steady state operation
- Effect of noise filtering
- Effect of shading PV panel
- Closed loop fault operation

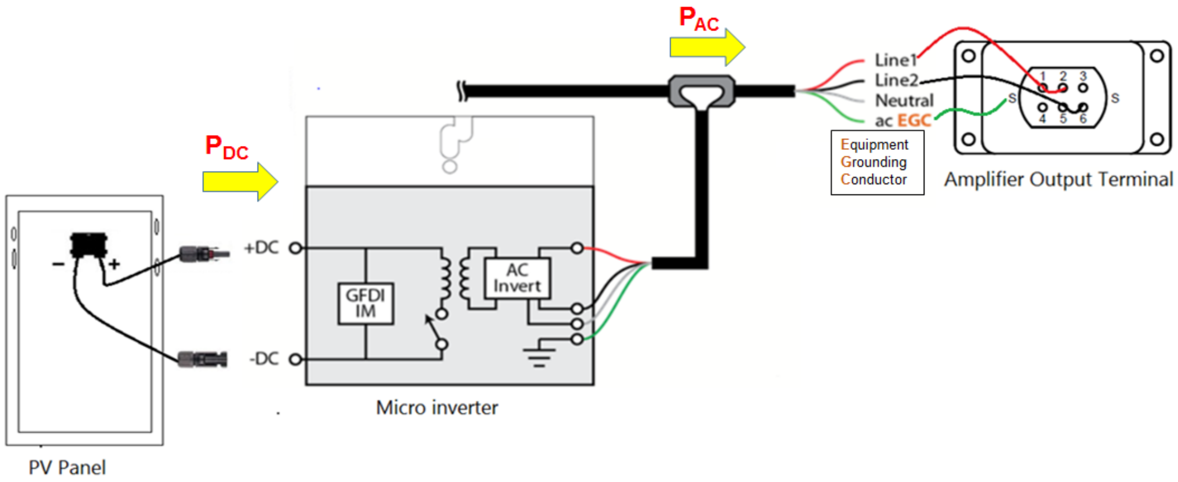


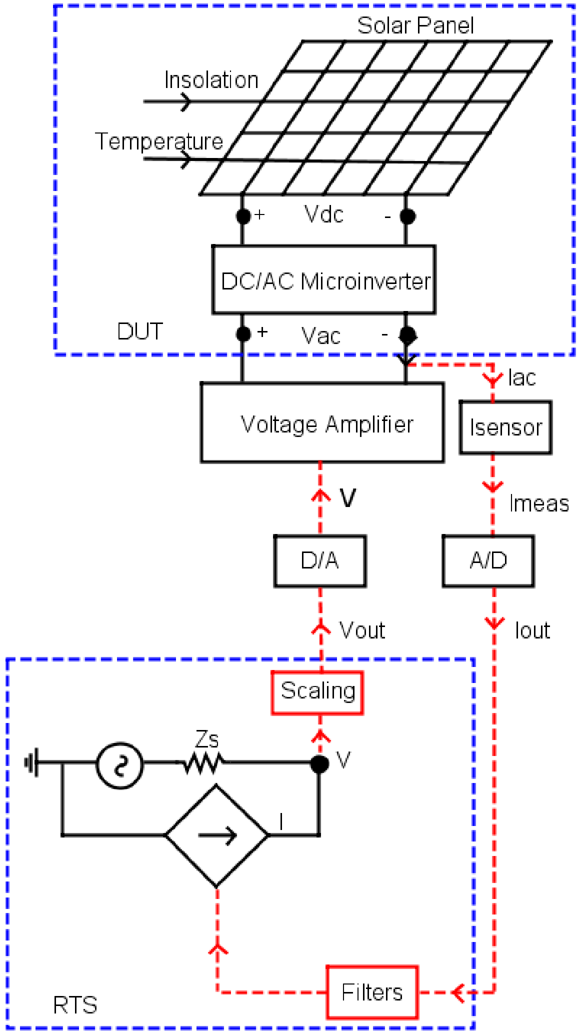
Onyinyechi Nzimako, Rudi Wierckx, "**Modeling and Simulation of a Grid-Integrated Photovoltaic System Using a Real-Time Digital Simulator**", Industry Applications IEEE Transactions on, vol. 53, pp. 1326-1336, 2017, ISSN 0093-9994.

PHIL for a PV Micro Inverter

- PHIL Simulation with a 255W PV Panel and 225W Micro Inverter

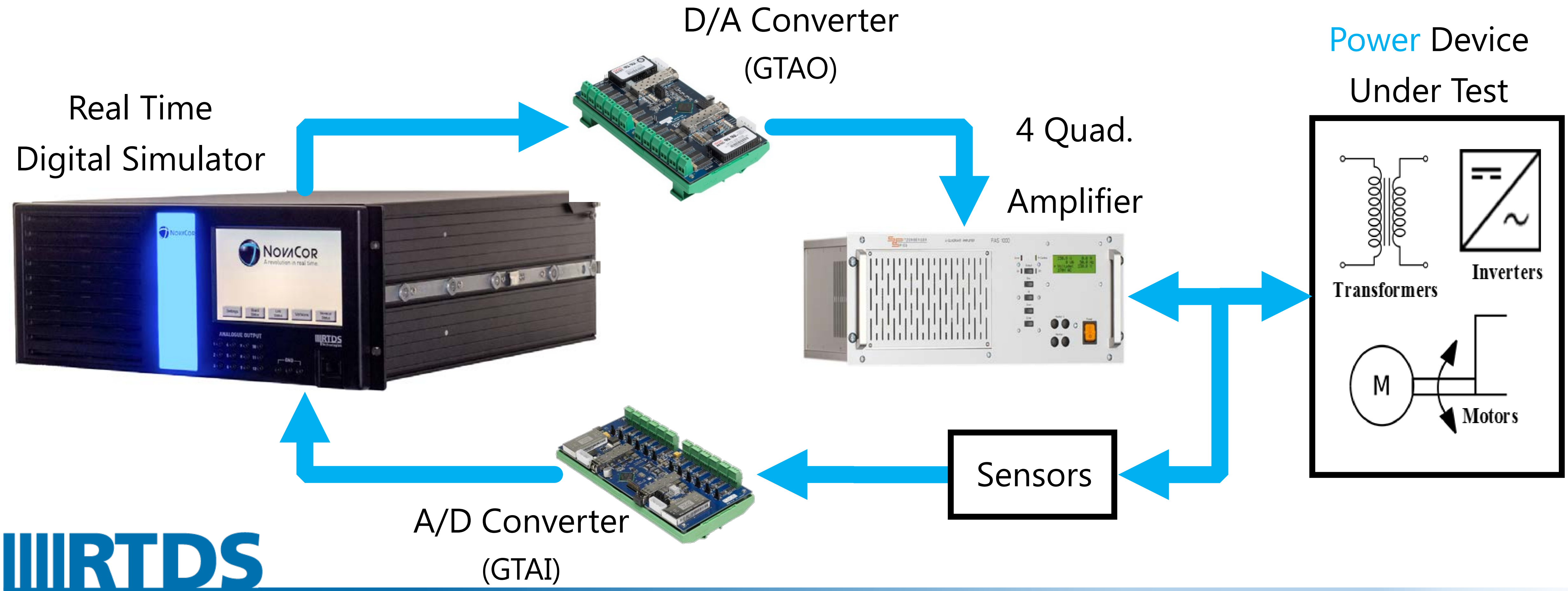






Key Factors for PHIL Simulation

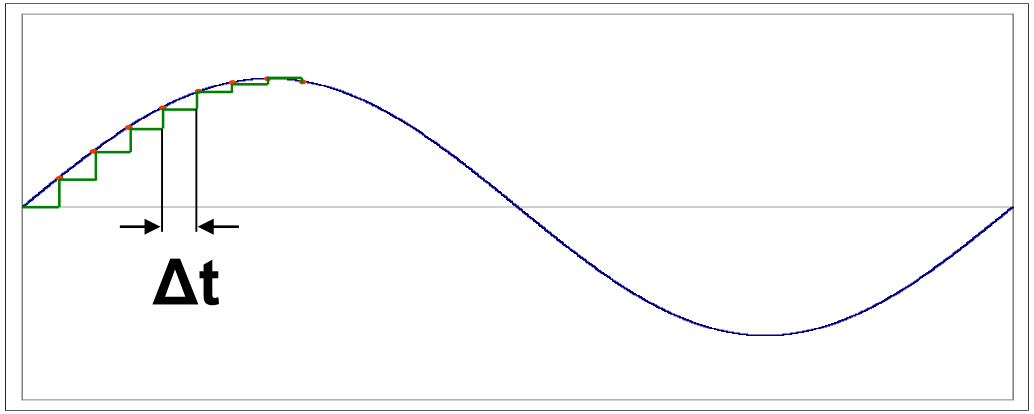
- Delays in the PHIL interface affect simulation accuracy and stability



Key Factors for PHIL Simulation

- Simulation time step of RTDS contributes to delay of PHIL interface

Electromagnetic Transient Simulation	
Typical Time Step	1.4 – 50 μs
Output	Instantaneous Values
Frequency Range	0 – 3 kHz (Large Δt) 0 – 15kHz (Small Δt)

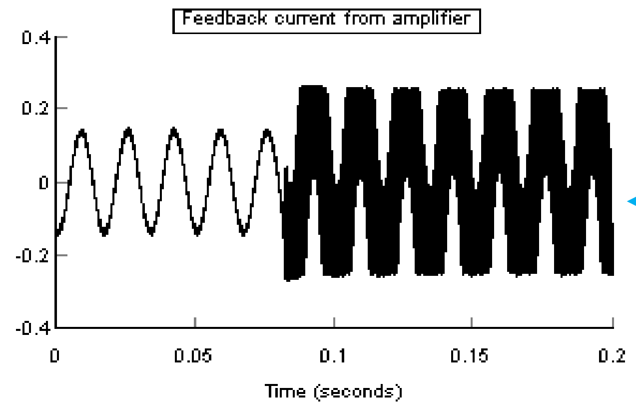


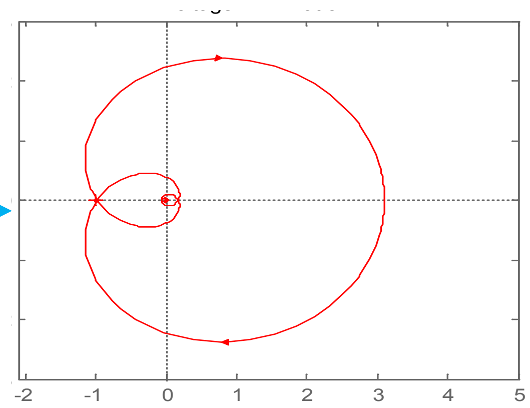
Key Factors for PHIL Simulation

- Small Time Step Simulation in RTDS (1.4-3.5μs) improves stability and accuracy in PHIL simulation

Large Time Step (Unstable)

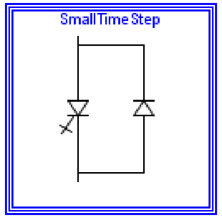
$\Delta t = 50\mu s$

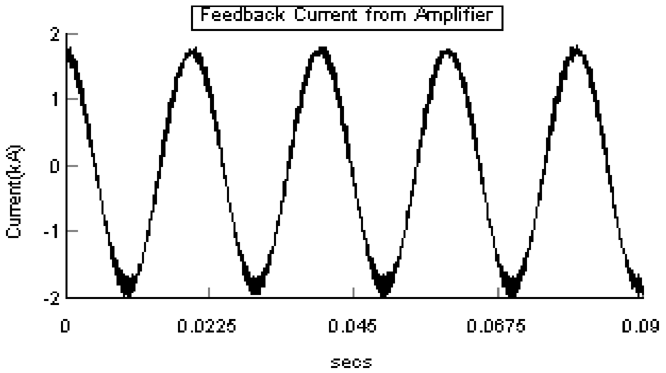


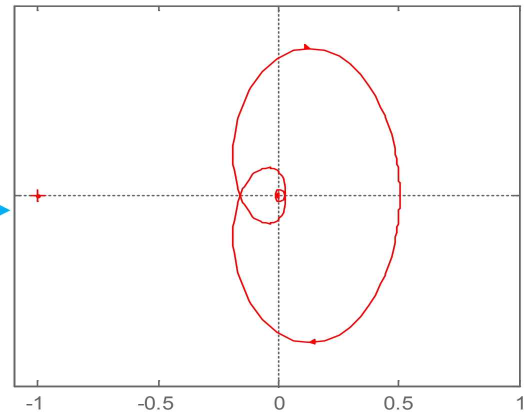


Small Time Step (Stable)

$\Delta t = 1.92\mu s$

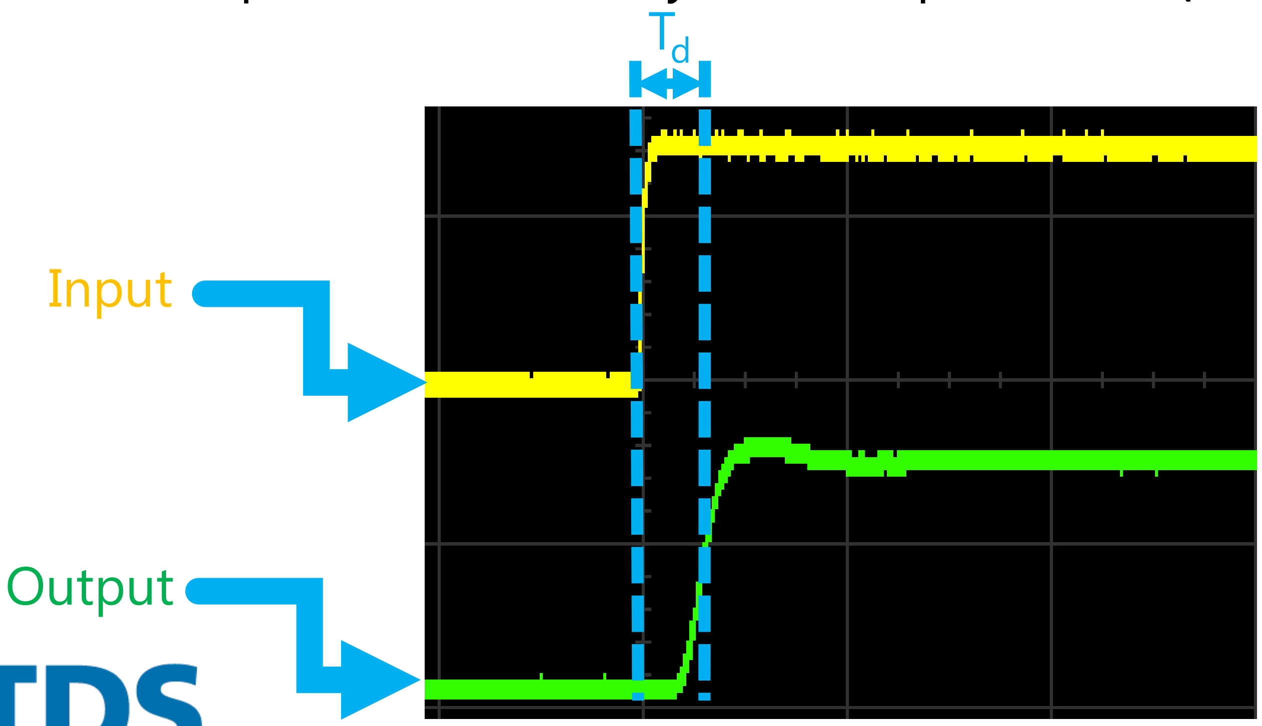






Key Factors for PHIL Simulation

- Amplifier Characteristics (Bandwidth, Frequency Response) impact stability of interface
- Type of Amplifier, Switched Mode or Linear type
- Linear amplifiers have fast dynamic response (<10μs)



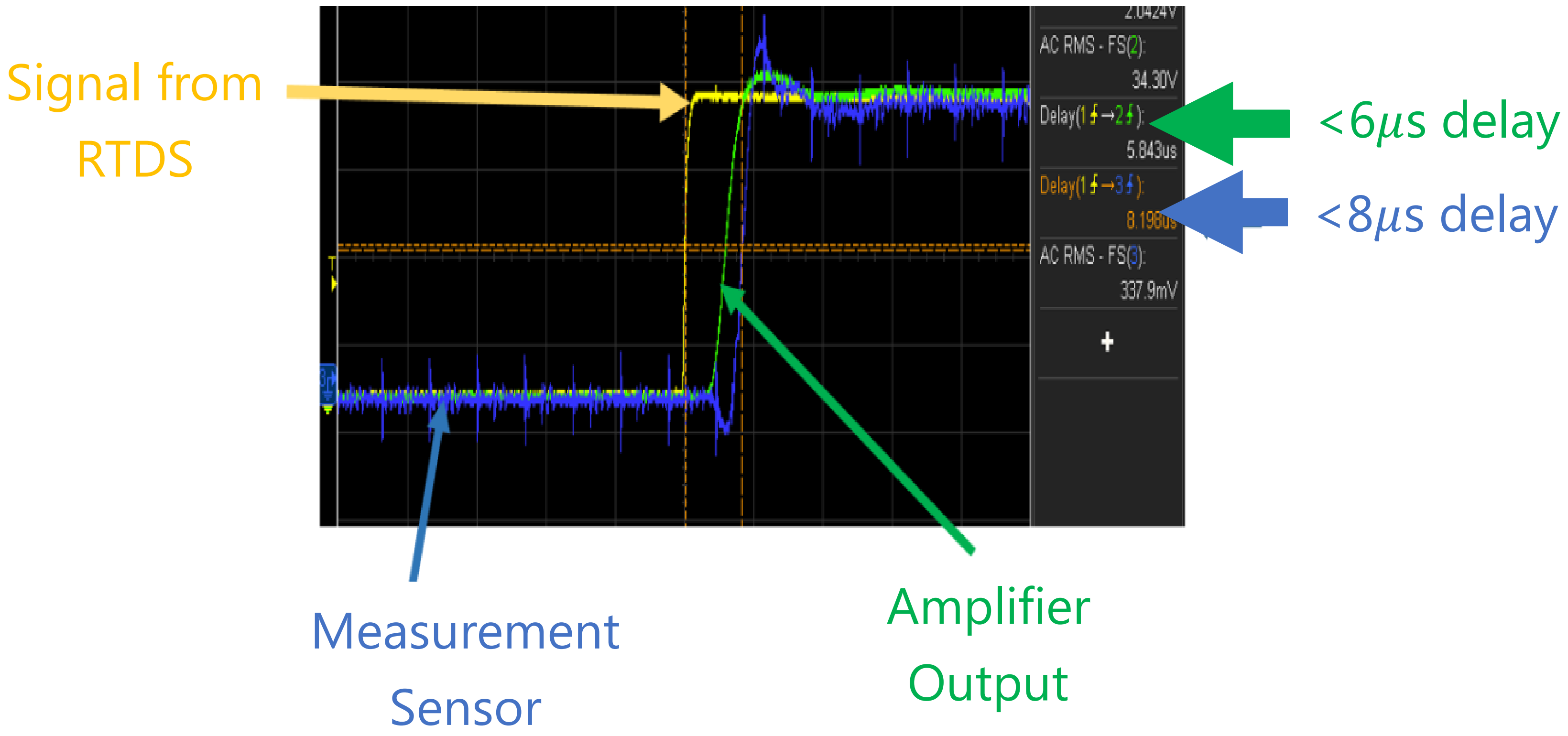
SPS Linear Voltage Amplifier (1 kVA)

- Volt. Range: 60V, 150V, 300V, 630V (DC)
- Freq. Range: DC to 5kHz
- Dynamic reponse (T_d): < 6μs

RTDS Technologies

Key Factors for PHIL Simulation

- Noise, wiring and measurement sensors all impact stability
- Noise can be filtered out but results in increased delay and loss of accuracy



Hardware Developments

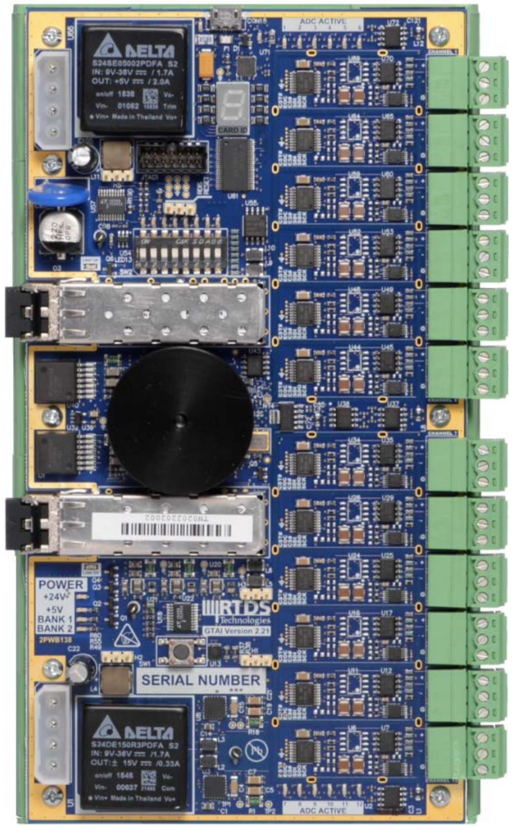
NovaCor
A revolution in real time.

- New generation of RTDS Simulator hardware - NovaCor
- Completely redesigned around IBM's POWER8® RISC-based 10-core processor
    - OpenPOWER Foundation provided access and support
- Large Δt reductions
- Small Δt reductions
- Check out our YouTube video: https://youtu.be/ByMIgNZ3_tg

Hardware Developments

- Faster A/D converter sampling rate (1 million samples per second previously 167 thousand samples per second)
- Independent A/D converters for better channel isolation and more consistent results between channels
- Improved filtering on power supply inputs to reduce noise coupling
- New digital filtering capability and smaller form factor
- Improved error checking on internal states and processes

A/D Converter (GTAIv2)



Hardware Developments

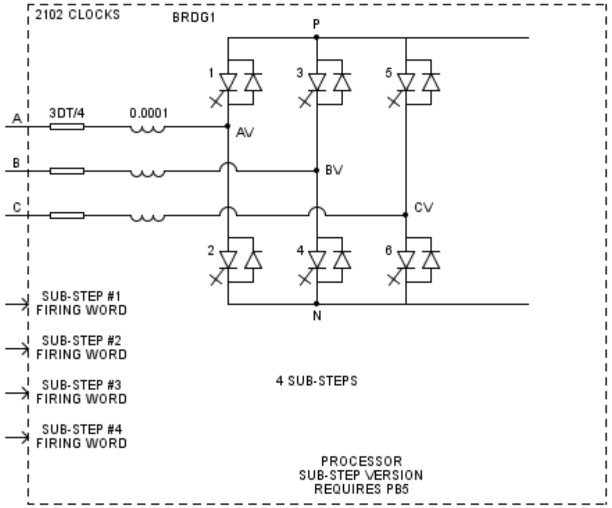
- Digital link between RTDS and Amplifiers with Aurora Protocol (SPS)
- Eliminates A/D and D/A converters
- Reduces delay
- 64 inputs and 64 outputs per port

Software Developments

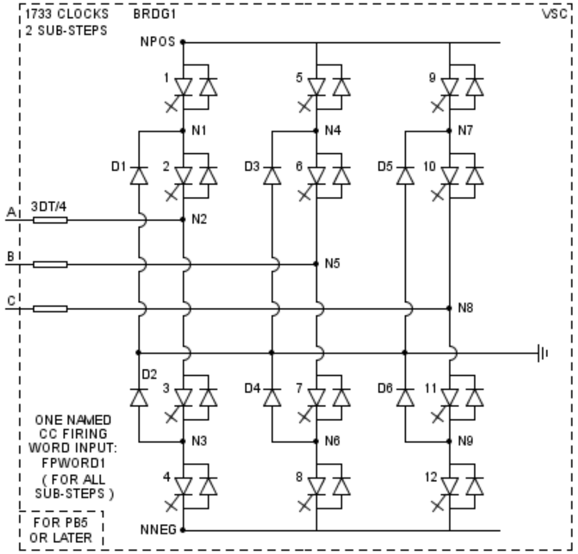
- Two and three level bridge VSC models running at a fraction of a small time step, also known as a sub time step

$$\Delta t_{sub} = \frac{\Delta \mathrm{t}_{\mathrm{small}}}{\mathrm{N}}, \mathrm{N} = \{2,3,4,5\}$$

- Multi-rate simulation model
- Δt_{sub} in the range of 750 nano seconds
- Allows for switching frequencies up to 40kHz (two level)



Two Level Bridge



Three Level Bridge

Conclusions

- Several Key Factors to consider in PHIL applications
  - Delays in interface
  - Size of simulation time step
  - Amplifier characteristics
  - Noise from transducers
  - Interface Algorithm
- Reducing the simulation time step (via small time step) can improve stability and accuracy of PHIL interface
- RTDS has continuously made hardware and software developments to enhance PHIL applications

Questions?

OpenPOWER Foundation

- The OpenPOWER Foundation is an open technical community based on the POWER architecture, enabling collaborative development and opportunity for member differentiation and industry growth.
- Member companies are enabled to customize POWER CPU processors and system platforms for optimization and innovation for their business needs.
- Opening the POWER architecture to give the industry the ability to innovate across the full Hardware and Software stack.