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Fabrication of Stable Large-Area Thin-Film CdTe Photovoltaic Modules

Annual Subcontract Report 10 May 1992 – 9 May 1993

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ABSTRACT

Solar Cells, Inc. (SCI) has made significant progress in its program to produce 60 cm x 120 cm solar modules based on CdTe films. During the past year confirmed efficiency has increased to 10.4% (active area) on a 1 cm^2 cell, 9.8% (aperture area) on a 64 cm^2 8 cell submodule, and 6.6% (total area) on a 7200 cm^2 module. A module measured in-house had a power output of 53 W for a total area efficiency of 7.4%. Average efficiency of modules produced is steadily increasing and standard deviation is decreasing; in a limited run of 12 modules results were 6.3% (± 0.2%). Field testing has begun; a nominal 1 kW array of 24 modules has been set up adjacent to SCI's facilities in Toledo. Analysis indicates that present modules are limited in efficiency by shunt resistance and optical absorption losses in the glass superstrate. Loss analysis of present devices allows us to project a module efficiency of 11.8%. A third generation deposition method - atmospheric pressure elemental vapor deposition, APEVD, has been brought on line and has produced good quality CdTe. In addition, SCI is expanding its proactive safety, health, environmental and disposal program dealing with issues surrounding cadmium.

INTRODUCTION

During the second year of the subcontract, SCI has made steady progress towards its goal of becoming a vertically integrated manufacturer of multi-megawatt solar electric generating fields. In late 1990, SCI began a program to investigate the viability of producing these modules using CdTe based films deposited from elemental vapors onto high temperature superstrates. CdTe was selected as the principal semiconductor layer due to its record of high efficiency and device stability, and its flexibility with respect to its method of deposition [1]. This flexibility allowed SCI the freedom to independently choose a manufacturing method based on attributes of low cost, high throughput, and reliability, and then to adapt that process to the deposition of CdTe based photovoltaic films. Elemental vapor deposition, EVD, was chosen due to its high deposition rate and its demonstrated capability to produce state of the art efficiency devices [2-5]. Although this strategy simplified the design of large area, high throughput semiconductor deposition equipment, it has not made it trivial. Several significant modifications have been made to adapt close spaced sublimation, CSS, which was the prior art, to a manufacturing environment. During the past two years SCI has designed, built and installed such equipment and has developed procedures for deposition of CdTe and CdS films which are compatible with high throughput manufacturing of large area photovoltaic modules.

In the SCI process semiconductor films are deposited from hot (>700 °C) elemental vapors onto SnO_2:F glass heated to about 600 °C. Typical partial pressures are a fraction of a torr and deposition rates are several microns per minute. The source of the vapor is powdered compound - CdTe or CdS. EVD differs principally from CSS in that the superstrate is inserted into and removed from the deposition zone hot rather than being both heated and cooled while in close physical proximity to the source material. Furthermore, deposition onto 0.72 m^2 superstrates occurs in a chamber in which the source material is contained in boats placed above and facing away from the superstrate. The superstrate is carried on rollers through the zone and deposition occurs as the hot vapors condense onto the relatively cooler superstrate. Total semiconductor deposition time is approximately one minute. By the end of the first year of the subcontract the fundamental soundness of the approach had been demonstrated. Semiconductor films had been deposited and modules had been produced [6]. During the second year subcontract we have begun to optimize the deposition procedure and to explore its potential and its limitations.

MODULE FABRICATION PROCESS

This section, which describes the deposition process, is largely adapted from Ref. 7. Table 1 lists the main steps in the process used to produce the PV modules. The incoming SnO_2:F coated 5 mm thick sodalime glass is inspected, seamed, washed and taken to the laser scriber for scribe #1 through the SnO_2. See Fig. 1. Figure 1 also shows the basic cell structure. The laser system consists of a pulsed Nd:YAG laser and optical system on an automated motion table. Scribe #1 is performed at a wavelength of 1.06 μm. The system is capable of motion at 10 inches per second. Only one beam is used and it takes about 5 minutes to scribe a complete module.

TABLE 1
Main Process Elements

Inspect glass superstrate	Ni deposition (sputtering)
Seam	Al deposition (sputtering)
Wash	Laser Scribe #3
Laser Scribe #1	Bus bar application
Wash	Lead attachment
CdS deposition (EVD)	Module test
CdTe deposition (EVD)	Encapsulation (lamination)
Post Deposition Heat Treatment	Junction Box attachment
Laser Scribe #2	

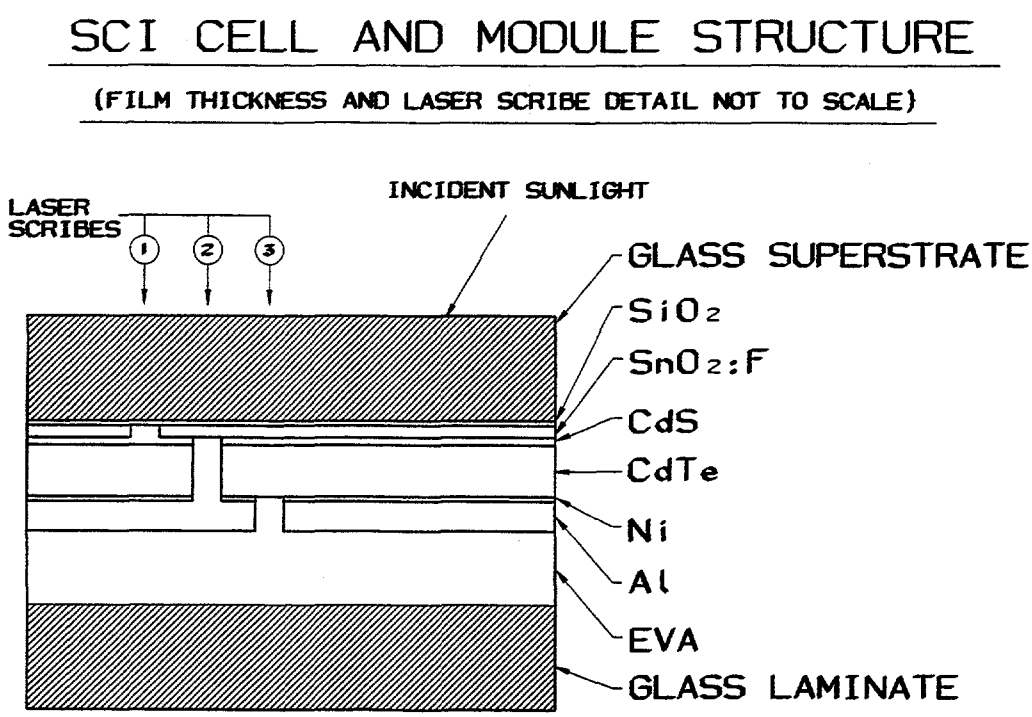


Fig. 1 Schematic drawing of SCI cell and module structure (not to scale).

After the glass is washed again, the CdS and CdTe are deposited from high temperature elemental vapors. The SCI semiconductor deposition system, known by the acronym LDS - Large Deposition System, is shown in a photograph in Fig. 2 and illustrated schematically in Fig. 3. The system consists of four stainless steel vacuum chambers each approximately 5' x 9' x 1' connected together as shown in Fig. 3. The glass superstrate enters the system from the entrance conveyer through a valve and travels typically at a speed of 4 cm/sec with the 60 cm edge leading. After the superstrate is completely within chamber #1, the valve is closed and chamber #1 is pumped down. While chamber #1 is pumping down the superstrate is heated by radiative heaters from above and below. The glass superstrate is conveyed on ceramic rollers inside the vacuum system. When the superstrate reaches the proper temperature (~ 600 °C) the valve between chambers #1 and #2 is opened and the superstrate is conveyed to chamber #2 where the deposition of CdS takes place. The CdS source material is contained in powder form in boats above the superstrate. The source material is heated to above 700 °C generating a vapor cloud in the deposition region. The superstrate is conveyed through this vapor cloud and the CdS film is deposited on the moving superstrate in one pass. In order to control deposition rate, nitrogen gas is admitted to the chamber to a pressure of up to 1 torr during deposition. The deposition time for CdS is typically about 10 seconds.

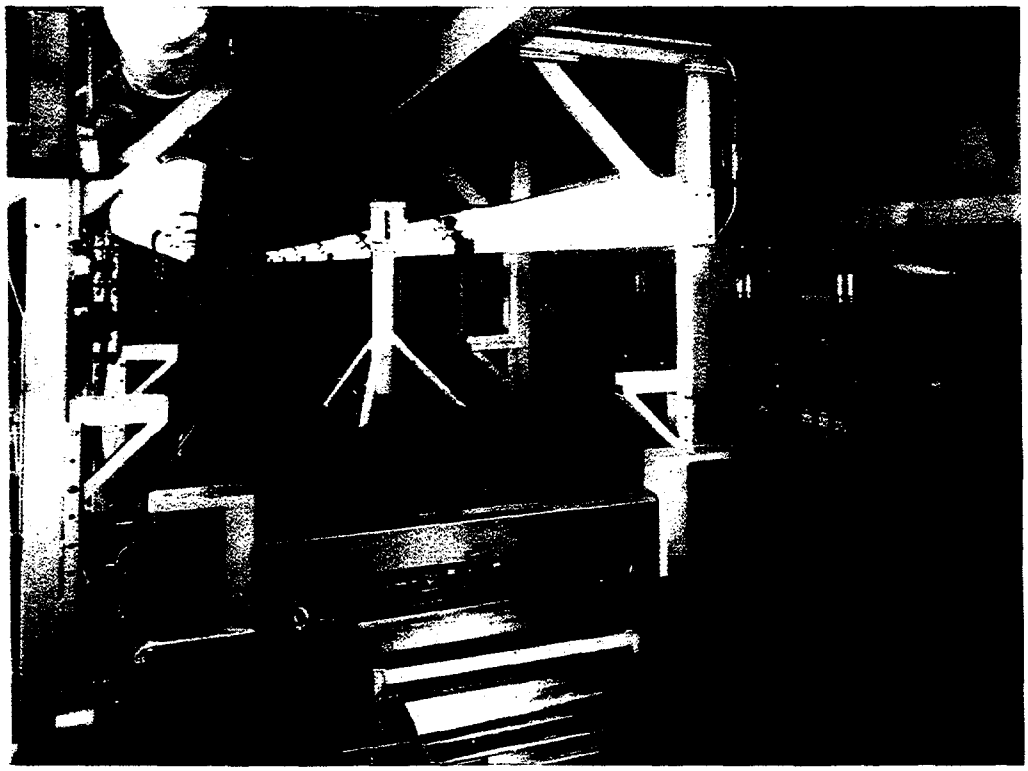


Fig. 2 Photograph of semiconductor deposition system.

The superstrate continues on into the CdTe deposition zone. The source temperature of CdTe is typically a little lower than the CdS source. CdTe deposition time is about 40 seconds. The superstrate is conveyed continuously through the CdS and CdTe deposition zones. When parameters are set properly, the superstrate exits the CdTe deposition zone with films of CdS and

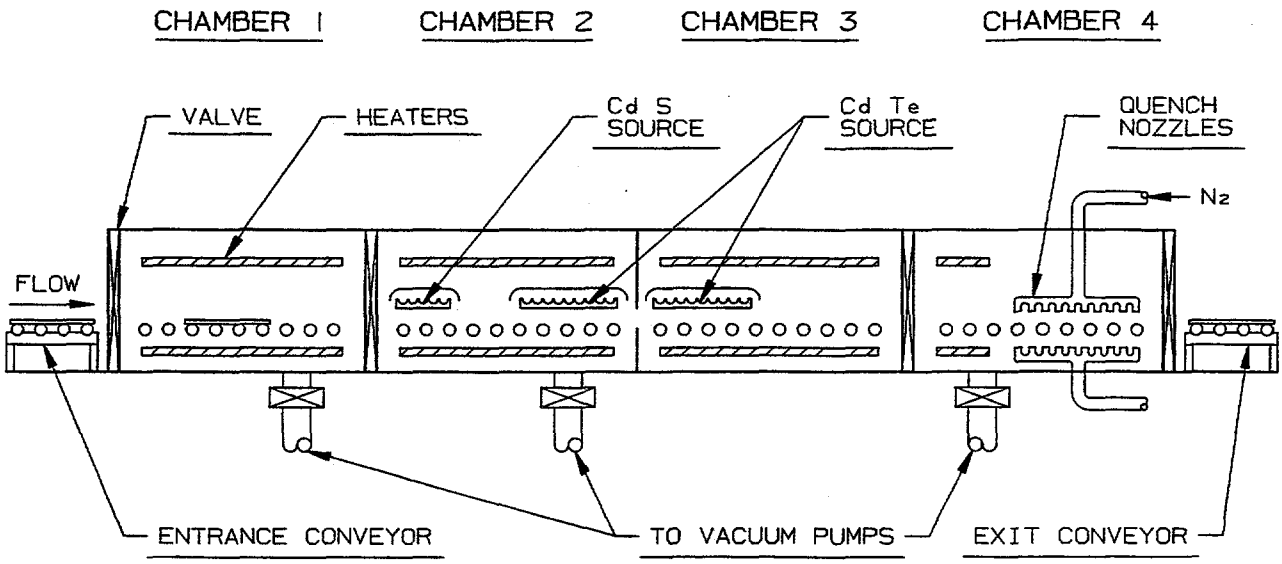


Fig. 3 Schematic representation of semiconductor deposition system. The glass superstrate is conveyed on ceramic rollers inside the vacuum chambers. The CdS and CdTe films are deposited in chambers #2 and #3 from powder source materials.

CdTe with desired thickness and material properties. The film thickness and microstructure are affected by the source temperature, superstrate temperature, ambient gas pressure and conveyer speed. Adhesion of the CdS and CdTe films is very good, routinely passing tape pull tests at 45 oz/in. The polycrystalline CdTe film has a crystal size of 2-3 μm. The superstrate is quenched (i.e., cooled rapidly) in chamber #4 by N_2 gas impinging on the top and bottom surfaces through multiple nozzles. This quenching imparts a partial tempering to the glass which gives it sufficient strength to withstand hail impact and strong wind in outdoor field installations. When the N_2 pressure in the chamber, which increases due to the in rush of quench gas, reaches atmospheric pressure, the exit valve is opened and the coated superstrate is transported to the exit conveyer. At this point the superstrate is still at a temperature of about 300 °C. Fans on the exit conveyer cool it further to room temperature.

After CdTe deposition the superstrate is subjected to a post deposition heat treatment at about 400 °C for 20 minutes. This heat treatment is similar to that used by others and reported in the literature [8] and has the effect of improving module efficiency. A number of modifications have been tried for this heat treatment. It is hoped that this step can be eliminated by the time we are ready to take the next step of constructing a high throughput production line.

The next step in the process is laser scribe #2. The same Nd:YAG laser is used as described earlier for scribe #1, except that a frequency doubler is used to produce a beam at 532 nm. After scribe #2 the back metal contact is deposited by sputtering. The sputtering chamber consists of two 5' x 9' x 1' vacuum chambers connected together. Films are deposited by DC magnetron sputtering while the superstrate is moved beneath the Ni and Al targets.

After metallization the module is taken back to the laser system for scribe #3 using the 532 nm beam. In order to provide adequate electrical isolation between the module and its surroundings, all films are removed in a 1 cm wide border around the edge of the module by grit blasting. Bus bars are applied at each end of the module and thin metal film leads are attached to the bus bars. The module pattern is displayed in Fig. 4. It consists of 116 cells connected in series, each cell being 1 cm x 58 cm.

The interconnected module is now tested on a solar simulator that uses multiple quartz halogen dichroic mirror lamps to approximate AM 1.5 conditions. An I-V curve is taken and recorded for each module.

The next step is encapsulation which is accomplished by laminating to a second sheet of glass using a 0.018" thick sheet of EVA as the laminating material. The two thin metal film leads are brought out through two holes drilled in the glass. After lamination a junction box is attached to the back of the module to facilitate later interconnect wiring to other modules and to house a by-pass diode.

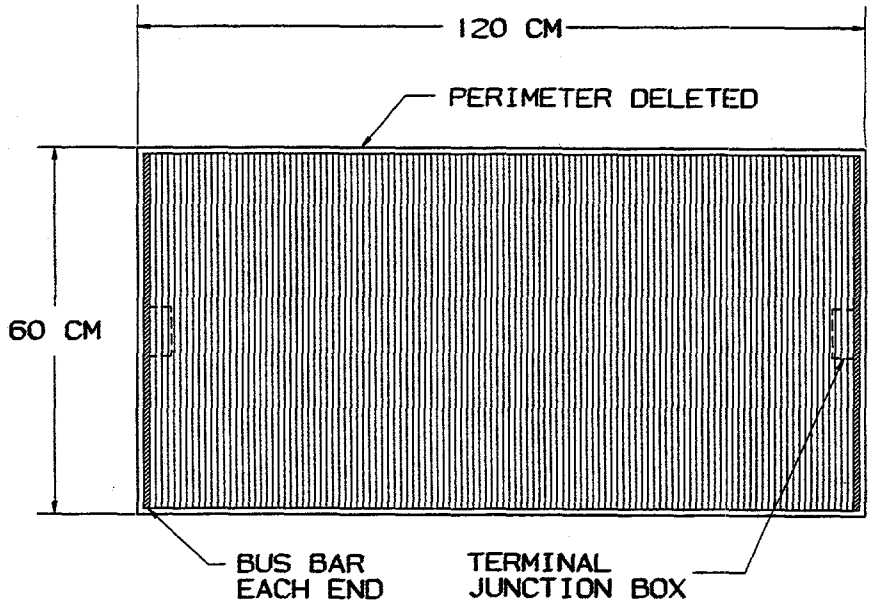


Fig. 4 Schematic drawing of module showing 116 series connected cells. Typical operating voltage is 65 volts.

The process optimization is still in progress and it is likely that some of the above steps will change prior to attaining the commercial version of the process. All steps in the process are compatible with an automated high throughput production line. The design of the semiconductor deposition system was aimed at a deposition process that is not overly sensitive to small temperature variations or small dimensional variations. Based on our experience with the pilot production deposition system, we believe that this process is suitable for a continuous high throughput module manufacturing line.

MATERIAL PROPERTIES

Film deposition rate can be controlled by varying the source boat temperature and the ambient pressure. Present apparatus is limited, however, in that only one superstrate can be inserted at a time. This introduces limitations on the uniformity achievable due to the fact that deposition conditions do not have time to stabilize to steady state values during a single run. When the superstrate is inserted into the hot vapor cloud, the deposition rate at the leading edge is higher than at the trailing edge which is, in turn, slightly higher than at the center. At present, therefore, uniformity is achieved through multiple passes of the superstrate through the deposition zones. In a production environment the superstrates would enter the deposition zone one right after the other and a steady state would prevail. Nonetheless, present thickness variation across a superstrate is ± 15% for both CdS and CdTe. See Fig. 5. Films appear to be non-porous with a crystal size on the order of one micron. See Fig. 6. Adhesion is excellent; semiconductor films are not removed using tape pulls of 45 oz/in. Photoluminescence measurements performed at NREL indicate that the carrier lifetime, which is ~0.2 ns in as-deposited films, increases to 1-2 ns after a standard heat treatment. Photoluminescence lifetimes in this range are characteristic of material used in 10+% efficient devices.[9]

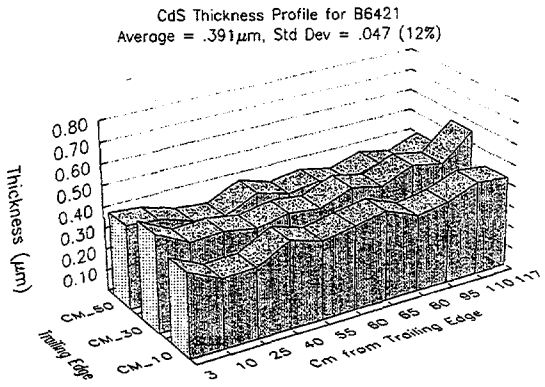


Fig. 5A CdS thickness profile.

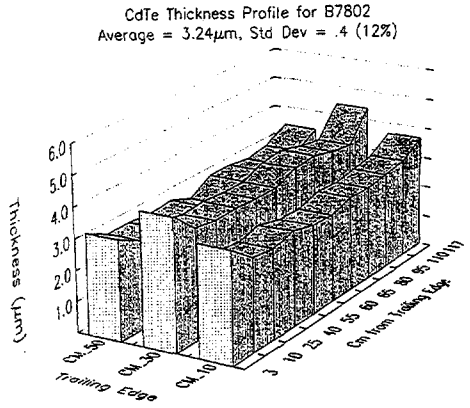


Fig. 5B CdTe thickness profile.

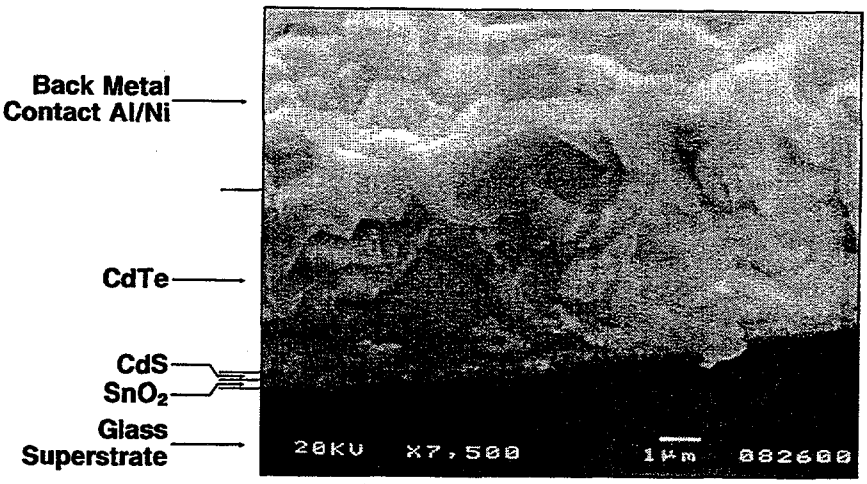


Fig. 6 SEM photo showing device cross section.

MODULE RESULTS

The first interconnected 60 cm x 120 cm module was produced in April, 1992. Over 400 modules have been produced to date. We are currently making modules at the rate of three per day (roughly 40 kW per year). The equipment can produce modules at a substantially higher rate than this but at the present stage of development there is little advantage to producing at a higher rate, since more time and effort are spent diagnosing modules than producing them. The primary emphasis in the past year has been to improve efficiency by identifying the main problems limiting efficiency and controlling them one by one.

When we began the development program, one of our primary targets was to achieve 6% total area efficiency on a 60 cm x 120 cm module. This goal was achieved rather quickly -within three months of producing the first interconnected module. Our larger goal, however, is to produce high efficiency modules with a high yield. Substantial progress has been made. The average total area efficiency of modules produced is now about 6% and we have not yet come close to exhausting the areas for efficiency improvement. Fig. 7 shows a graph of average total area module efficiency as a function of time; i.e., production sequence. Each point represents the average of 20 modules produced in sequence from the first modules to the present. The time interval covered by the data in Fig. 7 is approximately one year. It can be seen that the average

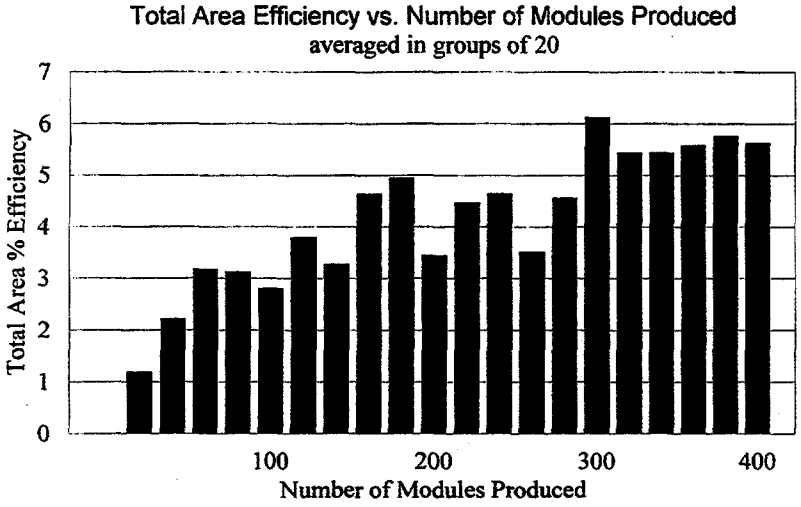


Fig. 7 Graph of average total area module efficiency vs. order of production. Each bar represents the average of 20 modules. The total time represented by the graph is approximately one year.

module efficiency has been in an increasing trend with some temporary reverses. We have been following the "designed experiment" approach of multiple variables which calls for "bold" variations to determine the significant variables. When a change is in the wrong direction, it is likely to lead to a module with substantially reduced efficiency. On the other hand, this process is helping us identify and control the variables which influence module power output. Uncontrolled variations were substantial in the beginning of the development effort and although they are being reduced with time, they are still higher than acceptable for a commercial high throughput production line.

For reproducibility of module efficiency our target is to reduce the standard deviation to less than 3% of the average efficiency. We have approached this target and believe that it can be achieved. In a recent mini-production run we froze the process parameters and attempted to produce 12 identical modules. No process variations were deliberately introduced. The efficiency distribution of these modules is shown in Fig. 8. The average total area efficiency of the 12 modules was 6.3% and the standard deviation was 0.19% which is approximately 3% of the average efficiency.

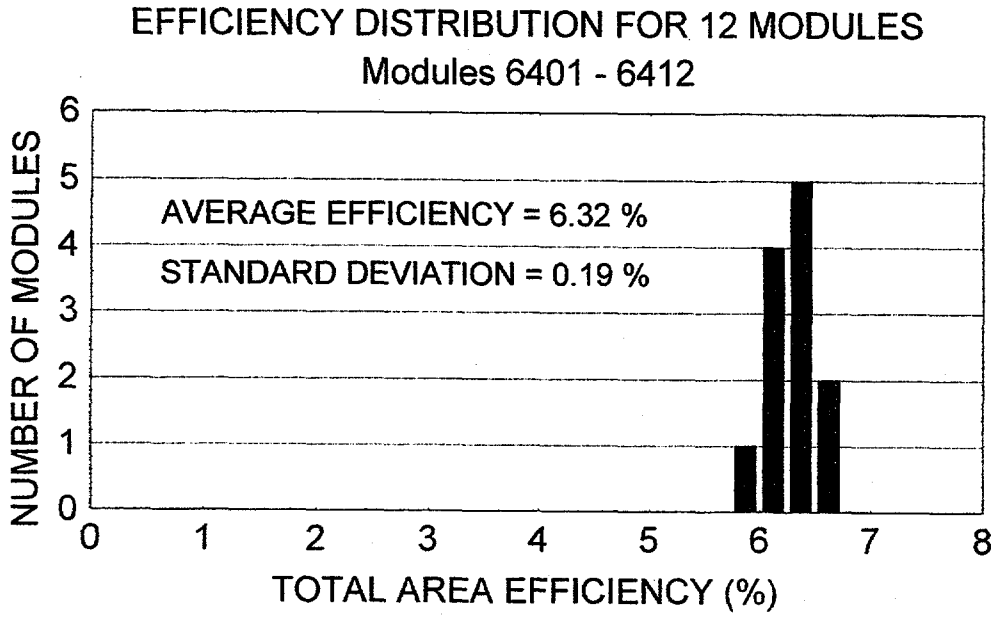


Fig. 8 Graph of efficiency distribution of a 12 module mini-production run where no variations in the process were deliberately introduced.

The data displayed in Fig. 9 is from the highest efficiency module produced during the past year. Module parameters are: 92.6 V Voc, 0.95 A Isc, 0.61 FF and 53 W power output. The maximum power point is 65.8 V and 0.81 A. This is a total area efficiency of 7.36%. Normalized cell parameters are 0.799 V/cell Voc and 17.7 mA/cm^2 Jsc.

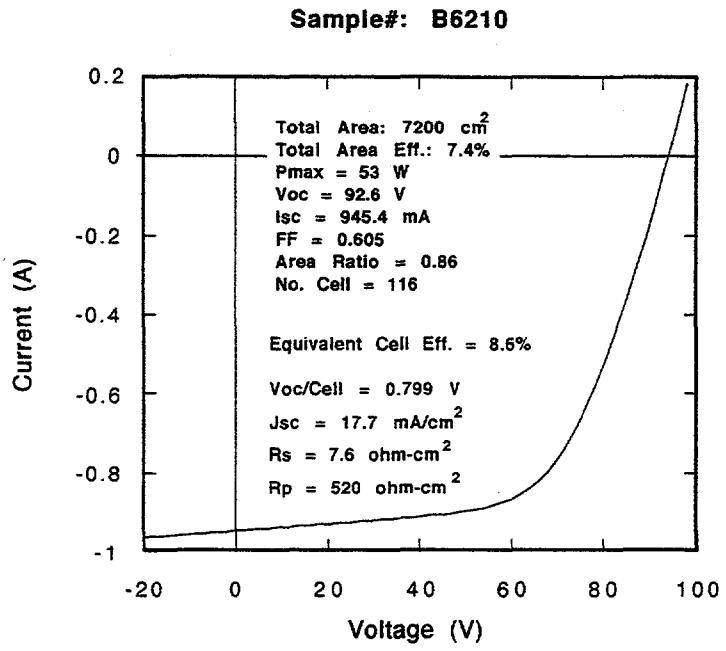


Fig. 9 I-V curve for module with 53 watt output under AM 1.5 conditions. Total area efficiency is 7.4%.

Fig. 10 1kW array installed adjacent to the pilot production facility.

As efficiency targets are approached and the process is better defined, we have been shifting emphasis to measuring stability and reliability. These measurements consist primarily of accelerated life tests such as those specified in the NREL *Interim* Qualification Tests (IQT).[10] This test procedure includes a thermal cycle test (200 cycles between 90 °C and -40 °C), humidity-freeze cycle test (20 cycles between 85 °C, 85% relative humidity and -40 °C), wet and dry electrical isolation tests, hot spot endurance test, hail impact test and mechanical loading test, among others. SCI 60 cm x 120 cm modules have passed the NREL IQT. In addition, we are developing an in-house testing procedure designed to measure the effects on module performance of elevated temperature, voltage bias, light soaking and ambient gas. It is hoped that these tests will provide insight into module degradation mechanisms and also allow us to project module properties out to their desired 30 year lifetime.

We have recently begun to deploy SCI modules in outdoor test arrays. A small array was installed in January, 1993 in a field next to the pilot production facility in Toledo. In April, 1993 this was expanded to 1kW. Fig. 10 shows a photograph of this installation. Stability results to date are very good but it is much too soon to conclude that stability has been demonstrated. Plans are to install a number of arrays at various locations in 1993 to generate data on stability and reliability.

SUBMODULES

In order to try out process variations on a small scale in a controlled manner, and to help establish the potential for the process, we routinely produce 8 cell submodules. Each cell is approximately 1 cm x 8 cm; the aperture area is 8 cm x 8 cm = 64 cm^2. The interconnect scheme is the same as that used for full size modules.

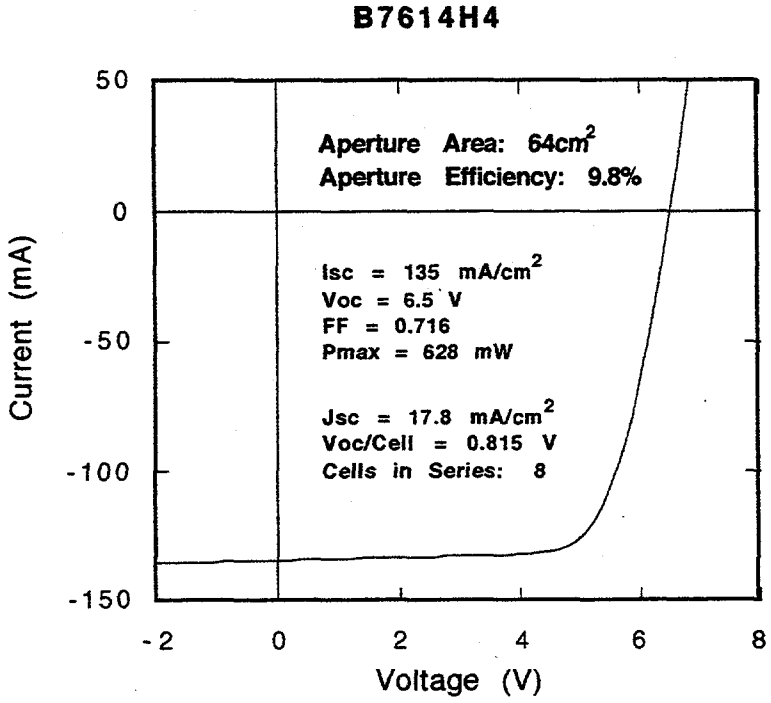


Fig. 11 I-V curve of 9.8% submodule.

Originally the semiconductor films for these submodules were produced in a research scale deposition system known by the acronym RMS - Research Multi-Stage. [6] The LDS was designed after the RMS was built, and therefore incorporates several improvements. At this point the LDS produces films which are often superior to those produced in the RMS. Thus many submodules are produced on 10 cm x 10 cm sheets of CdTe/CdS coated SnO_2 glass which are cut from 60 cm x 120 cm superstrates coated in the LDS.

Fig. 11 displays the I-V characteristics of the highest efficiency submodule produced at SCI. In this case the short circuit current has been increased from 133 mA to 137 mA (0.5 mA/cm^2) by using MgF_2 anti-reflection coating applied at NREL. This device is notable for its high Voc - 6.62 volts (0.828 V/cell). Other device properties were 0.69 FF and aperture area efficiency 9.8%. This device, produced on LDS material, demonstrates the potential of 7200 cm^2 modules.

CELL EFFICIENCY

The highest confirmed efficiency 1 cm^2 cell produced at SCI had an efficiency of 10.4%. See Figure 12. Device parameters were 0.801 V Voc, 18.5 mA/cm^2 Jsc and 0.699 FF.

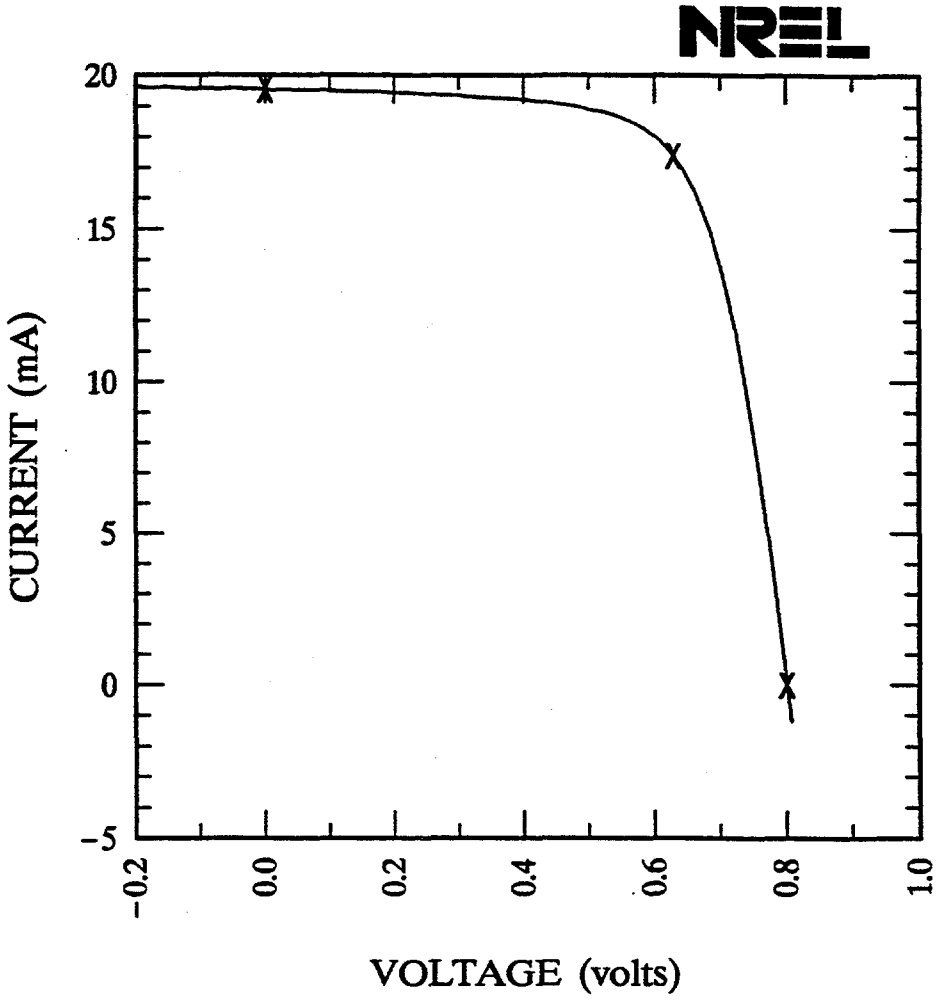
LOSS ANALYSIS

This analysis follows that given in Ref. 11. Dark I-V, light I-V, and spectral response measurements are utilized to analyze device performance in terms of a simple equivalent circuit involving a diode with series and shunt resistors. In this analysis the device performance parameters - Jsc, FF, and Voc - are treated as independent of one another.

Solar Cells Inc. SnO2/CdS/CdTe/Glass

Sample: 11 Temperature = 25.0°C

Dec. 23, 1992 4:13 pm Area = 1.055 cm²



V_{oc} = 0.8009 volts I_{sc} = 19.54 mA

J_{sc} = 18.52 mA/cm² P_{max} = 10.94 mW

Fill factor = 69.91 % I_{max} = 17.39 mA

Efficiency = 10.4 % V_{max} = 0.6291 V

Fig. 12 I-V curve of 10.4% cell.

Short Circuit Current

One of the more difficult parameters to measure is short circuit current. An accurate measurement requires a knowledge of the spectral irradiance of the light source as well as the spectral response of the reference cell and of the device being tested [12]. Measurements made at NREL [13] indicate that for the lamps used in the SCI solar simulator and the GaAs reference cell used at SCI, the spectral mismatch factor variation from cell to cell may reach 16%. The variation in mismatch factor is due primarily to variations in device spectral response in the wavelength region around the CdS absorption edge - 512 nm. The following analysis is based on Jsc and spectral response data measured at NREL.

The potential Jsc for CdTe, obtained by integrating the AM1.5 Global spectrum from 300 to 860 nm (1.44 eV), is 30.8 mA/cm^2. Based on the measured optical characteristics of the LOF 8 Ω/□ SnO_2 coated glass used in SCI's modules, this breaks down into 6.1 mA/cm^2 absorbed, 2.7 mA/cm^2 reflected, and 22.1 mA/cm^2 transmitted. See Fig. 13. Of the transmitted light, 4.8 mA/cm^2 is due to photons with energy greater than the CdS bandgap (2.42 eV) and 17.3 mA/cm^2 is due to lower energy photons. We can compare these calculations with experimental values.

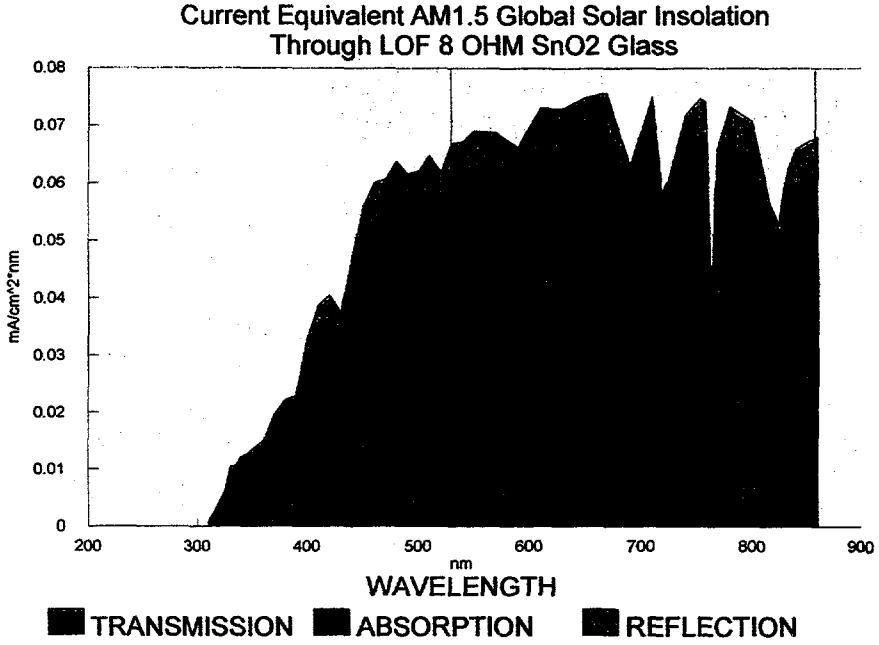


Fig. 13 Current equivalent AM 1.5 global solar insolation through LOF 8 Ω SnO_2 glass.

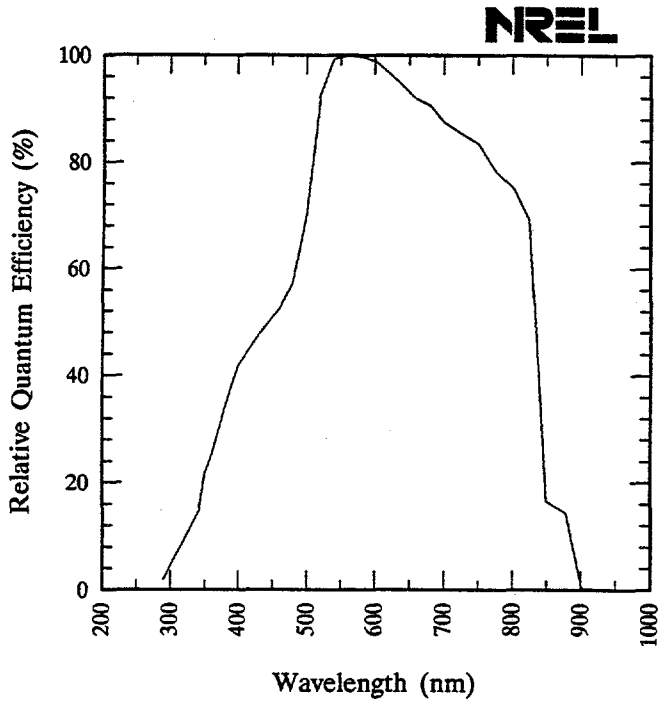
One of the most efficient single cells produced at SCI - 10.3% - had a Jsc of 20.0 mA/cm^2 as measured at NREL. This device was made in the RMS but employed the same source material and superstrates as are used for modules. Based on the NREL supplied spectral response, the cell generated 3.0 mA/cm^2 from photons with energies above the CdS absorption edge and 17.0 mA/cm^2 from photons with energies between the CdTe and CdS absorption edges. See Fig. 14. For this particular cell, it appears that 98% of the photons transmitted by the superstrate in the range 1.44 < hν < 2.42 eV were collected, while only 63% of photons with hν > 2.42 eV were collected. Thus, if all semiconductor material deposited on a module (presently 17.7 mA/cm^2 Jsc) were as good as the best that has been deposited on single cells (20.0 mA/cm^2), module Jsc would increase by 2.3 mA/cm^2. It would seem that beyond that point further material or device improvements alone have limited potential for improvements in Jsc.

Furthermore, according to this analysis there is the potential to collect an additional 1.8 mA/cm^2 due to photons above the CdS absorption edge. In principle this current could be generated if we could make the CdS layer sufficiently thin. Our experience teaches, however,

Solar Cells Inc, Cds/CdTe/SnO2/Glass

Sample: 91 Temperature = 25.0°C

Dec. 8, 1992 4:04 pm Area used = 1.081 cm²



Light bias = 10.0 mA

Zero voltage bias

Fig. 14A Spectral response of 10.3% efficient cell.

that it may be difficult to sufficiently thin the CdS without some loss in Voc. Therefore we do not anticipate increases beyond about 1.0 mA/cm² through thinning of the CdS.

Further increases in Jsc may also be realized through decreased reflection due to the SnO_2 coated glass superstrate. In a separate experiment, scientists at NREL measured the short circuit current density and aperture area efficiency of an 8 cell, 64 cm² submodule to be 19.3 mA/cm² and 8.9%, respectively. When the submodule was given a MgF_2 anti-reflection, AR, coating at NREL, Jsc increased by approximately 1.1 mA/cm² to 20.4 mA/cm².

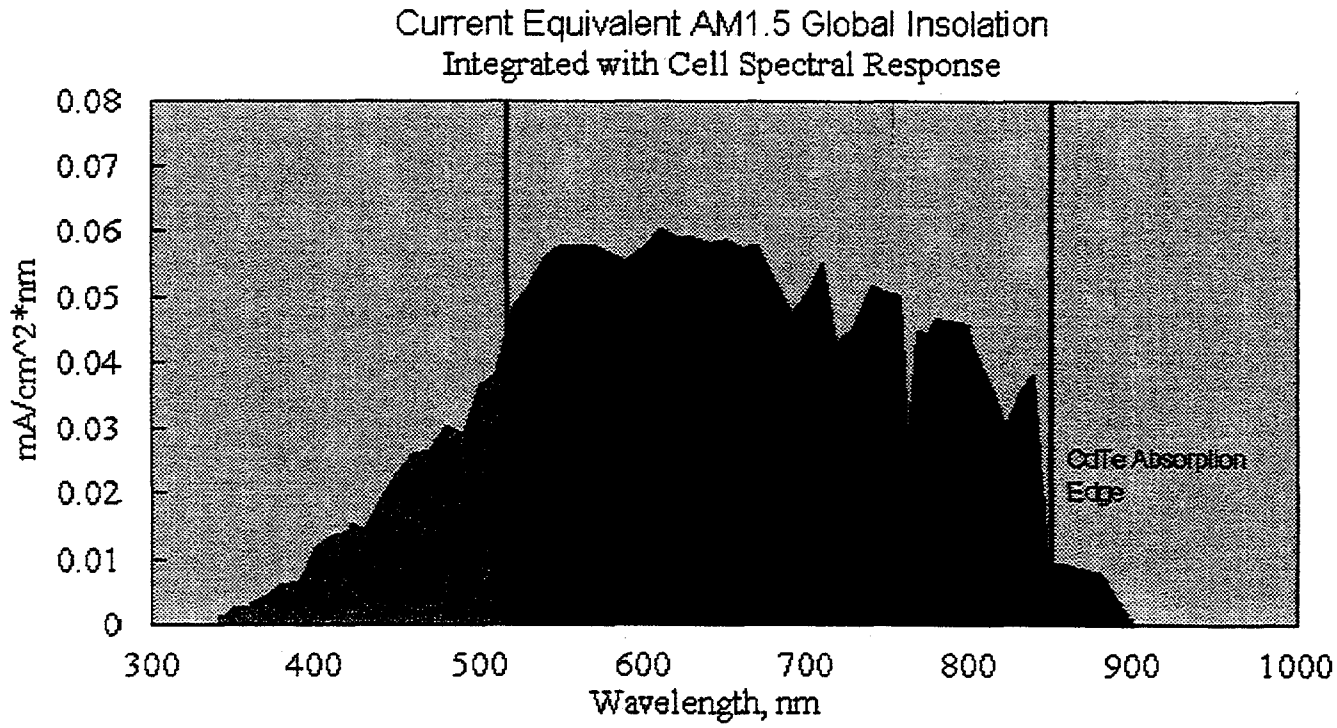


Fig. 14B Equivalent current.

Taking into account these three factors - optimization of material properties, thinning of the CdS, and use of an AR coating; it appears that 22 mA/cm^2 is a practical goal for module Jsc. Analysis of Jsc is summarized in Table 2.

TABLE 2
Jsc Summary

AM 1.5 Spectrum (300 - 860 nm)*		30.8	
Absorption Loss			
Superstrate *	(6.1)		
CdS **	(0.8)		
Net Absorptive Losses		(6.9)	
Reflection Loss			
Superstrate *	(2.7)		
AR Coating	1.1		
Net Reflective Losses		(1.6)	
Losses in CdTe **		(0.3)	
Projected Jsc		22.0	mA/cm^2

* Calculated ** Projected

Fill Factor

Fill factor is analyzed in terms of effective series and shunt resistances and of diode parameters. Series resistance is influenced by conductivity through the semiconductor, by the back contact to the metal, and by interconnect resistance. Shunt resistance is related to semiconductor properties, grain boundaries, localized film defects, and interconnect-related leakage. Diode parameters are related to semiconductor properties and to interface effects. All of these parameters can depend on insolation intensity.

Although all of the factors mentioned above have significant effects, fill factor, and therefore power output, is dominated by shunt resistance effects. See Fig. 15. On the 53 watt

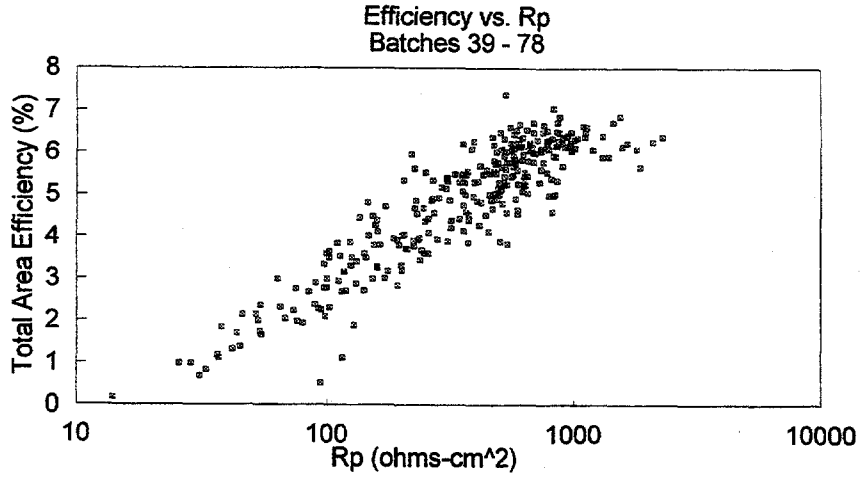


Fig. 15 Observed relationship between efficiency and shunt resistance for 0.72 m^2 modules. Rp is determined from a curve fitting routine.

module the FF was 0.605. The equivalent circuit shunt resistance, as determined from a curve fitting routine [14] was 1130 Ω. (The area normalized shunt resistance, Rp was 520 Ω-cm^2.) As the maximum power voltage was 66 volts, the calculated power loss due to this shunt is 3.9 W. Clearly this is a significant portion of the power output of the module.

Dark I-V measurements are made on 1.0 cm^2 devices which are isolated by laser scribing from the rest of the superstrate. Typical curves (see Fig. 16) exhibit a rectification ratio of 1:1 below ~0.3 volts increasing to 10:1 at 1 volt. Forward biased dark current at 1 volt can be 1-10 mA/cm^2 at 25 °C. This is equivalent to a series resistance of 100-1000 Ω-cm^2. In contrast, series resistance determined from fitting light I-V data indicate a value in the 5 - 10 Ω-cm^2 range. The apparent explanation is that photoconductive effects play a major role. Shunt conductance, on the other hand, is independent of light level below about 5 mW/cm^2.

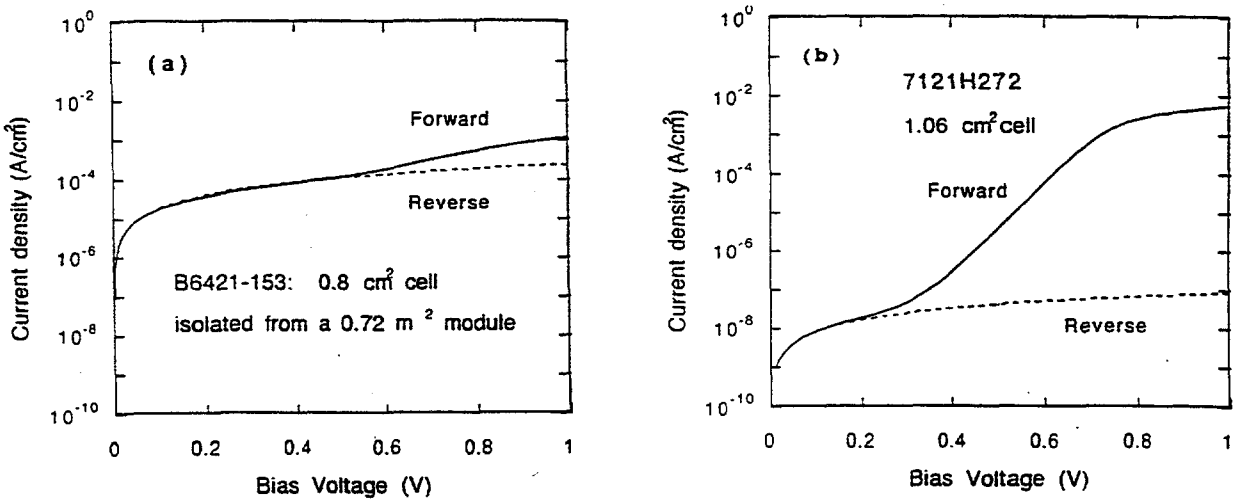


Fig. 16 Comparison of dark I-V curves exhibiting (a) low shunt resistance - typical of small devices isolated from a full module, and (b) high shunt resistance - typical of single cells made on 100 cm^2 superstrates in a research scale deposition system.

Typical dark shunt resistance, as determined from reverse bias current density is ~10^3 Ω-cm^2 and is insensitive to variations in temperature. The lack of temperature sensitivity suggests that reverse leakage is not through the semiconductor but is rather the result of some parallel path. Ebic (electron beam induced current) data reveals localized defects which are on the order of 1 mm^2 and of irregular shape. See Fig. 17. They have a dendritic shape which is suggestive

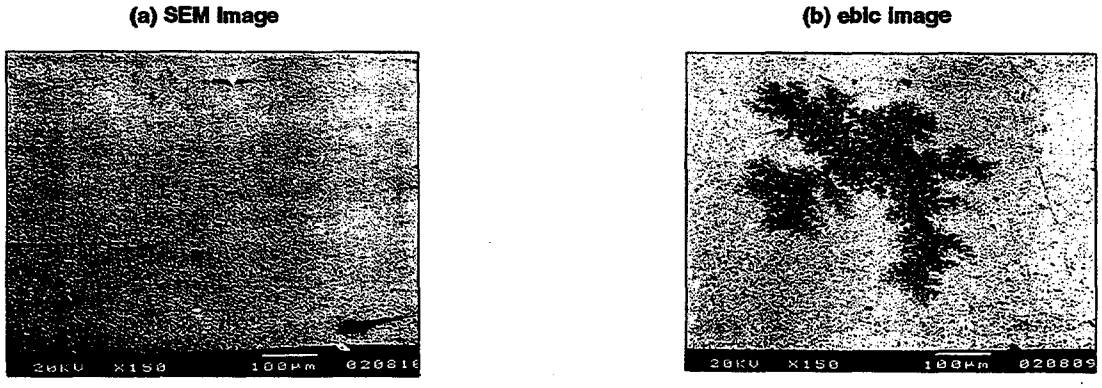
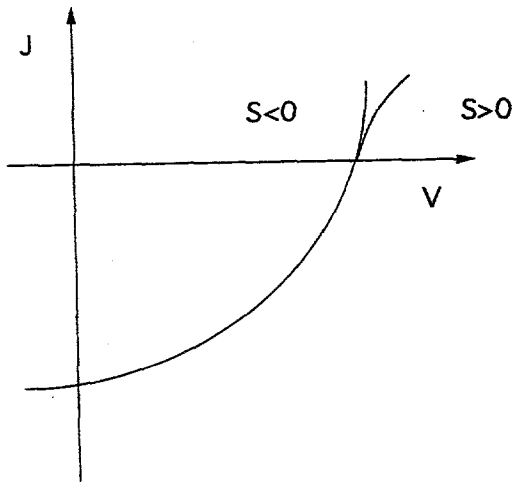


Fig. 17 Comparison of (a) SEM photo and (b) ebic photo of the same area. The ebic image indicates a dendritic shape defect area presumed to be a shunt path.

of a crystalline growth which affects many individual grains. The origin of these defects is unknown, but is under active investigation. Although we do not have direct evidence that these defects are responsible for the shunting, the number per unit area is highest in areas of low shunt resistance.

One manifestation of a back contact effect which is observed in these devices is the "S" curve. This is a characteristic bending over of the light I-V curve in the 1st quadrant. This effect is believed to be caused by a back diode resulting from band bending in the vicinity of the Ni-CdTe interface. At SCI this phenomenon is quantified by measuring the second derivative of voltage with respect to current density at Voc. That is, it is obtained from the best fit parameters to the polynomial $V = Voc + R_s \times J + S \times J^2$. See Fig. 18. The quantity S is negative for ohmic contacts. When S is expressed in units normalized to Jsc, it has the unit volts. Because it affects primarily the characteristics above Voc, even curves with fairly strong S factors can have greater than 7% efficiencies, but the highest efficiency cells have S < 0.5 V. Consistent with its diode nature, S is temperature sensitive and increases dramatically at low temperatures.



Near Voc: $V = V_{oc} + J R_{oc} + J^2 S$

$S = \frac{1}{2}(d^2V / dJ^2)|_{J=0}$

$R_{oc} = dV/dJ|_{J=0}$

$S\ Factor = S*(Jsc)^2$

Fig. 18 Schematic of S curve.

In the absence of parallel shunt paths, FF may be limited by collection of carriers generated in the bulk. As mentioned above, carrier lifetime in SCI's CdTe films is typical of that observed in other efficient CdTe devices, but there is some evidence that current may be limited by carrier mobility. Fill factor is often observed to increase with temperature - a characteristic which may be indicative of thermally activated mobility. [15] It seems more likely, however, that the FF increase can be attributed to a thermally activated decrease in contact resistance.

Other researchers have found that the diode factor is an excellent indicator of cell quality [16] with the highest efficiency devices exhibiting diode factors of ~ 2.1. In our case, however dark diode parameters are not easily obtained as there is no straight section on the typical Log I vs V curve. Diode factors obtained by curve fitting illuminated cells vary in the range of 1.6 - 4. We expect to address this issue more fully once the shunting paths have been better controlled.

In summary, FF is a significant factor in defining material quality and device parameters and it is affected by several factors. The most significant of these are related to localized defects and back contact effects. Some quantitative estimate of its potential for improvement can be obtained by comparison with results from 64 cm^2, 8 cell submodules. Small area interconnected modules have been produced with FF of 0.72. It is expected, therefore, that this same level will also be reached with full size modules.

Open Circuit Voltage

Voc of devices is a function of semiconductor deposition conditions as well as post-deposition treatment conditions. In addition, Voc has been observed to be strongly influenced by the back contact. On the same CdS/CdTe film, graphite contacts usually produce a Voc 10 - 30 mV higher than metal contacts. The highest Voc (830 mV) was observed on a device with Cu doped graphite contact. Graphite interconnects, however, tend to have high bulk and contact resistances. Thus our present strategy has been to continue working with metallic contacts. Recent results on a submodule, see Fig. 11, suggest that high Voc's are obtainable with metallic contacts to the CdTe.

Area Related Losses

As described above, the present module design consists of 116 cells on a 1 cm repeat pattern. In order to provide electrical isolation from ground and encapsulation there is a 1 cm border around the entire perimeter. At each narrow - 60 cm - end there is one additional centimeter provided for a screen printed busbar. The width of the interconnect region is 0.08 cm. Thus the area per cell is 53.4 cm^2 and the total area ratio is 0.86.

These dimensions are believed to be adequate for the present, but they have not been optimized. For example, a calculation that takes into account area losses and I^2R losses due to the SnO_2 resistivity suggests that we should use approximately 132 cells in series. The computed power increase, however, is less than 1% of total power (~0.5 W).

In the longer term, however, we do expect to gain further increases in output power through improved area ratio. At present approximately 538 cm^2 is lost due to interconnects. Reducing the interconnect width to 0.05 cm from 0.08 cm would reduce this lost area to 336 cm^2. The maximum area loss, however, is due to the borders required for electrical isolation from ground as determined form the wet high pot test.[10] With process optimization it may be possible to reduce this dimension. The reduction of the width of the border isolation and the busbars to 0.8 cm, combined with the reduced interconnect width, would increase the area ratio to 0.90.

Mismatch Losses

An important consideration in the production of 0.72 m^2 modules is the uniformity of PV properties across the superstrate. In the best case, module power is the sum of the maximum power of all locations over the surface. In practice, however, the whole can be less than the sum of its parts. This is believed to be due to the constraints that force all areas of a single 58 cm long cell to operate at nearly the same voltage and that force the total current of every cell to be the same. Although not quantified, the first factor seems to have a larger effect. Voltage differences of up to 45 mV have been measured laterally across a single contact with a measured resistance of about 8 Ω. This indicates that lateral currents exist in the back contacts of individual cells.

Figure 19A displays maximum power current and voltage data from several cells isolated by laser scribing from a full module. This destructive test was performed as part of a diagnosis of module operation. The module from which the data in Fig. 19A was obtained had a ratio of

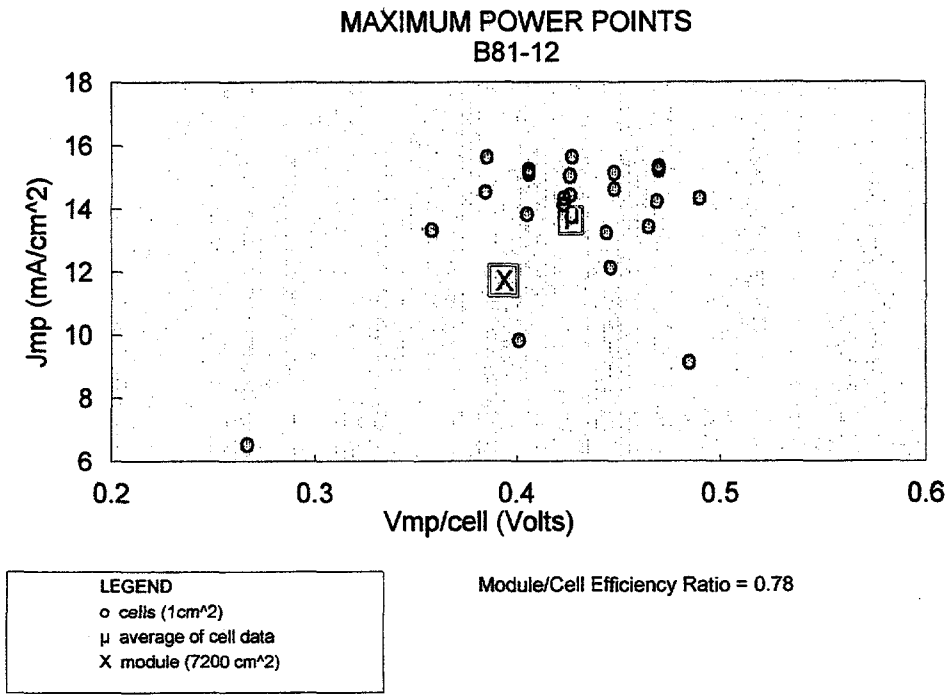


Fig. 19A Max power point distribution - B81-12.

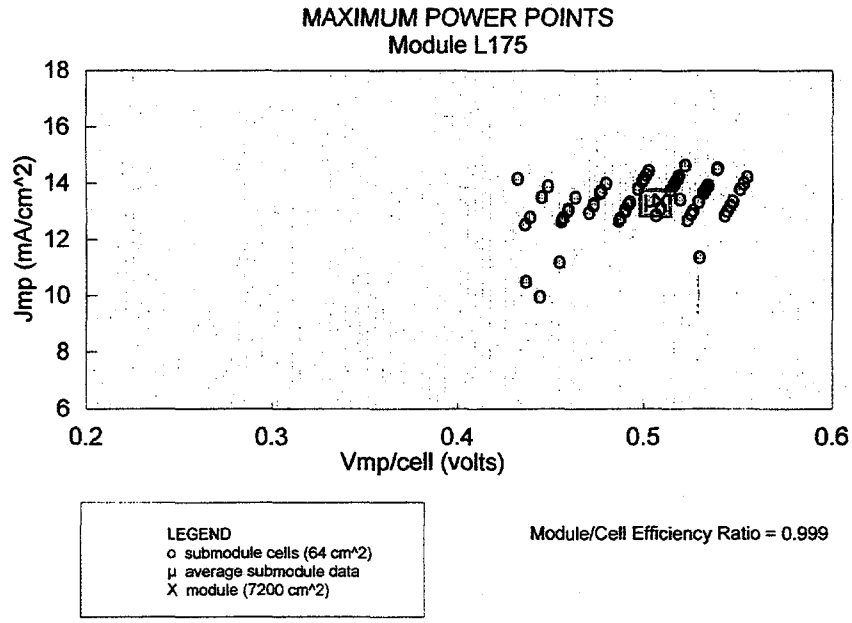


Fig. 19B Max power point distribution - L175.

module active area efficiency to average cell efficiency of 0.78. This data does not lend itself to quantitative analysis, but it does suggest that, in this case, the spread in maximum power points could be partially responsible for the reduced power output of the module.

Figure 19B displays similar data from a higher efficiency module. In this case, each data point represents a 64 cm^2 submodule. The fact that the calculated average of submodule maximum power points coincides with the observed module operating point would suggest that

we have an ideal situation and that there are no mismatch losses. In reality, however, this coincidence is probably accidental as it is probable that there was at least some damage to the submodules done during their isolation from the module. These results are consistent with the notion that a tighter pattern of maximum power points will lead to higher module output.

Considering all of these factors together, by increasing Jsc to 22 mA/cm^2, FF to 0.72, Voc/cell to 0.83 V, area ratio to 0.90, and minimizing mismatch losses, we could increase active area efficiency to 13.2% and power output to 85 W.

CFR (Channel Flow Reactor)

In order to improve control over the vapor pressure of the source elements at the deposition surface, SCI has a program investigating the use of elemental sources rather than powders to produce the Cd and Te_2 gasses. In this case the elemental vapors are carried by an inert gas from heated crucibles into a mixing tube, and then down a channel to the superstrate. The deposition equipment, which is called a channel flow reactor, CFR, is described more fully in Ref. 6.

During phase II of the contract, the CFR has been redesigned and rebuilt using graphite and quartz. In addition, the heating elements have been constructed using heavy duty elements. These changes have greatly reduced down time and increased the number of deposition runs performed. Nonetheless, progress has been slower than expected and this deposition process is relatively immature.

We have, however, demonstrated that atmospheric pressure EVD, APEVD, of CdTe is possible and feasible for use in a manufacturing environment. Using a N_2 carrier gas at 600 torr, CdTe has been deposited at a rate of one micron per minute onto 100 cm^2 superstrates. In order to better understand the mass transport, the CFR was designed to produce films as the carrier gas flows horizontally across the superstrate surface. The films produced vary in thickness approximately as exp {- X/L} where x is the distance from the upstream edge of the superstrate and L is a characteristic deposition length which is determined empirically. The characteristic length is typically in the range $2 < L < 10$ cm. See Fig. 20.

Although film thickness is intentionally non-uniform, a few small devices were produced. Cells fabricated using Cu-doped graphite contacts produced 8 + % efficient devices with an area of 0.24 cm^2.

APEVD continues to show promise as a next generation process for semiconductor deposition. Indications are that deposition rate and film quality are comparable with those achieved at lower pressure, while equipment design can be greatly simplified. Work remains to be done in the design and testing of crucibles, the gas flow system, and the superstrate transport and temperature control systems.

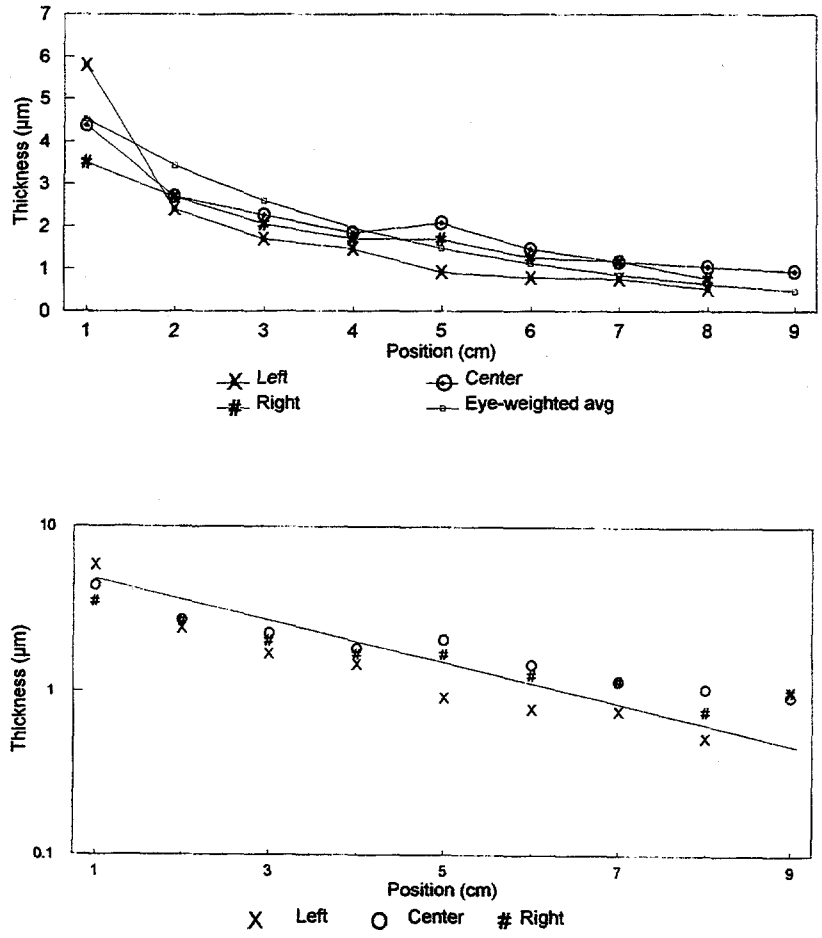


Fig. 20 Thickness profile of CFR deposited film.

SAFETY, HEALTH, ENVIRONMENT AND DISPOSAL

Safety and health of workers, environmental control of the production process, and disposal of product at the end of its useful life continue to be high priority objectives of the PV program. From its inception, SCI has pursued a vigorous policy of strictly monitoring and protecting employee safety and health. Prior to exposure to any Cd-bearing materials, all employees were given a complete physical including a urine analysis which tested for Cd. This is followed up by urine analyses on every employee at six month intervals. No employees have been found to have urine Cd levels above the normal range.

Airborne cadmium continues to be monitored periodically in work, laboratory and office spaces. Selected personnel have worn personal air samplers. In no case have airborne Cd levels been determined to exceed OSHA standards, even with the new PEL of 5 $\mu g/m^3$. As an additional precaution, however, personnel wear lab coats, gloves and goggles for certain operations.

In order to determine the amount of Cd-bearing compounds released into the environment, air exhausted from the deposition chambers is monitored for Cd compounds. In spite of the relatively high vapor pressures existing within the chambers, there is no evidence of Cd compounds in the pump exhausts or in the mechanical pump oil.

Regarding disposal of spent modules, active discussions continue between SCI and its suppliers, with government officials, and with other members of the PV community. SCI was an active participant in a workshop dedicated to the recycling of Cd and Se bearing wastes [17]. It is not yet known whether spent modules will have to be treated as toxic waste or whether they can simply be placed into landfills. In any case, it is hoped that spent modules will not have to be discarded, but rather can be recycled.

SUMMARY

The second year of the subcontract has emphasized process extension and optimization. The process was extended to include the steps of lead attachment, encapsulation, panelization and array construction. Optimization of the process has led to the fabrication of more efficient modules at higher yield. All three categories of devices - cells, submodules, and modules - attained efficiencies close to the contract goals. In addition, APEVD has been successfully demonstrated.

Specific accomplishments include:

1.) Fabrication of a 53 watt (7.4% efficiency) 7200 cm^2 module.

2.) Achievement of 9.8% efficiency on a 64 cm^2 8 cell submodule.

3.) Achievement of 10.4% efficiency on a 1 cm^2 cell.

4.) Design and construction of a 1kW PV array.

5.) Demonstration of the production of modules with an average power output of 43 watts (6% efficient) on a prototype manufacturing line.

6.) Successful completion of the IQT on a batch of modules.

7.) Demonstration of atmospheric pressure elemental vapor deposition as a viable technique for high throughput deposition of CdTe films.

8.) Performance of device measurements and loss analysis which indicate the potential of this process to produce 85 watt modules.

FUTURE PLANS

Future work will emphasize improvements in device efficiency, process yield, and device stability. In addition, work will continue to better control and improve the APEVD process and specifically to extend it to deposition of CdS films. Furthermore, issues relating to environmentally sound disposal and recycling of Cd bearing wastes and modules will be addressed and clarified.

Efficiency will be improved through designed experimentation, device analysis, and possibly through equipment modification. The process will be greatly enhanced as our in-house analytical capabilities continue to improve. We will add capacitance to the list of measurements available in our analytical system and will continue to take advantage of the vast analytical

resources available at NREL. Analysis of these measurements will allow us to model device operation and determine where best to minimize losses. The effects of process variations will be determined through analysis of designed experiments. If this analysis reveals deficiencies in the present process equipment, it will be modified accordingly.

Increases in yield will come about as a result of tightening of deposition process variations through the use of indicators to provide feedback on every step. "Indicators" are measured quantities which are directly related to a given portion of the process. Examples are the thickness, optical transmission and surface texture of films. These quantities are directly influenced by film deposition parameters but their precise relationship with device properties may be unknown.

Stability will be addressed first by developing a stress testing protocol which will provide accelerated life testing with some confidence in predicting device stability over time. Devices will be subjected to various combinations and levels of heat, voltage bias, light bias, humidity, and oxygen concentration. The effect on device operation will be measured and analyzed. This process will provide information on degradation mechanisms and will allow estimation of lifetime through extrapolation of results to the normal operating conditions.

Thus, the final phase of the subcontract is expected to result in improved device efficiency, higher process yield, proven stability, improved semiconductor deposition techniques, and a well defined environmental program.

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[1] Nolan, J.F., "Development of 60 cm x 120 cm Thin Film CdTe PV Modules", to be published in Proc. 23rd IEEE PVSC, May 1993.

[2] Meyers, P.V., T. Zhou, R.C. Powell, N. Reiter, "Elemental Vapor Deposited Polycrystalline CdTe Thin Film Photovoltaic Modules", to be published in Proc. 23rd IEEE PVSC, May 1993.

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16. Abstract (Limit: 200 words)

This report highlights the progress made by Solar Cells, Inc. (SCI), in its program to produce 60-cm x 120-cm solar modules based on CdTe films. During the past year, confirmed efficiency has increased to 10.4% (active area) on a 1 cm^2 cell, 9.8% (aperture area) on a 64-cm^2 8-cell submodule, and 6.6% (total area) on a 7200-cm^2 module. A module measured in-house had a power output of 53 W, for a total-area efficiency of 7.4%. Average efficiency of modules produced is steadily increasing and standard deviation is decreasing; in a limited run of 12 modules, results were 6.3% (± 0.2%). Field testing has begun; a nominal 1-kW array of 24 modules was set up adjacent to SCI's facilities. Analysis indicates that present modules are limited in efficiency by shunt resistance and optical absorption losses in the glass superstrate. Loss analysis of present devices allows us to project a module efficiency of 11.8%. A third generation deposition method—atmospheric pressure elemental vapor deposition (APEVD) has been brought on-line and has produced good quality CdTe. In addition, SCI is expanding its proactive safety, health, environmental, and disposal program dealing with issues surrounding cadmium.

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