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Advanced Processing Technology for High-Efficiency Thin-Film $CuInSe_2$ Solar Cells

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SUMMARY

This project has as its primary focus the development of novel fabrication processes for CIS solar cells that will result in improved performance and cost effectiveness at the manufacturing level. The primary approach that has been pursued involves all solid-state processing for CIS. This is augmented by efforts to provide novel alternatives for formation of the window layer/heterojunction contact. Inherent to the project is the need to develop generic understanding of the relationship between processing and performance so that broad-based transfer to industry can be facilitated.

We have achieved good electronic quality CIS by use of two selenization procedures for predeposited metal layers. We have demonstrated the achievement of good stoichiometry throughout the bulk of the film, have attained grain sizes of up to 1 μm, and have measured electron mobilities of up to 60 $cm^2/V\text{-}s$. However, we observe a complex relationship among grain size, adhesion and performance. Representative films have been delivered to NREL.

Our primary approach to characterization is to fabricate ZnO/CIS test devices and measure as many properties as possible in device format. The attainment of good bulk properties has been confirmed by attainment of J_{sc}'s in the mid thirties mA/cm^2 range. While on occasion we have attained V_{oc}'s of order 340 mV, in our routine devices V_{oc}'s are more typically in the 200 - 240 mV range. It is notable that for a given CIS layer V_{oc} is the same for both ZnO/CIS and ZnO/CdS/CIS structures. This suggests a defective surface that is pinning the fermi level. This is the primary mechanism that is limiting device performance.

We speculate that the surface of our films is defective due to the presence of excess In that is a consequence of conditions used to achieve good bulk properties. We have begun modifications to our process to eliminate the surface defects while maintaining bulk performance.

Reactive sputtering of ZnO is also being developed as an alternative window layer technology. With Al doping we have achieved resistivities of 9×10^{-4} ohm-cm and good optical properties.* In forming ZnO:Al/CIS junctions we have observed sensitivity of the interface to the presence of Al. Al appears to be similar to its group III counterpart In in creating interface defects. As an alternative we have used F as a dopant for the first time with reactively sputtered ZnO. F may not cause difficulties at the interface as Al apparently does. F can be an etchant as well as a dopant, and thus provides interesting opportunities for enhancing film properties. Initial results with ZnO:F films indicate similar performance to ZnO:Al films but also a need to further understand and control the dual etchant/dopant role. High deposition rates are also necessary for manufacturing feasibility, and we have thus far pushed the rates up to 9 Å/s without significant deterioration of properties. We also observe improved uniformity with reactively sputtered films which is due to a more favorable growth mechanism. These results indicate good potential for this technology at a manufacturing level.

* A value of 4.2×10^{-4} ohm-cm has now been achieved.

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INTRODUCTION

The success of $CuInSe_2$(CIS) as a photovoltaic material depends largely on its manufacturability. Its current laboratory efficiency of over 15%[1] assures that efficiency objectives can be met, but manufacturability is yet to be proven. While the predominant H_2Se based deposition technology looks promising, it is desirable to explore other possibilities to diversify the base of opportunities. To this end we have chosen to develop a novel deposition technology for CIS with the following key characteristics:

* All solid-state processing

* Manufacturing-driven processing steps

The first avoids H_2Se as a fuel and the inconvenience and added cost that accompanies its use. The coevaporation process developed by Boeing accomplishes this objective in achieving high efficiency without use of H_2Se, and thus is a proof of concept. However, we do not feel that the Boeing process represents optimum choices from a manufacturing perspective. Our second characteristic addresses additional constraints that we feel are important in choosing an approach. For example, our techniques include high deposition rates and relaxed control of arriving fluxes. In addition, we would also desire a process which is not very temperature sensitive because of the difficulty of maintaining uniform temperatures over large areas.

In studying available phase diagrams and other fundamental data we have identified pathways that we believe might meet our process criteria. However, the available data on CIS is limited in this regard in many key areas. We thus find it necessary to explore pathways to determine what can be done rather than knowing that a solution exists and that we need only find the way to it. Thus during the initial stages of the project we place temperature sensitivity at a lower level of priority because deposition rate and flux control constraints in themselves place significant limits on the range of opportunities in deposition space. Our approach is to first find at least one process sequence that meets these constraints and then determine its temperature sensitivity by variations in the anneal profile. We hope to determine that the resulting temperature sensitivity is acceptable and if not to try to make it so by varying other accommodating parameters. If the process sequence is found to not meet all of our criteria, we will then move on to search for another. The bottom line is that we are not interested in mapping out the regimes in deposition space that can produce efficient devices independent of the practicality of those regimes. Instead, we are driven to find those regimes which meet our manufacturability criteria as well as the necessary criteria for high efficiency.

In choosing deposition paths we are relying heavily on available, though limited, phase information. At a minimum this helps us to avoid regions which will produce material other than single phase, chalcopyrite CIS. However, within the regime of single phase, chalcopyrite CIS there is little more to guide us toward optimized material. The microscopic defect structure of CIS is rather complex. The relationship of electronic properties to that

structure is more complex, and the connection between these properties and device performance adds yet another layer of complexity. Consequently, our primary approach to evaluating material properties is to make solar cell devices and use them as a format for characterizing the material. Thus even the early stages of this project which emphasizes materials development are conducted under the format of device fabrication and evaluation. Virtually every CIS deposition (we are now completing two a day) results in fabrication of solar cell devices and evaluation of the material in that format.

The format of this report is structured according to the major task areas of the project. In Section I we discuss Processing and Film Growth. The emphasis of this section is on deposition methodology. Only "first order" film properties are discussed as they are used to guide processing choices. In section II we discuss Device Fabrication and Performance Analysis. Although our goal is to develop the highest efficiencies in fully engineered devices, during the early stages of the project the emphasis is on diagnostic devices to guide processing, and the discussion is focussed accordingly. In this section we also address the need for advanced analysis of our materials and devices. The intent is to contribute data and understanding to the development of a generic model for CIS that will expedite industry's drive to commercialization. In Section III we discuss efforts to develop Improved Contacts and Window Layers. Activities in this area address two primary objectives: improved understanding of the requirements for forming an effective heterojunction contact for our CIS films, and development of alternative deposition technologies for contact materials.

SECTION I

PROCESSING AND FILM GROWTH

1.1 PROCESS CHOICES

From a manufacturing perspective direct sputtering of CIS would be highly desirable. While reasonably good performance might be achieved, it appears that sputtering rates would be too low to meet cost objectives. Judicious use of binary sputtering targets may offer an acceptable solution if again high rates can be achieved.[2] It is, however, possible to sputter Cu and In at very high rates. Because of its high vapor pressure Se presents more of a problem for sputtering, but it can certainly be deposited at very high rates by thermal evaporation. Thus as an alternative to direct sputtering of CIS one should consider high rate sputtering/deposition of the elements. Ideally, one would hope to sequentially sputter/deposit layers of Cu, In and Se and perform a simple anneal to produce device quality CIS. The reaction

$$Cu(s) + In(s) + Se_2(g) \text{ ----> } CuInSe_2 \qquad (1)$$

(s - solid, g - gas) has a free energy of formation of -230 kJ/mole at 700 K, which is lower than the value of -200 kJ/mole for the H_2Se based reaction

$$Cu(s) + In(s) + 2\ H_2Se(g) \text{ ----> } CuInSe_2 \qquad (2)$$

and thus is thermodynamically favorable[3]. In the desired process sequence solid Se would be used which would result in an increase of the free energy, but the reaction would still be thermodynamically acceptable.

As further guidance one can look to available phase data[4]. While significant areas of the phase diagram have been mapped out, there are gaps and uncertainties relative to layering of precursors and controlled availability of components. The available phase data is thus useful in suggesting general approaches, but is not able to predict a priori what can and can not be accomplished.

Several laboratories have undertaken the development of CIS with these ideas in mind[3,5,6,7]. The recent work by D. Albin et al of NREL has nicely delineated some of the key issues related to this pursuit. Their approach involves deposition of Cu and In followed by use of a controlled Se flux. Thus the thermodynamics of equation (1) applies, while conventional phase data does not. In investigating phase related phenomena this group has shown that the formation of Cu and In precursors plays a key role in the eventual formation of CIS. Also, to achieve the best device performance it is necessary to properly control the Se flux. These insights have been very helpful in guiding our processing efforts.

The processing approaches that we are pursuing are those which are most desirable for manufacturing, but which also have the greatest technical uncertainty. These processes have as a common element the sequential deposition of Cu, In and Se. The primary variables are the anneal profile, the metal ratios, and the exercise of some control over the availability of

Se.

A schematic diagram of our process is given in figure 1 below. The glass substrate has been coated already with successive layers of Mo, Cu, In and Se by sputtering/evaporation. The substrate is then placed on a resistively heated platen in an annealing chamber.

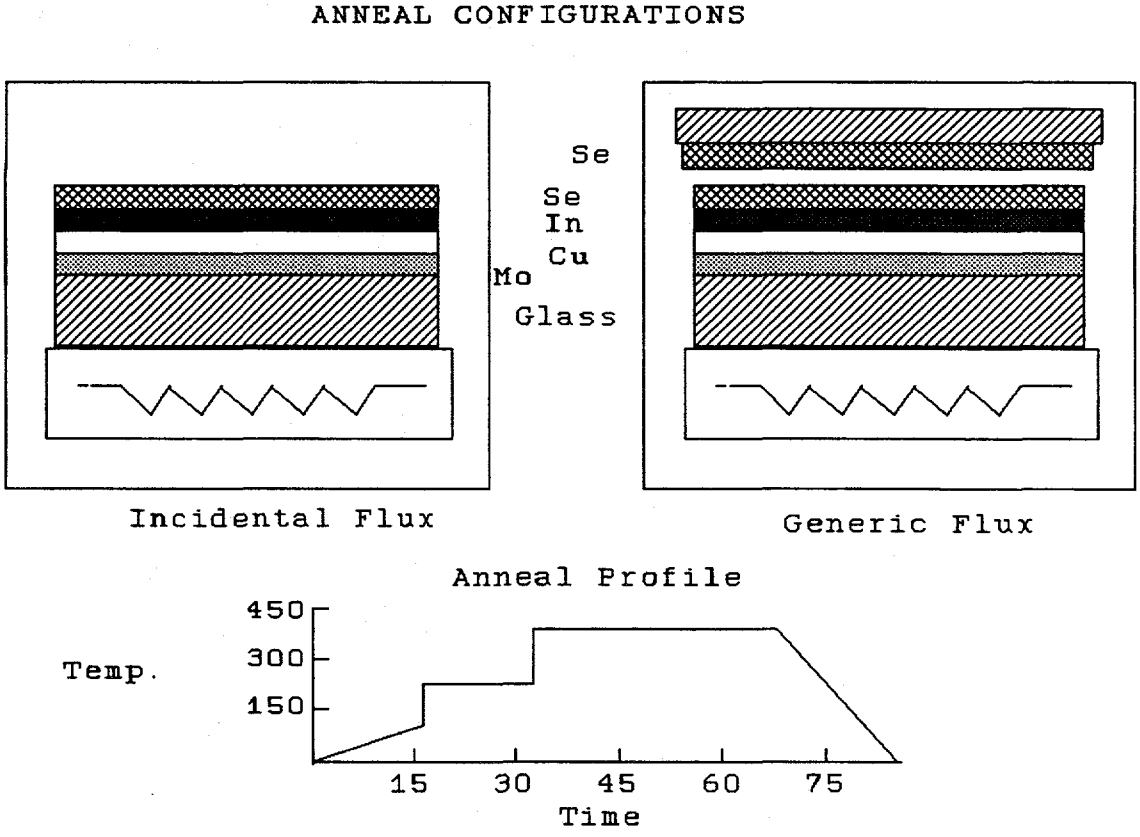


Figure 1

The configuration of the annealing chamber allows for two major variations in the anneal process relative to the availability of Se. In the case we term "incidental flux" excess Se is deposited on the substrate. As the anneal profile exceeds the vaporization temperature of Se the excess Se leaves the surface and is not constrained in its movement. There will be a residual incidental flux of Se in the chamber as the anneal process continues due to the presence of this excess. In the case we term "generic flux" the substrate and chamber are configured to achieve some control on the movement of excess Se. The intent in this case is to provide some control of Se flux on the forming CIS surface as it is annealed beyond the Se vaporization temperature. This is accomplished in part by placing a source of selenium above the substrate as shown above. From a manufacturing perspective both processes are straightforward, though the incidental flux case is the better of the two because it allows for greater flexibility in other parameters.

1.2 PROCESS DESCRIPTION

1.2.1 Substrate Preparation

Our substrate is 10 cm x 10 cm, 2 - 3 mm thick sodalime glass which we purchase from the local hardware store. Upon receipt the glass is cleaned by the following procedure:

* Detergent wash
* Ultrasonic wash and scrub in detergent
* Rinse in DI water
* Ultrasonic rinse in tichloro-trifloroethane
* Hot water rinse at 90° with bubbling nitrogen
* Rinse in DI water, blow dry
* Bake overnight at 80°

1.2.2 Metal Deposition

The substrate is then loaded into our deposition chamber which is designed to permit heating and movement of the substrate over the source during deposition. Our deposition sources for Mo, Cu and In are two 3 inch magnetron sputtering guns which are powered by D.C. Our sputtering targets are all 4 - 5 9's pure. The source to substrate distance is of order 10 cm, and a typical sputtering pressure is 2 mTorr of Ar. By movement of the substrate during deposition we achieve excellent thickness uniformity.

In a typical process sequence we first deposit .7 - 1 μm of Mo. The chamber is then opened to allow changeout of the Mo target with the In target. After pumpdown successive layers of Cu and In are deposited to the desired Cu/In ratio. The metal depositions are at room temperature. Layer thicknesses are monitored during deposition by judiciously placed thickness monitors. Film thicknesses are verified by cross checks on two thickness profilers. Typical Cu and In thickness are 1500 Å and 3360 Å respectively.

1.2.3 Selenium Deposition

The substrate is then loaded into another vacuum chamber for Se deposition. In this case the Se is deposited by thermal evaporation. Good uniformity is again achieved by moving the substrate during deposition. For our desired process sequence the substrate is kept at room temperature during Se deposition. For the Cu and In thicknesses indicated above we would deposit about 7500 Å of Se for stoichiometry and more as desired to provide for Se flux during the higher temperature stages of the anneal.

1.2.4 Annealing

Following Se deposition the substrate is cut into 5 cm x 5 cm pieces to allow for variations in the anneal step. The primary variable is the two types of flux environments discussed above. We have two different annealing chambers to accommodate this variable. Chamber A is used for generic flux annealing. It consists of a 6 inch diameter quartz vessel with full vacuum capability. The substrate carrier is resistively heated and is placed inside of the quartz vessel. The chamber is pumped down and then backfilled with Ar to a pressure of about 500 mTorr to accommodate effective transfer of heat to the substrate. The anneal profile is then dialed in to the controller according to the desired formula. Our anneal profiles range from a continuous ramp up to 400 ° in one hour(or less) to a 2 - 4 step sequence of up to 2 hours at each temperature increment.

Chamber B is used for incidental flux anneals. It is essentially a 3 inch diameter, 8 zone open tube furnace. There is a continuous flow of He through the tube to control the environment. The substrate is loaded onto a carrier and then moved from one temperature zone to the next according to the desired temperature profile.

1.2.5 Device Fabrication

As discussed above the primary means of evaluating materials properties in this project is measurement of these properties in device format. In order to minimize the influence of junction formation procedures on this evaluation process a reasonably non-intrusive process was chosen. The process consists of sputter deposition of Al doped ZnO. We avoid in this case the use of solution deposition because of the effect that the solution components can have on the CIS surface above and beyond the deposition of the heterojunction material. We also chose to use ZnO over CdS even though it is known to form inferior junctions because we feel that ZnO junctions will nevertheless allow a fair evaluation of bulk properties, and further, we believe that we will in time be able to develop ZnO or other non CdS junctions that will be as good as CdS.

The deposition of the ZnO heterojunction contact is accomplished by R.F. magnetron sputtering from either a doped ZnO target, or an undoped target with pieces of Al_2O_3 on its surface. We first deposit an undoped layer of about 200 Å in thickness followed by a doped layer about 5000 Å thick. The substrate is heated between 100° and 300° during the deposition. For diagnostic devices we deposit about 10 .1 cm^2 devices covering an area of about 10 cm^2. Additional devices are made by solution deposition of CdS for selected samples. Further details about this process as well as about experimental development of ZnO are provided in Sections II and III.

1.3 FILM PROPERTIES

1.3.1 Compositional and Structural Properties

The first level quality check on the CIS films is stoichiometry. This is monitored by using EDS on our JEOL 840 SEM. This technique is limited by both

the sensitivity and resolution of the instrument and by matrix effects in the sample. To minimize the latter it is necessary to have reference samples that closely match the composition of a given experimental sample. To facilitate this process NREL[8] has kindly provided us with a set of reference samples. Representative atomic composition results from three recent samples are shown in Table I below.

TABLE I. SAMPLE COMPOSITION DETERMINED BY EDS

SAMPLE	Cu(%)	In(%)	Se(%)
A21	23.43	25.04	51.53
A40	24.48	26.94	48.57
A45	24.13	25.34	50.53

As can be seen the samples are all near perfect stoichiometry, and slightly In rich as desired.

Because the electron beam only probes to a depth of order 5000 Å these values are representative of only that part of the sample, although it is the most important. Nevertheless it is desirable to know the composition of the entire sample both to gauge the extent to which CIS formation occurs throughout the layers and to understand the nature of the remaining bulk material even though it may be outside of the space charge region. To accomplish this a piece of film was peeled from the substrate so that the composition of the bottom of the film near the Mo substrate could also be measured. The results are shown in the Table II below.

TABLE II. COMPOSITION OF TOP AND BOTTOM OF SAMPLE

	PEELED SAMPLE		MO SURFACE
	TOP	BOTTOM	
CU	24.5	23.3	0
IN	27.0	27.6	03.2
SE	48.5	49.1	20.0
MO	0	0	76.8

As can be seen, there is little difference between the top and bottom composition for this sample indicating that CIS formation in terms of composition is fairly homogeneous. It is interesting to note that both top and bottom surfaces/interfaces of the sample are In rich as a result of using Cu/In < 1 in the deposited films. The composition of the Mo surface from which the film was peeled is also shown in the table. Although the exact values here are less reliable because they are standardless(i e, not against an appropriate reference), they confirm the presence of In at the back interface and highlight the great propensity for Cu to diffuse into and form CIS. The high level of Se is also important in that it verifies access by Se to the entire film thickness. It is likely that the Se in this region is in

the form of $MoSe_2$.

The gross structural features of the films were also examined by SEM imaging. Surface features of the films from Table I are shown in figure 2. As can be seen, although the stoichiometry is nearly the same for these samples, there are notable differences in structural properties. Sample A21 is one of the best samples(I_{sc} > 30 mA/cm^2). Its average grain size is of order .7 μm. Sample A45 has similar grain size to A21, but is notably lower in performance. Sample A40 exhibits large clusters composed of finer grains which is due to a lower processing temperature. Although it is notably different in structure and performs poorly with the standard ZnO contact, its performance approaches that of A21 with a CdS heterojunction contact. It is apparent that grain size is not correlated in a straightforward way with performance. One also has to be concerned with the presence of subphases and point defects as well as the interplay between surface and bulk properties and how these are affected by contact formation. These issues will be discussed in further detail in later sections.

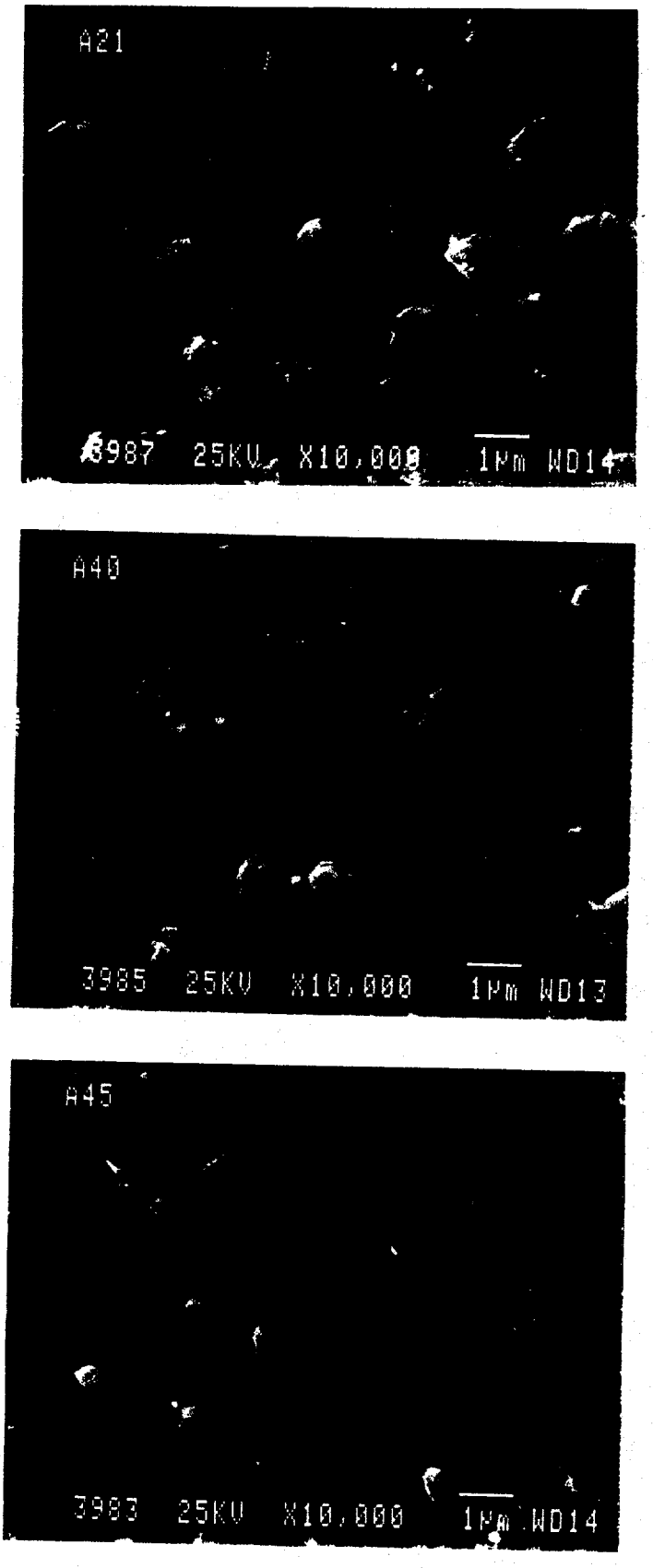

A21
3987 25KV X10,000 1μm WD14
A40
3985 25KV X10,000 1μm WD13
A45
3983 25KV X10,000 1μm WD14

Figure 2

1.3.2 Adhesion

Of equal complexity to the formation of CIS is the formation and performance of the interface with Mo. In all processes such as those here starting with deposition of the elemental components there is a large change in density as the film is formed. It is somewhat unexpected that good adherence should occur under such conditions, and yet it does, though not always. As we have studied the influence on adhesion of various parameters we have observed some distinct dependencies, but we have also seen many of these become ineffective as we extended another parameter beyond a certain range. From this ongoing interplay we have distilled a few observations which seem to be fundamental and which help guide our thinking. The first is chemical in nature. As the data in Table II above show we are able to effect good stoichiometry throughout the film. Of equal importance is the presence of Se in the Mo as well as in the back surface of the film. The formation of $MoSe_x$ serves as an effective buffer between the Mo and CIS, perhaps because of its similarity to MoS_2 which is sometimes used in "lubricating" formulations. If selenization is incomplete, this layer does not form, and the integrity of the back interface is sacrificed. In general we have found that it is not difficult to achieve complete selenization. However, as we try to reduce the time of the selenization/anneal steps we find some shortcomings in back interface properties.

Adhesion and film formation are also found to be somewhat in competition. That is, we have observed an apparent correlation between grain size and adhesion. Unfortunately, the larger the grain size, the poorer the adhesion. Our hypothesis is that this phenomenon is somewhat due to the large change in density. That is, the nucleation density and eventual grain size determine the topology of the interface. Low nucleation density and larger grains result in fewer bonding sites with the interface, and adhesive strength is directly proportional to the density of these bonding sites. However, the transport properties of CIS are good enough that one can back off a bit in grain size for the sake of adhesion and not suffer in carrier collection. It is thus important in a given process to understand this interrelationship and be able to tune the process accordingly. In our process we observe that the transition through 227° is critical to adhesion and electronic properties. Our films undergo a critical phase change at this temperature which is instrumental in nucleation and growth. By proper control of our anneal profile through this range we have been able to achieve good adhesion. However, we have just begun to examine this issue and can offer only a hypothesis and preliminary supportive data at this time. As we vary deposition parameters to improve other aspects of performance we fully expect new dimensions to the adhesion phenomenon to unfold.

1.3.3 Electronic Properties

As a defect semiconductor CIS presents a significant challenge to optimization of its electronic properties for PV device fabrication. The literature is replete with examples of devices which require post fabrication annealing, treatment in oxygen, or treatment in hydrazine, etc. Collectively this represents our ingenuity in engineering our way around our lack of true understanding. This situation is not going to change easily, but ongoing

efforts to fill this void of understanding must be maintained. In recognition of the overall challenges which we face, as with others, our project contains a large measure of pragmatism. As a comprehensive-device oriented project we can not dwell upon a systematic approach of first building up a complete understanding of materials properties and then moving on to device fabrication. Rather, we must identify those key material properties which we feel are necessary for device fabrication, attain them and then immediately begin making devices. Device performance is then used to guide process development, while materials properties and their understanding become a by-product of this process. As device success is attained we can then cycle back and gain understanding of key material properties in proper context. We have taken a somewhat unique approach in that we first developed our CIS deposition process for fabrication of thin-film transistors(TFT). TFT's are surface devices, and much of what we learned about interface properties is helpful to PV device fabrication. However, certain types of TFT's also require good bulk properties, particularly control of the bulk fermi level. We were successful in controlling both bulk and surface properties and reported the first TFT's made with CIS[9]. In particular, we reported the attainment of both near intrinsic and "doped" electronic quality CIS which made fabrication of these devices possible. However, the film thickness in TFT's is only 1000 Å, and the challenge was to extend these capabilities to 2 μm thicknesses which seems to be necessary for solar cells.

Another major difference from our TFT work is the need to deposit CIS on Mo rather than glass. This affects both the properties of the film as well as the options available for characterizing those properties. Consequently, as discussed above, the main technique which we use for characterizing electronic properties is fabrication and analysis of ZnO/CIS diagnostic devices. For bulk electronic properties we use I_{sc} as our key parameter. Achieving a high I_{sc} is an existence proof that good transport properties have been achieved. It tells us little, however, about the aspects of the material that resulted in those properties. For our better devices we use additional measurements to learn more of those properties, though again within the constraints of what can be measured in device format.

At present our best devices are exhibiting I_{sc}'s in the range 30 - 33 mA/cm^2. We believe that this is indicative of the attainment of good bulk electronic properties. These currents are also still somewhat limited by device level problems which will be discussed in the section on devices. A typical spectral response is shown in figure 3. As can be seen the response drops off slowly from the peak at about 750 nm out to 1200 nm indicating good collection efficiency out to the band gap. Note that the response below 500 nm has been cut off pending calibration with a suitable reference. The spectrum as shown has been generated using an NREL supplied reference cell[10] with a CdS heterojunction which precludes its use below 500 nm.

Additional information about the properties of the CIS in the space charge region of the device are determined from C-V measurements. For these films we determine a "doping" level of 9 x 10^{15}/cm^3 at present from analysis of the slope of the C-V curves. While this is a reasonable value and is consistent with the observed spectral response, it is about an order of magnitude higher than we were able to achieve with 1000 Å films on glass substrates. Part of

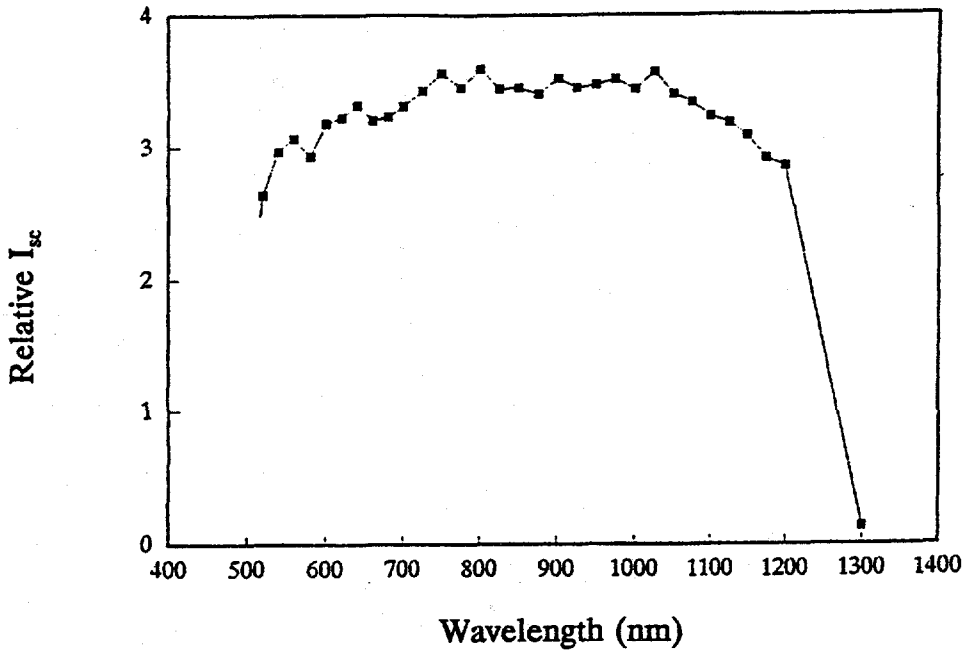


Figure 3

the difficulty is that the analysis is not straightforward. We observe frequency dependence in the C-V data as well as some dispersion in the slopes as shown in figure 4. This behavior is not unexpected because we know that surface phenomena are contributing to these signals, and we know that our surface properties are not yet ideal. Thus these measurements are giving us lower limits on our bulk properties(and in fact are indicating that even those lower limits are good) and are providing useful insights into surface phenomena. The details of these surface phenomena and their interaction with the bulk will be discussed in the section on devices.

The final aspect of material properties which we wish to discuss here is uniformity. As discussed above we have designed our deposition process to achieve good uniformity over 10 cm x 10 cm areas. While thickness uniformity to within 10% is desired, the kinetics and thermodynamics of the process are expected to be self limiting and can thus tolerate some deviations. That is, the films are always grown in an excess of Se rather than requiring an exact amount, and both In and Cu are very mobile and are likely to find their way to where they are needed rather than to conform to a local environment. The volatility of both elemental and compound species is also instrumental in this self regulating process. Therefore, irregularities in device level phenomena are more likely to pose uniformity problems. We thus focus on device level measurements to evaluate the uniformity of our processing.

Defects in glass substrates and glass cleanliness are critical to nucleation and growth and must be carefully monitored. Irregularities in the interface during formation of the heterojunction can also be instrumental in limiting performance. Although we are not yet paying due diligence to these issues, we show a set of data below to indicate how "representative" the data which we present actually is. The data is from a 5 cm x 5 cm section of sample. The top figure is I_{sc} in mA/cm^2 and the bottom is V_{oc} in mV. The location of the data is according to device location on the sample.

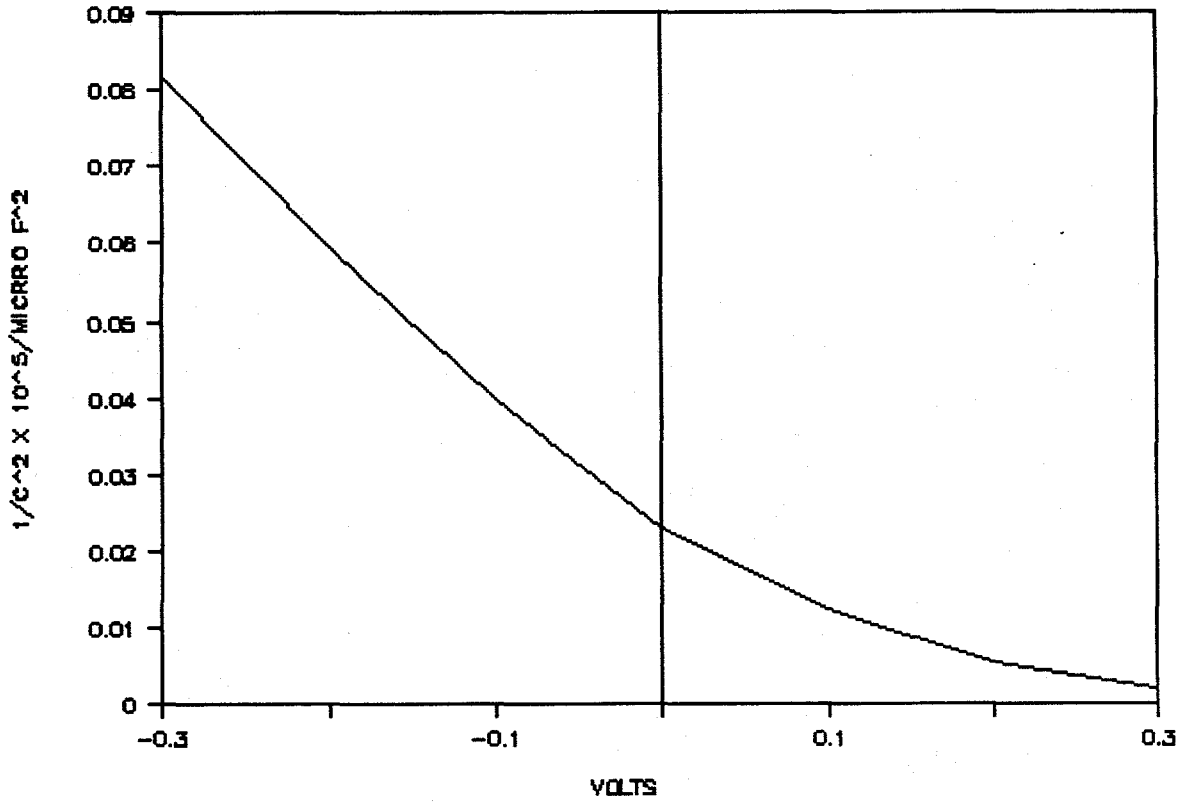


Figure 4

17 180	21 180	19 170
16 175	25 185	24 190
19 190	29 200	28 200
25 215	33 220	30 215
22 180		

Figure 5

As can be seen, the data indicating the best bulk properties(sic, high I_{sc}) is clustered in the lower right hand corner. The nonuniformity is due either to variation in bulk properties or to the junction formation process. It should be noted that low I_{sc}'s are accompanied by low V_{oc}'s. This and other data suggests that the nonuniformity is due to junction formation rather than bulk properties. We have been able to ascertain this in some cases by depositing a second set of ZnO dot junctions between the first set and observe good performance in areas which the first set indicated as poor. Device processing is thus the weakness in performance at this time and will be discussed in the next section. We are confident that we are able to attain good bulk properties in a reproducible manner with current processing. Improved device performance now depends upon controlling surface properties within the constraints that define good bulk performance.

SECTION II

DEVICE PERFORMANCE AND ANALYSIS

2.1 Device Fabrication

2.1.1 ZnO

The fabrication procedure for ZnO devices is discussed above. The process is designed to be "neutral" in terms of not introducing new defects to the interface. To first order this appears to be true. However, there are certain aspects of the process which require attention. For example, it is known that high energy charged and neutral species are present during ZnO sputtering[11]. These species are thought to be more troublesome during transients in the sputtering plasma, and we have observed some correlations with poor device performance and periods of plasma instability. To ameliorate the problem we place the substrate at some distance from the reactive zone and endeavor to maintain plasma stability. We suspect that some of the nonuniformities discussed above may be attributable to this phenomenon and are trying to understand the relationships.

Of greater concern is the effect of substrate temperature during ZnO deposition. Since high quality sputtered ZnO requires a substrate temperature of about 300°, we attempt to form our junctions at that temperature. With the substrate temperature at 300° the procedure is to deposit 200 Å from an undoped ZnO target and then 5000 Å from a doped target. As will be discussed below, this results in inoperative devices. Thus our baseline procedure is to let the substrate temperature fall from 300° down to about 80° during deposition of the doped layer. While this results in working devices, the resulting ZnO is "mushy" and must be handled carefully. Nevertheless the ZnO films have an average resistivity of about 1×10^{-3} ohm-cm with a transmission of about 90% at 1200 nm. While these properties are not thought to be limiting proper evaluation of our CIS films in diagnostic devices, we are concerned about the sensitivity to substrate temperature and the implications regarding the interface.

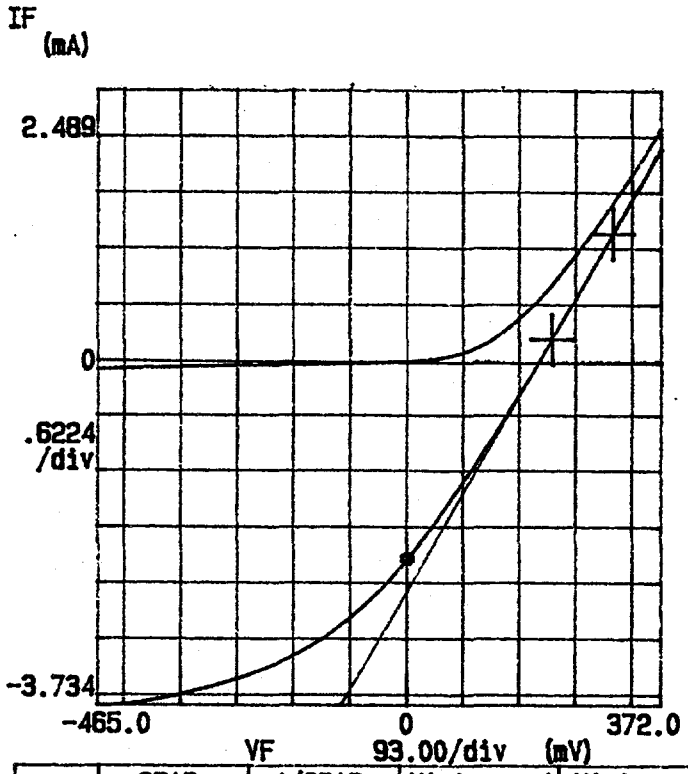
2.1.2 CdS

Because of the known better performance of CdS heterojunctions we also fabricate CdS/ZnO heterojunctions with our better films on a regular basis. Since, as will be discussed below, we have a particular difficulty with our surface, we find solution deposition of CdS a useful tool. That is, by adjusting the chemistry of the solution one is able to not only deposit a CdS layer, but also selectively etch and/or modify the CIS surface. Fabrication of devices with both our neutral ZnO technique and the invasive CdS technique is particularly helpful in deconvoluting surface and bulk phenomena and in identifying the origins of adverse surface properties. Thus our CdS process is a variable that we are experimenting with and does not have a fixed formulation. It involves use of both the chlorides and acetates of Cd, variations of pH's and temperature, as well as of the pH of the controlling species.

2.1.3 Device Performance

2.1.3.1 Series Resistance Limitations

Device performance is measured under a 1 sun ELH lamp which is monitored by a silicon reference cell calibrated by NREL. Dark and light I-V curves for a typical device are shown in figure 6 below. This device has a J_{sc} of about 30



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	11.7E-03	85.2E+00	219E-03	-2.57E-03
LINE2				

Figure 6

mA/cm^2 and a V_{oc} of 219 mV. The most notable feature about the I-V curve is that it is dominated by series resistance(R_s). The resulting device efficiency is thus about 2%. J_{sc} is decent, and a loss of x 2+ in V_{oc} for a ZnO heterojunction vs. CdS is also to be expected. With a reasonable ff the device would be a 10% equivalent(sic, allowing for the lower V_{oc} relative to CdS). The main issue of concern then is to learn the origin of the high R_s and eliminate it. The slope of the line through the hatchmarks is used to determine the size of R_s. The value in this case translates to 8.5 ohm-cm^2. This is large enough to not only dominate the ff, but also to reduce J_{sc}. As can be seen, under reverse bias the continuing rise in current can be attributed to this loss as well as to what appears to be collection from the periphery of the dot contact.

We have conducted a number of experiments to try to determine the origin of high R_s in these devices. Although we have not unequivocally eliminated bulk CIS properties, no evidence pointing in that direction has emerged, and thus we have focussed our efforts on the two interfaces. Our first concern was the undoped ZnO layer. To determine its contribution to R_s we varied its thickness between 0 and 250 Å and measured device performance. As shown in figure 7,

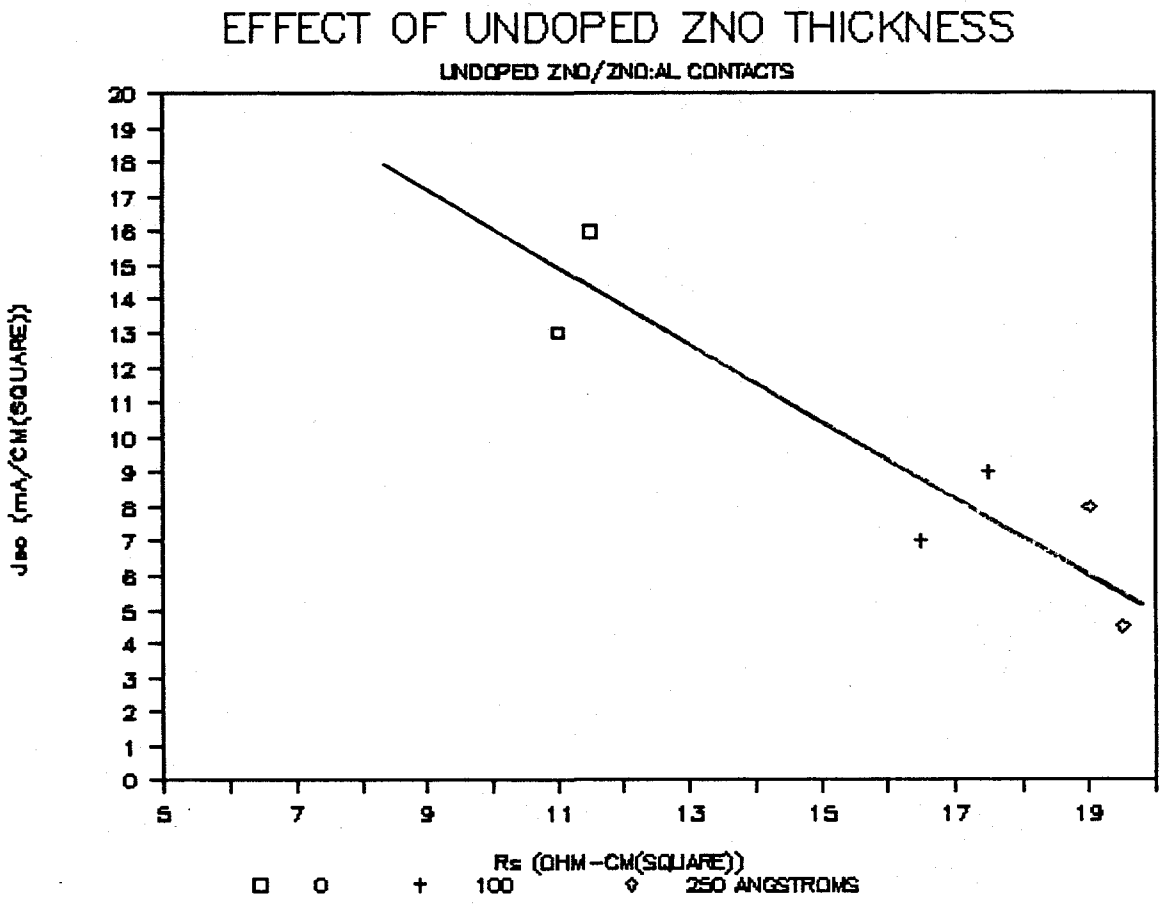


Figure 7

increasing the thickness of the layer resulted in a systematic increase in R_s and a concomitant decrease in J_{sc}. Unfortunately without the presence of an undoped layer shunting became a problem and the resulting lowering of V_{oc} offset increases in J_{sc}. Also, the R_s value of 11 ohm-cm^2 for 0 undoped ZnO layer thickness indicates the presence of an additional large contribution to R_s.

In the course of varying anneal profiles we have been able to accomplish significant reductions in R_s. To try to determine whether the R_s is associated with the front or rear interface we fabricated a series of CdS devices to compare with ZnO. The intent is to keep the rear contact constant while varying the front contact by ranging the heterojunction formation procedures. The procedure was as follows. Using a baseline CIS sample ZnO heterojunctions

were fabricated in the standard manner, i e, 200 Å undoped/5000 Å doped. Using the same CIS sample, CdS junctions were formed by solution casting. All CdS deposition parameters were kept constant except the dip time which was varied from 30 to 45 to 60 minutes. An equivalent 200 Å/5000 Å ZnO layer was then deposited on the CdS. The range of R_s values attained and their effect on J_{sc} is shown in figure 8. It should first be noted that the ZnO devices have R_s values significantly lower than the samples of figure 7 and

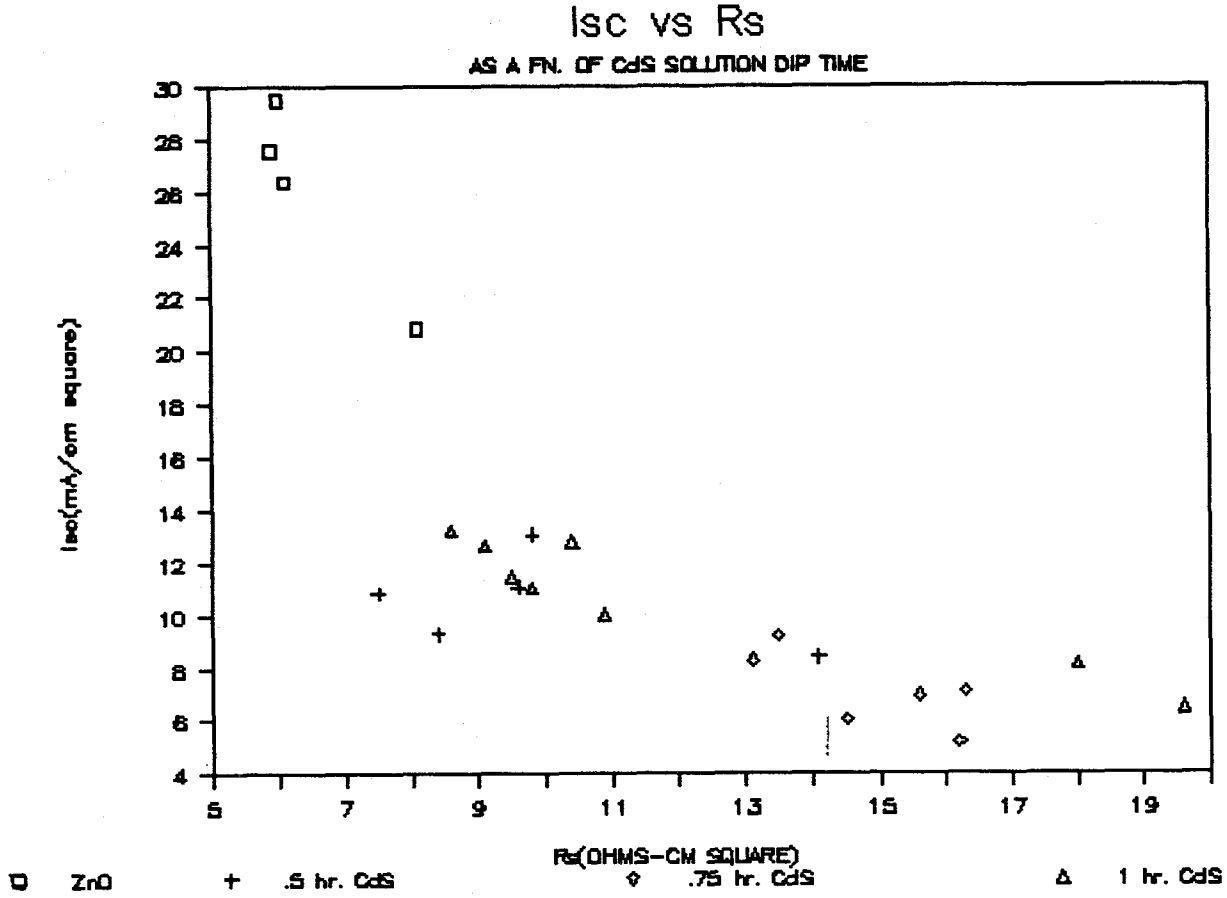


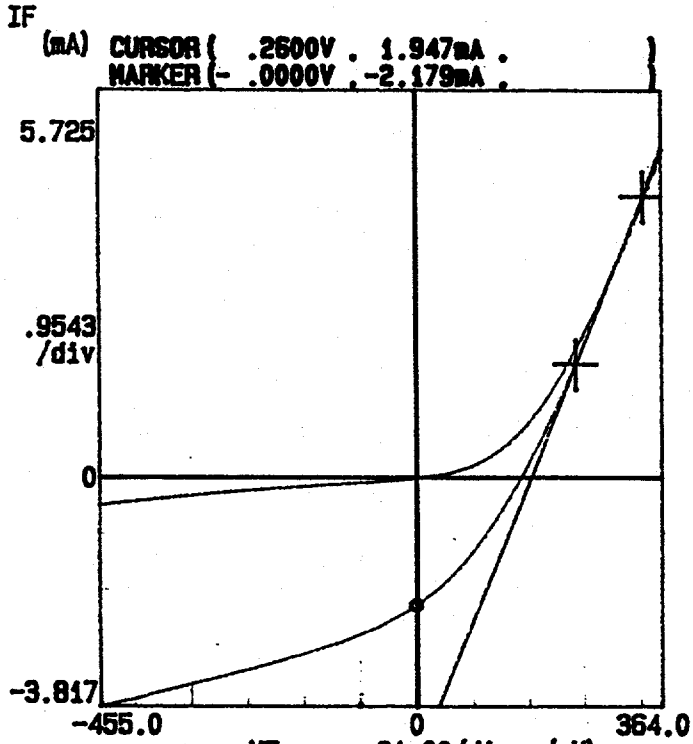
Figure 8

concomitantly higher J_{sc} values. The breadth of R_s values caused by CdS deposition suggests that the unknown R_s is associated with the front of the device. In particular, it might be associated with the contact between the undoped layer and the CdS. In comparing with figure 7 we note that in going from a 200 Å undoped layer to no doped layer resulted in a decrease in R_s of about 6 ohm-cm^2. This is about the value of the cluster of high J_{sc} ZnO points in figure 8. The cluster of CdS points around 9 ohm-cm^2 likely represents the additional 3 ohm-cm^2 contribution of the undoped ZnO/CdS interface. The spread in R_s beyond that value for the other CdS data represents additional contributions to R_s that can be realized due to local variations in the CdS deposition process. The bottom line is that the residual R_s for ZnO devices may be due only to the undoped layer. As we reduce the thickness of the

undoped layer, we must contend with the onset of shunting. For the CdS devices there is an additional contact resistance problem that must be examined more closely. Control of each of these phenomena is important to development of viable device options.

2.1.3.2 Open Circuit Voltage Limitations

As discussed above the initial series resistance problem which we encountered has been resolved to the point where it is now just limiting ff. By lowering the value of R_s to 3 - 4 ohm-cm^2 we are now seeing improved curved shape for our current devices as shown below in figure 9. As we further reduce R_s by



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	26.0E-03	38.4E+00	185E-03	-4.82E-03
LINE2				

Figure 9

decreasing the influence of the undoped ZnO layer we expect to see the curve square up to a proper fill factor. However, we must now turn our attention to V_{oc} generation. Our diagnostic devices with ZnO junctions routinely produce expected V_{oc}'s of order 200 mV. However, we have also found that CdS junctions produce the same voltage. Although at times we have achieved V_{oc}'s of 340 mV with CdS, in our highest J_{sc} generating devices we routinely observe the same 200 mV values for CdS that we do for ZnO. This of course suggests that the fermi level is pinned by surface states resulting in loss of control over junction formation.

An overview of the effect of CdS on device performance is provided by comparing the performance of several types of samples. Those in figure 2 are appropriate as they represent variation in processing and in structure. A summary of performance factors is given in Table III below.

TABLE III

SAMPLE	ZnO		CdS	
	V_{oc}	J_{sc}	V_{oc}	J_{sc}
A21	220	33	225	27
A40	90	12	200	31
A45	25	5	175	24

Added to this data is a common observation of complete destruction by CdS deposition of a device that works reasonably well with ZnO. The destructive mechanism is shunting and its occurrence and domination is indicative of high defect density. The CdS devices above are not dominated by shunting, but do exhibit sufficient shunting to reduce the ff. The data in Table III is more indicative of device behavior. We observe several types of behavior. Sample A21 is basically indifferent to the presence of CdS. Sample A45 is structurally similar to A21, but has undergone a lower temperature anneal. It only comes alive with a CdS junction. Sample A40 is structurally very different from the other samples, again due to a modification of the anneal profile, works poorly with ZnO, but approaches top performance with a CdS junction. The following comments summarize the data. 1. There is an upper limit of about 225 mV for these films. 2. A film with a "proper" surface reaches this limit with either CdS or ZnO. 3. Films with deviations from the "proper" surface can not achieve the limiting voltage with ZnO but can with CdS.

In the case of sample A40 it is also noteworthy that a longer CdS dip was required to achieve the values listed above. The progression is shown in Table IV below for a 30 minute and 45 minute dip time in the CdS solution.

TABLE IV

SAMPLE	ZnO		CdS 30 min.		CdS 45 min.	
	V_{oc}	J_{sc}	V_{oc}	J_{sc}	V_{oc}	J_{sc}
A40	90	12	130	17	200	31

The unusual surface features of A40 are thought to be responsible for this behavior. Samples with a "proper" surface typically only require a short dip and get worse with a longer dip due to onset of increased shunting. One might surmise then that the etching action of the solution is the dominant aspect

of its role for these devices. Etching can remove excessive defects leading to control by the predominant surface mechanism. This mechanism must be understood and controlled to realize higher V_{oc}'s.

2.2 DEVICE/PROCESSING MODEL

Each aspect of device performance has been discussed as an independent phenomenon for sake of clarity. However, there are interrelationships, and it is necessary to put all of the pieces together to formulate a model that is consistent with the collection of data. Although we have shown data to verify proper bulk stoichiometry for our films, we are certain that the surfaces are not stoichiometric and contain entities other than CIS. In processing films to achieve good bulk stoichiometry we use Cu/In < 1. The data in Table V suggests a possible reason for this. The small difference in

TABLE V

ELEMENT	ATOMIC SIZE	ELECTRONEGATIVITY
Cu	2.55 Å	1.8
In	3.14	1.6
Se	2.32	2.3

electronegativity between Cu and In suggests that reactivity is not an issue, while the much larger size of In suggests that movement of In and availability at a local site might be the rate limiting mechanism. Thus excess In must be used to assure availability at all bulk sites, however, the excess must also be properly disposed of. Most of the excess In is known to migrate to the surface[12] where it can form species such as In_xSe_y, some of which may be volatile. Thus the disposition of the In arriving at the surface is largely determined by the available Se at the surface. In the absence of Se In can evaporate, though it has a low vapor pressure.

The residual In species at the surface is likely to be n-type in character and thus capable of forming a p,n junction with the bulk. If that species were just In rich chalcopyrite CIS, with a fermi level near the conduction band, a good homojunction would result. The more likely species to form can form an effective junction, though less ideal than a properly formed heterojunction. We feel that our current devices are in this latter category. In the process of using excess In to form a good bulk, and in relaxing control over the availability of Se during surface formation we have allowed the formation of In_xSe_y or perhaps $Cu_xIn_ySe_z$ species which are dominating the surface and not allowing heterojunction materials to contact the bulk. Hence good samples such as A21 are indifferent to whether CdS or ZnO forms the contact. The junction is already formed between the surface and the bulk, and the CdS or ZnO are just acting as TC window layers.

We have recently embarked on a series of experiments to try to determine the nature and cause of these surface species. Others typically use various post deposition anneal procedures to activate their samples and have been able in

some cases to explain the mechanisms. We have tried annealing our devices in oxygen after ZnO deposition and between CdS deposition and ZnO deposition and have observed no effect. We tentatively assign this procedure to fixing Se vacancies and conclude thereby that such vacancies are not the problem. We have also varied deposition parameters to further define the domain of activity of the surface species. In varying the Cu and In film thickness we find a peak ratio which results in slightly In rich stoichiometry in the completed films. Performance drops to 0 for variations of a few percent in either direction for this ratio. We observe similar behavior with Se availability during growth. Though we always observe stoichiometric Se content in the completed film, by limiting Se availability during the later stages of growth we are able to manipulate the Se content of the surface and hence the formation of surface state species. In fact, by using an excess of Se we have been able to effect the formation of reverse junctions. This is consistent with our model which would indicate that the surface should become Cu rich as the excess In is removed by the formation of volatile In_xSe_y species. The p+ Cu rich surface on a p-type bulk then results in an inverse junction as measured experimentally. This result implies that we have been able to move the surface fermi level from its normal above mid gap location through mid gap and to a p+ location. The implication is that somewhere between these two extremes is a surface neutral state which will relinquish control of junction formation to the heterojunction contact. We are presently conducting the experiments to pursue this opportunity.

In addition to trying to learn more about the chemistry of formation of surface states and their relationship to processing, we are also trying to improve our understanding of the band structure of the devices. We have previously reported the formation of near intrinsic CIS[13] and incorporate that methodology into the design and fabrication of devices. Our targeted device structure is a p+ base with a near intrinsic(p-) space charge region on top which is contacted by an ideal n-type contact. The p+/p- layers are supposed to form as a natural consequence of depositing the Cu layer on the bottom of the Cu/In/Se stack and by judicious design of the anneal profile. We are using C-V, measurements in TFT structures and other techniques to develop the data needed to build this understanding. The preliminary data which we have thus far suggests that in the space charge region $E_i - E_f \approx .37$ eV and that the effective surface contact is just above mid gap. One may interpret this to mean that the defective surface is not only pinning the fermi level, but is also resulting in increased defect density just below the surface. The latter, however, does not seem to be as significant a problem because of the high J_{sc} values that are being achieved.

Additional insights to these phenomena are being provided by TFT measurements. With TFT structures we are able to probe within 200 Å of the surface which is useful in helping to study and understand the problematical surface states. We have recently measured electron mobilities of up to 60 $cm^2/V\text{-}s$ from transistor characteristics. Because the surface is usually defective relative to the bulk these transport properties are thought to represent a lower limit. This is thus a respectable value for what is characterized as a defective region and is consistent with the high J_{sc} values being realized. Combining these terms results in an estimate for the carrier lifetime of $\tau \approx .5$ ns. This is likely the parameter that is being affected

most by the defects. To further this understanding and help guide its evolution we have initiated a plan to start modeling our data with the Penn State AMPS program developed by Professor Fonash. We will also begin a similar collaboration with Professor Schwartz at Purdue.

SECTION III

CONTACTS AND WINDOW LAYERS - ZnO

3.1 BACKGROUND

ZnO has become increasingly important to photovoltaics as a transparent conductor(TC) because of its excellent electro-optical properties and its greater stability in a reducing environment relative to tin oxide. ZnO can be deposited by several techniques including CVD, sputtering, solution casting, etc. For low band gap PV devices which generate high current densities it is necessary to have TC film thicknesses of a couple of microns or more, therefore high deposition rate for the TC is necessary. Since sputtering is a successful commercial process for many applications, it is desirable to determine its capabilities for deposition of ZnO. While conventional sputtering from a ZnO target produces films of high quality, sputtering rates are typically too low for commercial applications. An alternative approach is to use a Zn target and reactively sputter in an oxygen environment. Sputtering of metals is known to be much faster than from ceramic targets. There have been reports of deposition rates of 30 Å/s for reactive magnetron sputtering of ZnO, but concomitant electronic properties with doping were not verified[14]. More recent results report attainment of good electronic properties by reactive sputtering, but at low deposition rates of order 1 μm/hour[15]. We are unaware of the achievement of good electronic properties for ZnO sputtered at high rates, e g, 10 Å/s and higher.

To address this opportunity we have begun exploration of sputtering techniques which might lead to deposition of high quality ZnO at high rates. Our primary approach is reactive magnetron sputtering from a Zn target. We have also tried to evaluate F as a dopant because of its successful use with CVD deposition[16]. Because of the added chemical complexity that F brings to an already reactive environment we have also tried F as a dopant with a ZnO target to help separate its effect on growth chemistry from its role as a dopant.

In addition to interest in developing other options for deposition of ZnO we are also interested in developing effective heterojunction contacts with ZnO, i e, without CdS. It is our contention that if band mismatch is not an issue, competitive ZnO/CIS devices should be possible.

3.2 PROCESSING RESULTS AND DISCUSSION

Reactive sputtering of Zn in Oxygen produces an environment of complex kinetics and thermodynamics. In addition to the high reactivity of excited oxygen, there are also complex ion bombardment effects to contend with. Consequently the deposition rate and film properties are a function of location relative to the target. We are using a 3 inch target and placing a 10 cm x 10 cm glass substrate about 15 cm above the target, but offset from its center to evaluate the properties as function of position.

Similar phenomena occur with conventional sputtering from a ZnO:Al target. We see a systematic decrease in thickness from the target center as expected,

but, as seen in figure 10 below which is a profile of resistivity values over the 10 cm x 10 cm area, film properties go through a peak just past the perimeter of the target. Our hypothesis is that ion

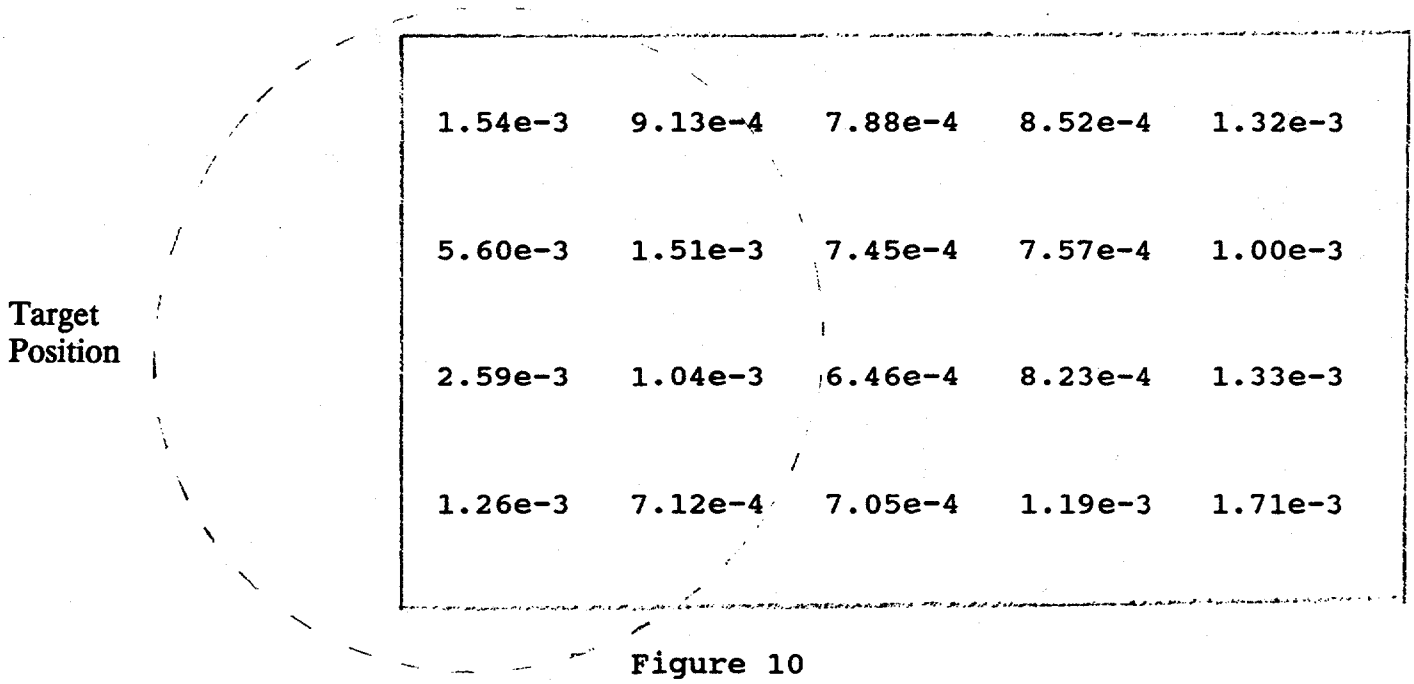


Figure 10

bombardment is affecting both the quality of the ZnO as well as the doping incorporation efficiency. Some bombardment is necessary; excessive bombardment results in deteriorating film properties. It has been reported that increasing the substrate temperature above 300° improves the uniformity of the film, especially over the racetrack area[17]. The data above is for a 300° substrate temperature. Below in figure 11 we show data for 350°. Although we

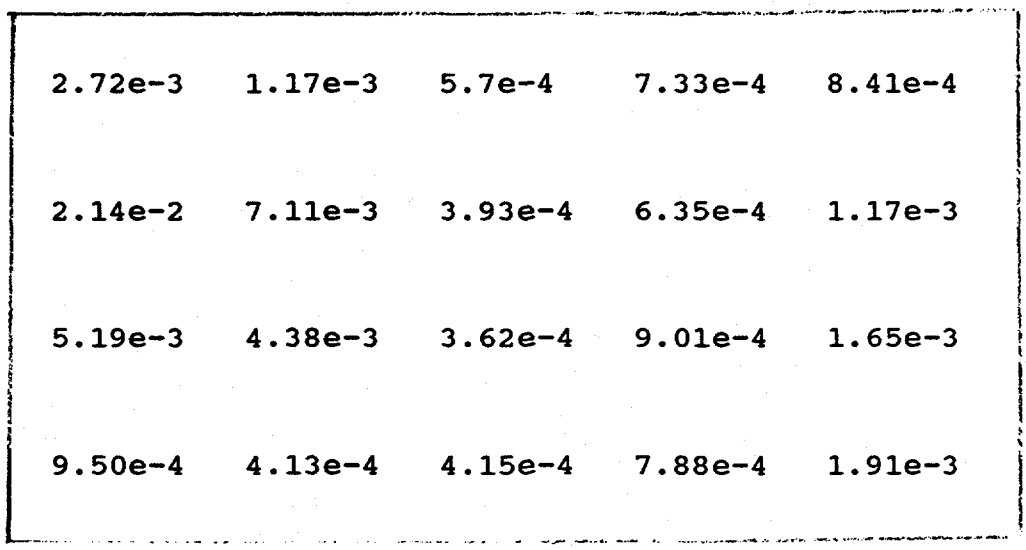


Figure 11

note an overall reduction in resistivity down to values as low as 3 - 4 x 10^{-4} ohm-cm, there is no apparent improvement in uniformity in the racetrack area(columns 1 and 2).

Our baseline reactively sputtered ZnO films are produced in a near-oxygen-deficient regime containing about 1 millitorr of Ar to help sustain the plasma. It is necessary to carefully control the oxygen supply to maintain low pressure and not enter an oxygen starved regime which results in deposition of Zn. Doping with Al is accomplished by placing an Al source on the Zn target. For a moderate deposition rate of 1.5 Å/s we attain resistivities of 9 x 10^{-4} ohm-cm. The transmission spectrum for a 3000 Å film is shown in figure 12. It exhibits good transmission out to 1500 nm and just a small onset of free carrier losses.

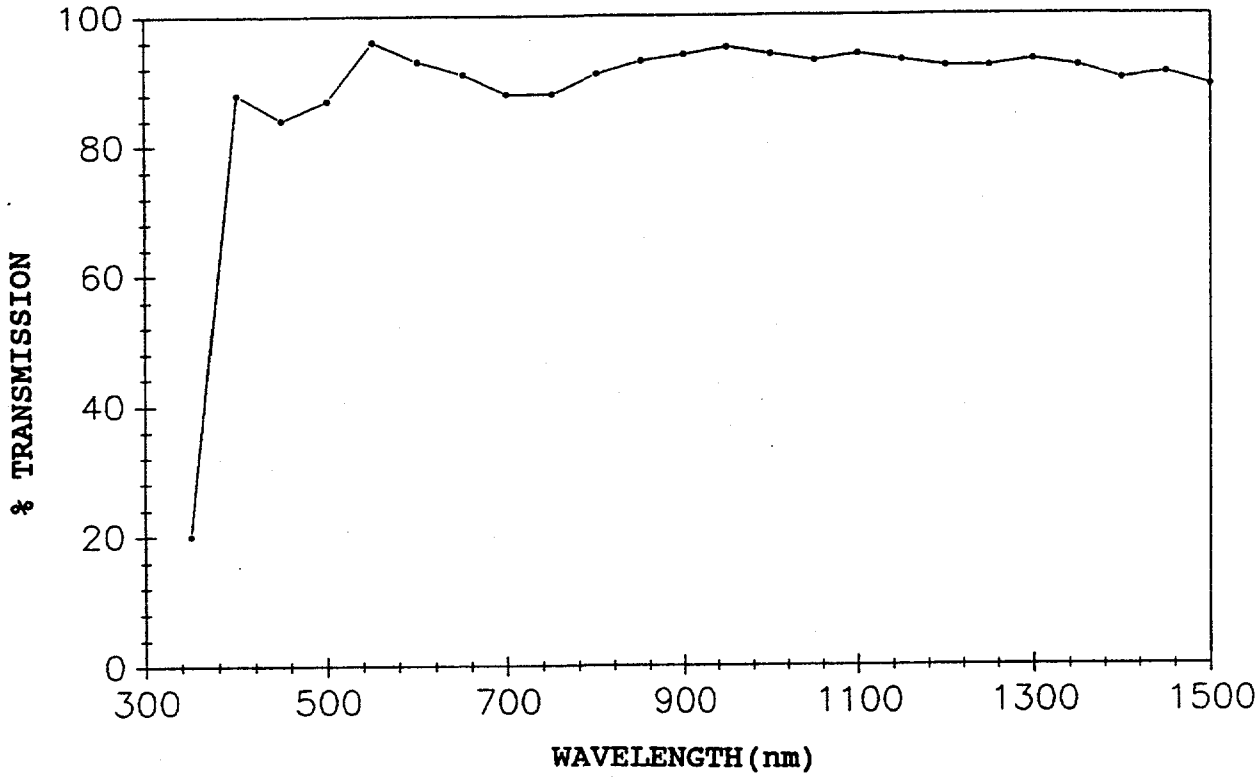


Figure 12

Because of the successful use of F in CVD deposited films[16] we have also tried it as a dopant. We use CF_4 as our F source, and in an attempt to limit its chemical role we used a ZnO target for the first set of experiments. We were able to achieve resistivities of order 10^{-3} ohm-cm and representative optical properties. For these experiments we used relatively small levels of CF_4 in an attempt to dope only and yet observed large perturbations in film growth indicating that F was slowing the growth process. We speculate that F extracts Zn from the growing film to form ZnF_2. It thus plays the role of an etchant as well as a dopant.

We also tried using CF_4 as a dopant in reactive sputtering. Not surprisingly we found a rather large perturbation in film growth here as well. A delicate balance in deposition conditions is required to push F into the role of dopant rather than etchant. Nevertheless we were able to achieve film properties comparable to our Al doped reactively sputtered films. Resistivities down to 8.9×10^{-4} ohm-cm were achieved. The transmission spectrum for this film(thickness = 1600 Å) is shown in figure 13. In spite

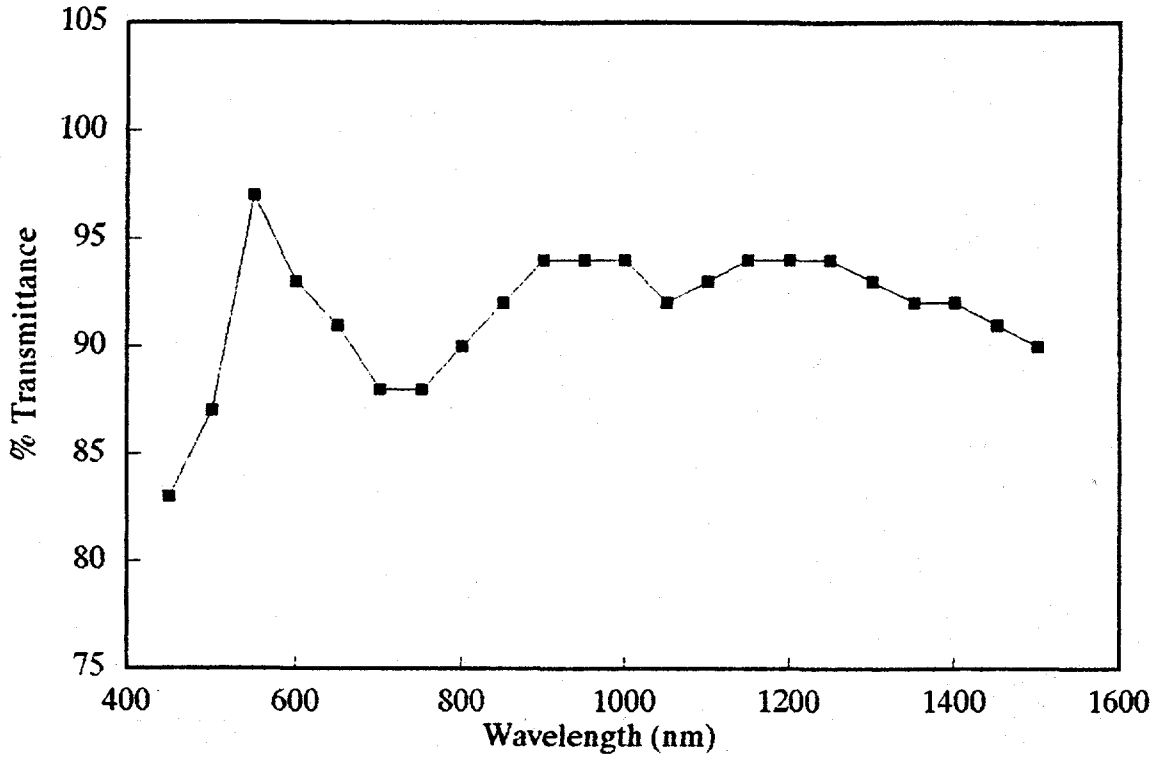


Figure 13

of the structure it is apparent that the transmission is good out to 1500 nm, showing little evidence of free carrier effects, although the films are too thin to justify conclusions along these lines. However, figure 14 shows transmission spectra for somewhat thicker films grown under similar conditions to the devices of figure 13. In addition to the usual patterns in conductivity shown in figures 10 and 11, as the films grow thicker we observe patterns in the optical properties as well. The locations closet to and farthest from the target are hazy while the center is specular. The upper curve in figure 14 is for the specular film and the lower for the hazy film. The haze affects the overall transmission of the hazy area of the film, while what must be some residual haze in the specular film affects the blue roll off. Also, the conductivity is somewhat lower for these thicker films, $\approx 2 \times$

10^{-3} ohm-cm. Nevertheless, the optical properties show minimal free carrier effects. We speculate that the etching action of the F removes defects and produces highly ordered films with high mobility. We are just now initiating measurement efforts to verify these contentions. We also note that the reactivity of F may be effecting the generation of other doping species from the vacuum chamber that may be incorporated in the films along with F. This is presenting difficulties in characterizing the role of F as a dopant, but its role as a growth modifier seems clear.

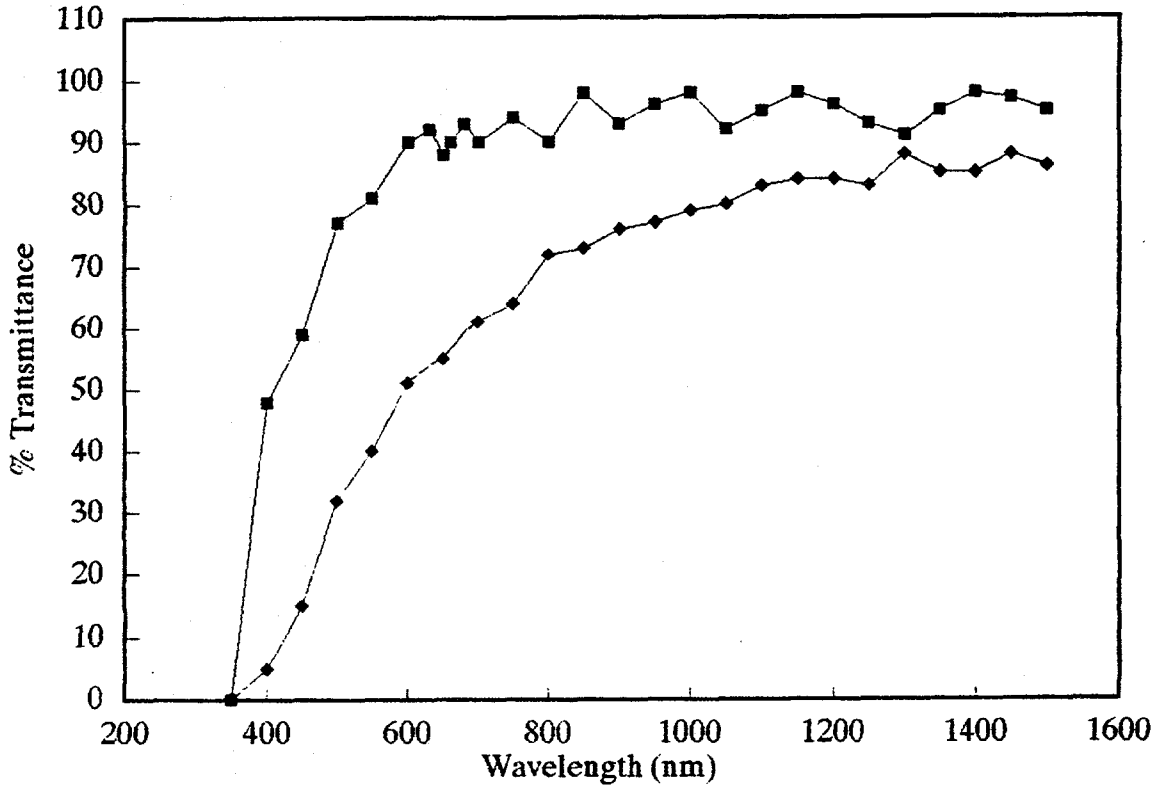


Figure 14

The results presented above were for low deposition rates of 1.5 Å/s, but at an equally low power of only 64 W for the ractively sputtered Al doped films. The dependence of growth rate on power is shown in figure 15. As can be seen there is a linear dependence of growth rate on power up to a value of 9 Å/s for a power level of 200 W, the power supply limit. Preliminary measurements indicate minimal loss in properties as the rate is increased. We will extend these measurements further to determine the practical limits.

3.3 HETEROJUNCTION FORMATION

Assuming that the deposition rate and performance objectives discussed above

can be met by use of reactive sputtering, we must also establish compatibility with device fabrication. Thus far this has not been a problem since our ZnO/CIS devices work as well as ZnO/CdS/CIS devices. However, the ZnO has been deposited from a ZnO target, and, as discussed above, our working model is that the ZnO is just acting as a TC window and not as the junction forming agent as well. We have not yet attempted to use reactively sputtered ZnO as our contact because we place elimination of surface domination by the hypothesized In_xSe_y at a higher level of priority, and use of a ZnO target makes working that problem more straightforward. In the event that the environment for reactive sputtering is too harsh for forming good

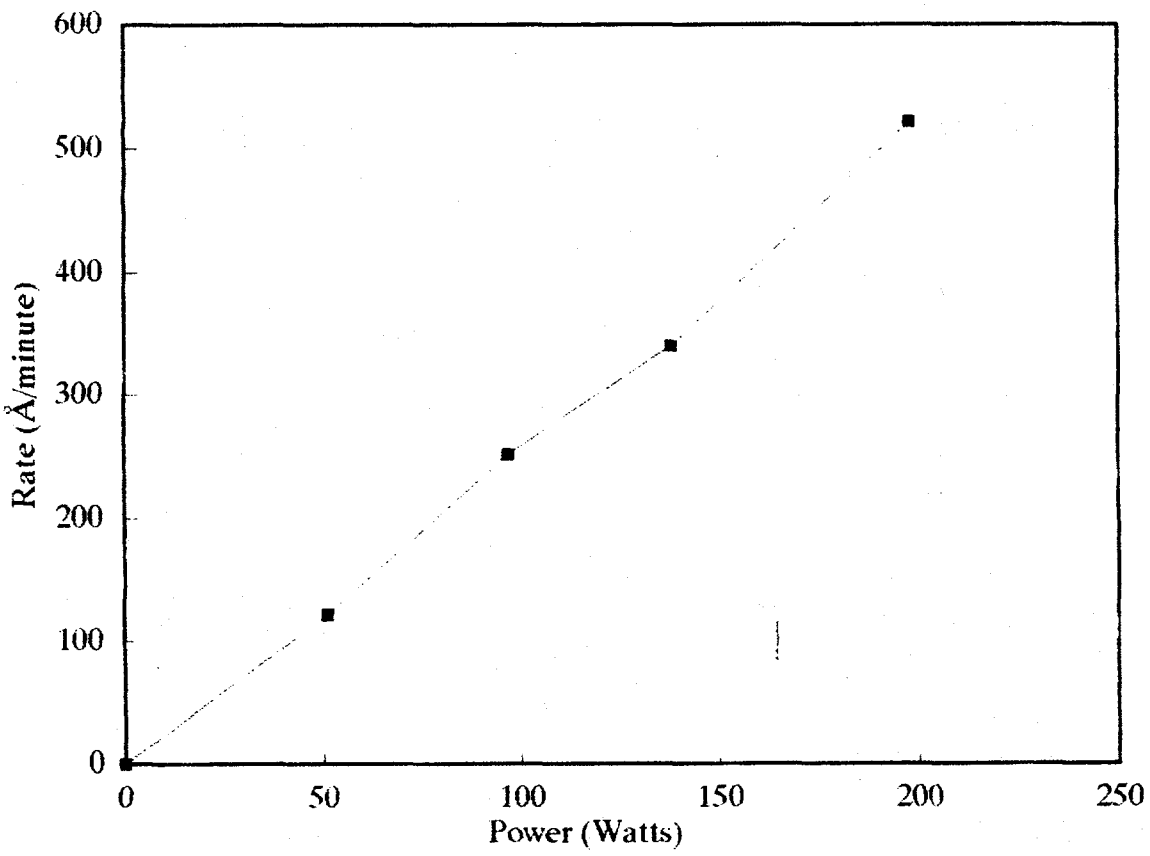


Figure 15

heterojunction contact, there are other options. For example, one could form the heterojunction contact by benign low deposition rate sputtering from a ZnO target of a 200 - 300 Å thick film and then deposit the remainder of the ZnO layer that plays the role of TC by high rate reactive sputtering.

To evaluate the various options for contact formation we have been working with ZnO targets and varying the deposition conditions. A key observation is that holding the CIS substrate at temperatures above 200° during deposition of the Al doped ZnO layer results in significant deterioration of device performance for ZnO/CIS junctions. This does not occur for ZnO/CdS/CIS

junctions. The ZnO layer in this case denotes a 250 Å undoped ZnO layer topped by a 5000 Å doped layer. The primary implication of this result is that something from the ZnO is diffusing into the CIS, and Al is the likely culprit. The secondary implication is that CdS slows down or perhaps eliminates the problem. While this may be satisfactory for CdS junctions, it is an issue that must be worked if we hope to succeed with ZnO junctions.

At this time we are basing the future development of our devices on the contention that they are presently dominated by a surface state caused by the presence of excess In at the surface. It is somewhat ironic that Al is also a Group III element and is perhaps assisting In in its role as surface spoiler. The favored dopant for CVD deposited ZnO, Boron, is also Group III with equal potential for complicity. Fluorine should behave differently. It is likely to diffuse less, and certainly does not practice Group III chemistry; hence our interest in pursuing F as a dopant. The film properties exhibited thus far look promising, what we must now do is establish compatibility by fabricating devices.

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16. Abstract (Limit: 200 words)

This report describes work to develop novel fabrication processes for $CuInSe_2$ (CIS) solar cells that will result in improved performance and cost effectiveness at the manufacturing level. The primary approach involves all solid-state processing for CIS. This was augmented by work to provide novel alternatives for the formation of the window layer/heterojunction contact. Inherent to the project was the need to develop a generic understanding of the relationship between processing and performance so that broad-based transfer to industry can be facilitated. We achieved good-electronic-quality CIS by the use of two selenization procedures for predeposited metal layers. We achieved good stoichiometry throughout the bulk of the film, attained grain sizes of up to 1 μm, and measured electron mobilities of up to 60 $cm^2/V\text{-}s$. However, there is a complex relationship between grain size, adhesion, and performance. Our primary approach to characterization was to fabricate ZnO/CIS test devices and measure as many properties as possible in device format. We are also developing reactive sputtering of ZnO as an alternative window layer technology.

17. Document Analysis
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