NREL/SR-520-24641 • UC Category: 1260

Light-Trapped, Interconnected, Silicon-Film™ Modules

Final Technical Status Report

R.B. Hall, J.A. Rand, D.H. Ford, and A.E. Ingram
AstroPower, Inc.
Newark, Delaware

NREL technical monitor: H.S. Ullal

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A national laboratory of
the U.S. Department of Energy
Managed by Midwest Research Institute
for the U.S. Department of Energy
under Contract No. DE-AC36-83CH10093

Prepared under Subcontract No. ZAF-5-14142-02
April 1998

NOTICE

Available to DOE and DOE contractors from:
Office of Scientific and Technical Information (OSTI)
P.O. Box 62
Oak Ridge, TN 37831
Prices available by calling (423) 576-8401

Available to the public from:
National Technical Information Service (NTIS)
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161
(703) 487-4650

Printed on paper containing at least 50% wastepaper, including 20% postconsumer waste

TABLE OF CONTENTS

TABLE OF FIGURES

TABLE OF TABLES

1 Introduction

1.1 Project overview

AstroPower is employing Silicon-Film™ technology toward the development of an advanced thin-silicon-based, photovoltaic module product. This module combines the design and process features of advanced thin-silicon solar cells, is light trapped, and integrated in a low-cost monolithic interconnected array. This advanced product includes the following features:

- silicon layer grown on a low-cost substrate,
- a nominally 50-micron thick silicon layer with minority carrier diffusion lengths exceeding 100 microns,
- light trapping due to back-surface reflection,
- back surface passivation.

The thin silicon layer achieves high solar cell performance and can lead to a module conversion efficiency as high as 19%. These performance design features, combined with low-cost manufacturing using relatively low-cost capital equipment, continuous processing and a low-cost substrate, will lead to high performance, low-cost photovoltaic panels.

The three year project involved five tasks and built on present processes and capabilities. Tasks I and II addressed increases in module efficiency by optimizing the sub-module and sub-element material properties and structure. Tasks III and IV examined the reduction in the cost of module integration by improving the module fabrication process and module efficiency. Task V improved the technical base supporting the manufacturability of the near-term product by developing prototype manufacturing processes. During the third year of the program, our efforts were focused on Tasks II, III, IV and V.

1.2 Technical Approach

Thin films of silicon grown on an insulating substrate allow for the fabrication of large-area, series-interconnected sub-modules (see Figure 1)[1]. The sub-module design incorporates a method of partitioning the thin-film photovoltaic layer into sub-elements and reconnecting them as a series connected array.

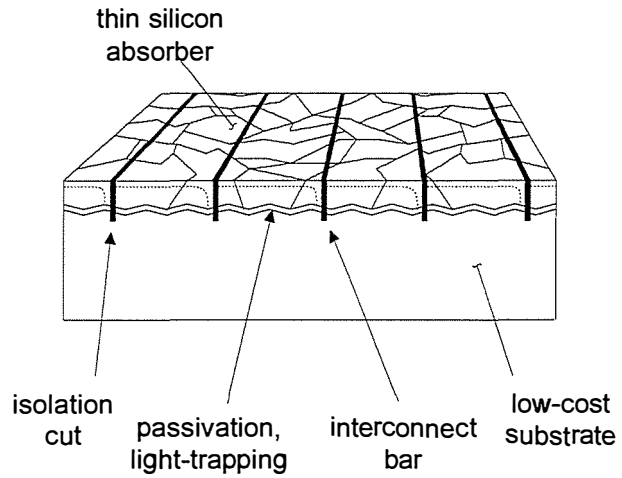

Figure 1. Solar cell sub-module device structure

The solar cell sub-element device design (Figure 2) consists of a thin (35–50 μm) polycrystalline silicon layer which is grown on a low-cost substrate material. The thin layer/low-cost substrate approach results in lower cost by minimizing the use of relatively expensive silicon feedstock material. Diffusion lengths equivalent to twice the device thickness are required to assure high carrier collection throughout the bulk of the base layer. Thin silicon enables the use of imperfect materials and increased doping levels. The addition of light-trapping and back-surface passivation in comparison to thick silicon solar cells leads to improved solar cell voltage and fill factor.

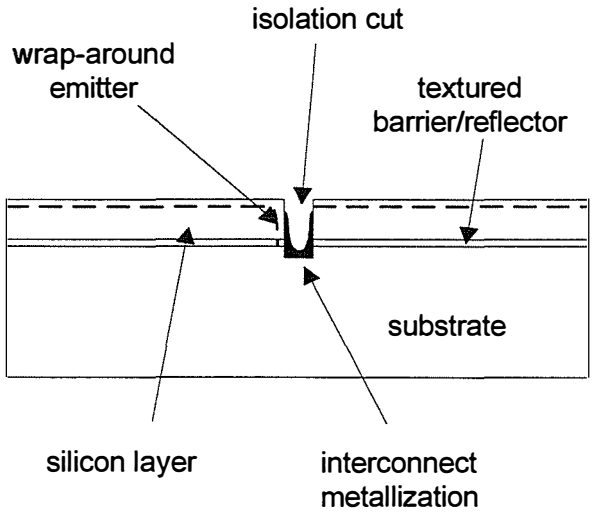

Figure 2. Sub-element device structure

The solar cell device structure incorporates light trapping and back-surface passivation to improve energy conversion efficiency. Light trapping is achieved by using a diffuse reflector and/or a random texture at the back surface of the thin film, resulting in enhanced optical absorption of weakly absorbed light and improved current generation. Electrical passivation of the back surface is achieved by developing the barrier layer to minimize surface recombination velocity at the barrier/silicon interface. Back-surface passivation results in improved voltage and fill factor by minimizing the reverse saturation current.

Research and development efforts of the third year of the program focused on the continual improvement of Tasks II and III of the work plan, and development of Task IV, intended to reduce the cost of module integration by improving the module fabrication process and module efficiency. Task V is intended to improve the technical base supporting the manufacturability of the near-term product by developing prototype manufacturing processes.

1.3 Key Results

The first year of the program was marked by a systematic investigation into processing options for the thin film material. Figure 3 shows the progress in solar cell efficiency during the course of procss development effort. Key process changes are shown at each point. The program began with an efficiency of 6%, and ended the first phase with 13.8%.

The second phase focused on improving the uniformity of the grain morphology and thickness over large areas (greater than 500 cm^2). In the area of device design, a new technology was developed to improve light trapping in the thin silicon solar cells. During the second phase, sub-module design issues were addressed. This included detailed investigations into resistive losses, as well as experimentation regarding different metallization approaches.

In the final year a significant reduction of active layer thickness was accomplished. An NREL verified conversion efficiency of 12.5% on a sub-element fabricated on an insulated substrate with an active layer less than 100μm was achieved. See Figure 4.

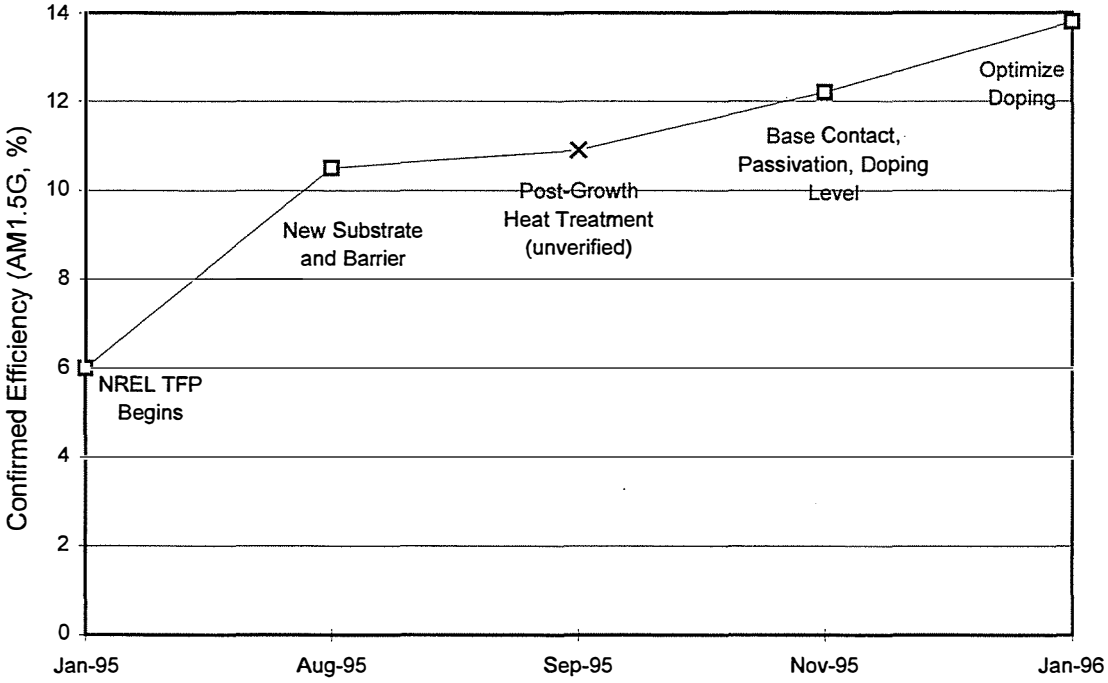

Figure 3. *Progress of best efficiency solar cells during the first year and the key process developments responsible for efficiency improvement (verified at NREL unless noted).*

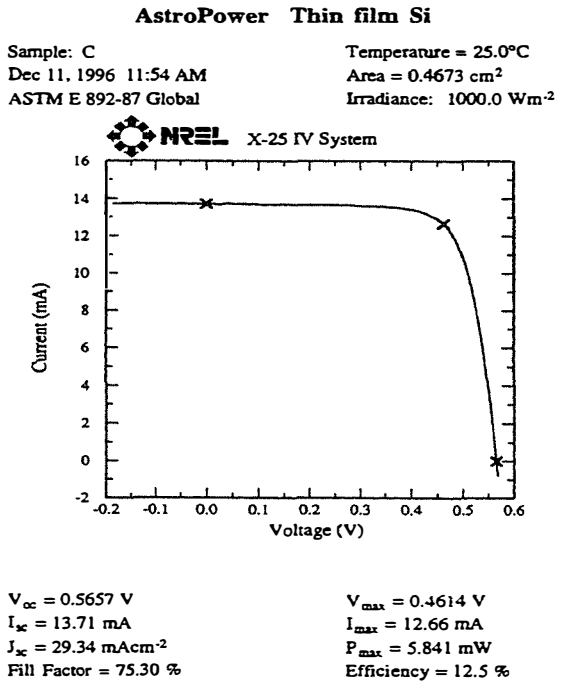

Figure 4. *Current-Voltage characteristic of a thin solar cell sub-element fabricated on an insulated substrate.*

Figure 5 shows a photomicrograph of a cross section of a sub-element on an insulated substrate.

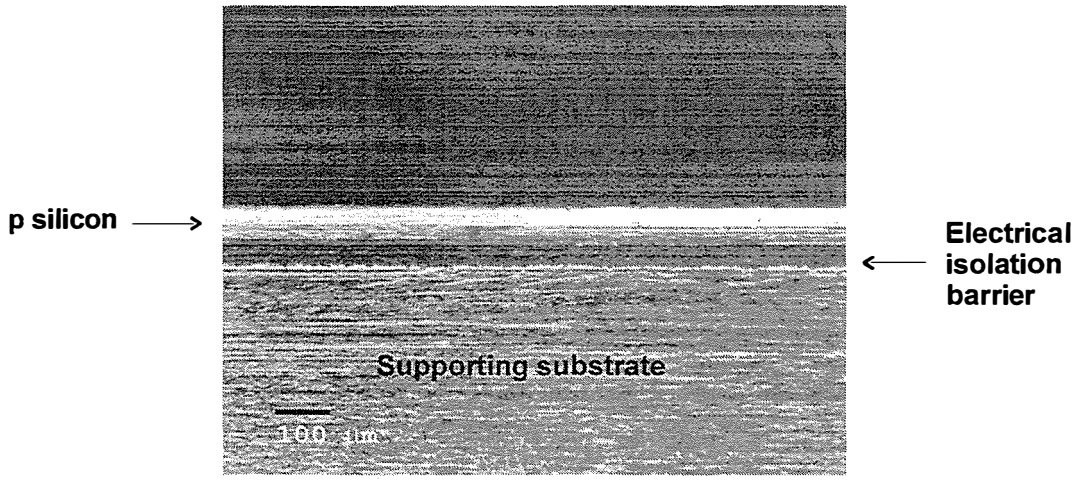

Figure 5. Cross section of thin silicon and electrical isolation barrier on a supporting substrate.

Included in the third year results is also a modified metalization technology for a monolithically interconnected device structure (Figure 6). This modified metalization provided a more fault-tolerant fabrication sequence. Further description is provided later in this report.

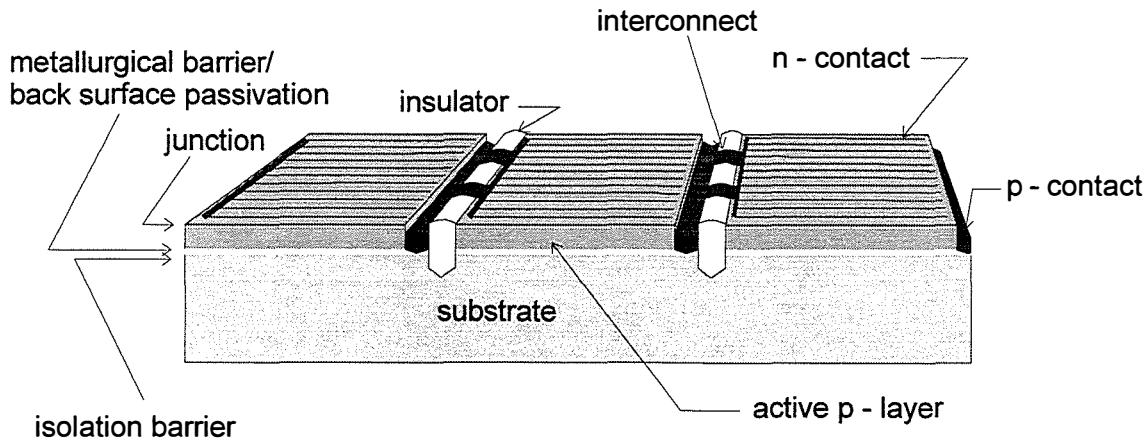

Figure 6. Modified metallization/interconnect.

The modified metalization/interconnect technology was employed on a 36 segment 321 cm^2. Figure 20 shows the current-voltage characteristic of a 36 segment monolithic interconnect device as measured by NREL.

Continual improvements in the monolithic interconnect technology to reduce shunting and shading losses associated with the modified metalization technology have resulted in the present device design (Single Back Contact) and interconnect technology (see Figure 7). This design is described in more detail in Section 2.3 Advanced Device Design.

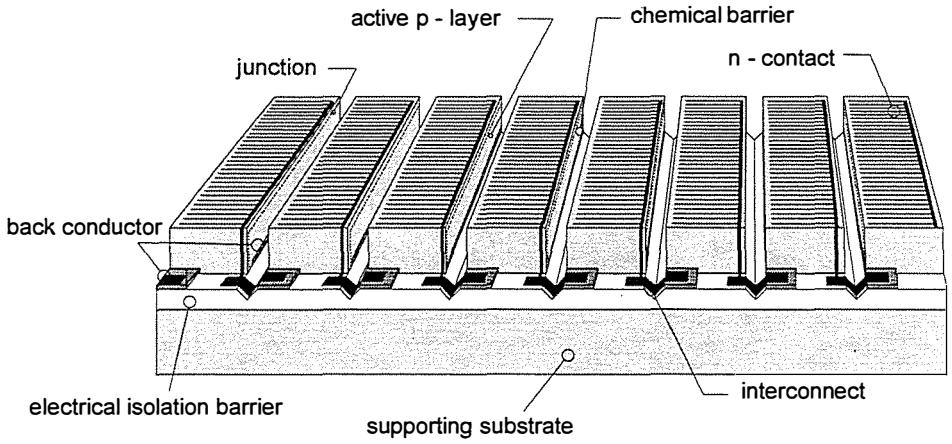

Figure 7. Advanced monolithic interconnect design (Single Back Contact)

2 Sub-module Development

Significant progress was made in the area of film growth during the first two years of this program. During this effort, thin (nominally 100μm thick) active layers were grown on barrier-coated substrates [2]. The average diffusion length of devices processed with phosphorous gettering exceeded 100μm. Devices with thicker (greater than 100μm) active layers exhibited diffusion lengths in excess of 250μm.

Near the end of the second year and into the third year an alternative method of forming a thin layer of silicon on a low cost substrate was evaluated as a method of defining a relationship between thickness and diffusion length [3]. This new test structure has provided critical data to refine sub-module development toward an interconnect technology with back surface passivation.

In this approach, the substrate would be added to the thin (nominally 100μm), free standing film immediately following the growth process. Significant advantages of this method include access to the back surface after the film growth, which allows for the investigation of back surface passivation, back surface reflectors and back surface conductors suitable for sub-modules and subsequent monolithically interconnected device structures. Figure 8 shows a schematic of a sub-module configuration with this test structure approach.

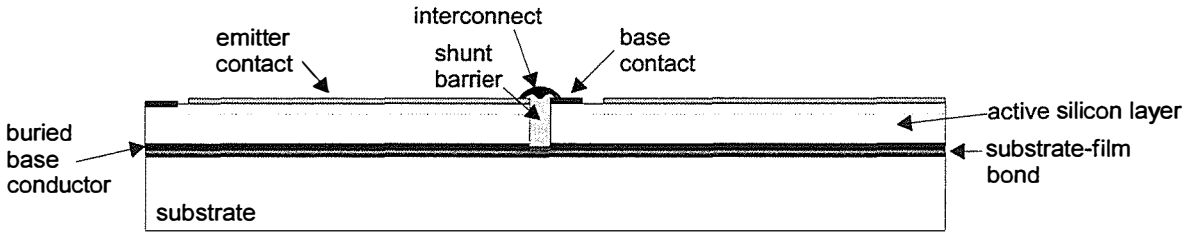

Figure 8. Schematic view of monolithic sub-module

2.1 Sub-Module Design Issues

Most of the design issues for the integrated sub-module relate to the conductor grid structure. There are three possible configurations: all grids on the top surface, emitter grids on the top surface/buried base grids, and all buried grids. We evaluated, constructed and tested the first two sub-module configurations. The key issues are discussed in the following paragraphs.

All Grids on the Top Surface

Figure 9 shows the layout of one sub-cell of this configuration. The emitter and base contacts/conductors conduct current laterally across the sub-element to the interconnect metallization located over the isolation cut. The different type conductors are staggered from one sub-element to the next to allow easy interconnection of the base of one sub-element to the emitter of the adjacent sub-element (to the right side in Figure 9).

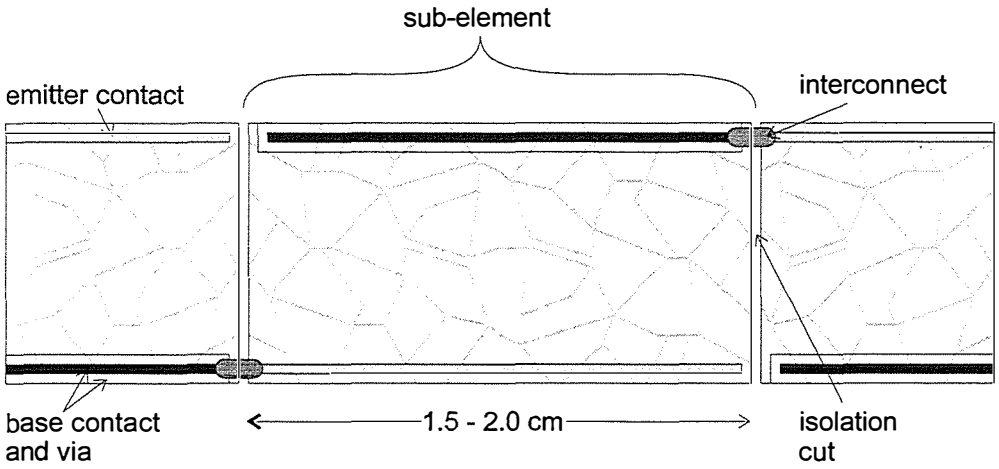

Figure 9. Plan view of sub-module grid structure when all grids are located on the top surface.

The advantage of this configuration is that the base conductors can be applied after the thin film of silicon has been grown on the substrate, and existing, well-developed metal contact metallization techniques (namely aluminum evaporation or aluminum-glass screen print paste) can be used. The major disadvantage is that, when on the top surface, the base conductor contributes to the overall shading loss of the grid structure. This problem is exacerbated by the need to form a via through the emitter to allow the base conductor to contact the base layer without shunting to the emitter. (The base contact and via arrangement are shown in Figure 9). This increases the effective shading of the base conductor and can result in a total shading loss that is greater then twice that of a standard silicon solar cell contact structure. Therefore, optimization of the grid design is required for minimal losses.

A model was developed to predict the parasitic series resistance and shading losses. Series resistance losses arise from lateral conduction in the emitter and base, grid conductors and interconnect metallization, and contact resistance effects between the grid conductor and the silicon layers. Figure 10 defines the relevant geometric quantities used in the model.

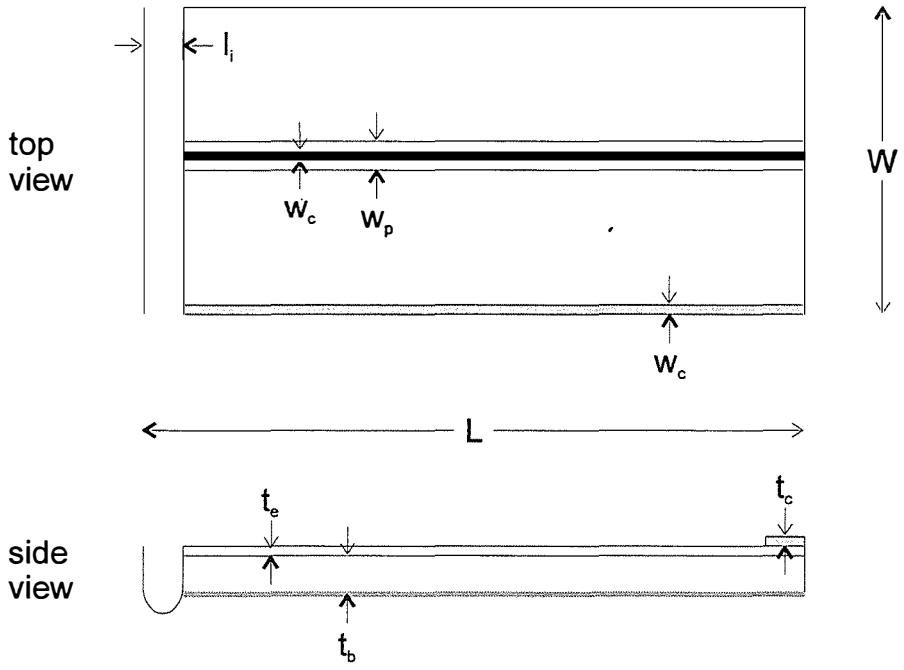

Figure 10. Geometric details of the sub-module used for modeling parasitic series resistance and shading losses.

Using conservative design rules (see Table 2) for conductor width, thickness, conductivity, etc. leads to relatively high predicted total power loss of 18–20%. Table 1 summarizes the contribution of various loss mechanisms for the design rules listed in Table 2.

Table 1. Contribution of various loss mechanisms to the total predicted power loss of the all-grids-on-top configuration.

Loss Mechanism	% Loss (of Total Available Power)
Emitter Series Resistance	1.88
Base Series Resistance	0.45
Emitter Grid Series Resistance	0.44
Base Grid Series Resistance	0.47
Total Grid Contact Resistance	4.85
Interconnect Metal Resistance	0.30
Interconnect Metal Shading	0.52
Kerf-related shading	0.80
Emitter Grid Shading	3.70
Base Grid and Via Shading	6.89
Total Losses	20.46

Table 2. Fabrication parameters used in the summary presented in Table 1.

Fabrication Parameter	Symbol	Value
Emitter Sheet Resistivity (ohm/sq.)		35
Base Sheet Resistivity (ohm/sq.)		6.7
Grid Width, Height (μm)	w_c, t_c	150, 15
Base Via Width (μm)	w_p	300
Grid Resistivity (ohm-cm)		5e-6
Grid Contact Resistivity (ohm-cm^2)		.01
Isolation Kerf (μm)	l_i	150
Grid-Grid Spacing (cm)	W	0.360
Sub-Element Length (cm)	L	1.57

Emitter Grids on the Top Surface/Buried Base Conductor

The relatively high shading loss associated and the series resistance associated with locating the base contact on the front surface can be eliminated by burying the contact below the thin silicon active layer. In the case where the film is grown on the substrate, the buried base conductor must be incorporated before the film growth step. In the case where the substrate is attached to the film after growth, the base conductor can be incorporated after the film growth step, and existing, well-developed metal contact metallization techniques can be used. The interconnection metallization is relatively more complicated in this configuration, because connection must be made from the front emitter to the buried base contacts. Figure 11 illustrates this configuration.

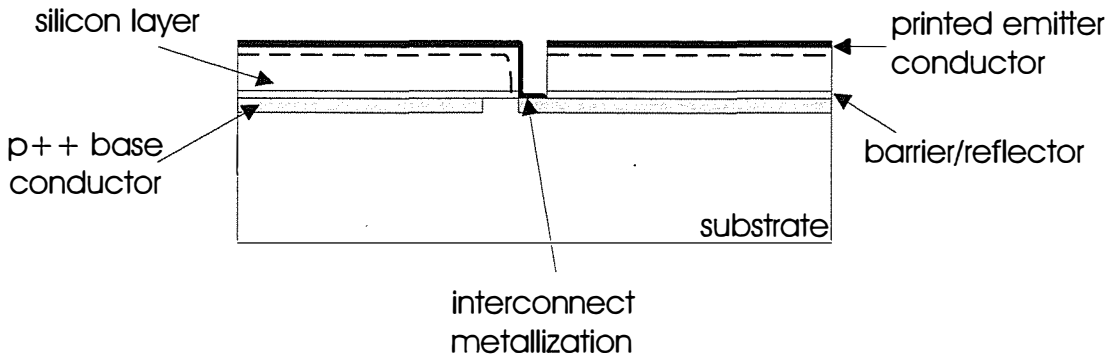

Figure 11. Side view of structure incorporating buried base contacts. Connection is achieved by feeding the interconnect metal through the isolation trench.

This configuration was modeled to compare the total parasitic losses. Using the same conservative design rules for conductor width, thickness, conductivity, etc. leads to lower predicted total power loss of 9–11%. Table 3 summarizes the major contributing loss mechanisms of this configuration.

Table 3. Contribution of various loss mechanisms to the total predicted power loss of the emitter grids on the top surface/buried base conductor configuration.

Loss Mechanism	% Loss (of Total Available Power)
Emitter Series Resistance	2.37
Base Series Resistance	1.32
Emitter Grid Series Resistance	1.88
Base Grid Series Resistance	0.02
Total Grid Contact Resistance	0.19
Interconnect Metal Resistance	0.30
Interconnect Metal Shading	0.52
Kerf-related Shading	1.80
Emitter Grid Shading	2.41
Base Grid and Via Shading	0.00
Total Losses	10.81

Light Trapping with Pigmented-Glass Layers

As part of this program a new technology was developed to improve the light trapping in the thin silicon solar cell. This technology is based on the use of pigments in a high-temperature glass medium. "Pigmented materials" consist of two substances of different refractive index. The "pigment" is in the form of small particles, usually of high refractive index. The "medium" is a binder, usually of low refractive index, throughout which the pigment is dispersed. Paint is a good example of a pigmented material. If the particle size and refractive indices are carefully chosen, light interacts very strongly with and is strongly scattered by the pigment. The result is a broadband and highly diffuse reflecting material.

Figure 12 illustrates the general principle of light trapping through the use of pigmented materials. Adjacent to the back surface, the pigmented material acts as a reflector, scattering weakly absorbed light back into the thin silicon layer. Furthermore, the reflector scatters the light in a diffuse pattern, and the escaping light can be perfectly reflected again at the front surface, back into the silicon layer, by the phenomenon of total internal reflection. In this case, light will travel a much greater distance than the thickness of the silicon layer and the absorption of light will therefore be enhanced.

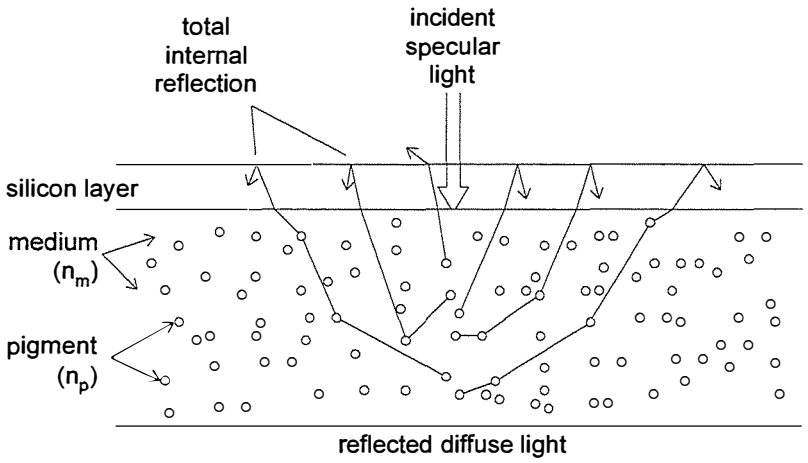

Figure 12. The concept of pigmented materials for light trapping in thin films of silicon.

The scattering phenomenon is described by Mie Scattering Theory [4]. When the pigment particle size is optimized (at near the wavelength of light), the scattering efficiency is highest as illustrated in Figure 13. When the pigment particle size is either much larger or much smaller than the wavelength, Fresnel Refraction Theory and Rayleigh Scattering Theory explain the scattering behavior . This is due to the strong electromagnetic interaction between the scattering particle and the light that occurs when the particle size is similar to the wavelength of light.

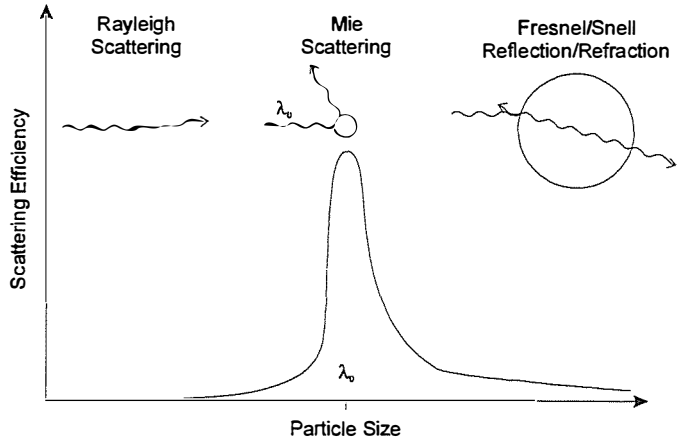

Figure 13. Relative scattering efficiency as a function of pigment particle size.

Mie theory describes how an electromagnetic plane wave interacts with a dielectric sphere when the sphere diameter is approximately equal to the wavelength of light. The incident light excites one or several electromagnetic modes within the sphere. Figure 14 illustrates the electric and magnetic field lines of the first three electromagnetic modes. The electromagnetic oscillations of the sphere then excite secondary electromagnetic waves (of the same wavelength) outside of the sphere. If the sphere size is optimal, the effect is analogous to a quarter-wavelength optical coating. The interference results in backward reflection of the incident wave. At larger sphere sizes, the incident wave excites multi-pole modes, and a smaller fraction of the incident wave is reflected backward. In the limiting case (i.e., a very large sphere), the backward reflected wave is given by Fresnel theory.

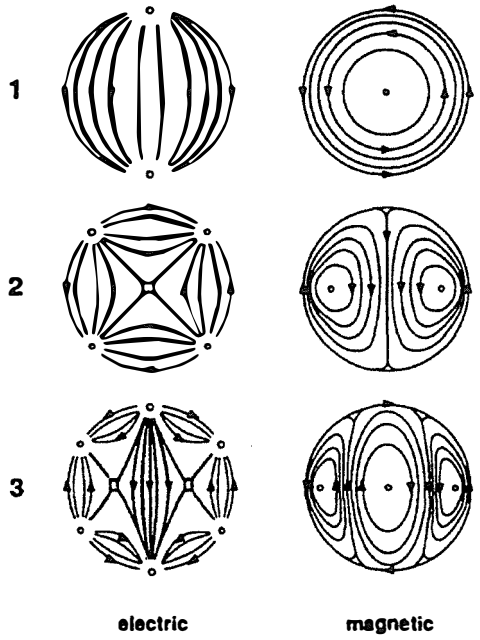

Figure 14. The first three partial electric and magnetic modes of oscillation within a dielectric sphere excited by light incident normal to the page [4].

Achieving a high degree of optical confinement is complicated by the fact that, at least for films grown on substrates, access to the back surface is limited after the film is grown. Substrate removal and subsequent application of a reflector seem incompatible with low-cost, high-throughput manufacturing. Therefore, arrangement for optical confinement must be made before the film is deposited. This almost certainly restricts metallic reflectors from all but the very lowest-temperature film growth techniques because, in general, most highly-reflective metals are unstable at higher temperatures. On the other hand, dielectric layers, either single layers or multiple layer reflective stacks (i.e., Bragg reflectors), are more stable at higher temperatures. However, these types of reflectors either suffer from low reflectivity (i.e., about 15% for single-layer dielectric-silicon interface), or limited wavelength range (typical of a Bragg-type reflector).

Pigmented materials are capable of high reflectivity over a broad wavelength range, and their diffuse pattern of reflection is preferred for light trapping. A wide variety of high-temperature materials like silica, silicon nitride, silicon carbide, and related glassy materials could allow compatibility with high growth temperatures. A reflecting material could be applied and fired on a substrate material like enamel paint, or a suitable pigment could be added directly to the substrate, making it reflective. Furthermore, pigmented materials have potential for low cost. White paint, for example, costs approximately \$0.50 per m^2.

The science and technology of pigmented materials, especially paint, are well known [e.g., 5]. The following design rules can be used to achieve high reflectivity.

1. There is an optimal pigment particle size for the wavelengths of interest.
2. A high ratio of pigment-medium refractive indices is desired.
3. There is an optimal pigment volume fraction.
4. Low absorption coefficient and high scattering coefficient are desired for both media.

During the second year of this program, the application of pigmented materials was explored. An optical model was developed to predict the optical enhancement factor of thin silicon layers with pigmented reflectors. The optical enhancement factor is the ratio of effective optical thickness to actual thickness. It is an often-cited figure of merit for light-trapping schemes. Yablonovitch and Cody [6] derived an expression for the upper limit to the equivalent optical thickness for light uniformly distributed within the silicon. They predicted that, for weakly absorbed, uniformly distributed light in a layer with an ideal front anti-reflection coating and perfect rear reflector, the optical enhancement factor for silicon is $Z = 4n_{Si}^2$, where n_{Si} is the refractive index of the silicon layer. For silicon, the optical enhancement factor approaches 50 for weakly absorbed light.

An analogous expression for thin layers of silicon with scattering back-surface reflectors is

$$Z = 2 L_{eff} n_{refl}^2 ,$$

where L_{eff} is the effective path length (normalized to the silicon layer thickness) of diffuse light traveling in the silicon layer and n_{refl} is the effective refractive index of the pigmented material (approximately equal to the medium's refractive index). For the special case where $n_{refl} = n_{Si}$, the effective optical path length, L_{eff} equals 2, and this equation reduces to Yablonovitch and Cody's original expression.

From this expression, it is evident that a high refractive index for the medium of the back scattering reflector is desired. If a glass material is used as the medium, the refractive index of the pigmented glass would be approximately between 1.5 and 1.6. This leads to an optical confinement factor of approximately five. This represents a

modest improvement in optical confinement and techniques to improve this figure will be explored in the coming year.

Several pigmented glass materials were constructed by mixing glass paste precursors with titanium dioxide powder. Figure 15 shows a mock up of a thin silicon film grown on a substrate coated with a pigmented glass material. The film has been cut away to reveal the underlying reflective coating. The reflectivity curve of a similar coating is shown in Figure 16. The measured external reflectivity of the layer is about 90% over the wavelength range between 750 and 1200 nm. The bulk or internal reflectivity of the pigmented glass (that which is corrected for the effect of the surface reflectivity) is above 95% over this wavelength range. When in contact with silicon, the reflectivity of the pigmented glass/silicon interface is predicted to be about 95% over this wavelength range.

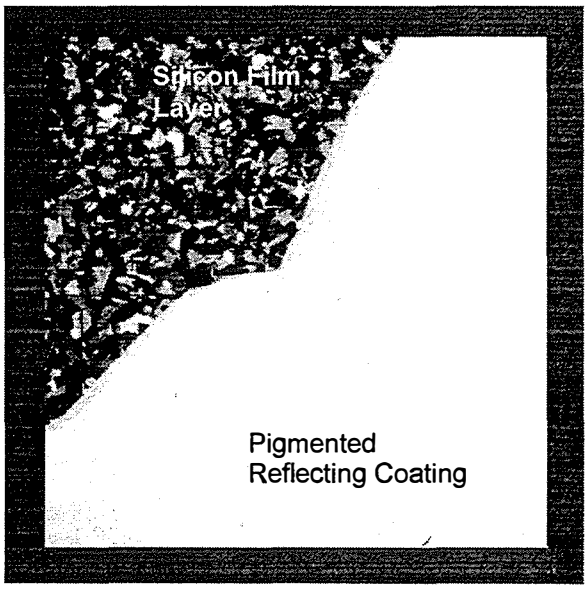

Figure 15. The silicon layer is cut away to show the underlying pigmented reflecting coating on the substrate.

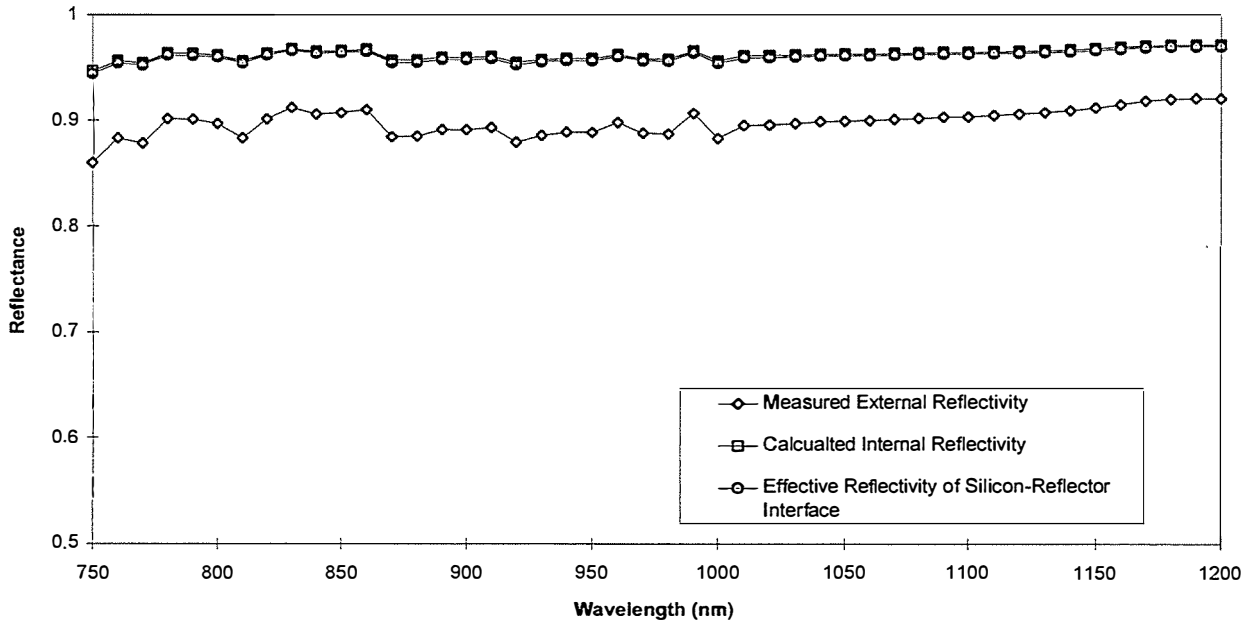

Figure 16. Measured external, calculated internal reflectivity of pigmented glass barrier layer. Also included is the predicted silicon/pigmented glass interface reflectivity.

2.2 Sub-Module Process Development

A solar cell fabrication sequence was developed specifically for the thin-film material. The process is very similar to standard high-efficiency polycrystalline silicon solar cell processes, including phosphorous gettering, emitter etchback after diffusion, emitter passivation by PECVD oxide deposition, evaporated contacts, and double layer anti-reflection coating. The baseline fabrication sequence is outlined in Table 4.

Several additional fabrication steps are required for the sub-module integration. These include top-side base contacts, sub-element isolation and interconnect metallization. The development of these fabrication steps follows.

Table 4. *Solar Cell Fabrication Process*

Process Step	Process Details
Sample clean:	-Chemical polish (90:10::HNO_3:HF) ~ 10–15 min. -Organics etch (1:1::H_2SO_4:H_2O_2) 10 min. -Heavy metals etch (1:1::HCl:H_2O_2) 10 min. -Oxide strip (20:1::H_2O:HF) until hydrophobic *each step followed by DI water rinse
Getter:	-Steam clean tube with DI water; clean boat in 20:1::H_2O:HF -Push samples (890°C) flowing N_2 ~7–8 min. -Purge with N_2 15 min. -Getter for 2 hours @ 7:5::O_2:$POCl_3$ -Cool to <800°C in O_2, then pull ~7–8 min.
Sample clean:	-Repeat clean as above
Phosphorous Diffusion:	-Steam clean tube with DI water; clean boat in 20:1::H_2O:HF -Push samples (850°C) flowing N_2 ~7–8 min. -Purge with N_2 15 min. -Pre-deposition 7 min. @ 2:1::O_2:$POCl_3$ -Purge with N_2 15 min. -Oxidation in O_2 50 min. -Switch from O_2 to forming gas (5% H_2/balance N_2), 15 min. -Turn furnace off, anneal samples until temperature is ≤ 300°C
H+:	-Oxide strip (20:1::H_2O:HF), brief DI water rinse -RF hydrogenation 40 min. (300°C)
Damage etchback:	-Oxide strip, DI water rinse -Etchback (1000:100:1::HNO_3:H_2O:HF) for 1 min. intervals checking sheet resistivity to final sheet resistivity of 60–70Ω/sq. (~ 2–3 min.), DI water rinse
Emitter Isolation	-Photolithography to define active device area -Plasma etch isolate (~ 5–10 min.) -Remove photoresist in acetone followed by methanol, DI water rinse
Emitter passivation:	-Oxide strip, DI rinse -Deposit 100Å CVD oxide n=1.47 (300°C) -CVD oxide anneal, 30 min. in forming gas (400°C)
Base Contact	-Photolithography to define base contact -Evaporate 5000Å aluminum, liftoff in acetone, methanol, DI water rinse -Alloy contacts 1 min. (525°C)
Emitter Contact	-Photolithography to define emitter contact with overlap on base contact -Evaporate Ti/Pd/Ag (500/500/500Å) -Liftoff in acetone, followed by methanol, DI rinse
Silver Plate Up and Sinter	-Ag plate contacts to 10 μm thickness -Sinter contacts 1 min. (425°C)
Anti-Reflection	-Deposit MgF/ZnS double layer AR coating

Silicon Nitride Passivation

The passivation of low resistivity silicon surfaces using PECVD Si_3N_4 was investigated by Georgia Tech as a lower tier subcontractor. The objective of the study was to determine the passivation quality of Si_3N_4 on a 0.6 ohm-cm p-type <100> Si surface. This low temperature passivation scheme is potentially useful for partial back coverage solar cells or for monolithically interconnected device structures.

The experimental approach involved fabricating test diodes with contacts on the front surface at AstroPower. The back surfaces were bare. The samples were sent to University Center of Excellence for Photovoltaics Research and Education at Georgia Tech for PECVD Si_3N_4 deposition on the back surface. (Oxidations could not be attempted since metal contacts were already defined.) The samples were cleaned using the following process:

1. Front surface protection with photoresist
2. BOE etch to remove native oxide from rear surface
3. Photoresist removal
4. Si_3N_4 direct deposition at 300°C in an RF PECVD reactor (Deposition time: 6 minutes, Deposition power: 3OW, Deposition pressure: 900 mtorr)
5. Varying post deposition annealing

Three samples were processed with the above sequence. The Si_3N_4 deposition was identical in each case. However, the post-deposition thermal treatment was varied.

The processed samples were returned to AstroPower for rear-illuminated IQE measurements. These measurements allowed for the extraction of the surface recombination velocity at the Si_3N_4-Si interface. The rear-illuminated IQE spectra are shown for the three samples in Figure 17.

The results in Figure 17 indicate that a post deposition anneal is critical to the Si_3N_4 passivation quality. Clearly, of the three schemes investigated here, the highest temperature (400°C) resulted in the lowest recombination velocity. Numerical analysis done at AstroPower revealed the effective surface recombination velocity (SRV) for each sample.

Similar to other studies, the SRV for a SiN passivated surface was reduced by over one order of magnitude by implementing a 5 minute anneal at 400°C in an RTP unit. The resulting SRV values (100-300 cm/s on 0.6 Ω-cm, p-type Si) are consistent with those required for high-efficiency solar cell fabrication.

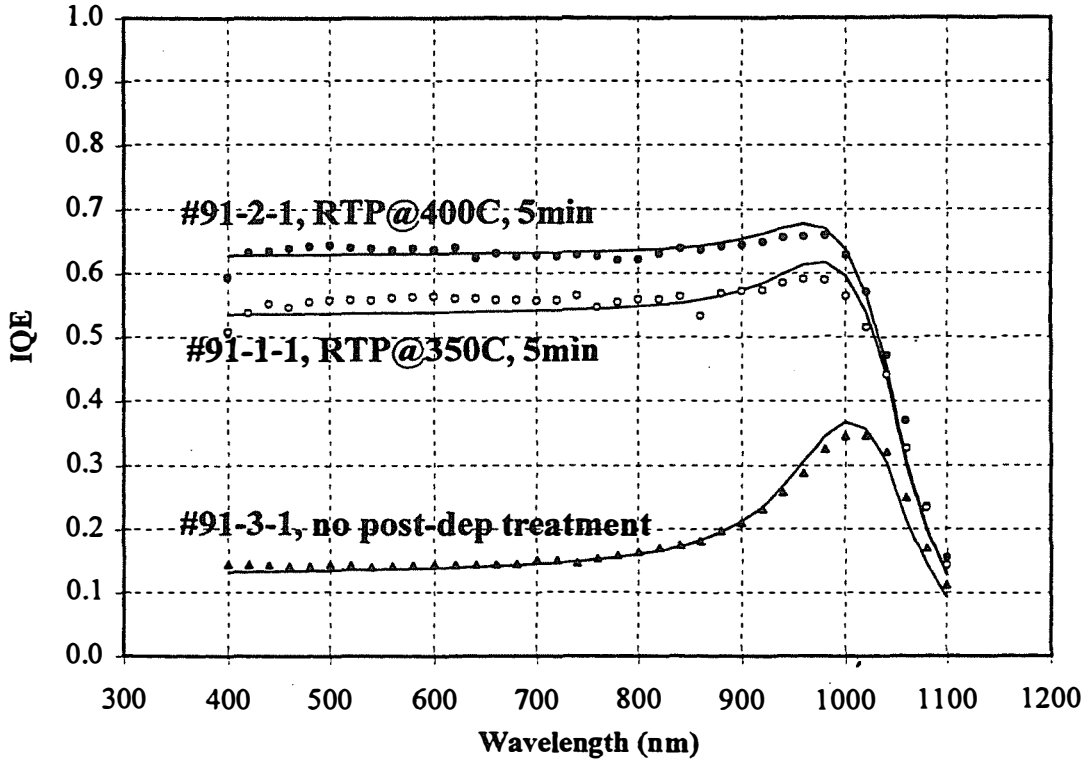

Figure 17. Effect of post Si_3N_4 deposition annealing condition on rear-illuminated IQE. Si_3N_4 depositions were done at Georgia Tech.

Single Junction Devices

Sub-modules with top-side base contacts were examined because of the relative ease of forming the sub-element interconnection with both conductors located on the top surface. An oxide diffusion mask was used to reveal the base layer on the front surface. The diffusion mask was applied before the wafer was diffused, and after the diffusion step, the oxide was removed by chemical etching in dilute hydrofluoric acid. The oxide diffusion mask is patterned lithographically by screen printing an etch-resistant paste on the wafer.

One of the key issues is printing the base contact within the via area. Sufficient width for the base via is required to prevent accidental electrical contact between the base contact and the emitter. This would result in severe shunting. At the same time, it is desirable to minimize the base via width to reduce the effective shading losses of the via.

We examined conventional, screen printed glass-paste-based materials for the top-side grid conductors. Because of the lithography limitations of screen printed conductors,

the conductors are relatively wide (w_c >100 μm). This leads to relatively high shading losses. Further, the via opening through the emitter, w_p, must be relatively large for alignment purposes.

Alignment of the p-contact within the p-via is generally good across the entire area of completed sub-modules. However, in some areas of the sub-module the p-via pattern is not complete due to two factors. First, the surface of the polycrystalline wafer is highly textured due to the anisotropic etch used in surface preparation. Second, the wafer is not uniformly flat. Therefore, some additional work is needed to improve the print quality of the p-via. It is likely that switching to a isotropic etch, like the CP etch, and improving the wafer flatness by optimizing the growth conditions can improve the print quality of the p-via.

Individual sub-elements of a working sub-module were tested for voltage, current, shunt resistance and series resistance characteristics. A completed sub-module was partitioned into an array of small-area test solar cells by scribing through the emitter with a dicing saw. Each solar cell is 0.64 cm^2 and contains one emitter grid and one base grid. A schematic view of the metalization scheme (all top contact) for the individual working sub-module is shown in Figure 18.

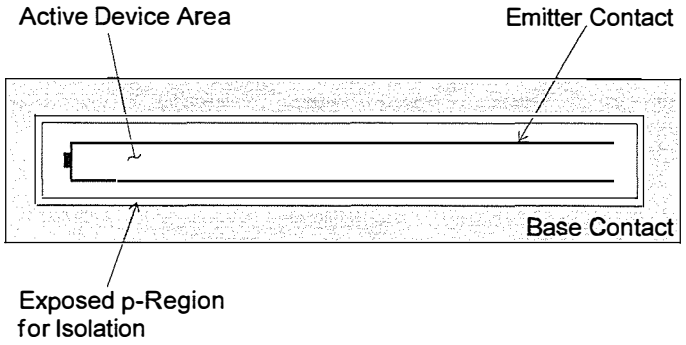

Figure 18. Schematic view of all top contact metalization for small-area sub-element solar cells

Interconnected Devices

The original interconnecting technology was achieved by feeding the interconnect metal through an isolation trench. This technology however, resulted in severely shunted devices due to a critical emitter wrap. In order to simplify the interconnect technology and provide a more robust device fabrication sequence, and a modified metalization/ interconnect was developed. The modified metalization/interconnect schematic can be seen in Figure 19.

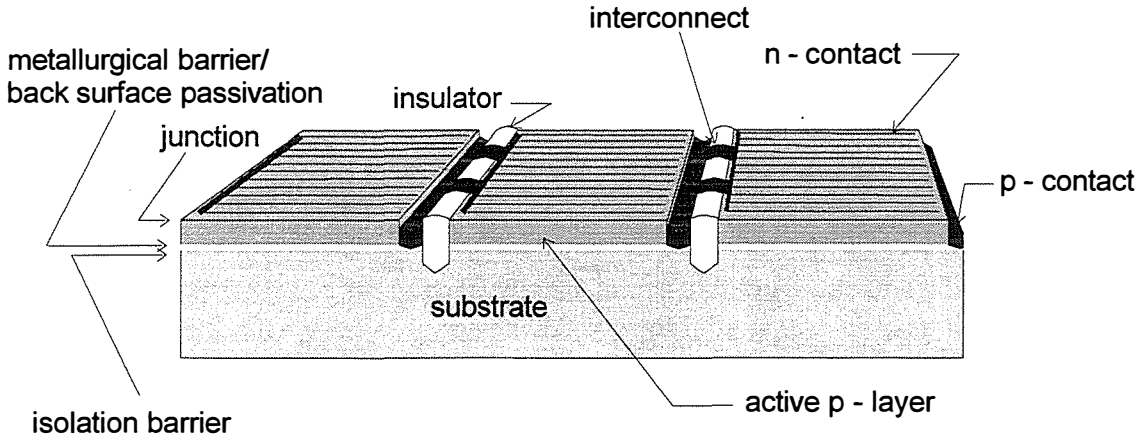

Figure 19. Modified metalization/interconnect

The modified metalization/interconnect eliminated the need for an emitter wrap down one side of the sub-element isolation trench. Following a single junction diffusion an isolation trench is made to accomplish sub-element isolation. This trench was then filled with an electrical insulating epoxy designed for sealing hybrid circuit packages. Following the trench fill, a second trench is cut to allow feeding the interconnect metalization in the trench to make contact to the now exposed p-layer, over the insulating epoxy to the n-contact. This interconnect can be accomplished with a single metallization step. Figure 20 shows the current-voltage characteristic of a 36 segment, 321 cm^2 device as measured by NREL.

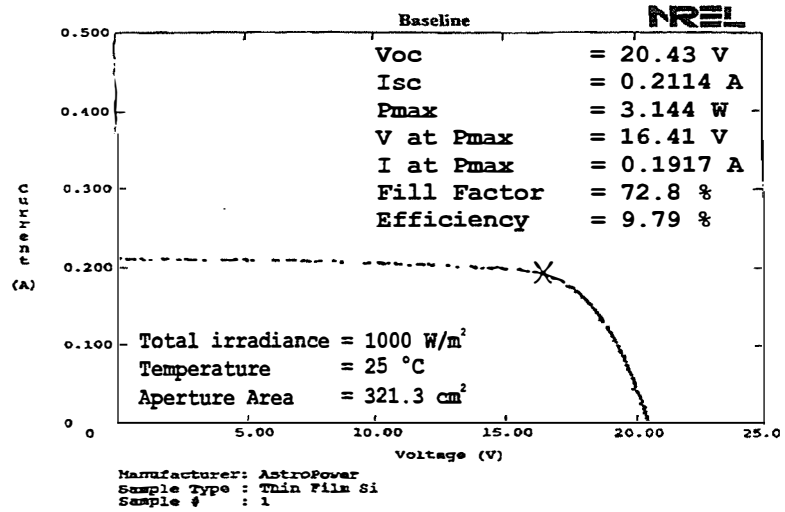

Figure 20. Current-Voltage characteristic of a 36 segment, monolithically interconnected device.

2.3 Advanced Device Design

Single Back Contact Development

During growth and fabrication sequences for the modified metalization/interconnect technology, it became apparent that further improvements in the device design would result in significant reductions in the number of process sequence steps and a greatly simplified interconnect technology. This new design eliminates the need for two trench cuts and also eliminates the need to back-fill any saw kerfs with an insulator. The new design also permits the emitter and cross-over matallization to occur simultaneously. Figure 21 shows a schematic view of the advanced monolithic interconnect device design that AstroPower is presently pursuing.

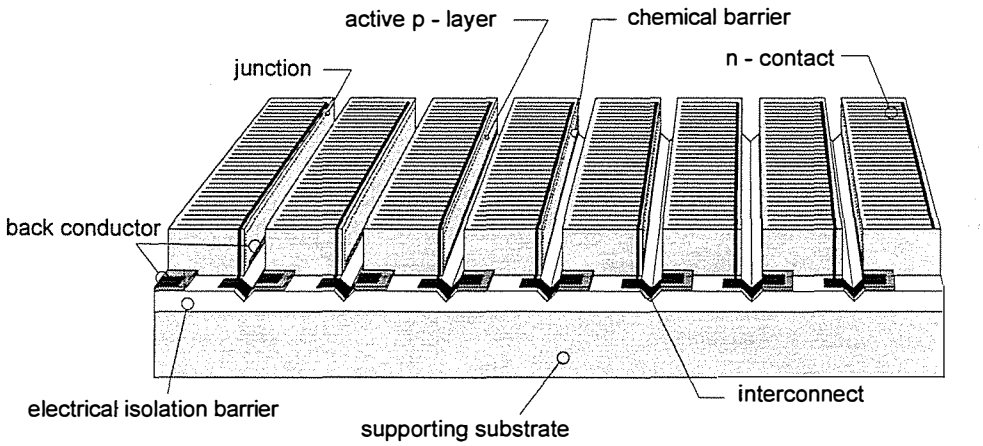

Figure 21. Schematic view of advanced monolithic device design which includes a new back conductor (Single Back Contact).

The new device design that includes the back conductor provides a random back surface texture which is expected to enhance light trapping effects of the final device.

Thin silicon layers have been achieved on randomly textured back conductors having aspect ratios greater than 5:1 (width:height). The current area being developed is 400 cm^2 and is limited by the dice isolation capabilities presently available. Figure 22 is a post growth picture of a 421 cm^2 Single Back Contact Structure.

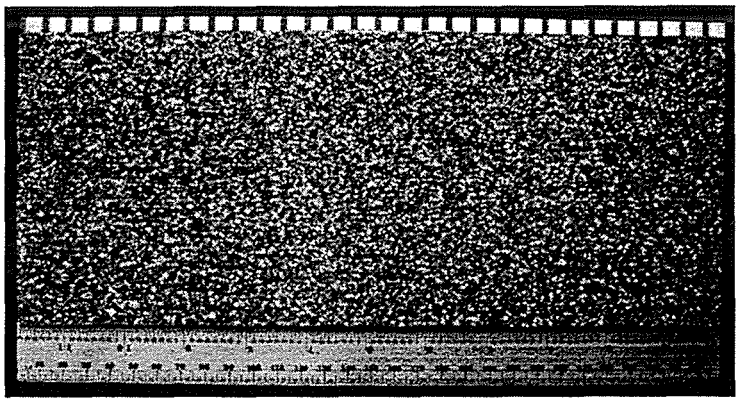

Figure 22. Front view of a post growth Single Back Contact structure. Grain sizes in excess of 500μm can be seen over an area of 400 cm^2.

3 Summary

AstroPower has continued its development of an advanced thin-silicon-based photovoltaic module product. This module combines the performance advantages of thin, light-trapped silicon layers with the capability of integration into a low-cost monolithically interconnected array. This report summarizes work carried out over a three year cost-shared contract.

Key results accomplished during this phase include an NREL verified conversion efficiency of 12.5% on a 0.47 cm^2 device. The device structure utilized an insulating substrate and an active layer less than 100 um thick.

A new metalization scheme was designed utilizing insulating crossovers. This technology was demonstrated on a 36 segment, 321 cm^2, interconnected array. That array was tested at NREL with an efficiency of 9.79%. Further advances in metallization have lead to an advanced "single back contact" design that will offer low cost through ease of processing and higher performance through reduced shading.

4 REFERENCES

[1] Cotter, J.E. et al., "Polycrystalline Silicon-Film™ Thin-Film Solar Cells: Advanced Products", *Progress in Photovoltaics,* **3**(5), (1995a), pp. 351-358.

[2] Cotter, J.E. et al., "Advanced Silicon-Film™ Product Development", *13th PV Program Review Meeting,* (May, 1995b).

[3] "High-Speed Sheet Growth of Thin Silicon Films", *Final Subcontract Report,* DOE subcontract # DE-FG05-94ER81713.
[4] G. Mie, *Ann. Physik,* Vol. 25, 1908, p. 308
[5] Volz, H. G., "Industrial Color Testing: Fundamentals and Techniques," VCH Verlagsgesellschaft mbH, Weinheim, Federal Republic of Germany, 1995.
[6] Yablonovitch, E. and Cody, G. D., "Intensity Enhancement in Textured Optical Sheets for Solar Cells", *IEEE Transactions on Electron Devices,* Vol. ED-29, No. 2, 1982, pp. 300-305.

REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	April 1998	Final Report

4. TITLE AND SUBTITLE

Light-Trapped, Interconnected, Silicon-Film™ Modules; Final Technical Status Report

5. FUNDING NUMBERS

C: ZAF-5-14142-02
TA: PV804401

6. AUTHOR(S)

R.B. Hall, J.A. Rand, D.H. Ford, and A.E. Ingram

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

AstroPower, Inc.
Solar Park
Newark, DE 19716-2000

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

SR-520-24641

11. SUPPLEMENTARY NOTES

NREL Technical Monitor: H.S. Ullal

12a. DISTRIBUTION/AVAILABILITY STATEMENT

12b. DISTRIBUTION CODE

UC-1260

13. ABSTRACT *(Maximum 200 words)*

AstroPower has continued its development of an advanced thin-silicon-based photovoltaic module product. This module combines the performance advantages of thin, light-trapped silicon layers with the capability of integration into a low-cost, monolithically interconnected module. This report summarized work carried out over a 3-year, cost-shared contract. Key results accomplished during this phase include an NREL-verified conversion efficiency of 12.5% on a 0.47-cm^2 device. The device structure used an insulating substrate and an active layer less than 100 um thick. A new metalization scheme was designed using insulating crossovers This technology was demonstrated on a 36-segment, 321-cm^2, interconnected module. That module was tested at NREL with an efficiency of 9.79%. Further advances in metalization have led to an advanced "single back-contact" design that will offer low cost through ease of processing and higher performance through reduced shading.

14. SUBJECT TERMS

photovoltaics ; photovoltaic modules ; Silicon-Film™ modules ; thin-silicon solar cells ; conversion efficiency ; monolithic interconnect array ; metalization

15. NUMBER OF PAGES

30

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL