NREL/SR-520-22740 • UC Category: 1280 • DE97000232

# Large-Area Silicon-Film™ Panels and Solar Cells

## Phase II Technical Report, January 1996 - December 1996

J.A. Rand, A.M. Barnett, J.C. Checchi,
J.S. Culik, S.R. Collins, D.H. Ford,
R.B. Hall, E.L. Jackson, C.L. Kendall
*AstroPower Inc.*
*Newark, Delaware*

NREL technical monitor: R.L. Mitchell

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A national laboratory of
the U.S. Department of Energy
Managed by Midwest Research Institute
for the U.S. Department of Energy
under Contract No. DE-AC36-83CH10093

Prepared under Subcontract No. ZAF-5-14271-3

March 1997

Available to DOE and DOE contractors from:
Office of Scientific and Technical Information (OSTI)
P.O. Box 62
Oak Ridge, TN 37831
Prices available by calling (423) 576-8401

Available to the public from:
National Technical Information Service (NTIS)
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161
(703) 487-4650

Printed on paper containing at least 50% wastepaper, including 20% postconsumer waste

# Table of Contents

# List of Figures and Tables

# Introduction

The Silicon-Film™ process is on an accelerated path to large-scale manufacturing. The present manufacturing effort is based on solar cells with an area of 240 $cm^2$ (the solar cell is referred to as the AP-225). Efficiencies in excess of 12% have been demonstrated for these large area cells. Smaller, laboratory devices have demonstrated efficiencies of 14.6% (see Figure 2).

In support of large-scale production, development work has been underway to determine the optimum width of the Silicon-Film™ sheet. The sheet presently in production is nominally 15 cm wide. Advantages to increased sheet width include reduced capital costs, improved material utilization, and the capability to increase solar cell size. Increased solar cell size has the advantage of higher power per piece with fixed cost for handling during solar cell and module fabrication.

The investigation into width has resulted in the construction of a new, wide, Silicon-Film™ machine. This equipment has demonstrated that Silicon-Film™ sheet material can be fabricated at a width greater than 30 cm. At this point, there is no known limit to the width capabilities of the Silicon-Film™ sheet growth process. This machine capability has permitted us to evaluate a number of different solar cell sizes. Solar cells with areas of 240 $cm^2$, 300 $cm^2$, 400 $cm^2$, 675 $cm^2$, and 1800 $cm^2$ have been fabricated. A critical element in the optimization process is the capability of cutting finished solar cells into smaller sizes for different applications, as illustrated in Figure 1.

A low cost manufacturing process for Silicon-Film™ solar cells is under development. Under this effort, each step used in Silicon-Film™ cell fabrication is being developed into a continuous/in-line manufacturing process with the goal of significantly increased production capacity and a reduction in handling and waste streams.

The long term stability of Silicon-Film™ solar cells continues to be demonstrated by the performance of the PVUSA array installed in Davis, California in 1994. In addition to validating the field stability of this technology, the PVUSA array has demonstrated very good performance in terms of energy delivery. Published performance information for 1995 [1] shows that the AstroPower Silicon-Film array produced more energy (AC kWhr) per rated watt of array capacity than any of the other EMT arrays, which include mono-crystalline and polycrystalline silicon arrays, amorphous silicon arrays, and a two-axis tracking system.

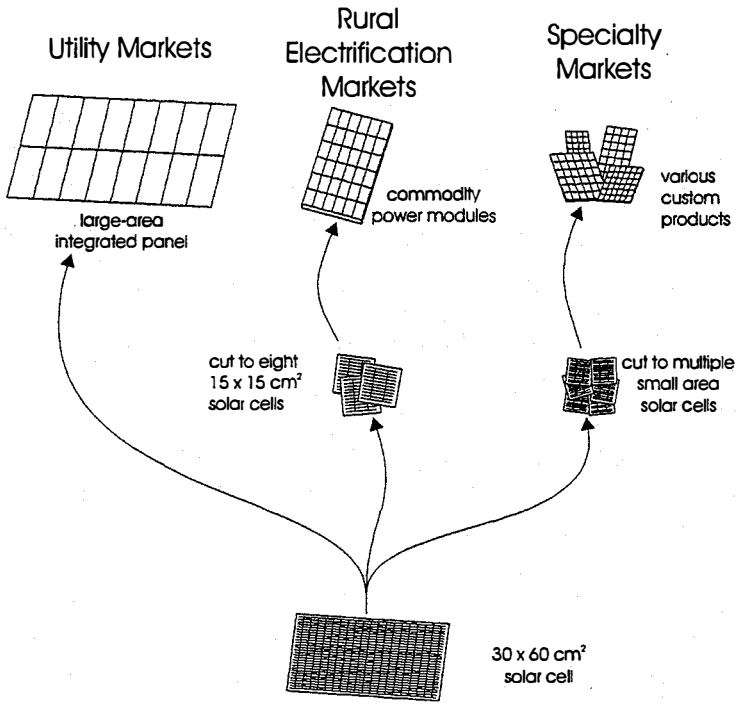



FIGURE 1. **Flexibility of a 30 cm x 60 cm solar cell in meeting several different PV markets.**

## PROCESSING DEVELOPMENTS

The flexibility in substrate size has led to the need for advances in fabricating uniform, large-area emitters and anti-reflection coatings. In contrast to "traditional" solar cell manufacturing based on integrated-circuit technologies, these next-generation Silicon-Film™ processes are inherently free of substrate size boundary conditions. The use of reliable industrial coating application equipment and low-cost, environmentally responsible precursors, make these advanced processes particularly attractive to large-scale adaptation.

Large area Silicon-Film™ emitter processing is accomplished by continuous-feed application of a phosphorous-based coating. This is followed by thermal cycling, using conditions approaching those encountered in rapid thermal processing (RTP). The resulting emitter sheet resistance is typically uniform to within 10% over the full device area. Wafer deglazing is straightforward, and requires no specialized equipment or chemicals.

For the anti-reflection coating, simple liquid precursors are applied to preheated solar cells using commercial coating equipment to form an oxide layer which is index-matched to module encapsulants. Advances made in this technology include the ability to

chemically vary the index of refraction, and the improvement in coating uniformity using conductive and radiative heating methods.

Improvements in the characterization of Silicon-Film™ material have been accomplished with the use of a RFPCD lifetime measurement technique developed by Dr. Richard Ahrenkiel of NREL. The measurement method allows a contactless measurement of the minority carrier lifetime in grown material with little or no sample preparation.

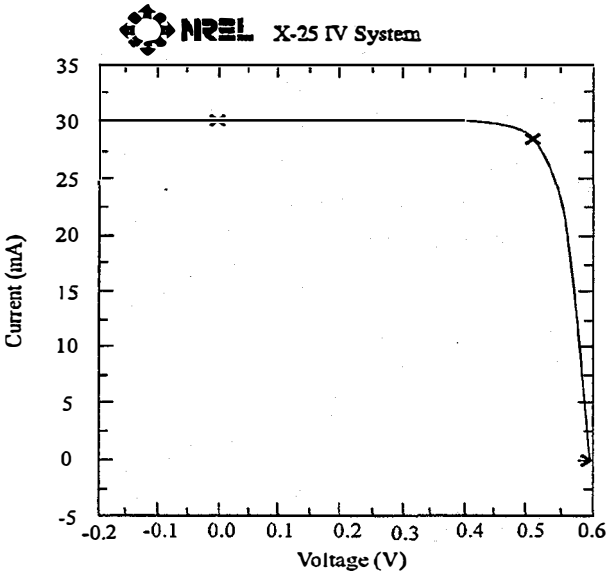
## DEVICE PERFORMANCE

A summary of the solar cells being evaluated is shown in Table 1. Some of the devices have been tested at NREL (see Note). Testing of these large devices has required the use of special testing apparatus. One such testing jig is being evaluated by NREL now with AP-225 and AP-300 solar cells. A second jig has recently been supplied to NREL for performance testing the AP-1800. The I-V curve for the highest efficiency laboratory cell is shown in Figure 2.

**TABLE 1.** Summary of device data on different size solar cells.

| Product | Area | Power | Efficiency | Note |
|---|---|---|---|---|
| Laboratory Solar Cells | 1.0 $cm^2$ | 14.6 mW | 14.6% | (1) |
| AP-225 Solar Cell | 240 $cm^2$ | 2.93 W | 12.2% | (1) |
| AP-300 Solar Cell | 311 $cm^2$ | 3.48 W | 11.2% | (2) |
| AP-400 Solar Cell | 412 $cm^2$ | | | (3) |
| AP-675 Solar Cell | 676 $cm^2$ | 7.87 W | 11.6% | (1) |
| AP-1800 Solar Cell | 1800 $cm^2$ | | | (3) |

(1) NREL test , (2) AstroPower test, (3) Fabricated, but not yet tested




$V_{oc}$ = 0.5966 V
$I_{sc}$ = 30.14 mA
$J_{sc}$ = 30.14 mA/cm$^2$
FF = 81.00%

$V_{max}$ = 0.5086 V
$I_{max}$ = 28.63 mA
$P_{max}$ = 14.56 mW
Eff = 14.6%

FIGURE 2. **Current-voltage curve for a 1-cm$^2$, Silicon-Film™ solar cell with an energy conversion efficiency of 14.6%.**

## Solar Cell Characterization and Performance

### *Post-growth Material Improvements and Device Optimization*

Like other multicrystalline and polycrystalline silicon materials, the steps of post-growth material quality enhancement are integral parts of high performance Silicon-Film™ solar cell fabrication. In this work gettering techniques were used to remove lifetime-limiting impurities from active device region (bulk) to the gettering sites (surfaces). These techniques involve extended heat treatments in the presence of aluminum and phosphorus. The passivation of bulk crystal defects is accomplished with hydrogen treatment (forming gas anneal and hydrogen plasma). These techniques have been integrated at different stages in the cell processing sequence. Typical starting minority carrier diffusion lengths in Silicon-Film™ sheet materials are in the range of 20-30μm. The diffusion length of finished solar cells ranges from 50 to 200μm. Some devices exhibit close to 300μm diffusion length.

The optimization of gettering and passivation techniques as applied to Silicon-Film™ has been investigated in earlier work. Figure 3 shows a typical diffusion length distribution which was sampled on 27 solar cells (1cm$^2$) made on three prime wafers cut

from a single large 240 $cm^2$ Silicon-Film™ wafer. The lateral non-uniformities across the wafer require further understanding and optimization in upgrading these materials. Therefore, one of the areas of investigation in the last year was the *evolution* of minority carrier diffusion length (or lifetime) along with solar cell processing steps, especially those quality enhancement steps, such as P/Al gettering, forming gas annealing, and RF $H^+$ treatment. This investigation will identify the nature of these non-uniformities and determine process strategies.

In general, Silicon-Film™ materials are highly responsive to hydrogenation treatment. However, the overall improvement was found to be dependent on the effectiveness of the gettering step. A four hour P/Al gettering was found effective in removing both fast and slow metallic impurity species and lead to a significant increase in effective minority carrier diffusion length. However, the degree of improvement from the gettering step was material and site specific, as shown in the Figure 4. This can be related to localized dislocation densities in the materials, which could impact the effectiveness of gettering steps. Effort in tracing these lifetime-limiting impurities is continuing.

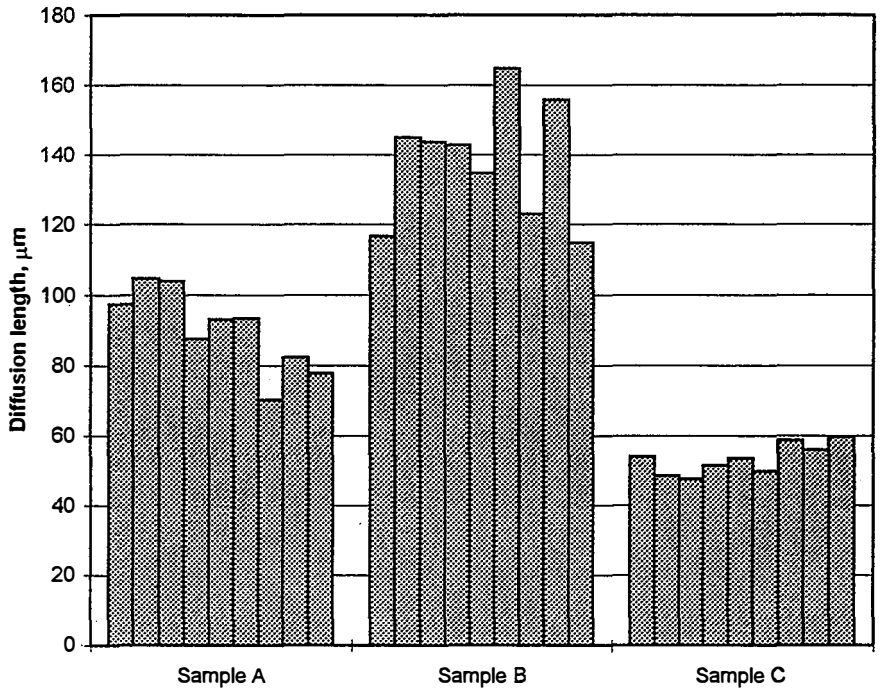



**Figure 3. A typical carrier diffusion length distribution for 27 solar cells (1$cm^2$) that were made on three samples cut from the same large 240 $cm^2$ wafer. Processing was nominally the same for all three samples.**

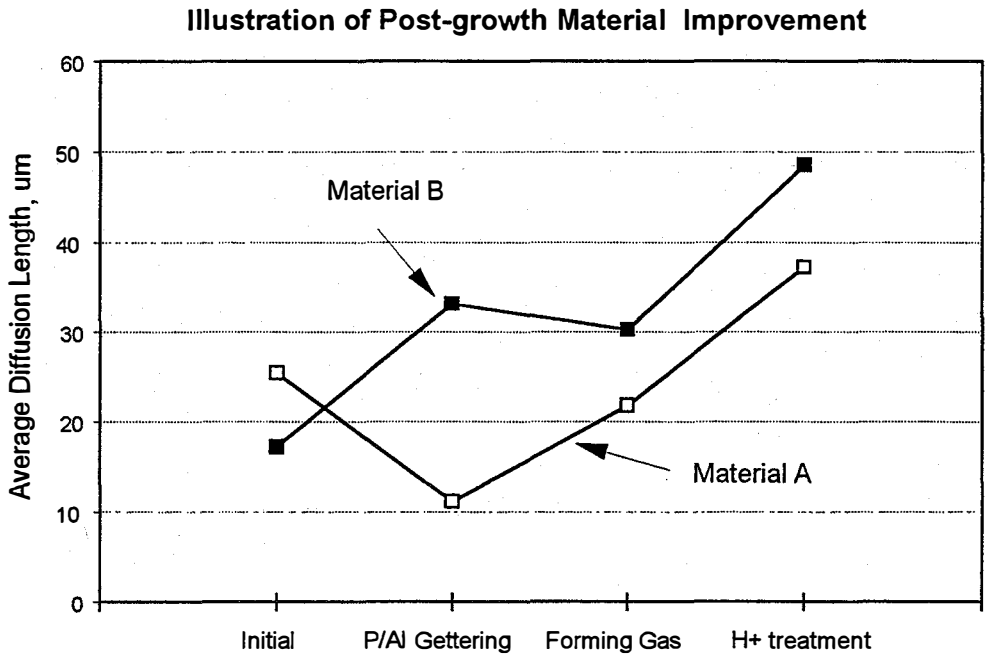



**Figure 4. Evolution of carrier diffusion lengths measured on mesa diodes from two typical Silicon-Film™ materials during the solar cell fabrication**

Another interesting phenomenon of Silicon-Film™ material is the illumination-dependent minority carrier lifetime. Historically the lifetime of Silicon-Film™ material increased with bias light intensity. In more recent devices this trend has been reversed, and lifetime is decreasing with increased bias light intensity. According to the historical explanation, the carriers generated by bias light saturate the dangling bonds (traps) at dislocations and grain boundaries, leading to a reduction in carrier recombination at these regions. The change in illumination dependence indicates other mechanisms are present in Silicon-Film™ solar cells, either material or process related. More interestingly, the diffusion lengths extracted from light biased IQE data show a better uniformity than those extracted from IQE data taken without light bias. An observation of this is listed in Table 1. The causes of this "reverted" dependence is currently under investigation.

**Table 1. Diffusion lengths of three adjacent Silicon-Film™ solar cells determined from IQE with and without light bias.**

| Diffusion length (μm) | Cell#1 | Cell#2 | Cell#3 |
|---|---|---|---|
| With light bias | 90 | 88 | 87 |
| Without light bias | 114 | 148 | 174 |

In addition to the bulk material improvement, surface passivation of the emitter is another important area to maximize the utilization of AM1.5G spectrum. In order to avoid the additional high temperature cycle and depassivation of hydrogenated materials, a low temperature deposited PECVD oxide followed by forming gas annealing was used to passivate the emitter surface. Combined with the optimization of the emitter doping profile, an IQE of over 70% at 400nm wavelength has been routinely achieved. The deposited PECVD silicon dioxide is at 100Å thickness, compatible with the ZnS/$MgF_2$ double layer AR coating system. After several months, no degradation in passivation was observed (with the sample stored in the dark). Figure 5 illustrates the benefit from bulk gettering/passivation and emitter surface passivation. In order to maximize the short-circuit current, a thermal oxide passivation combined with a backside hydrogenation is also under investigation.

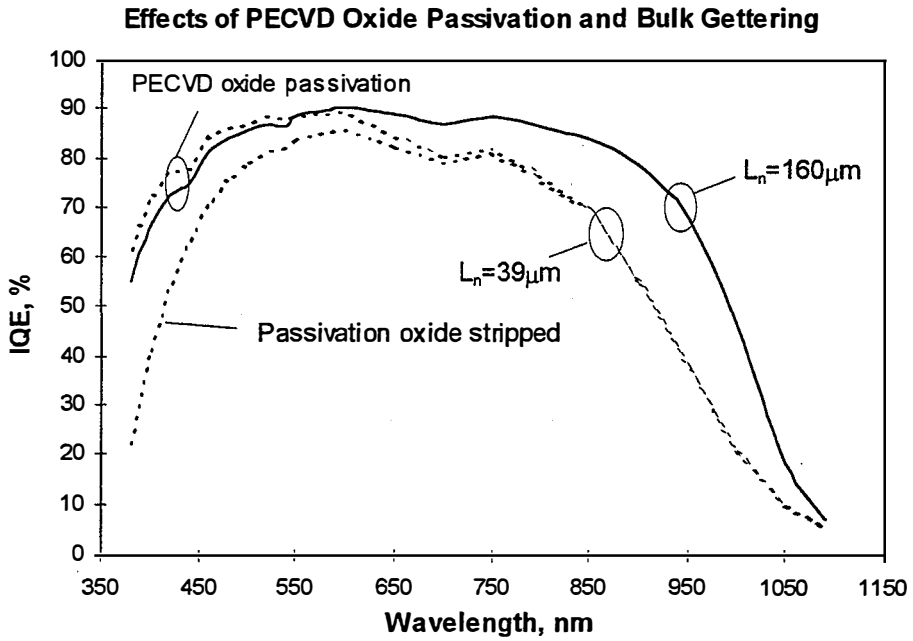



**Figure 5. Improvement of internal quantum efficiency from bulk gettering/passivation and low temperature surface passivation.**

The large variation in fill factor in Silicon-Film™ solar cells (75%-79%) has been found to be due to the high diode ideality factor at maximum power point rather than $R_s$ (~0.6Ω-$cm^2$) or $R_{sh}$ (>10KΩ-$cm^2$). This indicates that significant carrier recombination is occurring in depletion regions (junction, grain boundaries, and other defects). Efforts are presently underway to minimize this recombination. Plans include controlling the depletion region width in the area of grain boundaries and defects by changes in the gettering and emitter diffusion steps. Efforts to control this recombination with hydrogen have been successful in the past and are continuing to be studied.

## Solar Cell Process Development

### Surface Preparation

Production-scale surface preparation before diffusion of AP-225s includes dry abrasive blasting followed by a series of wet chemical etches, cleaning solutions, and rinses. The etching and cleaning solutions include baths of sodium hydroxide, hydrochloric acid, and hydrofluoric acid with extended de-ionized cascading rinses in between. The process is batch mode with 50 wafers in upright cassettes in each batch.

During the past year, investigations were conducted in the following areas:

i. mechanical yield and surface damage associated with dry blasting,
ii. throughput and manual operation of the wet-etch process.

The secondary problems associated with manual operation include the potential hazard of operator exposure to chemicals, high labor costs, and inherently inconsistent solar cell performance.

The results of the above investigations are summarized in the following sections.

### Dry Abrasive Blasting Alternatives

High pressure water jetting was thoroughly investigated as an alternative to our present dry blasting technique. The present dry-blast technique removes the top four micrometers of the as-grown sheet. However, the resulting damage to the underlying silicon is substantial requiring chemical removal of the damaged silicon. Although the high pressure water jetting process proved to be a cleaner method of surface removal, chemical removal of the damaged silicon was still necessary. In addition, mechanical yields due to the high pressure water jet were of concern and significant engineering development was considered necessary. Modifications in the surface cleaning process, described below, eliminated the necessity to choose a dry-blast alternative.

### Surface Cleaning

Sodium hydroxide is the main component in AstroPower's wet-chemical surface preparation processing line. It acts both as a degreaser and as a silicon etch to remove surface damage. Our standard surface preparation process called for two separate sodium hydroxide etching steps: (i) pre-getter and (ii) pre-junction diffusion. During the past year, we were able to eliminate the pre-getter etch step with no significant change in solar cell performance. One important improvement was noted in grid line width. Sodium hydroxide acts as an anisotropic etch on polycrystalline silicon; the longer the surface is exposed to sodium hydroxide solution the rougher the surface becomes. Due to the elimination of the first etch step, gridline widths could be reduced by 26%. The reduced

surface texturing allowed us to successfully minimize necking on our narrower gridline screen print pattern. This became a significant advantage in achieving consistent solar cell performance as our solar cell production volumes increased during the fourth quarter of 1996.

## Wet-Etch Equipment

Considerable effort has been made to specify an optimized wet-etch process and associated equipment to achieve high throughput (1000 wafers per hour), improved process control, and improved operator safety. In 1996, we continued to investigate two different options: (i) automation of our present conventional batch process where cassettes of wafers are brought in and out of open tanks of solutions, and (ii) continuous wet-etching where wafers are loaded onto a continuous belt and are immersed or sprayed with the appropriate solution or rinse.

We have delayed making the final decision on wet-etch equipment until the process steps of dry-blasting, gettering, junction diffusion, and screen-printed gridlines are completely evolved. We expect this to occur as production volumes continue to increase in early 1997.

### *Continuous In-Line Diffusion*

The objective of this effort is to develop a low-cost process to produce the emitter junction in large-area Silicon-Film™ sheet material. Prior work as reported in our previous Annual Report was concerned with developing an N-type dopant source that is low-cost, readily available, non-hazardous, and stable; and a deposition technique to uniformly apply the dopant to Silicon-Film™ wafers. A necessary requirement is that the deposition technique be easily scaleable to even the largest area wafer, and, ideally, could be adapted to an in-line process for diffusing continuous sheets of Silicon-Film™ material, possibly directly from the sheet formation system without cooling.

Our most recent work has focused on developing specifications for a continuous system to perform the high temperature dopant drive-in process. Specifically, we determined the time-temperature (recipe) for a rapid thermal process tailored to Silicon-Film™ wafers. Using an in-house thermal model, we developed the specifications for two high temperature belt furnaces -- one based on silicon carbide (SiC) heaters and one using tungsten-halogen lamps. Specifications for the lamp-based furnace were distributed for bids by furnace vendors. Based on the response to our specifications, we have ordered a belt furnace for delivery in the first quarter of 1997. A dopant deposition system was designed for integration to this furnace. We will utilize this diffusion system to evaluate the throughput, yield and cost of the continuous emitter process.

Silicon-Film™ emitter junction diffusion has historically been performed at AstroPower as a batch-type process using large-bore diffusion tubes. The emitter diffusion process is quite simple -- 200 wafers are loaded into a quartz diffusion "boat"; the boat is slowly pushed into the center zone of the furnace; and a dopant gas -- a combination of nitrogen, oxygen, and N-type dopant -- flows through the tube for a measured period of time. The dopant source is semiconductor grade $POCl_3$, a highly corrosive liquid which produces the dopant glass phosphorus pentoxide ($P_2O_5$) at diffusion temperatures on the surface of the wafer.

The performance of a solar cell is sensitive to the emitter junction. A diffused emitter layer is characterized by surface concentration and depth. These are controlled by the diffusion process variables: diffusion dopant deposition and drive-in temperatures, time at temperature, and ambient atmosphere at temperature. The emitter characteristics are optimized by maximizing light absorption and carrier generation while minimizing series resistance losses associated with the contact metallization.

Although the junction diffusion process is simple, it is made complicated by the ever-increasing areas of the Silicon-Film™ wafers. In a batch-type tube furnace diffusion process, the deposition and drive-in times must be long enough to ensure that dopant phosglass is uniformly deposited across the wafers and throughout the length of the diffusion boat. For large-area wafers, this time is on the order of one hour, and a typical cycle, which includes the load and unload time, might be two hours. As a result, emitter diffusion of large-area solar cells is characterized as a low-throughput (100 wafers per hour) process.

When discussing tube diffusion, it is important to note that the weight and thermal mass of a loaded diffusion boat is substantial. Although the thermal mass of an individual wafer is not large, a fully-loaded boat consists of approximately 6 kg of silicon and 2 kg of quartz (for the boat). The number of wafers in a boat is constrained by the handling weight and the temperature response of the furnace to the thermal mass of the cold load as it enters the furnace. Most tube furnaces require relatively long equilibration times (on the order of tens of minutes) when subjected to large thermal transients such as temperature setpoint changes or rapid loading/unloading.

**Diffusion Process Development:**

Previously we had demonstrated a liquid N-type dopant source for silicon wafers that is low cost, non-hazardous, and stable. We had shown that typical solar cell sheet resistances, as low as 30 ohms/square, could be obtained in fairly short process times and at only moderately high temperatures, five minutes at 950°C, in a nitrogen ambient. We also developed several deposition techniques for applying the dopant to the surface of the wafers. By heating only a few coated wafers at a time in a tube furnace, we were able to perform a high-temperature drive-in that approximated the thermal "profile" of a "rapid

thermal" process. Using this approach we investigated dopant formulation and developed the time-temperature emitter response surface This laboratory-scale work involved small quantities of wafers that were fabricated into solar cells.

During the past year we focused our development efforts on one of the dopant deposition techniques. A prototype system capable of throughput rates of about 300 wafers per hour was designed and assembled. Once the dopant deposition process was validated, larger quantities of wafers, both single-crystal and Silicon-Film™, were processed through the system. The remainder of the diffusion process (the equivalent of a tube furnace "drive-in" step) was performed either in a tube furnace, as before, or in a 24-inch lamp-based infrared (IR) belt furnace, originally designed for firing thick-film inks, that was made available for this project. Since the high temperature zone in this particular furnace is only 50-cm long, the belt drive system was modified to reduce the maximum belt speed to 30 cm/min (from 120 cm/min); a typical drive-in setpoint was 4 or 5 cm/min. In spite of the limitations on speed and throughput, this belt furnace is still capable of and was used for diffusing the very large area 1800 sq-cm Silicon-Film™ wafers.

The results obtained using this furnace proved that short heat cycles adequate for producing emitter junctions could be achieved using lamp-based IR furnace technology of the type currently used for silicon solar cell manufacturing. Based on these results, an effort was initiated to develop the design and specifications for an IR furnace that would comprise the major portion of a continuous diffusion system for Silicon-Film™ wafers. The initial design enclosed a process space of drive-in temperature from 900 to 950°C and belt speed from 25 to 75 cm/min.

As part of this work, the visual quality of the diffused wafers was addressed. Adjustments to the ambient gas composition resulted in a more uniform oxide deposition, with considerably fewer macroscopic defects. This is significant in terms of final solar cell visual appearance, and in maintaining a consistent set of conditions for deglazing following diffusion.

**Continuous Diffusion System Design:**

It has been shown that rapid thermal processing (RTP) without additional high temperature "annealing" can be used to produce emitter junctions for high-efficiency solar cells, even with screen-printed metal contacts [2]. The key to the process appeared to be the relatively slow cooling temperature profile [3]. The temperature profile seen during the process is similar to that obtained from a tungsten-halogen lamp-based belt furnace operated with a "spike" power profile and a high belt speed. Screen-printed metal contacts on silicon solar cells are typically processed in tungsten-halogen lamp-based IR belt furnaces. The goal of our effort during this report period was to develop the specifications for an "RTP-like" continuous diffusion system to produce the emitter

junction of large-area Silicon-Film solar cells. We have investigated the application of lamp-based belt furnaces, as well as a SiC-based belt furnace.

Specifications for a lamp-based IR furnace were distributed for bids by several furnace vendors. These specifications were very similar to that of IR furnaces typically used for firing thick film inks used for contact metallizations, and we found that we did not need to have a custom furnace designed and built. Rather, an available furnace design was adapted and modified by adding an extended entrance to accommodate the dopant deposition system. Based on the response to our specifications, we ordered a continuous diffusion belt furnace for delivery in the first quarter of 1997. A dopant deposition system similar to that used during the process qualification trials during the beginning of this reporting period was designed for integration with this furnace. We will utilize this system to evaluate the throughput, yield and cost of the continuous emitter process.

## 15 cm Wide Silicon-Film™ Sheet Material Development

The production of AP225 solar cells from nominally 15 cm wide sheet continued in 1996. In addition to the existing wafer production machine and wide sheet development machine, a third wafer production machine was designed and assembled in 1996. That machine will be devoted to production of continuous sheet for fabrication into AP225 solar cells. Quick turn-around analysis of the sheet continues to be under development. The latest tool is a contactless lifetime measurement technique developed by Richard Ahrenkiel of NREL.

### *New Silicon-Film™ Machine*

The next generation wafer production machine, designated SF-4, was designed and built during 1996. The SF-4 machine will reduce manufacturing costs by increasing the sheet generation rate and producing higher performance material than its predecessor, SF-3.

The SF-4 wafer production machine will have the capability of producing Silicon-Film™ sheet at a rate 50% higher than the present SF-3 machine. It was designed to be capable of continuous wafer production. By redesigning the heater element configuration, SF-4 will have the capability of producing wafers with better crystal morphology than exist in present material, which should lead to better performance. The new production machine has been outfitted with distributive control, data-logging, and precise monitoring devices to improve machine yields and reduce the manufacturing costs of the Silicon-Film™ wafer formation process.

### *Minority Carrier Lifetime Measurement*

During the previous reporting period we investigated lifetime characterization techniques based on both transient and quasi-steady-state measurements of the photoconductance decay of silicon wafers. Both approaches have the advantage of a contactless measurement with little or no sample preparation. The transient decay system is based on a microwave (10 GHz) source and a pulsed laser diode operating at 904 nm. The quasi-steady state system is based on a low-frequency RF (10 MHz) source and a xenon flashlamp. Although both techniques provide adequate measurement for single-crystal silicon, neither approach was sufficiently sensitive to measure the lower lifetimes of Silicon-Film™ material.

During this reporting period we have assembled and have begun to use a transient photoconductance decay lifetime measurement system that is based on a high-frequency RF (400-500 MHz) source and a Q-switched YAG laser. We have verified the technique by re-producing transient decay measurements that were made by Dr. Richard Ahrenkiel using his instrument at NREL. Although the minority-carrier lifetime of Silicon-Film™ material is significantly shorter than single-crystal silicon, this technique has been shown to have sufficient sensitivity to resolve variations minority-carrier lifetime from sample to sample. Future work will be focused on reducing the sample acquisition and analysis time, and on further improvements in the resolution of the instrument.

Several Silicon-Film wafer samples were forwarded to Dr. Richard Ahrenkiel at NREL for measurement using RF-PCD [4]. Although initial measurements using this technique seemed to yield results that were dominated by trapping effects, further efforts to measure and analyze wafers showed that this technique was capable of resolving differences in minority-carrier lifetime between samples. Based on these positive results, an effort was begun to obtain an agreement with NREL to allow AstroPower to utilize the technique.

Once this agreement was approved, AstroPower immediately began to design and assemble an RF-PCD system to be based on the instrument at NREL. However, unlike the NREL system, the AstroPower instrument is designed for use in an open, industrial environment. Although it will be initially used for single-spot measurements, the instrument at AstroPower is capable of future development into a scanning system. Ultimately we hope to use this technique as an in-line, real-time monitor of sheet growth quality.

First measurements with the system at AstroPower were obtained in October after on-site instruction by Dr. Ahrenkiel. The data is presently analyzed using a spreadsheet program and assuming that the minority-carrier lifetime is characterized by a simple exponential decay time constant. Figure 6 shows the RF-PCD curve for a recent Silicon-Film™ sample. A diffusion length of 58 microns was independently measured by spectral response analysis, which correlates well with a lifetime of 4.3 microseconds.

Measurements on single crystal silicon have also been successfully correlated to data from both spectral response and a quasi-steady state RFPCD measurement.

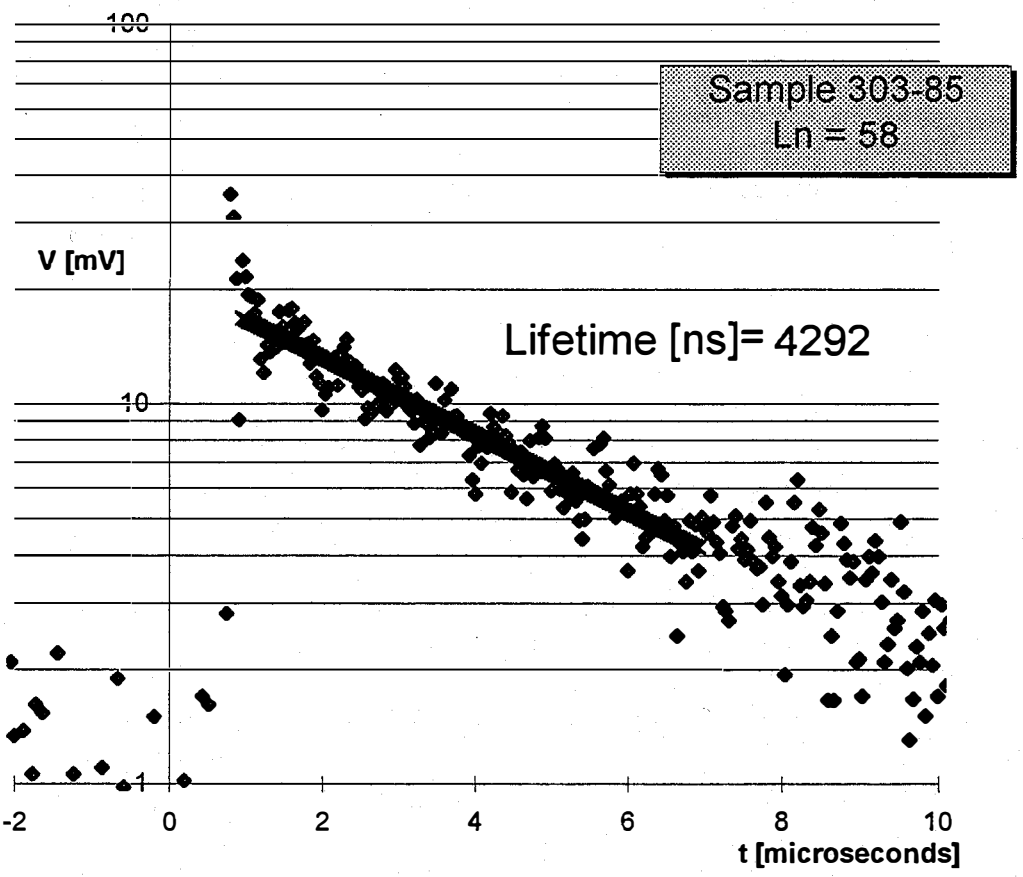



Figure 6. **A sample of the data measured on the new RFPCD equipment.**

## 30 cm Wide Silicon-Film™ Sheet Production

Silicon-Film™ sheets up to 38 cm wide have been produced in the development Silicon-Film™ machine. During 1996, the task of fabricating large-area solar cells from these very large planks was undertaken. A number of improvements were required in solar cell processing to accommodate such large devices. Optimization of device processing is not yet complete. Most notably, the correct conditions for firing of the screen printed contacts has not yet been determined. This process has been known to be very sensitive to different wafer sizes. The present process does not use a gettering step. This process step will be developed in 1997.

The solar cell fabrication process presently in use for AP1800 solar cells follows;

- Remove the front surface of the wafer using normal dry sandblast technique.
- Chemically clean with a NaOH wet etch and DI water rinse.
- Due to the large size of the AP1800 wafers and size limitations of our conventional diffusion furnaces we are utilizing a belt diffusion process.
- HF acid strip and DI water rinse.
- Apply Ag / Al ink to the back surface of the wafers and dry.
- Apply Ag ink by screen printing to the front surface of the wafers.
- Fire the wafers (using our standard AP225 belt furnace for contact firing)
- Mechanically edge isolate with a commercially available diamond impregnated pad.
- AR coat by spraying using a HVLP spray and a custom built hot plate for thermal uniformity over the large wafer area.

The first solar cell fabrication sequence has been completed. A special test jig has been fabricated that allows cells to be tested prior to lamination (cells are tabbed). This jig has been sent to NREL with a representative AP1800 attached. This will act as calibration sequence that will allow further testing and optimization of the process.

## Conclusion

The Silicon-Film™ process is on an accelerated path to large-scale manufacturing. A key element in that development is optimizing the specific geometry of both the Silicon-Film™ sheet and the resulting solar cell. That decision has been influenced by cost factors, engineering concerns, and marketing issues. The geometry investigation has focused first on sheet nominally 15 cm wide. This sheet generated solar cells with areas of 240 $cm^2$ and 675 $cm^2$. Most recently a new sheet fabrication machine was constructed that produces Silicon-Film™ with a width in excess of 30 cm. The results of testing have indicated that there is no limit to the width of sheet generated by this process. The new wide material has led to prototype solar cells with areas of 300, 400 and 1800 $cm^2$. Significant advances in solar cell processing have been developed in support of fabricating large-area devices, including uniform emitter diffusion and anti-reflection coatings.

## References

[1] PVUSA Project Team, "1995 PVUSA Progress Report", Pacific Gas and Electric Company, San Ramon, CA, Brian Farmer Project Manager, March 1996.

[2] P. , J. Mejia, K. Tate, S. Karma, A. Rohatgi, S. Narayanan, and R. Singh, "High-efficiency silicon solar cells by low-cost rapid thermal processing, screen printing, and plasma-enhanced chemical vapor deposition", *Proc. 25th IEEE Photovoltaic Specialists Conference,* Washington, DC, 1996, pg. 421-424.

[3] P. Doshi, A. Rohatgi, M. Ropp, Z. Chen, D. Ruby, and D.L. Meier, "Rapid thermal processing of high-efficiency silicon solar cells with controlled in-situ annealing", *Proc. 24th IEEE Photovoltaic Specialists Conference,* Hawaii, 1994, pg. 1299-1302.

[4] R.K. Ahrenkiel and D.H. Levi, "Minority-carrier lifetime studies of silicon spheres", *Proc. IEEE First World Conference on Photovoltaic Energy Conversion* (Hawaii), 1994, pg. 1368.

# REPORT DOCUMENTATION PAGE

*Form Approved*
*OMB NO. 0704-0188*



| 1. AGENCY USE ONLY (Leave blank) | 2. REPORT DATE | 3. REPORT TYPE AND DATES COVERED |
|---|---|---|
| | March 1997 | Phase II Technical Report, January 1996 - December 1996 |

**4. TITLE AND SUBTITLE**

Large-Area Silicon-Film™ Panels and Solar Cells; Phase II Technical Report, January 1996 - December 1996

**5. FUNDING NUMBERS**

C: ZAF-5-14271-3
TA: PV705101

**6. AUTHOR(S)**

J.A. Rand, A.M. Barnett, J.C. Checchi, J.S. Culik, S.R. Collins, D.H. Ford, R.B. Hall, E.L. Jackson, and C.L. Kendall

**7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)**

AstroPower Inc.
Solar Park
Newark, DE 19716-2000

**8. PERFORMING ORGANIZATION REPORT NUMBER**

**9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)**

National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

**10. SPONSORING/MONITORING AGENCY REPORT NUMBER**

SR-520-22740

DE97000232

**11. SUPPLEMENTARY NOTES**

NREL Technical Monitor: R.L. Mitchell

**12a. DISTRIBUTION/AVAILABILITY STATEMENT**

**12b. DISTRIBUTION CODE**

UC-1280

**13. ABSTRACT** ***(Maximum 200 words)***

The Silicon-Film™ process is on an accelerated path to large-scale manufacturing. A key element in that development is optimizing the specific geometry of both the Silicon-Film™ sheet and the resulting solar cell. That decision has been influenced by cost factors, engineering concerns, and marketing issues. The geometry investigation has focused first on sheet nominally 15 cm wide. This sheet generated solar cells with areas of 240 $cm^2$ and 675 $cm^2$. Most recently, a new sheet fabrication machine was constructed that produces Silicon-Film™ with a width in excess of 30 cm. Test results have indicated that there is no limit to the width of sheet generated by this process. The new wide material has led to prototype solar cells with areas of 300, 400, and 1800 $cm^2$. Significant advances in solar-cell processing have been developed in support of fabricating large-area devices, including uniform emitter diffusion and anti-reflection coatings.

**14. SUBJECT TERMS**

photovoltaics ; Silicon-Film™ ; large-area panels ; large-area solar cells

**15. NUMBER OF PAGES**
22

**16. PRICE CODE**

| 17. SECURITY CLASSIFICATION OF REPORT | 18. SECURITY CLASSIFICATION OF THIS PAGE | 19. SECURITY CLASSIFICATION OF ABSTRACT | 20. LIMITATION OF ABSTRACT |
|---|---|---|---|
| Unclassified | Unclassified | Unclassified | UL |