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Large-Area Silicon-Film™ Panels and Solar Cells

Final Technical Report July 1995–March 1998

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Executive Summary

The Silicon-Film™ process is on an accelerated path to large-scale manufacturing. The present manufacturing effort is based on solar cells with an area of 240 cm^2 (the solar cell is referred to as the AP225). Efficiencies in excess of 12% have been demonstrated for these large area cells. Smaller, laboratory devices have demonstrated an efficiency of 16.6%.

The Silicon-Film™ process generates a continuous silicon sheet of variable width. This three year program was focused on manufacturing and processing this sheet material. The investigation into sheet width has resulted in the construction of a new, wider, Silicon-Film™ machine. This equipment has demonstrated that Silicon-Film™ sheet material can be fabricated at a width greater than 30 cm. At this point, there is no known limit to the width capabilities of the Silicon-Film™ sheet growth process. This new machine capability has allowed us to evaluate a number of different solar cell sizes. Solar cells with areas of 240 cm^2, 300 cm^2, 400 cm^2, 675 cm^2, 900 cm^2, and 1800 cm^2 have been fabricated. An efficiency of 11.6% was measured for a solar cell with an area of 675 cm^2.

Silicon-Film™ solar cells continue to demonstrate long term stability as shown by the performance of the PVUSA array installed in Davis, California in 1994. In addition to validating the stability of this technology, the PVUSA Silicon-Film™ array has demonstrated very good performance in terms of energy delivery. Published performance information for 1995 and 1996[1] show that the AstroPower Silicon-Film™ array produced more energy (AC kWhr) per rated watt of array capacity than any of the other flat panel EMT arrays, which include mono-crystalline and polycrystalline silicon arrays, as well as other thin film technologies.

A 130 kW array was completed for Niagara Mohawk Power Company. The array utilized a new panel product based on the AP225 solar cell. The new product was successful in reducing manufacturing and installation costs of the array. In addition to the new panel product, a new junction box was developed that has lowered costs by a factor of two.

The quality of Silicon-Film™ material, and the maturity of the solar cell processing have progressed during this program as reflected by increased solar cell efficiencies. A laboratory optimization effort achieved an efficiency of 16.6% (NREL measurement) on a 1.0 cm^2 solar cell. The contract goal for this device was an efficiency of 15.6%. Performance on production-sized solar cells (240 cm^2) has reached a verified efficiency of 12.2% (NREL measurement).

Significant progress was also made in the area of processing large area solar cells and planks. New, continuous processing sequences were developed for gettering, junction formation, and antireflection coating. New equipment was developed in each case to allow for the processing of large area devices. The new processes are being transferred from the laboratory to production and will result in lower solar cell fabrication costs. Other improvements in processing related to this contract include a 67% reduction in chemical costs required in the wafer surface preparation process.

Introduction

This program had the following general objectives:

1. Extend continuous processing from sheet fabrication into the solar cell fabrication steps,
2. Reduce the cost per watt of Silicon-Film™ products by increasing efficiency and reducing manufacturing costs,
3. Develop new, large area solar cells,
4. Develop new utility-scale panel products.

A series of specific tasks were performed over three phases of work, each phase was approximately one year in length. The specific tasks were as follows:

Task 1. Develop New Panel Products and Processes
Task 2. Improve Solar Cell Performance
Task 3. Reduce Cost of the Critical Baseline Solar Cell Processes
Task 4. Develop Solar Cell Processes Based on 31 cm Wide Sheet Material
Task 5. Reduce Manufacturing Costs of the Production Sheet Process
Task 6. Produce 31 cm Wide Sheet Product.

This report will detail substantial improvements in each of the task areas above. A number of new products were developed, including a 130 kW array built using a new panel design. Improvements in laboratory-scale solar cell processing resulted in an confirmed efficiency of 16.6%. A new Silicon-Film™ production sheet machine was built which increased throughput by 70%. Three solar cell fabrication processes were converted from low throughput batch processes to high throughput, continuous, belt processes. These new processes are capable of processing sheet over 31 cm in width. Finally, a new Silicon-Film™ sheet machine was built that demonstrated a sheet width of 38 cm. This tool enabled AstroPower to demonstrate a wide range of solar cell sizes, many of which have generated considerable market interest.

Figure 1 illustrates the propagation of the continuous sheet fabrication process down through the process stream. It is envisioned that all solar cell processes could be carried out while the silicon substrate is in sheet form. The solar cell can then be sized at the last step, just before incorporation into a large panel or smaller module. The achievement of continuous processing has led to lower cost per watt by reducing labor, as well as improving control, quality, and yield. Under this program three process steps were made continuous. These processes are gettering, diffusion of the emitter layer, and large-area antireflection coating.

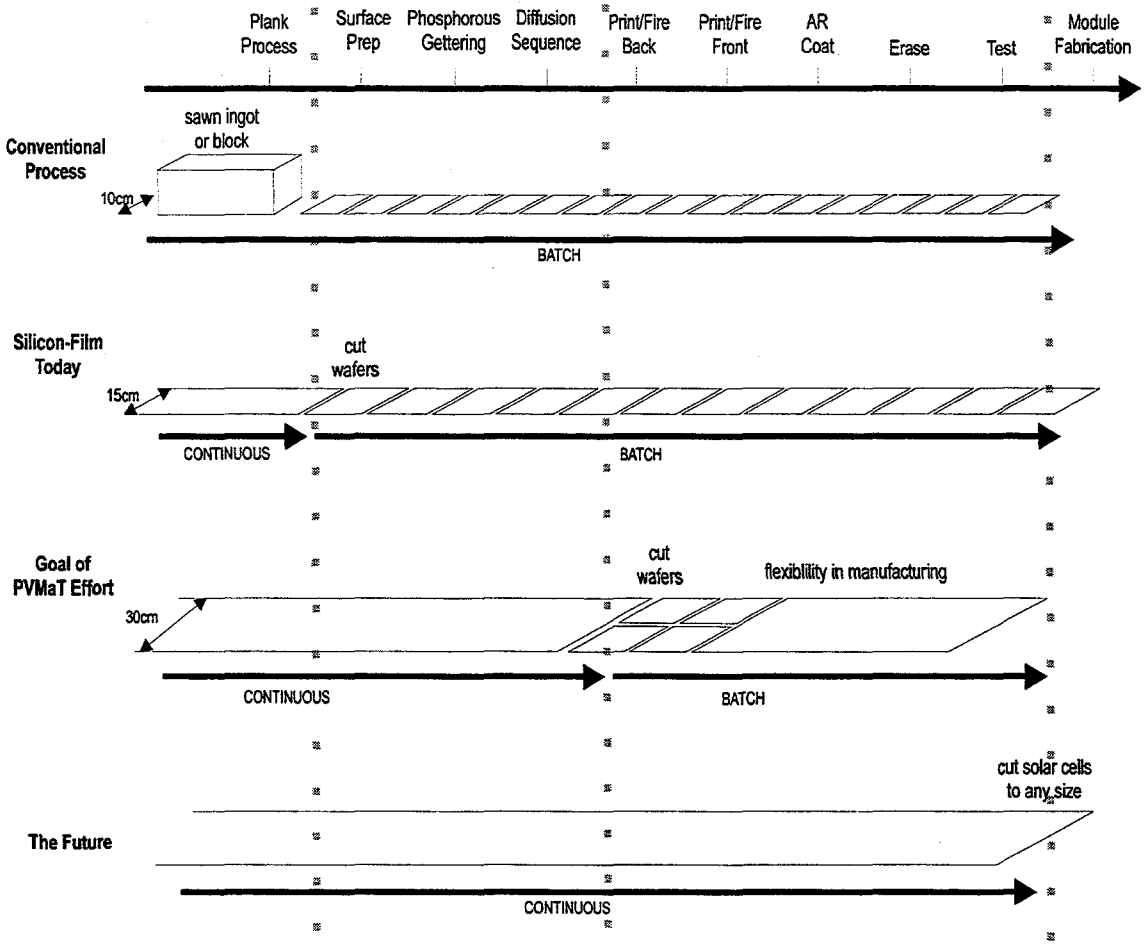


Figure 1. The history and future for in-line, continuous manufacturing technologies at AstroPower.

The flexibility of the fully developed Silicon-Film™ solar cell product is illustrated in Figure 2. The solar cell process will operate continuously and fabricate processed material that will result in solar cell sizes up to 30 cm x 60 cm. The actual size of the solar cells and panels will depend on the specific customer applications. As indicated, the market segments addressed include a 384 watt utility-scale panel, a 100 watt commodity power module, and a broad range of specialty modules. A summary of the different solar cell sizes and results to date are shown in Table 1.

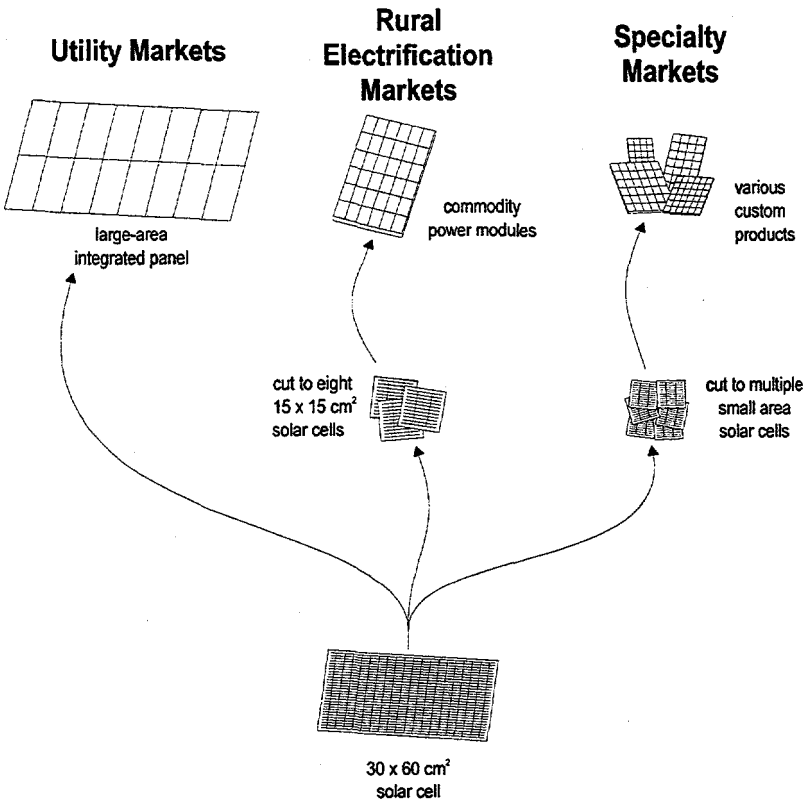


Figure 2. Flexibility of a 30 cm x 60 cm solar cell in meeting several different PV markets.

TABLE 1. Summary of device data on different size solar cells.

Product	Area	Power	Efficiency	Note
Laboratory Solar Cells	0.976 cm^2	16.2 mW	16.6%	(1)
AP-225 Solar Cell	240 cm^2	2.93 W	12.2%	(1)
AP-300 Solar Cell	311 cm^2	3.48 W	11.1%	(2)
AP-400 Solar Cell	410 cm^2	3.89	9.5%	(1)
AP-675 Solar Cell	676 cm^2	7.87 W	11.6%	(1)

(1) NREL test , (2) AstroPower test

New Panel Products

AstroPower has completed the design and testing of a new 320 W photovoltaic panel. The panel utilizes Silicon-Film™ solar cells in large-area frameless laminates. The laminates are directly attached to a structural steel member.

The new panel was used at an installation near Albany, NY for Niagara Mohawk Power Company. A photograph of the installation is shown in Figure 3. The array consists of 434 panels. Panel delivery was completed September 1, 1997, and panel installation was complete by October, 1997. Niagara Mohawk cost shared the panel development effort. Final array testing is waiting on the arrival of the inverter.

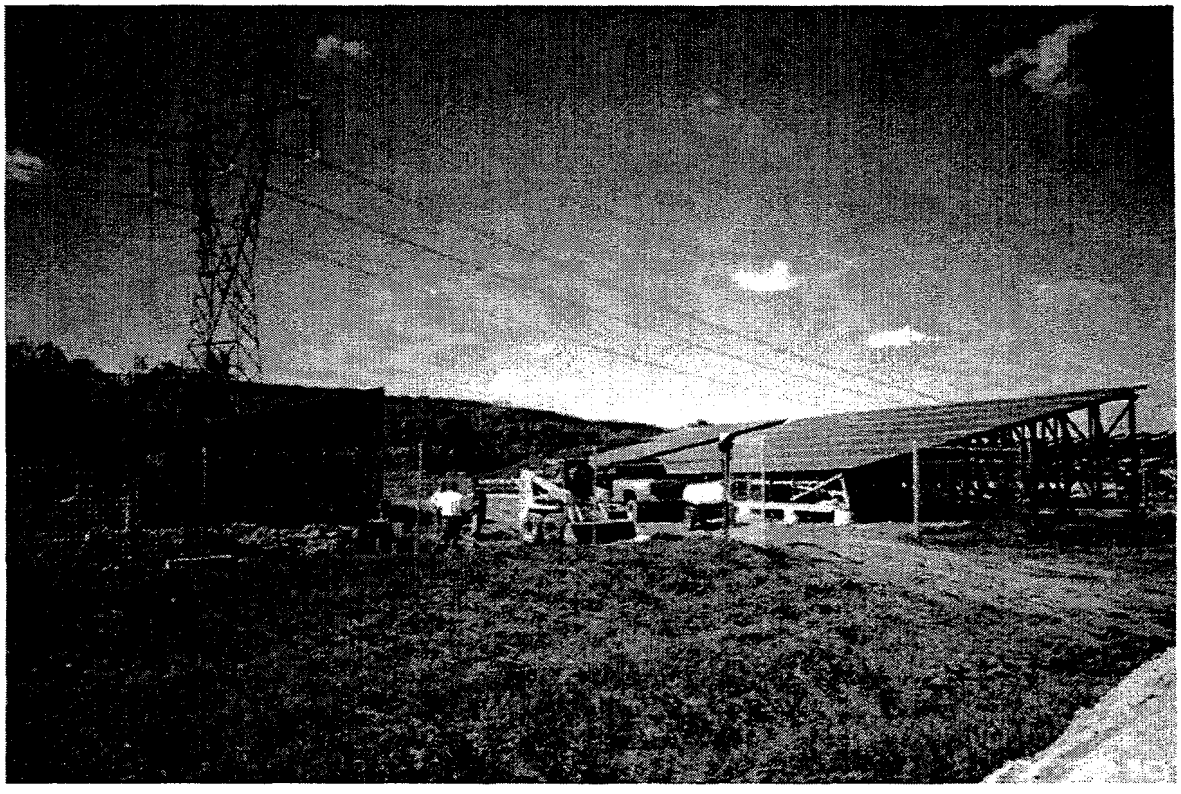


Figure 3. Photograph of the installation for Niagara Mohawk Power

Design

The panel design was developed with assistance of Jefferson Shingleton, P.E., who has experience in the mechanical design and fabrication of a number of other photovoltaic installations. The design involved a Product Preliminary Analysis of a photovoltaic panel. A loading analysis was performed to identify candidate product structural design loading conditions.

Environmental Exposure and Mechanical Loading Test

Structural issues for the new 320 W panel were investigated in detail. Test structures were fabricated for environmental exposure testing, and a number of testing sequences were performed. Different attachment methods between the galvanized steel support rails and the Tedlar back sheet of the laminate were evaluated. Attachment methods used either double coated acrylic foam tape, or a silicone adhesive, or both.

The most rigorous test performed began with 20 cycles of 10 hours at 85°C (85% relative humidity) and 20 minutes at -40°C. The test structure was then subjected to a mechanical-loading test. That test involved subjecting the panel to a static load of 30 pounds per square foot for a period of 30 minutes. The test structure was 10 square feet, requiring 300 pounds. Early testing resulted in failure at the foam/adhesive interface within the tape, and failure at the silicone adhesive/steel interface. After some experimentation, a combination of specialized tape and silicone products were found that survives the humidity/freeze cycling. With the revised adhesive, the test structure successfully completed the mechanical loading test.

Module Developments

Several improvements to the module design were made during this program. Low-cost bypass diodes were qualified for use. A new junction box for Silicon-Film modules was designed. With the exception of the box itself, all of the remaining components associated with the junction box will be literally "off-the-shelf". We project that this new design will reduce the cost of the box and its associated components by up to a factor of two. Furthermore, this new box will be capable of accommodating the higher current bypass diodes that will be necessary as the cell area increases.

During Phase II of this program we significantly reduced the costs and increased the reliability associated with the module bypass diodes. We tested and successfully qualified a low-cost silicon Schottky diode with an 8-Amp current rating. These diodes are used in large quantity in switch-mode power supplies, so their availability has been very good. Previously we have used an expensive, custom-manufactured germanium part. We have identified silicon Schottky diodes that have even larger current ratings that can be used as the size of the Silicon-Film™ solar cell and the current increase.

The present UL-approved Silicon-Film™ panel design incorporates a commercially-available junction box (J-box) that requires a custom printed circuit (PC) card to support the terminal block and bypass diodes. The number of components and the total cost of the box are high. The new box design eliminates the expensive printed circuit card and terminal block which are presently used and is based instead on low-cost, readily available terminal blocks that are already UL-listed for operation at 600 Volts. Some of the features of the new box design are: significantly increased volume to improve wiring ease, four 20 mm knockouts for conduit wiring, spare terminal to reduce

external wiring, wire/cable strain relief, large Phillips/slotted screws with wire clamps, optional o-ring cover seal, and a tethered cover.

UL testing of the new J-Box is scheduled for Summer 1998. The new box will enter production by the third quarter of 1998.

Solar Cell Performance

To establish a benchmark for Silicon-Film™ material quality, "high performance" solar cells are routinely fabricated. Both 1.0 cm^2 and 240 cm^2 devices are fabricated. Advanced processing techniques, such as passivation and evaporated contacts are used. This exercise is designed to provide direction to our production processing development, especially in the areas of diffusion and gettering. The general process for high performance solar cells is as follows;

1. Chemical Polish Etch
2. RCA Clean
3. Al deposition
4. Diffusion/Getter Heat Treatment
5. Aluminum Etch
6. Chemical Polish Etch (remove gettered impurities)
7. RCA Clean
8. Diffusion
9. Passivation Oxide
10. Evaporated Contacts (Ti/Pd/Ag)
11. Double Layer AR coating.

1.0 cm^2 Solar Cell Effort

The process sequence for high efficiency laboratory size solar cells follows the general process described above. Other processes investigated include pre-gettering preparation, phosphorus/aluminum gettering, removal of diffused/alloyed layers, and RF hydrogenation. Because of the synergistic and complementary effects of impurity diffusion and segregation during phosphorus and aluminum gettering, a four-hour gettering step using simultaneous phosphorus diffusion and aluminum alloying was used to increase the effective minority carrier diffusion length in Silicon-Film™ materials. Passivation of bulk structural defects was accomplished using hydrogen treatments. This treatment was found to be additive to the gettering step. An indication of the improvement was also found by EBIC mapping that showed significantly suppressed grain boundary activities. Effective carrier diffusion lengths in finished solar cells can exceed 150 μm after these material quality enhancement steps.

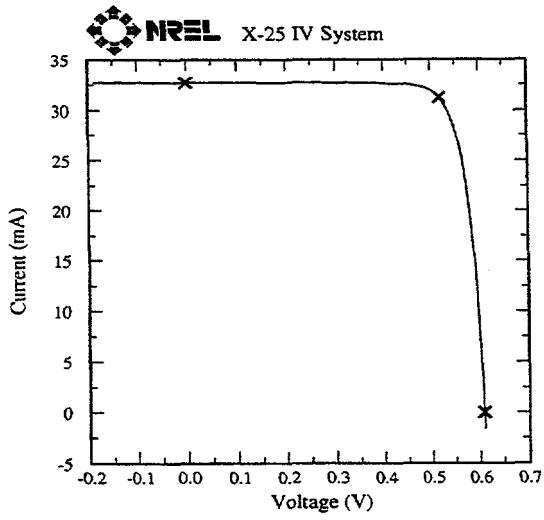
The effectiveness of emitter surface passivation impacts the utilization of the blue part of the solar spectrum in high efficiency silicon solar cells. In order to avoid the depassivation of hydrogenated materials from a high temperature oxidation process, a low-temperature emitter surface passivation was implemented using a PECVD (Plasma Enhanced Chemical Vapor Deposition) oxide layer. When RF hydrogenation is used, the surface damage it generates can be repaired by an emitter etchback using a weak HF/HNO_3 based solution. Doping levels at the emitter surface was controlled by introducing an oxidation step immediately following the phosphorus predeposition and drive-in steps. Spectral response measurements revealed that solar cells with passivated emitter surfaces exhibit an internal quantum efficiency (IQE) well above 80% at 400nm wavelength.

Figure 4 shows light I-V data for a one square centimeter solar cell with an efficiency of 16.6%. As a comparison, Table 2 lists the solar cell parameters determined from illuminated I-V data for the 16.6% cell and the previous 14.6% cell. Both results were achieved during this program. The increase in solar cell efficiency came mostly from an increase in short-circuit current density. This increase was attributed to an improved optical response in the blue part of the solar spectrum, reduction in grid obscuration, a re-optimized $MgF_2/ZnS/SiO_2$ AR coating, and improved minority carrier diffusion length. Improvements in voltage and fill factor are attributed to the improved top surface passivation, edge passivation and a reduction in the second diode component. QE data in Figure 5 clearly indicate a significant increase in short-wavelength response resulting from the recent optimization of emitter surface passivation. Internal quantum efficiency at 400 nm reaches 90%, approaching that of the best emitter surface passivation achieved by high temperature oxidation.

TABLE 2.
I-V data of Silicon-Film™ solar cells measured at
the National Renewable Energy Laboratories (NREL).
Cell A is new record and Cell B is the previous record.

Cell ID	η *(%)*	V_{OC} *(mV)*	J_{SC} *(mA/cm²)*	*FF (%)*
A	16.6	608.0	33.53	81.5
B	14.6	596.6	30.14	81.0

A detailed analysis was also made using PC1D to identify areas for further improvements in solar cell performance. Model calculations indicate that an efficiency of 18% is achievable when further optimizations in antireflection coating and minority carrier diffusion length can be made.



V_{oc} = 0.6080 V	V_{max} = 0.5194 V
I_{sc} = 32.70 mA	I_{max} = 31.20 mA
J_{sc} = 33.53 mAcm^{-2}	P_{max} = 16.20 mW
Fill Factor = 81.49 %	Efficiency = 16.6 %

Figure 4. Light I-V data of a 16.6% efficient Silicon-Film™ polycrystalline solar cell tested at NREL under AM1.5G spectrum.

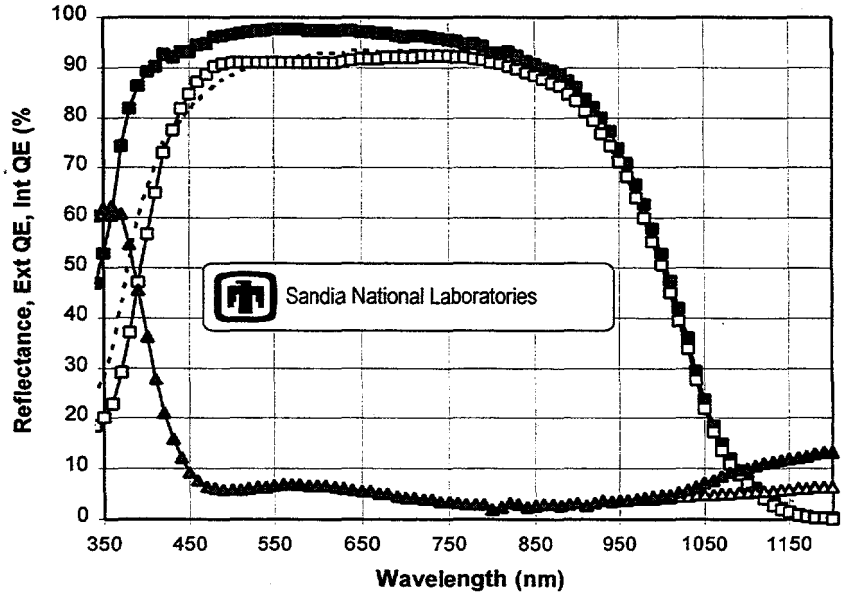


Figure 5. Internal quantum efficiency (IQE), external quantum efficiency (EQE,) and reflectance as a function of wavelength measured on the 16.6% efficient Silicon-Film™ solar cell. IQE of an earlier record cell (14.6%) is shown by a dashed line.

In summary, the major improvements in the processing of 1cm^2 solar cells under this program have been:

- Simultaneous gettering of impurities by extended phosphorus diffusion and aluminum alloying. That gettering, combined with passivation of crystal defects by RF hydrogenation has lead to minority carrier diffusion lengths in the range of 150-200 μm.

- The combination of a low temperature surface passivation and an optimized emitter junction formation led to an internal quantum efficiency greater than 80% at a wavelength of 400 nm, further increasing the short-circuit current.

- Other optimizations of device performance include reduced grid shading loss, optimized triple-layer AR coating system, and benefits from forming gas annealing.

AP225 Solar Cell Analysis and Modeling

An analysis was performed to understand the efficiency loss mechanisms in the AP225 solar cell based on measurements of present production cells. Device and material parameters were obtained from analysis of measured I-V and spectral response data. Baseline modeling used these parameters as inputs to the PC1D software.

Figure 6 indicates the fractions of each loss component that limit the efficiency of an AP225 solar cell. The 22% "Un-encap. loss" reflects the difference between testing encapsulated and un-encapsulated cells for which the AR coating has been optimized for encapsulated performance (the converse of "encapsulation gain"). Reflectance measurements on both bare and encapsulated solar cells indicate that there is room for improvement in the blue region. This can be done by reducing the *nd* product (index of refraction times thickness) of the TiO_2 coating. For a passivated emitter, this measure is particularly important. An increase in fill factor requires improvements in the second diode component (J_{02}), series resistance (R_s) and shunt resistance (R_{sh}). The biggest potential gain is in diffusion length, which requires substantial efforts in both material growth and post-growth processing. Diffusion length loss, grid shading loss and a large second diode component are shown to be the three major performance-limiting factors. Modeling also indicates that, to achieve a 15% efficiency, an additional increase in minority carrier diffusion length (i.e., 120 μm) and emitter surface passivation will be required.

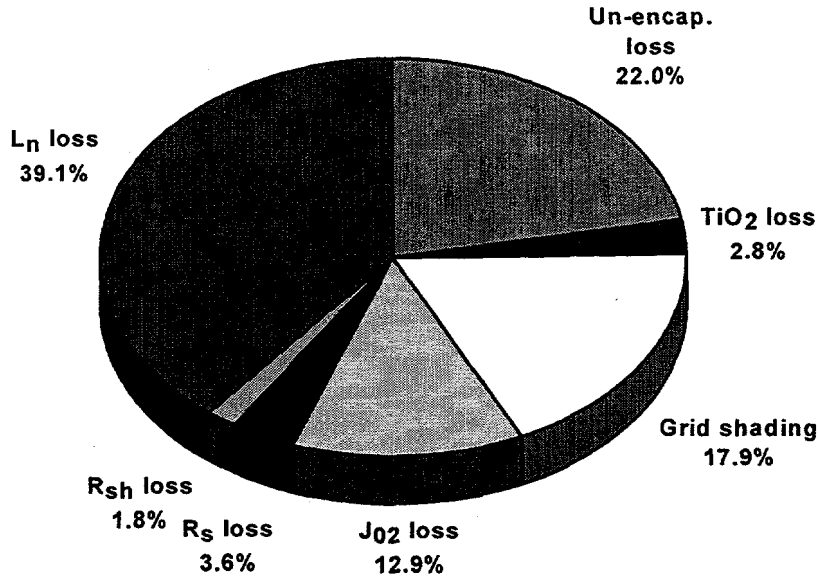


Figure 6. Fraction of Each Loss Component

Post-growth Material Improvements and Device Optimization

Like other multicrystalline and polycrystalline silicon materials, the steps of post-growth material quality enhancement are integral parts of high performance Silicon-Film™ solar cell fabrication. In this work gettering techniques were used to move bulk lifetime-limiting impurities from the active device region to gettering sites at the surface of the wafer. These techniques involve extended heat treatments in the presence of aluminum and phosphorus. The passivation of bulk crystal defects is accomplished with hydrogen treatment (forming gas anneal and hydrogen plasma). These techniques have been integrated at different stages in the cell processing sequence. Typical starting minority carrier diffusion lengths in Silicon-Film™ sheet materials are in the range of 20-30 μm. The diffusion length of finished solar cells ranges from 50 to 200 μm. Some devices exhibit diffusion lengths close to 300 μm.

This program included a detailed examination of diffusion lengths in as-grown, phosphorus-diffused and anneal-treated Silicon-Film™ materials. Annealing was found to dominate the increase in L_n during a production diffusion process. A series of annealing optimization experiments were performed. Results showed that an optimized annealing step not only improves diffusion lengths but also increases material response to P-diffusion and Al-treatment. New understanding obtained from these activities has provided an opportunity to begin the development of a manufacturing-compatible procedure that would lead to long diffusion lengths in Silicon-Film™ production solar cells.

A simplified gettering process that utilized both phosphorus and aluminum was evaluated. This procedure combines annealing and gettering in one thermal step. Such a process would reduce overall processing time. The heat treatment was carried out at 900°C for various durations. Materials from two different growth runs were included. Figure 7 indicates the measured diffusion length evolving along with the gettering time. It can be seen that after a four-hour getter the initial diffusion length is almost doubled. As gettering time continues, diffusion lengths of one material continue to increase while the diffusion lengths of the other material tended to saturate.

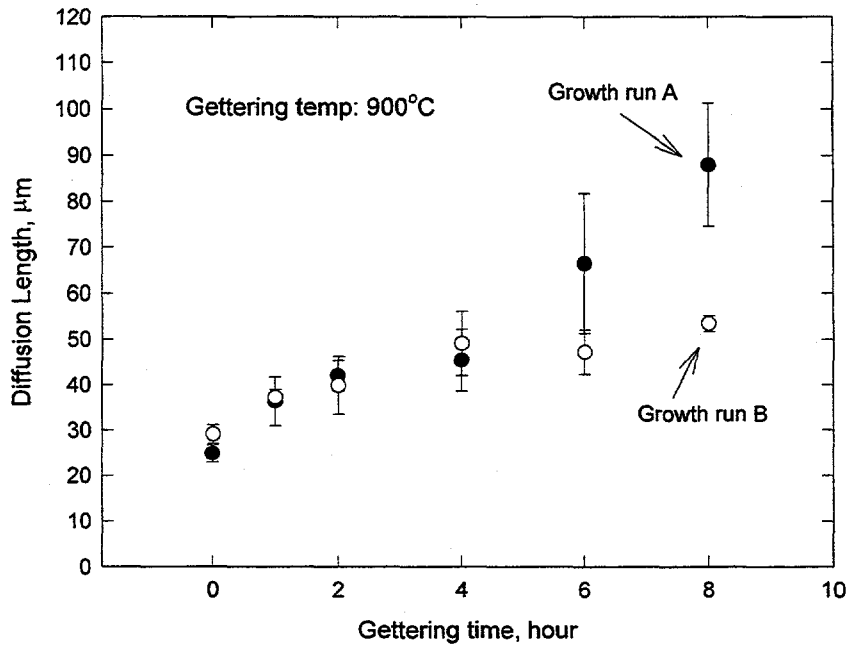


Figure 7. Minority carrier diffusion lengths as a function of phosphorus gettering time.

AP225 Field Performance

AstroPower has installed a 17 kW AP-225 array as part of the PVUSA Emerging Technologies (EMT) program. This array has been operating without fault or significant performance degradation since installation in November, 1994. A comparison of the energy produced by all the EMT arrays in 1995 and 1996 is displayed in Figure 8. The Silicon-Film™ array has demonstrated strong energy production since its installation.

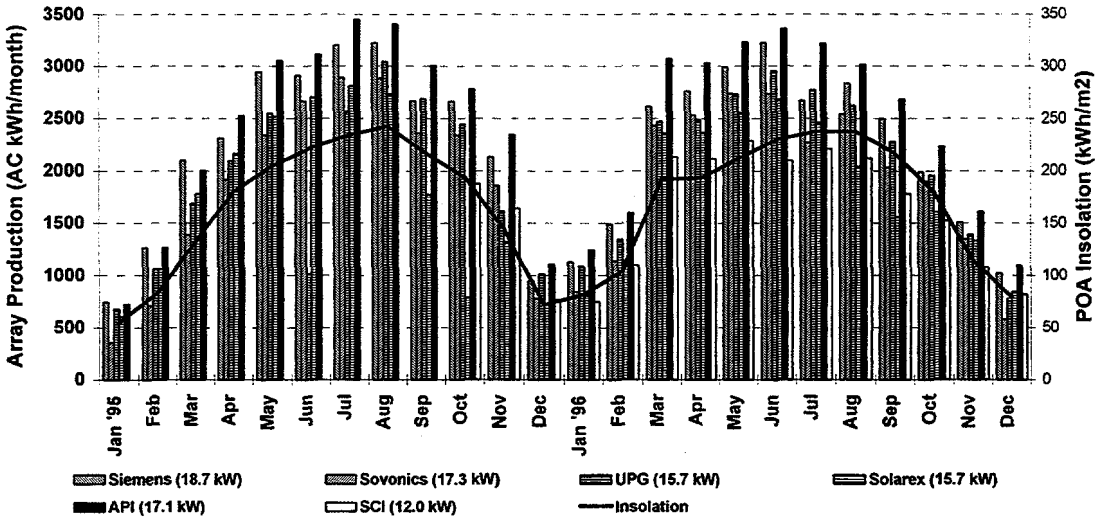


Fig. 8. Summary of the PVUSA EMT array energy production for 1995 and 1996 [1].

Solar Cell Process Development

Surface Preparation

Production-scale surface preparation before diffusion of AP225 solar cells includes dry abrasive blasting followed by a series of wet chemical etches, cleaning solutions, and rinses. The etching and cleaning solutions include baths of sodium hydroxide, hydrochloric acid, and hydrofluoric acid with extended de-ionized cascading rinses in between. The process is batch mode with 50 wafers in upright cassettes in each batch.

Investigations were conducted in the following areas:

i. mechanical yield and surface damage associated with dry blasting,

ii. throughput and manual operation of the wet-etch process.

The secondary problems associated with manual operation include the potential hazard of operator exposure to chemicals, high labor costs, and inconsistent solar cell performance.

The results of the above investigations are summarized in the following sections.

Dry Abrasive Blasting Alternatives

High pressure water jetting was thoroughly investigated as an alternative to our present dry blasting technique. The present dry-blast technique removes the top four micrometers of the as-grown sheet. However, the resulting damage to the underlying silicon is substantial, requiring chemical removal of the damaged silicon. Although the high pressure water jetting process proved to be a cleaner method of surface removal, chemical removal of the damaged silicon was still necessary. In addition, mechanical yields due to the high pressure water jet were of concern and significant engineering development was considered necessary. Modifications in the surface cleaning process, described below, eliminated the necessity to choose a dry-blast alternative.

Surface Cleaning Chemicals

Sodium hydroxide is the main component in AstroPower's wet-chemical surface preparation processing line. It acts both as a degreaser and as a silicon etch to remove surface damage. Our standard surface preparation process called for two separate sodium hydroxide etching steps: (i) pre-getter and (ii) pre-junction diffusion. During this project we were able to eliminate the pre-getter etch step with no significant change in solar cell performance. One important improvement was noted in grid line width. Sodium hydroxide acts as an anisotropic etch on polycrystalline silicon; the longer the surface is exposed to sodium hydroxide solution the rougher the surface becomes. Due to the elimination of the first etch step, gridline widths could be reduced by 26%. The reduced surface texturing allowed us to successfully minimize necking on our narrower gridline screen print pattern. This became a significant advantage in achieving consistent solar cell performance.

Surface Preparation Equipment

Cassetteless Wafer Surface Etching

Previous attempts to automate silicon wafer surface etch processes have relied upon cassette-based systems to hold and to transport wafers through the wet processes. Our goal under this program was to eliminate cassette handling, to reduce material consumption, to reduce the machine complexity and cost, and to increase operator safety by reducing the amount of caustic solution and isolating the process from the operator. During Phase II we identified and successfully tested available belt chemical processing equipment that might be adapted for Silicon-Film™ wafer processing. This equipment is typically used to clean printed circuit boards using organic solvents. Unfortunately this specialized equipment is no longer produced by the manufacturer. Since the trend in the PCB industry is to eliminate VOCs and processes using them, we expect that PC board cleaning equipment of this type will become increasingly rare.

During Phase III of the program we investigated a new concept for a continuous process to perform chemical surface etching on Silicon-Film™ wafers. The process uses the same hydroxide solution, but applies it only to the top surface of the Silicon-Film wafer. Individual wafers are serially processed in a fashion that is similar to belt firing furnaces. This approach does not require any cassettes, and is fully scaleable to the largest area wafer. A small quantity of Silicon-Film™ wafers was etched to demonstrate the concept. These wafers were processed into solar cells along with control wafers. Solar cells processed by this technique were statistically identical to those processed using the standard, cassette-based etching equipment.

Continuous Wet Chemical Processing Equipment for Large Area Wafers

The as-grown layer on Silicon-Film™ wafers is removed prior to gettering or surface etching using a system that was developed at AstroPower. Once the layer is removed, the wafers are rinsed and dried. The throughput, both rate and area, of this "dippy dunk" system is very limited. Wafers must be loaded into plastic cassettes to be handled by any of this equipment. Larger-area wafers require bigger cassettes, and planks must be cut so that the smaller parts will fit into the rinse tank and the drier.

During Phase III of this program a wet chemical processing system capable of handling wafers without cassettes was identified. We tested a commercially available rinser-drier system using Silicon-Film™ wafers. A series of tests was performed by increasing the transport rate from an initial speed of 30 inch/min. At that speed the wafers were clean and dry. At 60 inch/min the wafers were clean, but had a small amount of moisture at the trailing edges that quickly evaporated. There was no problem with handling the wafers, and no breakage whatsoever. Since the system is designed as an in-line unit, large-area wafers or planks up to 30-inches wide can be processed using the same system.

This process equipment also has the potential for providing additional components that would be useful for cassetteless, continuous Silicon-Film™ surface treatment processes such as pre-getter damage and post-getter damage etch. Based on the results obtained during this work, we have ordered a rinser-drier system. It will be used to prepare large-area Silicon-Film™ wafers for the getter process.

Continuous In-Line Diffusion

The objective of this effort was to develop a low-cost process to produce the emitter junction in large-area Silicon-Film™ sheet material. We have developed two N-type dopant sources that are low-cost, readily available, non-hazardous, and stable; and a deposition technique to uniformly apply the dopant to Silicon-Film™ wafers. A necessary requirement for this process is that the deposition technique be easily scaleable to even the largest area wafer, and be adaptable to an in-line process for diffusing continuous sheets of Silicon-Film™ material. The time-temperature (recipe) for a rapid

thermal process tailored to Silicon-Film™ wafers has been determined. Using an in-house thermal model, we developed specifications for a high temperature belt diffusion furnace. We have verified this process and the furnace model using a 36-inch wide IR lamp-based belt furnace. All Silicon-Film™ getter and junction diffusions can be performed using this continuous diffusion process at a high hourly rate. Wafer handling systems capable of loading and unloading this 36-inch wide belt furnace were developed.

Background

Prior to the PVMat4a program, Silicon-Film™ wafer gettering and emitter junction diffusions were performed at AstroPower as a batch-type process using large-bore diffusion tubes. The emitter diffusion process is quite simple -- 200 wafers are loaded into a quartz diffusion "boat"; the boat is slowly pushed into the center zone of the furnace; and a dopant gas -- a combination of nitrogen, oxygen, and N-type dopant -- flows through the tube for a measured period of time. The dopant source is semiconductor grade $POCl_3$, a highly corrosive liquid which produces the dopant glass phosphorus pentoxide (P_2O_5) at diffusion temperatures on the surface of the wafer.

The performance of a solar cell is sensitive to the emitter junction. A diffused emitter layer is characterized by surface concentration and depth. These are controlled by the diffusion dopant deposition and drive-in temperatures, time at temperature, and ambient atmosphere at temperature. The emitter characteristics are optimized by maximizing carrier generation while minimizing series resistance losses associated with the contact metallization.

Although the junction diffusion process is simple, it is complicated by the ever-increasing areas of the Silicon-Film™ wafers. In a batch-type tube furnace diffusion process, the deposition and drive-in times must be long enough to ensure that dopant phosglass is uniformly deposited across the wafers and throughout the length of the diffusion boat. For large-area wafers, this time is on the order of one hour, and a typical cycle, which includes the load and unload time, might be two hours. As a result, emitter diffusion of large-area solar cells is a low-throughput (100 wafers per hour) process.

When discussing tube diffusion, it is important to note that the weight and thermal mass of a loaded diffusion boat is substantial. Although the thermal mass of an individual wafer is not large, a fully-loaded boat consists of approximately 6 kg of silicon and 2 kg of quartz (for the boat). The number of wafers in a boat is constrained by the handling weight and the temperature response of the furnace to the thermal mass of the cold load as it enters the furnace. Most tube furnaces require relatively long equilibration times (on the order of tens of minutes) when subjected to large thermal changes such as temperature setpoint changes or rapid loading/unloading.

Diffusion Process Development

Under Phase I we developed a liquid N-type dopant source for silicon wafers that is low cost, non-hazardous, and stable. Typical solar cell sheet resistances could be obtained in fairly short process times and at only moderately high temperatures (five minutes at 950°C) in a nitrogen ambient. We also developed several deposition techniques for applying the dopant to the surface of the wafers. By heating only a few coated wafers at a time in a tube furnace, we were able to perform a high-temperature drive-in that approximated the thermal profile of a "rapid thermal" process. Using this approach we investigated dopant formulation and developed the time-temperature emitter response surface. This laboratory-scale work involved small quantities of wafers that were fabricated into solar cells.

During Phase II we focused our development efforts on one of the dopant deposition techniques. A prototype system capable of throughput rates of about 300 wafers per hour was designed and assembled. Once the dopant deposition process was validated, larger quantities of wafers, both single-crystal and Silicon-Film™, were processed through the system. The remainder of the diffusion process (the equivalent of a tube furnace "drive-in" step) was performed either in a tube furnace, as before, or in a 24-inch lamp-based infrared (IR) belt furnace, originally designed for firing thick-film inks, that was made available for this project. Since the high temperature zone in this particular furnace is only 50-cm long, the belt drive system was modified to reduce the maximum belt speed to 30 cm/min (from 120 cm/min); a typical drive-in setpoint was 4 or 5 cm/min. In spite of the limitations on speed and throughput, this belt furnace could still be used for diffusing the very large area 1800 sq.-cm Silicon-Film™ wafers.

The results obtained using this furnace proved that short heat cycles adequate for producing emitter junctions could be achieved using lamp-based IR furnace technology of the type currently used for silicon solar cell manufacturing. Based on these results, an effort was initiated to develop the design and specifications for an IR furnace that would comprise the major portion of a continuous diffusion system for Silicon-Film™ wafers.

Continuous Diffusion System Design

It has been shown that rapid thermal processing (RTP) without additional high temperature "annealing" can be used to produce emitter junctions for high-efficiency solar cells, even with screen-printed metal contacts [2]. The key to the process appeared to be the relatively slow cooling temperature profile [3]. The temperature profile seen during the process is similar to that obtained from a tungsten-halogen lamp-based belt furnace operated with a "spike" power profile and a high belt speed. Screen-printed metal contacts on silicon solar cells are typically processed in tungsten-halogen lamp-based IR belt furnaces. The goal of our effort during this report period was to develop the specifications for an "RTP-like" continuous diffusion system to produce the emitter junction of large-area Silicon-Film solar cells. We have investigated the application of lamp-based belt furnaces, as well as a SiC-based belt furnace.

An existing furnace design was adapted and modified by adding an extended entrance to accommodate the dopant deposition system. A 36-inch wide belt furnace for developing the continuous Silicon-Film™ diffusion process was commissioned during Phase III. A dopant deposition system was designed, assembled and integrated with this furnace.

Initial process development using this 36-inch furnace and dopant deposition system focused on junction sheet resistance. Thermal modeling was used to set a target furnace belt speed. Through experimentation it was found to be necessary to triple the belt speed to in order to approach the sheet resistivity target. We believe that this was due to the evaporation of the dopant from the wafer surface before it could form the doping glass layer. The dopant deposition characteristics were also modified to "saturate" the surface. Comparable belt- and tube-diffused samples were sent to Solacon Labs (San Jose, CA) for spreading resistance measurements to determine the diffusion profiles. For the same sheet resistance, the depth of the belt-diffused junction was 0.2 microns, while the depth of the conventionally-diffused junction was about 0.3 microns. The profile of the belt diffused junction is much more abrupt than the tube diffused, but the depth of the heavily-doped surface layer may be slightly deeper on the belt diffused junction. One result of this change in belt speed is that the maximum throughput for the diffusion system doubled from initial estimates. This improvement was accomplished with no change other than belt speed (that is, no increase in temperature was required).

Two improvements to the dopant source were made during Phase III of the program. First, a second version of the dopant was developed to simplify the dopant compounding procedure. Second, a dye additive to the dopant was developed to allow inspection of dopant deposition characteristics. Addition of the additive to the dopant solution enables us to easily see the deposition pattern, even after drying, under short wavelength light.

During Phase III of this program a second large-area belt diffusion system was designed that incorporates the latest process changes. The dopant deposition system has been re-designed around advanced-technology IR emitter heaters. We identified, procured, and tested a new IR heater. Unlike the short-wavelength quartz halogen lamp technology used in thick film metallization firing and in our rapid thermal diffusion process, these IR heaters are based on longer wavelength IR. However, much of the radiated power still occurs within the absorption band of silicon.

Because of the throughput of the continuous diffusion system (due to belt speed and width), operation requires several operators to load and unload the belt. During Phase III we designed and built prototypes of a belt unloading system for the 36-inch wide belt diffusion furnace. It is capable of picking up five Silicon-Film™ wafers from the belt and placing them into five stacks. We also developed designs for a family of wafer handling components that would be capable of loading the belt as well as unloading. One system would load the diffusion furnace belt with five Silicon-Film™

wafers taken from a stack. A prototype pick-and-place arm based on a low-cost PLC controller, rather than an expensive robot arm, was developed as a component of this belt loading system.

Metallization Processes

Silicon-Film™ solar cells are produced with an aluminum-based screenprinted back contact metallization. We have been able to potentially reduce the cost of this process by qualifying a lower cost aluminum ink. We have increased the throughput of the Silicon-Film™ contact metallization process by increasing the width of the metallization firing furnace and by qualifying a new semi-automatic screen printer for Silicon-Film™ solar cells (previously the contact metallization was printed using manual screen printers). We are able to print Silicon-Film™ wafers using standard screen printers with only a few changes and adjustments to the vacuum hold-down, ejector, and collocator assemblies.

Back Contact Metallization

During this program we investigated several lower cost screen print inks for use with Silicon-Film™ wafer metallization. We also investigated an alternative to screen printed back metallization that is based on a thin layer of flame spray-deposited aluminum. The aluminum is sintered using an infrared belt furnace that is normally used to fire screen printed aluminum backs.

The spray aluminum process sequence is different from that used for alloyed aluminum back contacts. With screen printed back contacts, the back is printed and fired, and then the front contact is added. With sprayed aluminum, the front is printed and fired first, and the back aluminum contact is sintered, rather than alloyed, at a lower temperature. At present, front contacts processed using the baseline process sequence must be fired at low temperatures to avoid shunting the junction. Treatment of the contact metallization with a hydrogen plasma is then required to reduce the contact resistance of the front contact.

The performance of the sprayed aluminum cells was comparable to or better than cells with the baseline (screen printed back) process. There does not seem to be a strong sensitivity to front contact process temperature. The feasibility of this process has been proven and plans are in place to move it to the production level.

Metallization Equipment

One result of development work on a continuous diffusion process was experience with wider IR belt furnaces. Previously we have used 15- and 24-inch-wide IR furnaces for metallization processes. During Phase III of this program, we developed specifications for metallization firing furnaces based on 36-inch wide belts. These wider furnaces are now capable of handling Silicon-Film™ wafers 5-wide across the belt (over 1000 wafers per hour).

During this program we have screen printed contact metallizations on Silicon-Film™ wafers primarily using manual screen printers. During Phase III of this program we were able to successfully handle and print Silicon-Film wafers using a "stock" semi-automatic screen printer with only a few changes and adjustments to the vacuum hold-down, ejector, and collocator assemblies. However, due to the increased width of the 36-inch belt furnace, no collocators for this screen printer were available. During this program we developed specifications for a semi-automatic screen printer to mate with the 36-inch wide firing furnaces. As a result of this effort, a wider collocator for use with the 36-inch belt furnaces has been designed. Based on the results obtained during this work, AstroPower will use screen printers with collocators that will mate with 36-inch wide firing furnaces in production. They will be used for the large-area metallization process for Silicon-Film™ wafers.

Large-Area Anti-Reflection Coating

The objective of this work was to develop a continuous anti-reflection (AR) coating process for large-area Silicon-Film™ wafers. The AR coating process is based on the spray pyrolysis of titanium isopropoxides that are custom-designed for the appropriate index of refraction. This process is superior in cost, performance and safety compared to CVD deposition processes. We are presently coating large quantities of AP-225 Silicon-Film™ solar cells using AstroPower-designed, continuous coating equipment for 125- and 150-mm single-crystal solar cells; larger area cells have been individually coated using a platen-type heater and a "hand" sprayer.

Based on experiments which involved hand spraying large-area Silicon-Film™ solar cells, we have found that high volume low pressure (HVLP) spray technology significantly improves the uniformity of the TiO_x layer and significantly reduces overspray (which generates TiO_x powder). Furthermore, we have found that infrared heating, similar to that used for firing thick film metallizations, promotes improved thickness uniformity of the dielectric layer. It is possible to heat the surface of the wafer even while it is being coated without interference from the spray.

During Phase III of this program we designed and developed a continuous IR-AR coating system for Silicon-Film™ solar cells. The spray system consisted of a pre-heater section, together with a raster-spraying HVLP sprayhead. A belt-type conveyor system transports the wafers through the pre-heater and into the spray zone. We have investigated both long- and short-wavelength IR emitters for wafer heating, and we have found that short-wavelength IR heaters are superior for this application. This process is significantly different that used previously at AstroPower and will be capable of coating any size Silicon-Film™ wafer or plank. We have obtained good results on Silicon-Film™ cells using the continuous HVLP-IR. The average current increase for a group of test cells was 35.0% (range = 33.4 to 36.1%). The average power gain was 37.9% (range = 34.4 to 40.6%). The cells were then laminated using standard module materials. Their appearance (color; uniformity) after encapsulation was judged to be good, with improvements in area uniformity deemed to be the most important near-term task.

Large-Area Light Source

Silicon-Film™ solar cell testing is performed using a 1600W filtered-xenon short arc lamp source from Oriel (Stratford, CT). The maximum useful area is limited to about 150 x 150 mm. The objective of this effort was to identify alternate low-cost light sources for testing large-area Silicon-Film™ solar cells.

An effort was undertaken to identify alternate large-area light sources. These included conventional quartz halogen lighting. Key specifications were the ability to extend to large areas, good spectral match, low cost, high lifetime, and high stability. Although no single light source could be identified that meets all these specifications, combinations of different lights were investigated. Based on the results of the study AstroPower is pursuing a combination light source for use in the solar cell testers and module testers.

Silicon-Film™ Production Sheet Process

AP225 solar cells are produced from nominally 15 cm wide sheet grown in a continuous process. During this program, AstroPower fabricated two new Silicon-Film™ machines. One was a new production machine that increased the rate of sheet production by 70%. In addition to the production machine, a wide sheet development machine was fabricated. Tools for quick turn-around electrical analysis of the sheet are under development. The latest tool is a contactless lifetime measurement technique developed by Dr. Richard Ahrenkiel of NREL.

New Silicon-Film™ Machine

The next generation wafer production machine, designated SF-4, was designed and built during 1996. The SF-4 machine will reduce manufacturing costs by increasing the sheet generation rate and producing higher performance material than its predecessor, SF-3.

The SF-4 wafer production machine has the capability of producing Silicon-Film™ sheet at a rate 70% higher than the older SF-3 machine. Sheet material is now generated at a rate 17 times faster than any competing sheet technology. It was designed to be capable of continuous wafer production. By redesigning the heater element configuration, SF-4 has the capability of producing wafers with better crystal morphology than exists in present material, which should lead to better performance. The new production machine has been outfitted with distributive control, data-logging, and precise monitoring devices to improve machine yields and reduce the manufacturing costs of the Silicon-Film™ wafer formation process.

The new machine was put online in January 1997. Since that time it has logged over 650 hours of production. As part of the PVMaT project, two 24 hour runs were undertaken. These runs were very successful, with no failures of the growth machine. Approximately 2 miles of sheet material was generated in these two long runs.

Lifetime Measurement

An investigation into contactless lifetime measurements was conducted. The goal of this effort was to rapidly determine the minority-carrier lifetime of the as-grown Silicon-Film™ material.

AstroPower desired to quantify material parameters such as lifetime and mobility as part of its effort to determine the quality of its Silicon-Film™ wafers before they were sent to final test. Many test systems were sampled including microwave photoconductance decay (MW-PCD) and quasi-steady-state photoconductance (QssPC, a proprietary system developed by Dr. Ronald Sinton), but none proved satisfactory for Silicon-Film™ as most of the data was lost within the noise of the systems. AstroPower then learned of an RF-PCD system developed and built by Dr. Richard Ahrenkiel at NREL. In this system, the carriers produced within a sample by a laser pulse change the Q of a coil to which the sample is inductively coupled. This change is monitored electronically and the time constant of the change is equal to the minority carrier lifetime. From the same signal a relative mobility for the wafer (based on the magnitude of the signal) and a relative diffusion length (area under the curve) can also be calculated.

Dr. Ahrenkiel performed preliminary measurements on several wafers while control wafers were fabricated into solar cells. His data could distinguish between wafers with good potential and those with none. Based on this, AstroPower, with Dr. Ahrenkiel's assistance, built a copy of the RF-PCD (around a similar 1.063 μm Nd:YAG laser) in its own laboratory and began taking measurements on large numbers of wafers while continuing to send wafers to Dr. Ahrenkiel.

AstroPower's results from this system did not prove immediately encouraging. One thing that did become obvious, however, was that in Silicon-Film™, minority carrier mobility plays a much larger role in minority carrier diffusion length, and thus J_{SC}, than does lifetime. This had been hinted at in data from other systems, particularly MW-PCD. However, the lifetime and relative mobility data obtained from the RF-PCD testing at both sites showed poor correlation with J_{SC} and with minority carrier diffusion length (as obtained from spectral response data) compared to control wafers. Generally AstroPower observes a strong relationship between optically determined diffusion length and J_{SC} in processed solar cells enabling the use of diffusion length of lot samples to be used as an indication of material quality.

A new set of 50 Silicon-Film™ wafers was sent to Dr. Ahrenkiel for RF-PCD measurements using a shorter wavelength laser. These wafers, in an "as-grown" state, represented various performance levels for Silicon-Film™ and each was engraved on the backside for identification. After the testing, the wafers were to be returned to AstroPower for fabrication into solar cells. This would allow a direct comparison of RF-PCD data and device performance.

While the wafers were at NREL, data became available at AstroPower which showed that annealing a wafer has a significant effect on its diffusion length. The diffusion length of an as-grown wafer is always much lower. Dr. Ahrenkiel was advised of this and it was determined that the wafers would be returned to him for a second set of RF-PCD measurements after they were gettered and diffused (i.e. annealed). After this second RF-PCD test session, AstroPower completed the fabrication of the wafers into solar cells and their testing as such.

Figure 9 illustrates the best relationship that was found, that between P_{max} of the finished cells and the relative diffusion length calculated from the RF-PCD data. The correlation coefficient, or r^2 value, for this data set is 0.69.

AstroPower's conclusion regarding this RF-PCD system is that it is the best available for Silicon-Film™, but that the relation between the RF-PCD data and the solar cell performance is not strong enough to act as a predictive tool adequate for quality control. This is particularly true for "as-grown" or unannealed wafers due to the changes in material characteristics with processing.

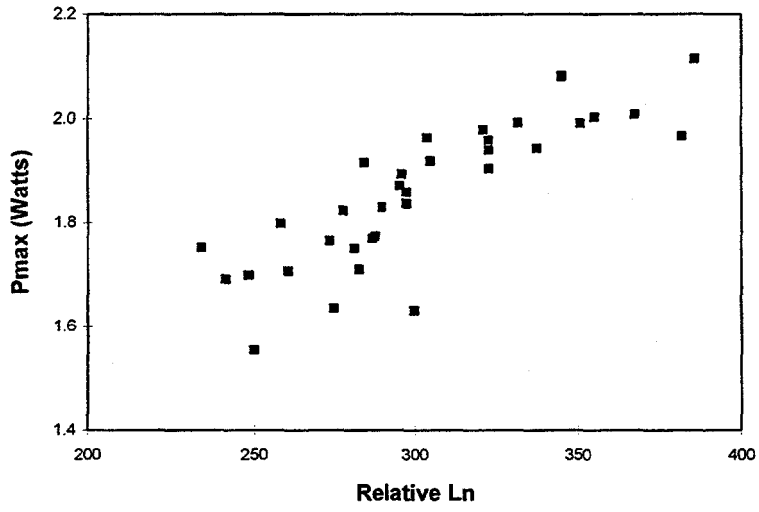


Figure 9. Correlation between power of finished solar cells and the relative diffusion length determined using the RF-PCD system.

30 cm Wide Silicon-Film™ Sheet Production

The construction, installation, and testing of the new Silicon-Film™ Wide-Body machine was completed during this effort. Silicon-Film™ sheet material with a width of 31 cm was generated.

Silicon-Film™ sheets up to 38 cm wide have been produced in the developmental Silicon-Film™ machine. During 1996, the task of fabricating large-area solar cells from these very large planks was undertaken. A number of improvements were required in solar cell processing to accommodate such large devices. Optimization of device processing is not yet complete. Most notably, the correct conditions for firing the screen printed contacts have not yet been determined. This process has been known to be very sensitive to different wafer sizes. The present process does not use a gettering step.

Conclusions

This project had the following general objectives:

1. Extend continuous processing from sheet fabrication into the solar cell fabrication steps,
2. Reduce the cost per watt of Silicon-Film™ products by increasing efficiency and reducing manufacturing costs,
3. Develop new, large area solar cells,
4. Develop new utility-scale panel products.

These goal were accomplished during the program.

Continuous processing. Significant progress was made in the area of processing large area solar cells and planks. New, continuous processing sequences were developed for gettering, junction formation, and antireflection coating. New equipment was developed in each case to allow for the processing of large area devices. These new processes are being transferred from the laboratory to production and will result in lower solar cell fabrication costs. Other improvements in processing related to this contract include a 67% reduction in chemical costs required in the wafer surface preparation process.

Efficiency Increases. The quality of Silicon-Film™ material, and the maturity of the solar cell processing have progressed during this program as reflected by increased solar cell efficiencies. A laboratory optimization effort achieved an efficiency of 16.6% (NREL measurement) on a 1.0 cm^2 solar cell. The contract goal for this device was an efficiency of 15.6%. Performance on production-sized solar cells (240 cm^2) has reached a verified efficiency of 12.2% (NREL measurement).

Large area solar cells. The Silicon-Film™ process generates a continuous silicon sheet of variable width. This project resulted in significant improvements in the manufacture and processing of this sheet material. The investigation into sheet width has resulted in the construction of a new, wider, Silicon-Film™ machine. This equipment has demonstrated that Silicon-Film™ sheet material can be fabricated at a width greater than 30 cm. At this point, there is no known limit to the width capabilities of the Silicon-Film™ sheet growth process. This new machine capability has allowed us to evaluate a number of different solar cell sizes. Solar cells with areas of 240 cm^2, 300 cm^2, 400 cm^2, 675 cm^2, 900 cm^2, and 1800 cm^2 have been fabricated. An efficiency of 11.6% was measured for a solar cell with an area of 675 cm^2.

Utility-scale panel products. A 130 kW array was completed for Niagara Mohawk Power Company. The array utilized a new panel product based on the AP225 solar cell. The new product was successful in reducing manufacturing and installation costs of the array. In addition to the new panel product, a new junction box was

developed that has lowered costs by a factor of two. Silicon-Film™ solar cells continue to demonstrate long term stability as shown by the performance of the PVUSA array installed in Davis, California in 1994. In addition to validating the stability of this technology, the PVUSA Silicon-Film™ array has demonstrated very good performance in terms of energy delivery. Published performance information for 1995 and 1996[1] show that the AstroPower Silicon-Film™ array produced more energy (AC kWhr) per rated watt of array capacity than any of the other flat panel EMT arrays, which include mono-crystalline and polycrystalline silicon arrays, as well as other thin film technologies.

Due to the success of this project, the Silicon-Film™ process is on an accelerated path to large-scale manufacturing. The AP225 solar cell, developed under the PVMaT program is now being produced in a new, 9 MW, facility. The first production runs for this facility were accomplished on May 4, 1998.

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13. ABSTRACT *(Maximum 200 words)*

Under this Photovoltaic Manufacturing Technology (PVMaT) subcontract, AstroPower, Inc., developed a number of new products, including a 130-kW array built using a new panel design. Improvements in laboratory-scale cell processing resulted in a confirmed efficiency of 16.6%. A new Silicon-Film™ production sheet machine was built that increased throughput by 70%. AstroPower also converted three solar cell fabrication processes from low-throughput batch processes to high-throughput, continuous, belt processes. These new processes are capable of processing sheet over 31 cm in width. Finally, a new Silicon-Film™ sheet machine was built that demonstrated a sheet width of 38 cm. This tool enabled AstroPower to demonstrate a wide range of solar cell sizes, many of which have generated considerable market interest. The achievement of continuous process has led to lower cost per watt by reducing labor, as well as improving control, quality, and yield. Under this program, three process steps were made continuous: gettering, diffusion of emitter layer, and large-area antireflection coating.

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