August 1996 • NREL/SP-413-21551

Sixth Workshop on The Role of Impurities and Defects in Silicon Device Processing

Extended Abstracts and Papers

August 12–14, 1996
Snowmass, Colorado

Workshop Chairman: B.L. Sopori

Program Committee:
R. Sinton, T. Tan, J. Kalejs, J. Gee
L. Jastrzebski, A. Rauber, B. Sopori

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A national laboratory of the U.S. Department of Energy
Managed by the Midwest Research Institute
for the U.S. Department of Energy
under contract No. DE-AC36-83CH10093

NREL/SP-413-21551 • UC Category: 1250 • DE96007959

Sixth Workshop on The Role of Impurities and Defects in Silicon Device Processing

Extended Abstracts and Papers

August 12–14, 1996
Snowmass, Colorado

Workshop Chairman: B.L. Sopori

Program Committee:
R. Sinton, T. Tan, J. Kalejs, J. Gee
L. Jastrzebski, A. Rauber, B. Sopori

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A national laboratory of the U.S. Department of Energy
Managed by Midwest Research Institute
for the U.S. Department of Energy
under contract No. DE-AC36-83CH10093

Prepared under Task No. PV622101

August 1996

NOTICE

This report was prepared as an account of work sponsored by an agency of the United States government. Neither the United States government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States government or any agency thereof.

Printed on paper containing at least 50% wastepaper, including 10% postconsumer waste

Sixth Workshop on
The Role of Impurities and
Defects in Silicon Device Processing

TABLE OF CONTENTS

Title/author(s): **Page**

WORKSHOP THEME: *Technology Transition for Fabricating High Efficiency, Low-Cost, Commercial Silicon Solar Cells* 1
Bhushan Sopori

Modeling Point Defect and Microdefect Formation in Silicon Crystal Growth: Toward a Unified Model of Defect Generation 4
Robert Brown (paper not available time of printing)

Impurity Segregation/Precipitation/Gettering at Dislocations 5
Koji Sumino

Redistribution of Impurities During Silicon Solidification 18
T. F. Ciszek

Current Status of the Polycrystalline Silicon Industry 26
James R. McCormick

Which Silicon Materials Parameters are Critical to Solar Cell Design and Resulting Efficiency? 30
Ronald A. Sinton

Oxygen, Carbon and Nitrogen in Multicrystalline Silicon 34
H. J. Möller, D. Yang, S. Riedel, M. Werner, D. Wolf

Recent Advances In Wet Cleaning Technology in Silicon Processing 38
Kamal Mishra, I. Malik

Influence of Defect-Impurity Interaction on Silicon Solar Cells 39
S. Martinuzzi

Investigation of Shunting Regions in Solar Cells by Dynamical Precision Contact Thermography 52
O. Breitenstein, K. Iwig, I. Konovalov

Thin Film Solar Cells from Crystalline Silicon 59
Jürgen H. Werner, Ralf B. Bergmann, Rolf Brendel, and Uwe Rau

Multicrystalline Silicon Solar Cells by Liquid Phase Epitaxy 64
A. W. Blakers, K. J. Weber

Light-Trapping in Thin Crystalline Silicon Layers 71
James A. Rand, Jeffery E. Cotter

Gettering of Defects and the Impurities in Solution Grown Silicon 77
Zhengrong Shi

Hydrogen Passivation in Silicon Solar Cells 82
Stefan Estreicher, Bhushan Sopori

Defect Passivation by Means of PECVD-nitride and Hydrogenation 83
for Crystalline Si Solar Cells
J. Poortmans, J. Szlufcik, F. Cuerinckx, K. Declercq, J. Horzel,
T. Vermeulen, O. Evrard, J. Nijs, R. Mertens

Charge State Control of Hydrogen in Silicon 96
Carl Seager, R. A. Anderson

New Trends in Defect Passivation 97
Sergio Pizzini, M. Acciarri, S. Binetti, D. Narducci, C. Savigni

Physical and Numerical Modeling of Impurity Precipitation, Precipitate 110
Dissolution, and Gettering of Precipitated Impurities in Silicon
Teh Y. Tan, R. Gafiteanu, U. Gösele

Redistribution Kinetics of Metal Impurities in Multicrystalline Silicon 118
M. Seibt, M. Apel, I. Hanke, W. Schröter

High Efficiency Cell Fabrication on Low Defect Density Material 128
A. Rohatgi and S. Narashima

A Review of Recent Advances in MIS Solar Cells 140
Rudolf Hezel

Fine-Line Printing for Silicon Solar Cells 155
H. H. C. de Moor, A. W. Weeber, J. Hoornstra, W. C. Sinke

Novel Process Sequences for Low-Cost Silicon Solar Cell Fabrication 172
James M. Gee, Douglas S. Ruby, Walter Worobey

Processing Large-Area Silicon Substrates with High Defect Densities 173
into Higher Efficiency Solar Cells
Mike Kardauskus

Antireflecting Silicon Solar Cells with Textured Zinc Oxide 178
Haifan Liang, Roy G. Gordon

Cost Analysis of High Efficiency Polycrystalline Silicon Solar Cell Sequences 184
S. Narayanan, J. Wohlgemuth

Status of RTP for Silicon Device Fabrication - A SEMATECH Perspective 191
Don Lindholm

A Review of RTP and Its Application in Display and Solar Device Fabrication 195
Chunghsin Lee

100 Micron String Ribbon Silicon 204
R. Wallace, J. I. Hanoka, A. Rohatgi, and Gerald Crotty

Interactions between Metallic Impurities and Structural Defects in 207
Photovoltaic Grade Silicon
Scott A. McHugo, H. Hieslmair, E. R. Weber

Iron Precipitation Kinetics in Silicon and the Relation to Carrier Diffusion 211
Lengths and Aluminum Gettering
Henry Hieslmair, Scott McHugo, Eicke Weber

Thermal and Microstructural Modeling for Cast Silicon 215
D. Franke, I. Steinbach, W. Krumbe, J. Liebermann, W. Koch, H. J. Möller

Long-time Stability of Quenched-in Self-interstitials Available for 219
Impurity-defect Kinetics in 5d^n - Doped Silicon Crystals
M. Höhne, U. Juda, O. Scheerer

Selective Solid Phase Crystallization with Controlled Grain Size and 223
Location in Ge Thin Films on Silicon Dioxide
C. M. Yang and H. A. Atwater

Selective Nucleation and Solid Phase Epitaxy Process 227
For Si Thin Film Phtovoltaics
Claudine M. Chen and Harry Atwater

Contactless Frequency Resolved Microwave Spectroscopy of the 231
p-Si in the Presence of CarrierTrapping
A. Romanowski, A. Karoui, G. Rozgonyi

Impurity Segregation During EFG of Silicon Octagons 232
J. Cao, M. Prince, J. P. Kalejs

Emissivity Measurements of Silicon Related Materials and Structures - 236
Applications to Rapid Thermal Processing
N. M. Ravindra, F.M. Tong, W. Chen, S. Abedrabbo, W. Schmidt
A. Nanda, T. Speranza, A.M. Tello, S. Narayanan

Solar Cell Materials and Device Characterization by PVSCAN 242
Bhushan Sopori, Jamal Madjdpour, and Marta Symko

Enhanced Hydrogenation in Polycrystalline Silicon Thin Films Using Ultrasound Treatment 246
J. Koshka, S. Ostapenko, L. Jastrzebski, J. Lagowski

The Effects of External Gettering on Silicon-Film™ 251
K.M. Dugan Cavanagh, D. H. Ford, J. A. Rand, R. B. Hall, A. M. Barnett

Screen Printed Aluminum Back Surface Fields for Silicon Solar Cells 255
S. Narasimha, J. Mejia, A. Rohatgi

A Simultaneous Front and Back Diffusion Technique for the Low Cost Production of High Efficiency Silicon Solar Cells 260
Thomas Krygowski, Ajeet Rohatgi

Effect of Oxidations on Phosphorus-Diffused Crystalline-Silicon Substrates 264
James M. Gee, Richard R. King, Joerg H. Reiss, Kim W. Mitchell, S. Narayanan

Self-Aligned Selective Emitter Plasma-Etchback and Passivation Process for Screen-Printed Silicon Solar Cells 268
D. S. Ruby, C. B. Fleddermann, M. Roy, and S. Narayanan

UltraSound Treatment (UST) Defect Engineering in Silicon-Based Materials 273
S. Ostapenko

Copper Gettering in Silicon Studied by Transient Drift Analyses 275
T. Hieser, E. R. Weber

Double Gettering Solar Grade Silicon Materials using Aluminum and Titanium 279
A. Karoui, A Romanowski, Q. Zhang

Porous Silicon Gettering 280
P. Menna, Y. S. Tsuo, J. R. Pitts, K. R. Jantzen, S. E. Asher,
M.M. Al-Jassim, T. F. Cizek

Process Optimization of Alloyed Aluminum Backside Contacts for Silicon Solar Cells . . . 284
Lynn L.Chalfoun, Aimee L. Smith, Song Zhao, and Lionel C. Kimerling

Impurity Gettering: Influence of Oxygen and Crystallographic Defects 285
I. Perichaud, S. Martinuzzi

Surface Passivation of Silicon by a Solution-Grown Film from Sopori Etch 286
Marta Symko, Bhushan Sopori, Dick Ahrenkiel, and Rick Matson

Technology Transition for Fabricating High Efficiency, Low-Cost, Commercial Silicon Solar Cells

Bhushan L. Sopori
National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, CO 80401

During the last few years much research was performed toward understanding basic mechanisms of impurity and defect interactions that occur in silicon device processing. This work has resulted in the identification of some of the mechanisms that limit the cell performance, and it has shown that processes such as impurity gettering and passivation can be successfully applied to mitigate such limitations. The work has also shown that incorporating steps such as phosphorus diffusion, aluminum alloying, and hydrogen passivation into the solar-cell fabrication process-schedule improves the material quality and hence yields better cell efficiencies. In fact, application of these concepts has yielded small-area, laboratory solar cells with efficiencies greater than 18.5% on commercial substrates, to large-area, prototype encapsulated cells of greater than 15% efficiency. Some of the important achievements, to date, consist of better understanding of:

- Defects in the substrates: Identifying the roles of point and crystal defects in multicrystalline substrates in controlling the minority carrier lifetime/diffusion length, and their behavior under various thermal processing conditions.
- Impurity gettering
  - — Mechanisms of phosphorus and Al gettering (gettering model);
  - — Impurity defect interactions: qualitative model for gettering in multicrystalline silicon that is consistent with the observed degradation in the cell performance due to high-temperature processing;
  - — Optimization of parameters for gettering during cell processing of Si substrates from different vendors;
  - — Additive effects of multiple gettering steps by sequential or simultaneous processes.
- Passivation
  - — Many intriguing results, such as variations in the degree of passivation in materials from different vendors seem to have explanations;
  - — Passivation from forming gas anneal;
  - — Passivation resulting from PECVD nitridation;
  - — Theoretical results of hydrogen diffusion mechanisms from *ab initio* and molecular dynamic calculations;
- How cell non-uniformities, arising from defect clusters and impurity precipitation, limit the performance of large-area cells.
- Minimization of impurity contamination by suitable cleaning processes
- Methods suitable for monitoring material quality and process parameters

It is expected that the concepts and the results of current research, if incorporated into production, can lead to 16% commercial solar cells, perhaps without increasing the cell costs. While the PV industry is evaluating these concepts, they have already begun to introduce several other cost-saving approaches. These include: growth of larger ingots while lowering the defect densities using appropriate thermal conditions, wire sawing (or high-speed laser cutting for ribbons) to get thinner wafers with less saw damage, optimization of gettering and/or hydrogen passivation to improve the cell performance.

These low-cost approaches, coupled with the advanced processing, can realistically promise PV energy costs approaching $2/Wp. An added advantage of advanced processing is that the cell performance becomes less vulnerable to the initial material quality. This is particularly important if the feedstock is obtained from different sources.

The near-term goal of the National Renewable Energy Laboratory/Department of Energy program is to perform coordinated research that can lead to the manufacture of silicon solar cells of 18% AM1.5 efficiencies. Clearly, further research is needed to understand basic material properties, identifying mechanisms that limit large-area performance, and arrive at processes that ameliorate the influence of performance-limiting mechanisms. It will be a big challenge to incorporate advanced processes into a low-cost production facility.

As we look forward to greater than 18% commercial solar cells, we need to develop appropriate research objectives. We also need to explore other avenues of cost reduction, such as new cell configurations that can overcome the limitations in the material characteristics by improved device design. Preliminary analyses suggest that defect-engineered, thin-layer cells can produce high-efficiency devices. However, this potential of thin-layer silicon solar cells can only be realized if these devices can be fabricated on low-cost substrates. Consequently, research is needed to investigate: growth/deposition of thin-silicon layers of good material quality, suitable device design with efficient light-trapping and low-interface recombination characteristics, and applications of gettering and passivation techniques, to thin-layer silicon solar cells.

NREL expects to send a Request for Proposal for a competitive procurement that will help us go from 15% to 18% large-area cells and to investigate realistic design/fabrication approaches for thin solar cells. It is clear that future research should include:

1. Further understanding the mechanisms that limit large-area cell performance and developing processes that can overcome these limitations to produce greater than 18% large-area cells. Recent work has shown that current gettering and passivation processes that work well in low-defect-density regions of a silicon wafer are not effective in the regions of high dislocation densities (defect clusters). As a result, regions of defect clusters lead to strong non-uniformities in the cell, with low-performing regions acting as "sinks." Therefore, emphasis must be placed on characterizing such defect clusters, determining what prevents effective gettering, and arriving at processes that can improve these regions.

- Identification of mechanisms that prevent impurity gettering and passivation in the regions of defect clusters
- Impurity-defect interactions during crystal growth that cause decoration of defects
- Impurity dissolution during gettering
- Dissociation of defect networks by post growth processes
- Passivation of defect clusters
- Optimum process sequences that can produce synergistic effects of gettering and passivation and are compatible with low-cost processing.

2. New approaches to low-cost silicon solar cells. The tasks under this area include:

- Identify suitable methods for silicon-film deposition/growth on low-cost substrates

- Identify characteristics of low-cost substrates for silicon-layer deposition
- Cell processing techniques compatible with thin silicon layers on low-cost substrates
- Novel cell designs.

The objectives of the workshop are to address:
— Current understanding of impurity and defect issues in solar cell processing
— How the laboratory technologies can make a transition and culminate as cell production processes
— approaches for thin-layer silicon solar cells.
There are other crucial issues for the PV community that such a workshop can address. Here we have included two issues of current interest — availability and quality poly feedstock, and viability of rapid thermal processing for solar-cell manufacture.

MODELING POINT DEFECT AND MICRODEFECT FORMATION IN SILICON CRYSTAL GROWTH: TOWARD A UNIFIED MODEL OF DEFECT GENERATION

Robert Brown

ABSTRACT NOT AVAILABLE
AT THE TIME OF PRINTING

Impurity Segregation/Precipitation/Gettering at Dislocations

Koji Sumino
Nippon Steel Corporation
Futtsu, Chiba Prefecture 293, Japan

Abstract: A review is given of the work of author's group on segregation and precipitation of impurities at dislocations in Si. The mechanism of impurity gettering by dislocations is discussed. Precipitation processes of oxygen, iron and copper impurities on dislocations are shown in detail.

1. Introduction

Impurity segregation at a dislocation may be defined as the phenomenon that an impurity-rich region develops around the dislocation owing to some thermodynamic necessity without forming new phase which involves the impurities. Impurities are recognized as impurities in such a region. The driving force for the segregation is the interaction between a dislocation and an individual impurity atom. The impurities may or may not be supersaturated in the matrix region.

Precipitation at a dislocation implies that particles of the thermodynamically stable phase are formed on the dislocation line by incorporating impurity atoms that are supersaturated in the matrix. It is well known that dislocations act as preferential nucleation sites for precipitates in a variety of materials. The driving force for the preferential precipitation is the liberation of strain energy associated with a dislocation in the region where a precipitate particle is formed. The early stage of precipitation may be same as impurity segregation along the dislocation line until the concentration of impurity atoms along the dislocation line attains some critical value to form the well defined precipitate phase.

Impurity gettering at a dislocation may be defined as the phenomenon that some specific type of impurities are concentrated on the dislocation and, as a result, a denuded zone of the impurities develops in the region apart from the dislocation. Both impurity segregation and impurity precipitation at a dislocation result in the development of denuded zone.

All of the above phenomena can be discussed within the framework of dislocation-impurity interactions. Generally speaking, dislocation-impurity interactions result in the spatial inhomogeneity in the impurity distribution and, in turn, result in the spatial inhomogeneities in the electrical and/or optical properties of the material, reflecting the dislocation distribution. On the one

hand, various properties of a dislocation are greatly affected by the segregation or precipitation of impurities at the dislocation. Electrical and optical effects inherent of a clean dislocation may be modified due to decoration with impurities. An originally mobile dislocation is immobilized when precipitate particles develop on it. This effect leads to the suppression of dislocation generation even in a nominally dislocation-free crystal [1,2].

This paper briefly reviews above-mentioned effects of dislocation-impurity interactions on the basis of the investigations of the author's group.

2. Impurities around Dislocation

2.1. Impurity distribution in thermal equilibrium

Distribution of impurities around a dislocation in a crystal in thermal equilibrium is first discussed for the case that impurities are in solution and not supersaturated.

Since any given impurity atom occupies a substitutional or interstitial site in the crystal and each site is occupied by only one impurity atom, the distribution of impurities within the crystal in thermal equilibrium obeys Fermi-Dirac statistics. The probability p that an impurity atom occupies a site where the energy of interaction between the impurity atom and a dislocation is E_i is given approximately by

$$p = 1 / [\, 1 + (1/C_0) \exp(-E_i \,/\, k_B T)], \qquad (1)$$

where C_0 is the mean concentration of impurities in the crystal, k_B is the Boltzmann constant and T is the temperature [3]. Impurity distribution around a dislocation governed by equation (1) is known as the Cottrell atmosphere.

Figure 1 shows p as a function of T (in ℃) for $C_0=10^{-6}$ and various values of E_i [4]. The occupation probability p changes from unity to C_0 within a rather narrow temperature range as the temperature increases. This temperature range shifts towards higher temperatures as E_i increases. At temperatures of about 700 ℃, at which most impurity atoms undergo diffusion motion at appreciable rates, impurities present at a concentration of 1 ppm are shown to be effectively trapped by the sites where the magnitude of the interaction energy is greater than about 1.5 eV.

The dependence of p on T is also influenced by the magnitude of C_0. Figure 2 shows the relationship between p and T for E_i=1.5 eV and different values of C_0 [4]. The temperature range in which impurities are trapped by the site becomes wider as the impurity concentration increases for any value of E_i.

The type of interaction of a dislocation with an impurity atom which

plays an important role at high temperatures is that due to their elastic strain fields. The interaction energy is calculated using elasticity theory. The magnitude of the interaction energy decreases rapidly as the impurity atom is separated from the dislocation. The maximum of the interaction energy is attained when the impurity is on the site nearest to the dislocation core. For a typical impurity atom accompanied by a large misfit strain in a semiconductor crystal, the maximum of the interaction energy is evaluated to be less than about 0.5 eV.

Thus, the following conclusion can be reached : in general, an extended impurity rich or impurity lean region is never developed around a dislocation in thermal equilibrium through the dislocation-impurity interaction at temperatures where the atomic diffusion is active for impurity concentrations typical in semiconductors, for example 10 ppm or less.

2.2. Impurity gettering at dislocation

From the analysis presented above it is known that impurity gettering at a dislocation is not related to the development of impurity atmosphere around it. Thus, it may be thought that impurities are gettered by dislocations by the following mechanism : impurities which are incorporated at a high temperature owing to contamination of a crystal become supersaturated when the crystal is brought to a lower temperature and precipitate on dislocations if the latter can act as preferential nucleation sites for precipitates.

However, the real mechanism has been found to be more complex. Three important experimental observations in this context are as follows:

① dislocations in GaAs are immobilized owing to the gettering of In and Al impurities at low concentrations in spite of the fact that these impurities are soluble in GaAs over the whole concentration range from 0 to 100 % [5,6]

② α dislocations in GaAs are selectively immobilized due to the gettering of In and Te impurities while β dislocations in the same material are selectively immobilized due to the gettering of Al and Zn impurities even if both types of dislocations are characterized by the same elastic strain fields[6]

③ Cu precipitates formed on a Frank-type partial dislocation have a lower thermal stability than Cu precipitates formed on a perfect edge dislocation [7].

The present author [8] has reached the following conclusion : generally, owing to the peculiarity of atomic arrangement, some type of reaction occurs in the core region of a dislocation in which impurity atoms are incorporated from the matrix region. The type of reaction is determined by the combination of the core structure of dislocation and the species of impurities. Such a reaction does not necessarily occur in the matrix region.

3. Oxygen Precipitation at Dislocation

3.1. Morphology of precipitates on dislocation

The morphology of silicon oxide precipitates in the matrix region of Czochralski-grown Si (CZ-Si) is known to depend on the temperature at which precipitation takes place. Temperatures for precipitation are often divided into three regions according to the precipitate morphology. The first is the temperature region lower than 650 °C (low temperature range) where precipitates are of the shape of a small sphere with a diameter of order of 2 nm [9]. So-called rod-like defects and interstitial-type dislocation dipoles are seen together with such sphere-shaped precipitates. The second is the temperature range of 850 to 1000 °C (intermediate temperature range) where precipitates are of the shape of a square-shaped platelet with the habit planes {100} and the edges parallel to the <011> directions [10]. Such a platelet-like precipitate is accompanied by a lattice strain in the matrix region around it and often emits punch-out dislocations. The third is the temperature range of 1100 to 1200 °C (high temperature range) where precipitates are in the shape of a octahedron with the habit planes {111} [11]. They are often accompanied by stacking faults of extrinsic type. Sometimes, punched out dislocations are found around them which are possibly generated during cooling of the crystal due to the difference in thermal expansion coefficients of Si and SiO_2. The structure of precipitates developed in all the temperature range is amorphous according to the analysis by transmission electron microscopy.

The dependence of the precipitate morphology on the temperature seen above has been well interpreted from an energy consideration. The formation of a silicon oxide particle causes a large volume expansion. In the low temperature range, because of the low diffusivity of oxygen, the volume of the precipitate formed is so small that the interface energy of the precipitate dominates over the strain energy. This leads to the sphere shape of precipitates. In the intermediate temperature range, the precipitate grows into a volume that the strain around it is appreciable. However, the rate of self-diffusion is not high enough to release the strain around the precipitate by means of diffusion-related processes. Thus, the precipitate assumes the shape of a platelet which has the lowest strain energy among various shapes of precipitates of the same volume. In the high temperature range, the volume of an individual precipitate is large and the self-diffusion of silicon takes place at high rates. The strain related to the volume expansion associated with precipitates is effectively released by emission of interstitial silicon atoms from the precipitate or the absorption of vacancies from the matrix. The precipitate now assumes the shape of a sphere with the smallest area of interface or a

polyhedron with habit planes of low energies.

The low, intermediate and high temperature ranges are thought to correspond to the early, intermediate and late stages, respectively, of precipitation. Indeed, it has been confirmed that precipitates formed after a prolonged duration of annealing in the intermediate temperature range assume the octahedral shape while those formed after a short duration of annealing in the high temperature range assume the platelet shape.

The morphology of precipitates formed on dislocations is different from those developed in the matrix region. In a very early stage of precipitation, high resolution electron microscopic observations revealed that some kind of impurity clusters of a size of about 1 nm were formed on the dilatational side of 90° Shockley-type partial dislocations but not around 30° Shockley-type partial dislocations [12]. The size of the cluster was too small to determine its structure and composition. The author believes it to be a cluster of oxygen atoms before evolving into silicon oxide.

Due to annealing in the low temperature range, a number of precipitates in an ellipsoidal shape, several tens nm in the length, are first closely aligned along dislocations, irrespective of the type of dislocations [12]. With an increase in the annealing duration, they grow along the dislocations and are connected to each other and, finally, all dislocation segments are continuously covered by precipitates of a cylindrical shape. The diameter of the precipitate cylinder is about 10 nm and the structure is determined to be amorphous.

Precipitates developed on a dislocation in the intermediate temperature range are first distributed discretely with a separation of about 100 nm. They are accompanied by strong lattice strain in the matrix and have the shape of a needle elongated along the direction of the dislocation [12]. The size of precipitates increases and the separation of precipitates along dislocation line also increases as the duration of annealing increases. After prolonged annealing dislocations are displaced from the precipitates which were originally formed on themselves. 60° dislocations undergo parallel displacement, while screw dislocations become helical [13]. Such motions of dislocations are thought to be accomplished by absorption of interstitial silicon atoms which are emitted from the precipitates. This implies that precipitates now grow by themselves without the help of the dislocations.

In the high temperature range, precipitates are formed along dislocations but sparsely. The precipitate assume the shape of a polyhedron with the habit planes {111} and the edges parallel to the <110>, similar to those developed in the matrix region at the same temperature [12].

The variation in the morphology of precipitates on dislocations with annealing temperature seen above is interpreted in the following way. In the low temperature range, where the diffusion rate is low, the energy of the system

may be the most efficiently released by replacing the core region of dislocation by the precipitates [14]. Thus, a cylinder of precipitate develops along the dislocation core. In the intermediate temperature range, the cylinder of precipitate is converted to precipitate particles discretely aligned along the dislocation line to reduce the energy contribution from the interface. The balance of the interfacial energy and the strain energy of a precipitate may lead to the development of needle-like precipitates aligned along the dislocation line. In the high temperature range the precipitate is free from the strain. Thus, the shape is determined in such a way that the interfaces takes the lowest energy.

3.2. Dislocation immobilization

Preferential precipitation of oxygen on a dislocation is the most important phenomenon underlying the fact that CZ-Si is almost exclusively used as the materials for microelectronics. A dislocation in a silicon crystal originally mobile become immobile when oxygen precipitates on it. This phenomenon results in an increase in the resistance to the occurrence of warping (plastic deformation) of wafers caused by thermal stress, when they are subjected to repeated thermal processing for device production[1,2]. An extra stress is needed to start a dislocation immobilized by precipitates. Such extra stress is termed release stress since it is the stress to release the dislocation from precipitates.

The release stress increases steadily with the duration of annealing in the low temperature range in CZ-Si [15]. The increasing rate of the release stress increases with an increase in the concentration of oxygen. This corresponds the observation in the previous section that a cylinder of oxygen precipitate grows steadily along the dislocation line due to annealing in this temperature range.

The upper yield stress of dislocated CZ-Si shows an interesting behavior against the duration of annealing in the intermediate temperature range. It first increases, shows the maximum, and then decreases with the increase in annealing duration as shown in Fig. 3 [16]. The first increase may be caused by an increase in the size of precipitates on dislocations at this annealing stage. The decrease in the upper yield stress in the late annealing stage is attributed to the increase in the density of mobile dislocations in the crystal. Such an increase in the mobile dislocation density is thought to be related to the increase in the separation of precipitates along the dislocation line.

4. Precipitation of Metallic Impurities at Dislocation

4.1. EBIC contrast of dislocation

Glide dislocations introduced by plastic deformation and Frank-type partial dislocations bounding extrinsic-type stacking faults formed around SiO_2 precipitates in Si both act as recombination centers for carriers and give rise to EBIC contrasts in the temperature range lower than about 200 K. However, they become recombination-inactive and their EBIC contrasts disappear at temperatures higher than 200 K if the crystal is not contaminated with metallic impurities [17]. These observations show that the energy levels of recombination centers associated with glide dislocations and Frank partials are shallow within the bandgap if they are not decorated with metallic impurities. An analysis of the contrast versus temperature relation on the basis of the Shockley-Read-Hall statistics leads to the conclusion that the energy levels of the recombination centers associated with these types of dislocations are located at about 0.06 eV from the band edges.

Both glide dislocations and Frank partials give rise to EBIC contrasts at room temperature when they are decorated with transition metal impurities [17]. This implies that deep levels are generated on these types of dislocations due to the decoration with such impurities. Utilizing this effect, we are able to investigate the precipitation process of transition metals on dislocations by observing the EBIC images of dislocations at room temperature.

4.2. Fe precipitation on dislocation

Fe impurities were introduced into a Si crystal containing Frank partials or glide dislocations at 1100 ℃ . The concentration of Fe impurities introduced is estimated to be 2.3×10^{15} atoms/cm^3. Precipitation behavior of such Fe impurities during cooling of the crystal from 1100 ℃ to room temperature was investigated.

Frank partials show distinct EBIC contrasts at room temperature in such a crystal [18]. The contrast of a Frank partial depends on the cooling rate of the crystal and is stronger in a slow cooled crystal than in a fast cooled crystal. More Fe atoms are lost from the Si matrix in the slow cooled crystal than in the fast cooled crystal according to the measurements of electron spin resonance.

Glide dislocations also show distinct EBIC contrasts at room temperature. The contrast is uniform along all dislocations in the crystal [19].

Precipitate particles of Fe or Fe-related defects are not observed on Frank partials or glide dislocations and also in the matrix region by means of transmission electron microscopy (TEM).

The above observations indicate that Fe impurities, at least at a

concentration of the order of 10^{15} atoms/cm^3, precipitate on Frank partials and glide dislocations during cooling. More Fe atoms are accumulated on these types of dislocations when the cooling rate is slow. Fe atoms accumulated on dislocations do not coagulate into particles of an appreciable size but seem to be distributed uniformly along dislocation lines.

4.3. Cu precipitation on dislocation

Precipitation behavior of Cu impurities at dislocations depends on the cooling rate and the Cu concentration of the crystal.

Cu impurities were introduced at 1000 ℃ into Si crystals containing Frank partials dominantly. The crystals contained also punched-out dislocations at a density much lower than that of Frank partials. The Cu concentration in the crystal is estimated to be 4.4×10^{17} atoms/cm^3.

Figure 4 shows temperature dependencies of the EBIC contrasts of Frank partials in a nondoped crystal and the crystals doped with Cu and cooled slow and fast [7]. Frank partials do not show any EBIC contrast at room temperature when the crystal is cooled slowly from 1000 ℃ (cooling rate<150 ℃ /s). EBIC contrasts due to large colonies of Cu precipitates are seen in regions apart from Frank partials in such a crystal. TEM observations reveal that no Cu precipitates are formed on Frank partials and colonies of Cu precipitates are bounded by a perfect-type edge dislocation in the slowly cooled crystal.

On the other hand, when the crystal is cooled rapidly (cooling rate: 1600 ℃ /s) from 1000 ℃ , Frank partials show EBIC contrasts at room temperature and colonies of a small size is formed in the crystal. A high density of uniformly distributed Cu precipitates are formed along Frank partials in the rapidly cooled crystal according to TEM observations. Cu precipitates formed on Frank partials dissolve due to annealing at temperatures higher than 800 ℃ , while Cu precipitates in colonies remain stable at higher temperatures [7].

The absence of Cu precipitation on Frank partials and the development of colonies in the matrix region are commonly observed phenomena in slowly cooled crystals dominated with stacking faults if Cu impurities are introduced at temperatures higher than 700 ℃ , namely, if the Cu concentration is higher than 6×10^{16} atoms/cm^3. However, Frank partials show weak EBIC contrast at room temperature even in a slowly cooled crystal if Cu impurities are introduced in the temperature range of 400 – 700 ℃ . Colonies developed in such a crystal are low in density.

Si crystals which contain a high density (1.5×10^5 cm^{-2}) of punched-out dislocations emitted from platelike oxygen precipitates and a much lower density of Frank-partials were also prepared. It was confirmed that colonies

developed from punched-out dislocations during cooling of the crystal after the introduction of Cu impurities at a high temperature [7]. Thus, colonies seem to be formed by means of repeated precipitation of Cu on punched-out dislocations which undergo climbing motion by absorbing Si interstitials emitted from Cu precipitates. Such a model was first proposed by Nes and Solberg [20,21]

Thus, we reach the conclusion that in slowly cooled crystals precipitation of Cu by means of repeated precipitation on climbing punched-out dislocations (perfect-type edge dislocations) dominates over the precipitation on Frank partials when supersaturation of Cu is high enough. However, such predominance of precipitation on perfect-type edge dislocations is lost when the supersaturation becomes low.

We propose the following interpretation for the observations on Cu precipitation at dislocations described above [7].

Precipitation of Cu on a Frank partial requires a larger supersaturation than that on a perfect-type edge dislocation. In a heavily contaminated crystal slowly cooled from the contamination temperature Cu precipitation first takes place on small punched-out dislocation loops during cooling while the crystal is still at high temperatures where the supersaturation of Cu is rather low. The dislocation loops undergo climb motion by absorbing Si interstitials which are emitted from Cu precipitates. The growing loops act as nucleation sites for repeated precipitation of Cu as the crystal is cooled. Since the cooling rate is low enough, Cu colonies can absorb most of the supersaturated Cu in the crystal. As a consequence, the supersaturation of Cu necessary to nucleate precipitates on Frank partials is never attained. Therefore, Cu atoms develop large precipitate colonies and do not precipitate on Frank partials.

On the other hand, fast cooling of a heavily contaminated crystal leads to sufficiently high supersaturation of Cu to nucleate precipitates on Frank partials as well as on small punched-out dislocation loops. The precipitation on Frank partials probably starts at a lower temperature than the formation of Cu colonies.

In slowly cooling of a lightly contaminated crystal dominated with stacking faults punched-out dislocation loops are much lower in density and smaller in size than stacking faults. These inhibit the development of colonies in the high temperature range. Cu atoms not absorbed in colonies precipitate on Frank partials at rather low temperatures. Thus, both formation of colonies and decoration of Frank partials are observed in such a crystal.

Precipitation behavior of Cu impurities on dislocations introduced by plastic deformation was investigated with float-zone-grown Si (FZ-Si) which is free from any defects related to oxygen precipitation [19].

In a crystal doped with a high concentration of Cu most dislocation segments do not show any EBIC contrasts at room temperature as a in

non-doped crystal when it is cooled slowly. However, large colonies of Cu precipitates are found to be formed on some parts of dislocations. TEM examinations revealed that the dislocation bounding such a colony is a helical dislocation developed from the screw part of dislocation.

In a crystal heavily doped with Cu and cooled fast all dislocation segments show uniform EBIC contrast along the dislocation lines at room temperature. Small-sized colonies are also formed on some parts on the dislocations. TEM examinations have shown that particles of Cu precipitate are uniformly distributed along all dislocation segments and colonies are also formed at helical parts of dislocations.

In a crystal lightly doped with Cu dislocations show a weak EBIC contrast at room temperature which is uniform along dislocation line irrespective of cooling rates. No colonies are seen to be developed. No precipitates are detected on dislocations by TEM. Dislocations are thought to be decorated with Cu lightly and uniformly.

The arguments on Cu precipitation on Frank partials given above may apply also in this case by replacing a Frank partial by a regular part of a glide dislocation and a punched-out dislocation by a helical dislocation emerging from a screw dislocation.

5. Conclusion

Impurities in Si in the presence of dislocations show a rich variety of behavior, depending on many parameters. The progress in semiconductor materials technology will be achieved on the basis of correct knowledge of dislocation-impurity interactions.

References

[1] Sumino, K. and Harada, H.(1981), Philos. Mag. A44, 1319.

[2] Sumino, K. and Yonenaga, I.(1994), in *Oxygen in Silicon* (Semiconductors and Semimetals Vol. 42), F. Shimura ed. (Academic Press, New York, 1994) p.449.

[3] Sumino, K. (1983), in *Defects in Semiconductors* II (MRS Symposia Proceedings Vol. 14), S. Mahajan and J. W. Corbett eds.(New York / Amsterdam / Oxford, North-Holland, 1983) p. 307.

[4] Sumino, K. (1989), in *Point and Extended Defects in Semiconductors*, G. Benedek, A. Cavallini, and W. Schröter eds. (New York/London, Plenum, 1989) p.77.

[5] Yonenaga, I. and Sumino, K. (1987), J. Appl. Phys. **62**, 1212.

[6] Yonenaga, I. and Sumino, K. (1989), J. Appl. Phys. **65**, 85.
[7] Shen, B., Sekiguchi, T., Jablonski, J. and Sumino, K. (1994), J. Appl. Phys. **76**, 4540.
[8] Sumino, K. (1992), Mater. Sci. Forum **105-110**, 139.
[9] Bourret, A., Thibault-Desseaux, J., and Seidman, D.N. (1984), J. Appl. Phys. **55**, 825.
[10] Tempelhoff, K., Spiegelberg, F. Gleichmann, R., and Wruck, D. (1979), phys. stat. sol. (a) **56**, 213.
[11] Bender, H. (1984), phys. stat. sol. (a) **86**, 245.
[12] Minowa, K. and Sumino, K. (1993), unpublished work : Minowa K. PhD Thesis, Tohoku Univ. 1993.
[13] Minowa. K., Yonenaga, I. and Sumino, K. (1991), Materials Letters **11**, 164.
[14] Cahn, J.W. (1957), Acta Metall. **5**, 169.
[15] Sumino, K. and Imai, M. (1983), Philos. Mag. A**47**, 753.
[16] Yonenaga, I. and Sumino, K. (1996), J. Appl. Phys. **80**, in press.
[17] Kusanagi, S., Sekiguchi, T., Shen, B. and Sumino, K. (1995), Mater. Sci. Technol. **11**, 685.
[18] Sekiguchi, T., Kusanagi, S., Shen, B. and Sumino, K. (1994), in *Proc. 7th Internatl. Symp. Silicon Materials Science and Technology,* H. R. Huff, W. Bergholz and K. Sumino eds. (Electrochemical Society, Pennington, N.J., 1994) p.635.
[19] Shen, B., Sekiguchi, T. and Sumino, K. (1996), Jpn. J. Appl. Phys. **35**, in press.
[20] Nes, E. (1978), Acta Metall. **22**, 81.
[21] Solberg, J. K. and Nes, E. (1978), J. Mater. Sci. **13**, 2233.

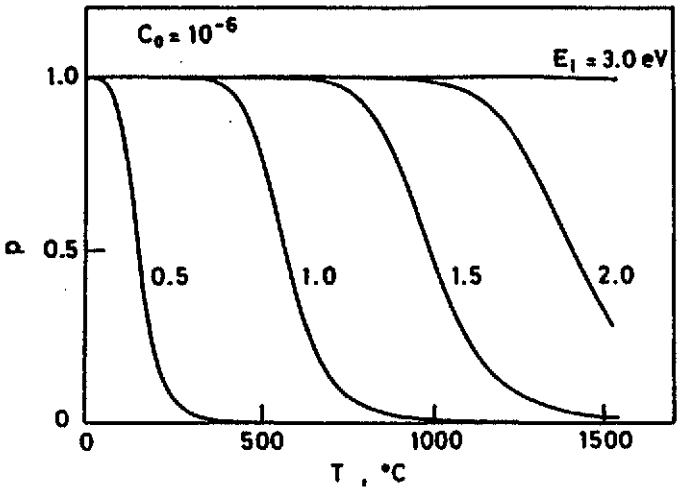


Fig. 1 Occupation probability p in thermal equilibrium of impurity atom at site with interaction energy E_i plotted as function of temperature T for impurity concentration of 1 ppm and various values of E_i [4]

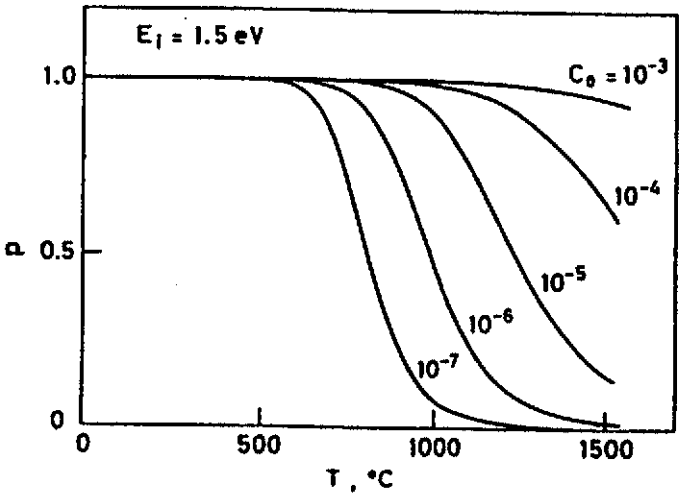


Fig. 2 Effect of impurity concentration C_0 on variation of p in thermal equilibrium for impurity atom at site with interaction energy of 1.5 eV as function of T [4]

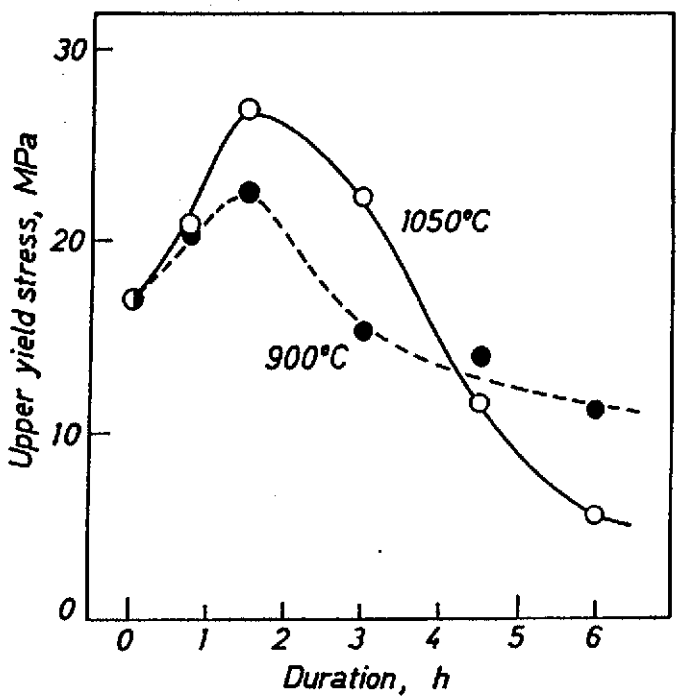


Fig. 3 Variation of upper yield stress of dislocated CZ-Si crystal plotted against duration of annealing at 1050 ℃ and 900 ℃ after solution treatment at 1300 ℃ for 2 h [16]

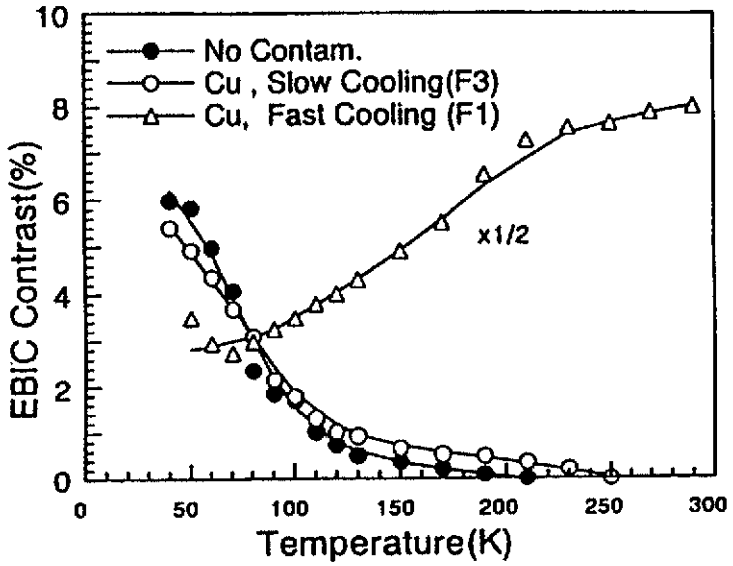


Fig. 4 EBIC contrast of Frank partial plotted against temperature in nondoped crystal and crystals doped with Cu at 1000 ℃ and cooled slow (F3) and fast (F1) [7]

REDISTRIBUTION OF IMPURITIES DURING SILICON SOLIDIFICATION

T. F. Ciszek

National Renewable Energy Laboratory
Golden, CO 80401 USA

Impurity redistribution takes place during silicon solidification by several mechanisms including segregation, evaporation, crucible/melt interaction, ambient/melt interaction, and longer-range interactions between hot-zone components and silicon. This paper discusses impurity segregation and evaporation effects in detail and also provides some examples of other impurity interactions.

INTRODUCTION

The primary means of impurity redistribution when silicon solidifies in an inert gas ambient is segregation. If solidification takes place in a high vacuum, there can also be appreciable impurity evaporation contributions to the impurity distribution. We will examine equations that govern the segregation and evaporation effects, using the idealized geometry of a cylindrical melt zone moving along a rod of silicon such that silicon is melted at one end of the zone and solidified at the other end. At the end of the rod, the last zone solidifies by normal freezing. Thus this geometry approximates float zoning. The melt solidification in the last zone to freeze approximates casting and directional solidification, and is also a reasonable representation of Czochralski (CZ) growth. Equations governing segregation and evaporation of impurities in these idealized cases are presented, and examples of distribution behavior for selected impurities (Al, Sb, As, B, Cu, Ga, Au, In, Fe, Mn, and P) in Si are given.

Differences in the mechanism of growth on and off facets can affect the microscopic distribution of impurities in dislocation-free silicon crystals. Some examples of this effect are presented in this paper. Impurities can also enter through the growth ambient. Any crucible container also is a source of impurities, e.g., O from quartz crucibles and C from the graphite crucibles or dies sometimes used in ribbon growth or casting.

IMPURITY SEGREGATION AND EVAPORATION EQUATIONS

In the general case, impurity redistribution is affected both by segregation and evaporation. The evaporation effect is only pronounced when growth is conducted in a vacuum ambient. We consider a long silicon ingot with initial uniform concentration C_o of any given impurity. One end of the ingot is melted, and a molten zone is moved along the rod at a travel rate f. Impurity evaporation increases as f decreases, because the molten zone is then exposed to vacuum for a longer time. Evaporation also increases as the ratio of free surface area to volume of the molten zone increases. Longer molten zones experience greater evaporation. Thus, the effective evaporation coefficient g is a function of specific growth conditions, as is the effective segregation coefficient k. Segregation increases as k decreases, but evaporation increases as g increases. Peizulaev [1] has derived an expression for the impurity distribution in an ingot after n zone passes, when both evaporation and segregation are operative:

$$C_n(x)/C_o = [k/(k+g)]^n[1-(1-k-g)Z_n e^{-(k+g)x}], \quad [1]$$

where

$$Z_n = n - \sum_{s=1}^{n-1}(n-s)(k+g)^{s-1}e^{-s(k+g)}[(s+x)^{s-2}/s!]\{(s-1)x + (s+x)[1-(k+g)x]\} \quad [2]$$

and n is the number of times the ingot is zone melted, k is the effective segregation coefficient, g is the effective evaporation coefficient, and $C_n(x)$ is the impurity concentration at position x along the ingot (x is in units of melt zone length) after n solidification passes.

For an ingot that is N melt zones long, the impurity concentration profile in the last melt zone to freeze (that is, for $N-1 < x < N$) is expressed by

$$C_n(x) = C_n (N-1)(N-x)^{(k-1)}e^{-g[x-(N-1)]}. \quad [3]$$

While equations 1, 2, and 3 together describe the impurity profiles resulting from zone refining or float zoning (FZ), they are also applicable to continuous casting techniques such as electromagnetic continuous casting, and in fact, to any silicon solidification process that uses melt replenishment, such as continuous Czochralski growth, continuous dendritic web growth, or continuous edge-defined, film-fed growth (EFG) (i.e., basically any method in which source material is continuously fed into a molten zone at the same rate as the product silicon is withdrawn). Of course the effective segregation and evaporation coefficients and the size and geometry of the molten zone may be very different for various growth methods.

Equation 3, taken by itself, is essentially the normal freezing equation. It thus describes the impurity concentration profile for techniques such as normal CZ, batch casting, batch directional solidification, or ribbon growth from a non-replenished melt (i.e. basically any growth method with a fixed, initial charge that is completely melted before the growth process is started). Again, the effective segregation and evaporation coefficients can be quite different for different growth methods.

In the case of a nearly cylindrical melt geometry with evaporative impurity loss from the cylindrical surface, g is a function of zone length ℓ, ingot radius r, and solidification rate f. In addition to the variable parameters, g also depends on fixed parameters such as the molar volume V of the host material (Si), the molar evaporation time τ of the impurity (the time required for one mole of the "pure" impurity to evaporate from 1 cm^2 surface area at a temperature equal to the zone melting temperature, the activity coefficient γ of the impurity, in the molten silicon host, and the Langmuir coefficient α for the impurity. The expression for g is then given by [1]

$$g = 2V\alpha\ell\gamma/\tau rf \quad [4]$$

The effective evaporation coefficient can also be experimentally obtained.

A few representative graphical representations of equations 1-3 are presented in Fig. 1, for ingots that are 20 zone-lengths long. Two of the three parameters -- g, k, and n -- are fixed in each case, while the other is varied to generate a family of curves. In Figs. 1a and 1b, g is the varied parameter. Its behavior is shown for one zone pass and the cases of strong segregation (k = 0.00001; Fig. 1a) and weak segregation (k = 0.1; Fig. 1b). In Figs. 1c and 1d, k is the varied parameter. Again n=1. The cases of weak evaporation (g = 0.2; Fig. 1c) and moderately strong evaporation (g = 5; Fig. 1d) are displayed. The number of zone passes n is the varied parameter in Figs. 1e and 1f. The value of k is 0.1 in both. The evaporation is weak (g = 0.2) in Fig. 1e and moderately strong (g = 5) in Fig. 1f.

For n > 1, the equations are not valid in the last n zone-lengths of the ingot. These regions are thus treated as though the ingot length is semi-infinite, and the curves are shown as dashed lines.

EXAMPLES FOR SELECTED IMPURITIES IN SILICON

Float-zoning (continuous solidification processes)

Using equations [1-3] and the effective segregation coefficients and effective evaporation coefficients from Table I for selected impurities in silicon, and assuming f = 3 mm/min, a cylindrical ingot, and a melt height equal to the ingot diameter, the calculated concentration profiles for the selected impurities after a single ingot solidification in argon (g=0) and in a vacuum are shown in Figs. 2a and 2b. Additional solidification passes further reduce the impurity concentrations. For example, Figs. 2c and 2d show the reduction after two passes (n=2) and three passes (n=3), respectively, in vacuum. With appropriate values of k and g, these equations are applicable to most melt-replenished, semicontinuous Si growth methods.

Table I. Effective segregation coefficients and evaporation coefficients for selected impurities in silicon

Impurity	Effective segregation coefficient	Effective evaporation coefficient
Al	0.003 [a)]	0.2 [e)]
Sb	0.07 [a)]	100 [e)]
As	0.5 [a)]	7 [e)]
B	0.9 [a)]	0.007 [e)]
Cu	0.04 [b)]	0.035 [b)]
Ga	0.014 [a)]	1.7 [e)]
Au	0.004 [b)]	0.012 [b)]
In	0.007 [a)]	7 [e)]
Fe	0.00001 [c)]	0.035 [e)]
Mn	0.00005 [c)]	0.35 [e)]
P	0.45 [d)]	0.71 [d)]

[a)] Calculated from equilibrium values [see e.g. Keller and Muhlbauer (2)]
[b)] From Hadamovsky (3).
[c)] Equilibrium (not effective) value
[d)] From Ziegler (4)
[e)] Theoretical value calculated from Bradshaw and Mlavsky (5) by Crossman (6), under the same assumptions used here for melt height and growth rate.

Directional Solidification (batch solidification processes)

In addition to describing the last zone to freeze in a zone refining process, equation 3 also applies to the directional solidification of batch melts. In Fig. 3, equation 3 is plotted for the same impurities listed in Table I, for growth in >1-bar argon (g~0, Fig. 3a) and in vacuum (Fig. 3b). With appropriate determination of the effective segregation and evaporation coefficients, equation 3 is relevant to most batch growth processes for silicon (CZ, EFG, dendritic web, batch casting, etc.).

Other Impurity Redistribution Mechanisms

In dislocation-free silicon growth, the growth mechanisms on and off (111) facets are different. The facets form because of the supercooling needed to nucleate new growth layers. Once nucleation takes place, rapid lateral growth sweeps up impurities and causes a locally enhanced impurity concentration in the facet region of the crystal.

Silicon crucible interaction is present in typical CZ growth systems. The SiO_2 crucible partially dissolves, contaminating the melt with oxygen, which then enters the growing crystal. The magnitude of the effect depends on the convective motion at the crucible-melt interface, the roughness of the crucible surface, and the composition and pressure of the growth ambient. A similar problem is seen with carbon crucibles used in some ribbon and casting systems. Crucible-free systems such as float zoning or electromagnetic (cold-crucible) melt confinement of course produce cleaner material. The choice of ambient also plays a role in the purity of the solidified silicon.

SUMMARY AND DISCUSSION

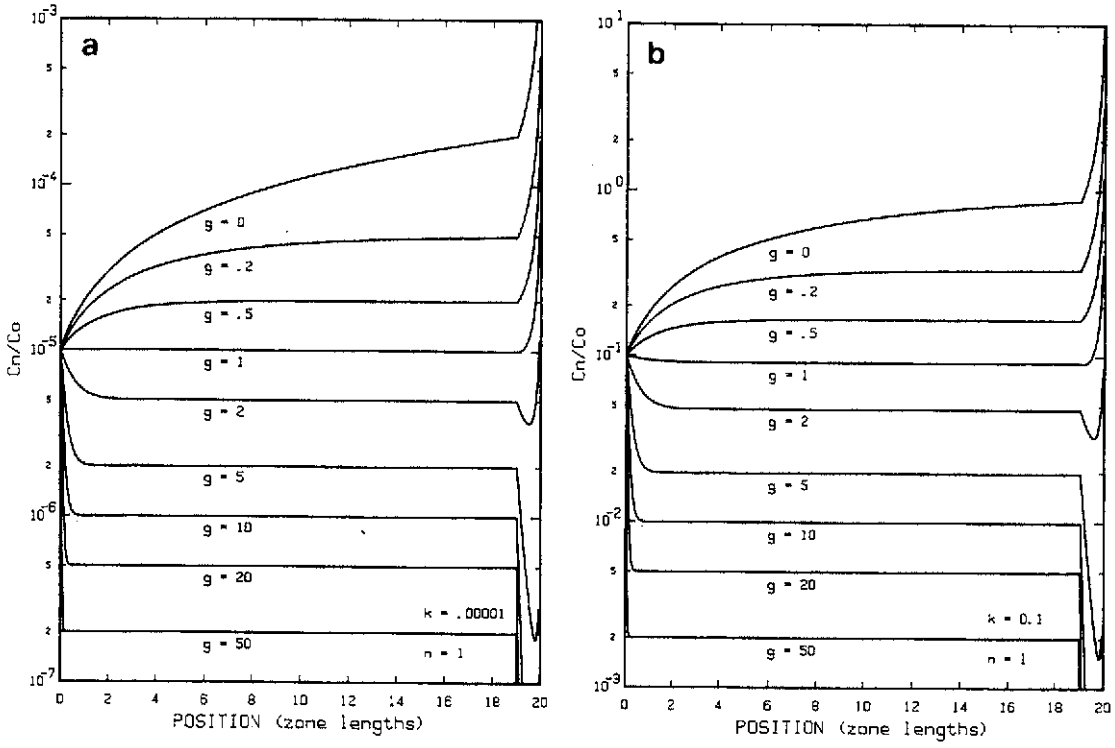
The equations describing impurity segregation and evaporation have been discussed, and graphical examples of impurity distributions were presented. While idealized for the case of cylindrical ingots and melts, the equations are also applicable to nearly all batch growth processes (e.g., CZ, casting, directional solidification, or ribbon growth from batch melts) and semicontinuous growth processes (e.g., float-zoning, continuous CZ growth, continuous ribbon growth, or electromagnetic continuous casting), providing that the appropriate values for effective segregation coefficient and effective evaporation coefficient are determined and used.

ACKNOWLEDGMENTS

Support for this work was provided by the United States Department of Energy under NREL contract DE-AC36-83CH10093.

REFERENCES

1. S. Peizulaev, *Inorgan. Mater.*, **3**, 1329 (1967).
2. W. Keller and A. Muhlbauer, *Floating-Zone Silicon*, pp. 116-153, Dekker, New York (1981).
3. H. F. Hadamovsky, *Kristall Tech.*, **2**, 415 (1967)
4. G. Ziegler, *Z. Metalik.*, **49**, 491 (1958)
5. S. E. Bradshaw and A. I. Mlavsky, *J. Electron.*, **2**, 134 (1956).
6. L. Crossman, private communication.


a
b
Cn/Co
POSITION (zone lengths)
g = 0
g = .2
g = .5
g = 1
g = 2
g = 5
g = 10
g = 20
g = 50
k = .00001
k = 0.1
n = 1

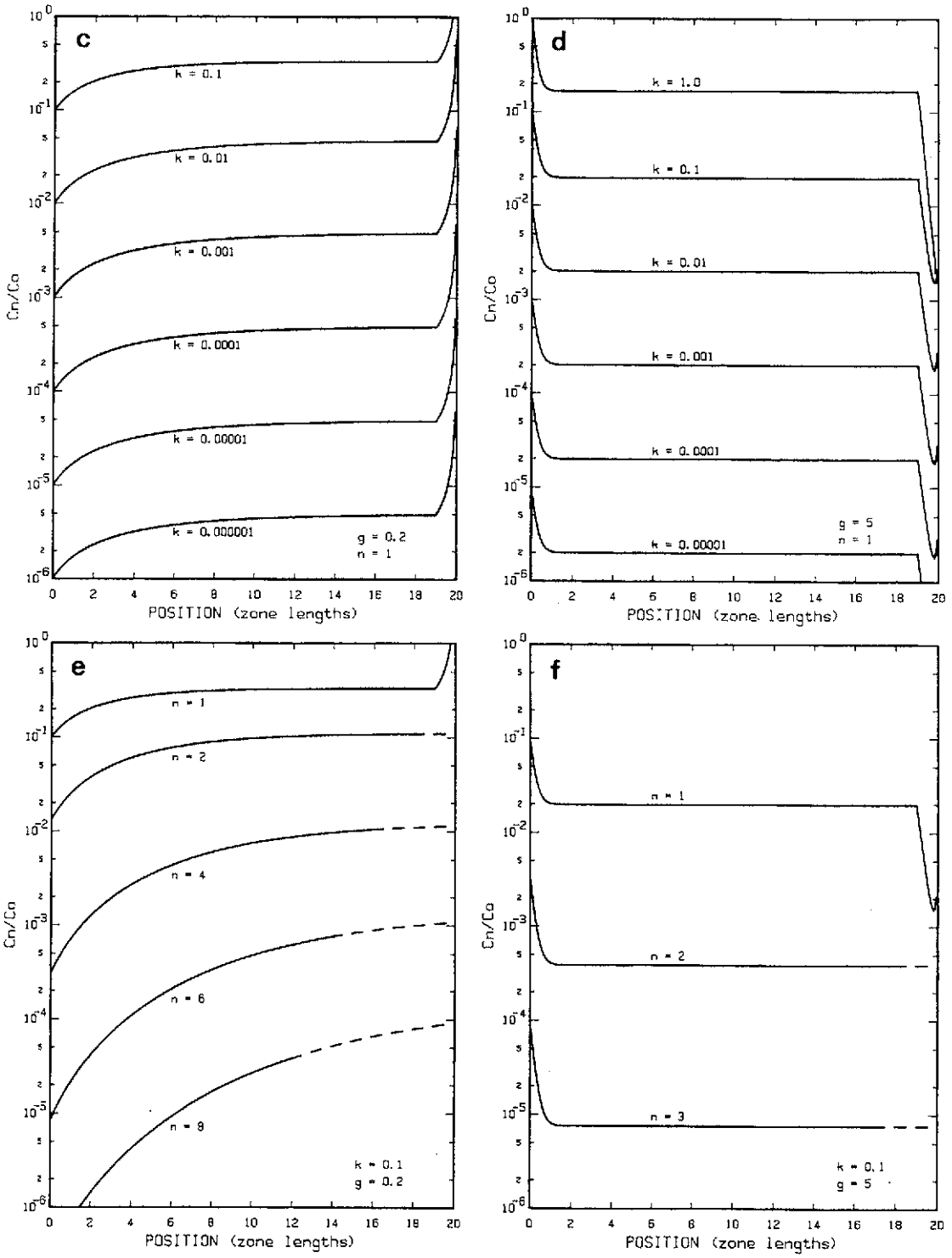


Fig. 1. Impurity concentration profiles (assuming C_0 is constant) for several values of k, g, and n: (a) $k = 0.00001$, $n = 1$; (b) $k = 0.1$, $n = 1$; (c) $g = 0.2$, $n = 1$; (d) $g = 5$, $n = 1$; (e) $k = 0.1$, $g = 0.2$; (f) $k = 0.1$, $g = 5$.

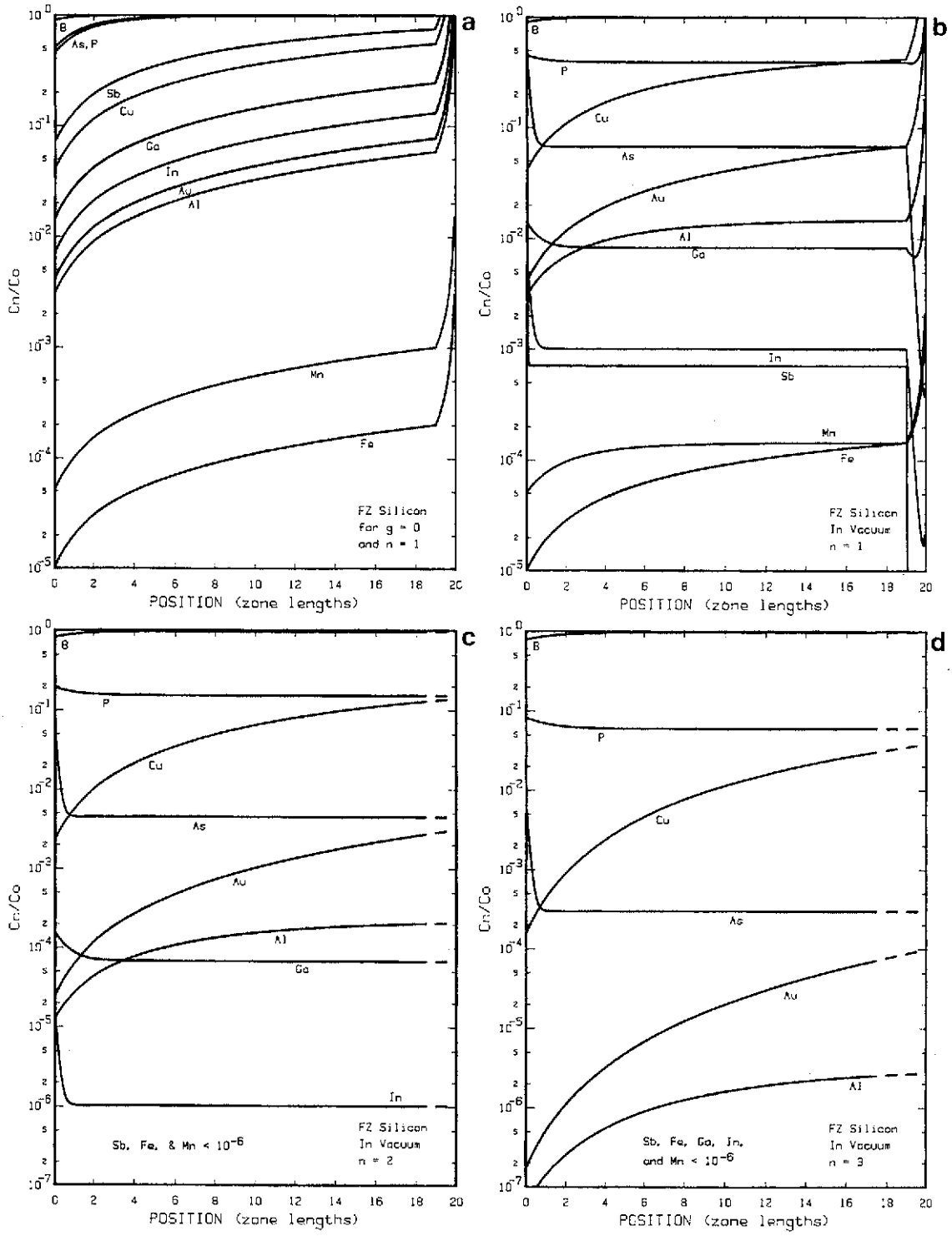


Fig. 2. Impurity concentration profiles (assuming C_0 is constant) for several impurities in float-zoned silicon: (a) one pass with no evaporation, (b) one pass in vacuum, (c) two passes in vacuum, and (d) three passes in vacuum.

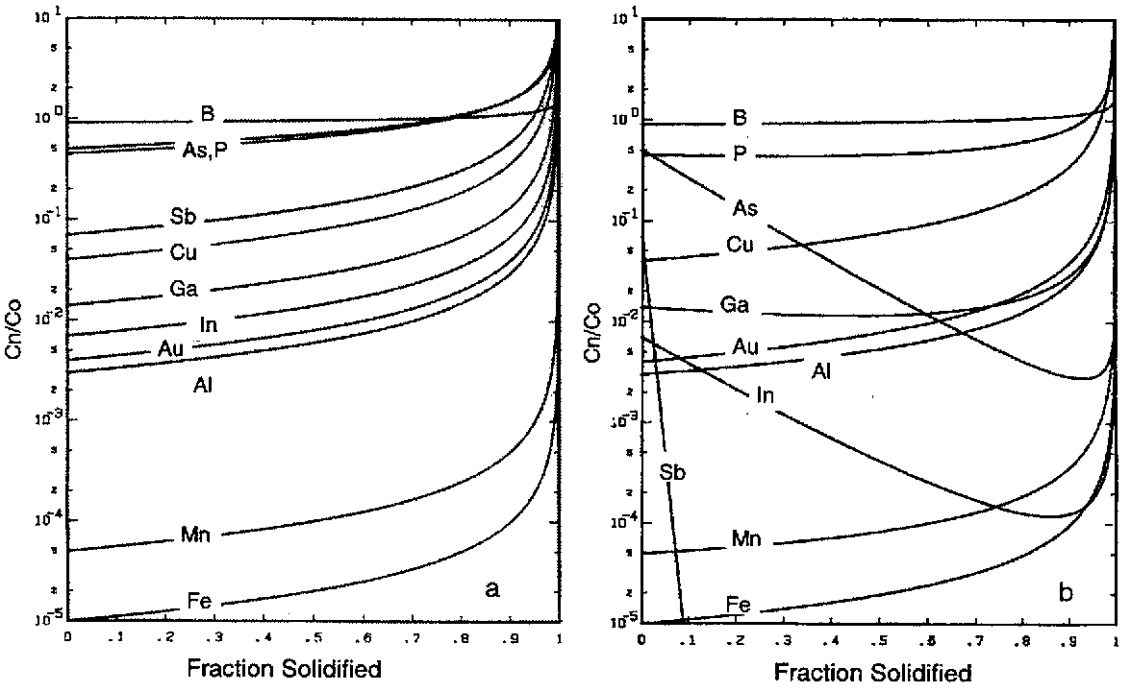


Fig. 3. Impurity concentration profiles for selected impurities in directional solidification or batch growth: (a) in argon at > 1-bar pressure (g~0) and (b) in vacuum

CURRENT STATUS OF THE POLYCRYSTALLINE SILICON INDUSTRY

James R. McCormick
Hemlock Semiconductor Corporation
Hemlock, Michigan

Polycrystalline silicon was identified as a key raw material for photovoltaic applications at the inception of the U. S. Solar Energy Program in the early seventies. It has also been the basic raw material for the Global Semiconductor Industry for the past three decades. In 1995, a Polycrystalline Silicon Industry with sales of approximately 600 million dollars, supported a 150 billion dollar Semiconductor Industry. In the past twenty years, polycrystalline silicon production has grown from approximately 1200 tonnes per year in 1975 to 12,000 tonnes per year in 1995. Plant size has increased from the 100 to 500 tonnes/year capacity to the 1000 to 3000 tonnes/year level. Increments of capacity addition have increased from a few hundred tonnes to the 1000 to 2000 tonne level. During this period, costs have been contained with prices today being less than they were two decades ago, while in constant dollar terms, today's prices are one half to one third those experienced two decades ago. Product quality has been steadily improved to meet the needs of the semiconductor industry during this time frame. The concentration of principle electronically active impurities (boron and phosphorus) are now one fifth or less the concentrations found in polycrystalline silicon two decades ago, and the carbon concentration in polycrystalline silicon has been reduced by an order of magnitude in the same time period. Total metals concentration, which was seldom specified twenty years ago, is now less than 5 parts per billion atomic and decreasing each year.

The polycrystalline silicon materials requirements of the Photovoltaic Industry have been met during most of this twenty year period, 1975-1995, by fallout material from the Semiconductor Industry. Material supplied by the single crystal manufacturers has consisted primarily of defective crystals, as well as tang ends and the shoulder area of normal production ingots. Polycrystalline silicon producers have supplied materials having elevated impurity concentrations that failed to meet semiconductor customer specifications, rough surface material which was unacceptable to semiconductor wafer manufacturers, and material produced in the breaking process employed to produce polycrystalline silicon chunks that failed to meet customer size specifications.

The historic supply/demand situation for the polycrystalline silicon industry is shown in Figure 1. The "presumed" demand for polycrystalline silicon in the early nineteen eighties, which peaked in 1984 when there was a year-to-year growth of 100% in semiconductor bookings, resulted in the construction of several new factories for polycrystalline silicon production. The subsequent collapse in semiconductor device demand in 1985 and a relatively slow growth rate in semiconductor sales in the 1985-1990 time frame resulted in a substantial excess in polycrystalline silicon production capacity throughout this period. It has only been in the past few years that polycrystalline silicon supply and demand have returned to a reasonable balance. The impact of this shift

in the supply/demand situation has substantially changed the availability of polycrystalline silicon for photovoltaic applications as both single crystal and polycrystalline silicon producers attempt to meet the needs of the integrated circuit and discrete devices manufacturers.

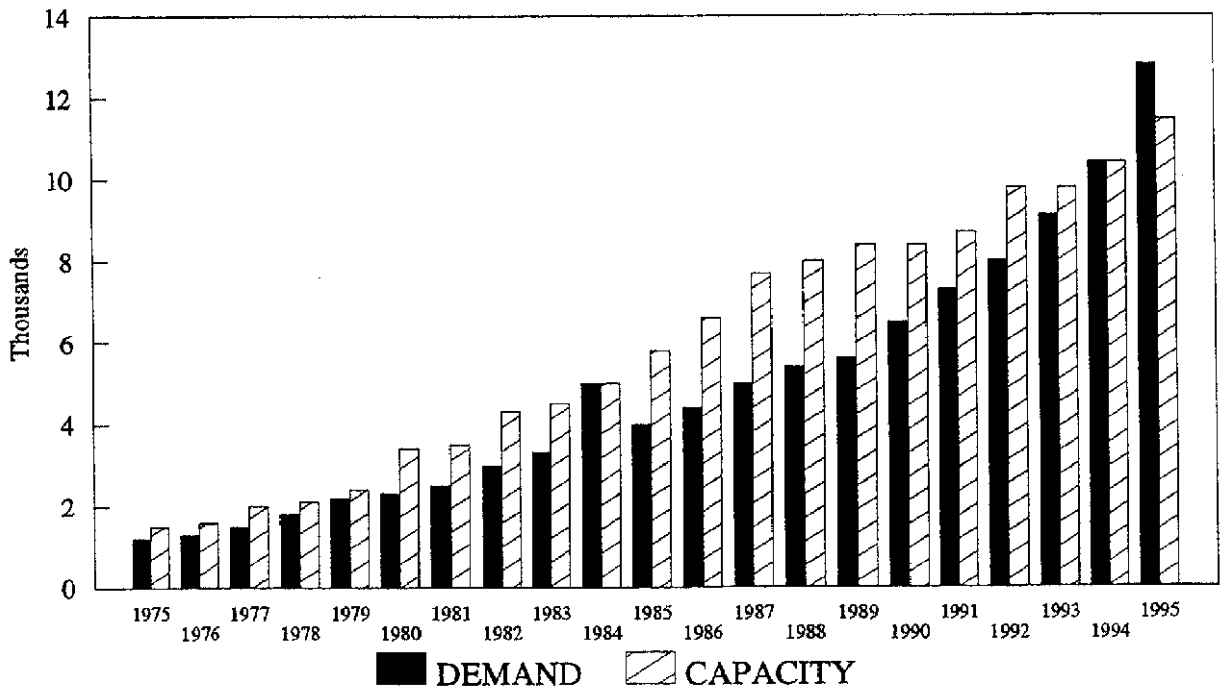
There have, in the past decade, been some process technology changes in the polycrystalline silicon industry. Prior to 1995, essentially all polycrystalline silicon was produced by the high temperature deposition of polycrystalline silicon on a silicon substrate using trichlorosilane as the silicon source intermediate (the Siemens Process). Metallurgical grade silicon was the basic raw material. This process is summarized in Figure 2a. Metallurgical grade silicon and anhydrous hydrogen chloride are reacted to produce trichlorosilane which is then decomposed to produce semiconductor grade polycrystalline silicon. Obviously there are numerous purification, recovery and recycle steps contained in the process that are not shown in this simplified process diagram. Numerous technology changes have also been made within the process to improve product quality and enhance process economics. Approximately eighty percent of the polycrystalline silicon produced today continues to be based on this process. Figure 2b and 2c describe two other commercial processes currently used to produce high purity polycrystalline silicon. Process 2b uses metallurgical grade silicon and silicon tetrachloride as silicon source materials to produce trichlorosilane and ultimately silane. The silane is then decomposed on a silicon substrate at high temperature to produce silicon rods. Rods produced by this process and the Siemens process are eventually broken into silicon chunks for use in the Czochralski crystal growth. The third polycrystalline silicon production process begins with a different silicon source material, fluorosilicic acid, which is converted to silicon tetrafluoride and then to silane before undergoing decomposition in a fluidized bed reactor to produce granular polycrystalline silicon. A by-product of this process is sodium aluminum fluoride. This process is illustrated in Figure 2c. The various intermediate chemical species produced in all of these processes, silane, trichlorosilane, dichlorosilane, and silicontetrachloride, are normally marketed to the semiconductor and other industries.

Growth in semiconductor sales for the 1993-1995 time frame was exceptional, growing at a rate of nearly 30% a year with 1995 sales growth at 40%. This compares to an average compound growth rate of only 9.5% for the decade of the eighties. Future growth projections for the remainder of the decade, while substantially lower than those of the past three years, remain well above the average compound growth rate of the 1980's. Current industry projections estimate that semiconductor sales will increase from one hundred and fifty billion dollars in 1995 to three hundred billion dollars or more by the year 2000, an average compound growth rate of at least 14.8%. This doubling of sales will require comparable growth in polycrystalline silicon production. The increased complexity and reduced element size for future integrated circuits, coupled with the use of larger diameter silicon wafers will impose more stringent material requirements on polycrystalline silicon. It is anticipated that the level of essentially all impurities in polycrystalline silicon will need to be reduced during the next five years. This could

benefit the photovoltaic industry by increasing both the level of fallout material and the overall quality of this material.

Essentially all polycrystalline silicon manufacturers have announced plans to expand their production capacity between now and the end of this decade. The current industry capacity is approximately 13,000 tonnes per year. The announced capacity additions will increase polycrystalline silicon supply capability in the year 2000 into the 21,500 tonnes/year to 25,700 tonnes/year range. This range of capacities should bracket the projected demand based on the compound growth rate projected for Semiconductor Industry sales. These major increases in polycrystalline silicon production capacity will meet the material requirements of the Semiconductor Industry but they are focused strictly on that Industry. Proportionately more of the traditional "fallout material" that has met the raw material needs of silicon photovoltaic applications will be generated. A doubling in the quantity of this material can be anticipated in the next five years. Availability of this material for photovoltaic applications will be determined on a year to year basis by the market conditions in the semiconductor segment.

FIGURE 1 POLYCRYSTALLINE SILICON CAPACITY/DEMAND OVER THE PAST TWO DECADES



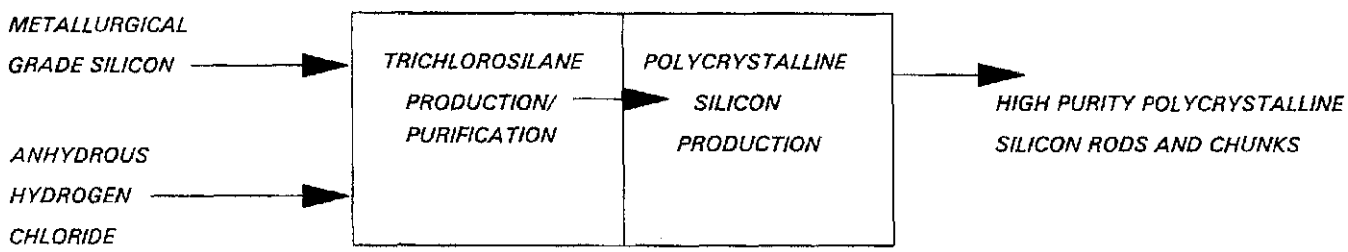


FIGURE 2a

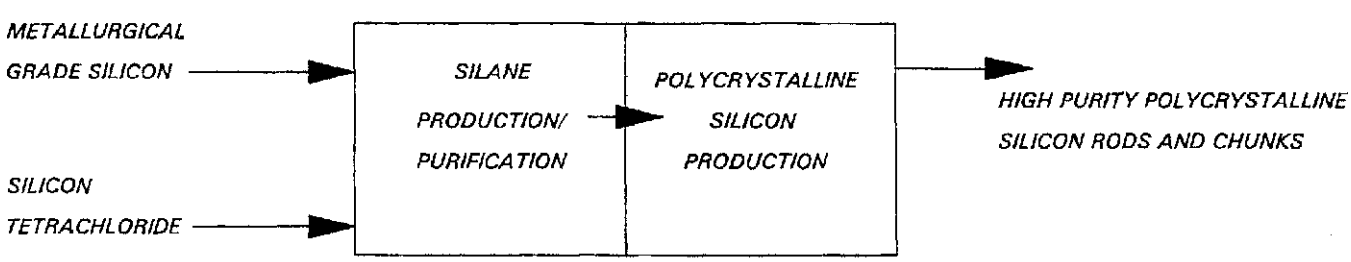


FIGURE 2b

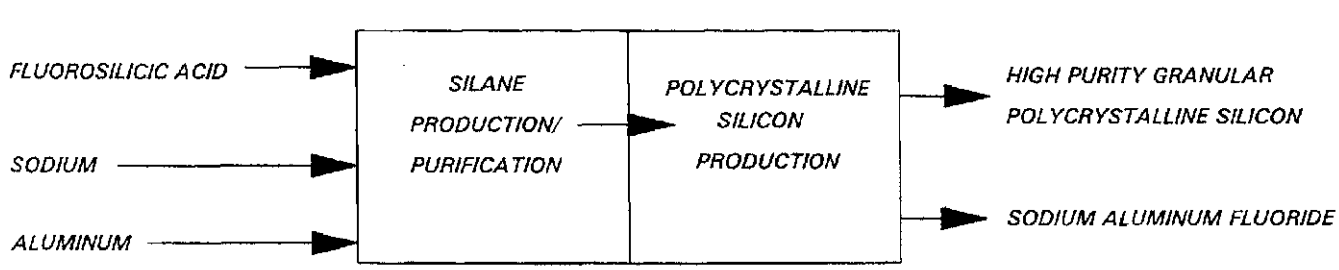


FIGURE 2c

FIGURE 2 Simplified process diagrams of commercial processes currently used for the production of high purity polycrystalline silicon

Which Silicon Materials Parameters are Critical to Solar Cell Design and Resulting Efficiency?

Ronald A. Sinton
Sinton Consulting
San Jose, CA

Abstract:

During the last decade, a number of numerical modeling tools have become widely available to aid in the evaluation of solar cell design and in the interpretation of test data. In many cases, this has provided a common foundation for comparison and discussion of results across company and research group boundaries. In a workshop on the role of impurities and defects in silicon processing, it is useful to understand how the information resulting from this improved fundamental knowledge will most likely be applied in the optimization of silicon solar cells. This paper will review some aspects of the influence of critical materials parameters on the design and performance of several current categories of silicon solar cells emphasizing the form of reporting of these results that would prove most immediately useful to solar cell design and optimization. The focus will be on lifetime data and modeling.

Introduction:

The physical properties of the silicon solar cell that most control its performance are:

1. Majority- and minority-carrier mobility
2. Majority-carrier density
3. Light absorption
5. Lifetime in bulk and doped regions
6. Surface recombination
7. Contact and metallization resistance

In crystalline silicon, the first two parameters, mobility and majority-carrier density, are relatively well-known parameters that depend nominally on the doping levels alone. Standard models for these are more or less automatic in modeling tools such as PC-1D (1). Light absorption is a fundamental property of the crystalline silicon, and is also relatively fixed and well known. An appropriate optical design, using light-trapping if possible, is used to maximize the available photogeneration. In cases where deviations from the common models are detailed in fundamental research, it may not be sufficient to simply publish these results or discuss them at workshops. The influence of the modeling tools is great enough that fundamental results may not have a significant effect on solar cell technology until these results are actually incorporated into the modeling programs to demonstrate the practical consequences.

The lifetime and surface recombination parameters are extremely dependent on the substrate material, device design, and process design and execution. These are where the most important results from this workshop are most likely to be incorporated. Most solar cell device modeling for silicon solar cells incorporates the properties of defects and impurities only through the lifetime parameter and an empirical form of shunt that can be imposed on the solar cell characteristic.

The Example of Minority-Carrier Lifetime:

One of the most comprehensive studies to date on the effects of impurities on silicon solar cells is the work by Davis et al. (2,3). In this work, over 200 boules of silicon were grown including intentional contamination by a variety of elements in order to evaluate the effects on lifetime and therefore efficiency. At that time, the best way to characterize and report the effects of these impurities was to actually fabricate solar cells and measure their performance in comparison to a baseline case. These solar cells were of a design with a thick substrate, such that the solar cell performance was primarily a function of the diffusion length. Similar work has been done for multi-crystalline wafers on a more limited scale(4).

In the snapshot provided by the Davis papers, it was indicated that for this particular solar cell technology on these particular CZ substrates, a variety of impurities affected the solar cell efficiency primarily through the effect on the lifetime (Al, Cr, Mn, Mo, P, Ta, V, Zr, W, Co, Nb). Three impurities also had a major effect on the cell efficiency through junction shunting. These impurities were Fe, Cu, and Ni.

Current solar cell designs, processes, and substrate types are more varied. One class of solar cell is the very-high efficiency solar cells in the 22-24% range. Another broad class includes Al Back-Surface-Field solar cells on single- and multi-crystalline silicon, capable of efficiencies approaching 19% (neglecting shadow and series resistance losses). A third category is thin-film-silicon solar cells.

Modeling from PC-1D indicates the trends in required lifetime for each of these classes of solar cells as a function of the substrate doping level. Both the 23% cells and the 19% BSF solar cells are assumed for simplicity to be 200 microns thick. The last category, thin-film solar cells, is represented here by cells identical to the BSF cells in all respects except for a thickness of 20 microns. These results are shown in Figure 1. Also shown is the default curve for the lifetime limits as calculated in Version 4.1 of this program. How these lifetimes might be achieved is the topic of detailed studies on material growth, fabrication processes, gettering, and defect passivation.

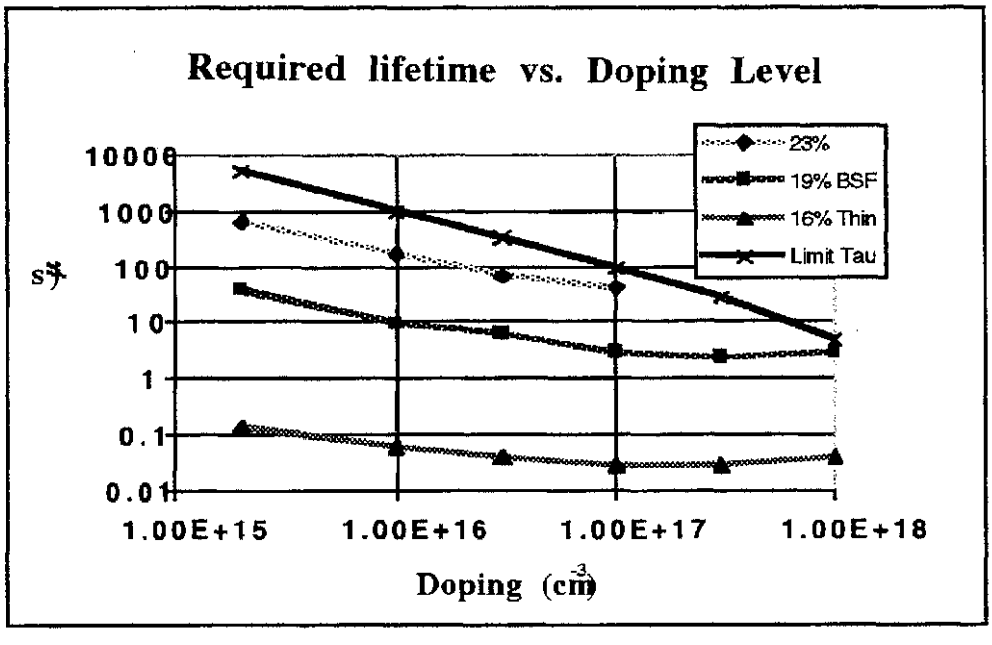


Figure 1. *Results from simulations of the required bulk lifetime to achieve the target efficiency for three example technologies.*

Although more complete alternatives are available within the modeling tools, it is most common to assume a lifetime parameter that is indicative of the low-level-injection lifetime and is constant as a function of the injection level with the exception of the effect of entering the high-level injection regime. The weakness in this practice is that most defects and impurities result in a lifetime that is decidedly NOT a constant as a function of the injection level. One well-known example is the lifetime of Fe-contaminated silicon (5). Fe has a strong injection-level dependence that distinguishes it from other elements and even can be used to identify the form that it resides in the silicon, dissolved or as Fe-B pairs. In order to do this with precision, the lifetime must be measured at a consistent injection level(5).

Similarly, in order to be relevant for the design and modeling of silicon solar cells it must be determined at the most relevant injection level. In general, it is well known that material properties measured without the use of some bias light are often misleading with respect to predicting solar cell performance.

The lifetime that is best for modeling solar cell performance is the lifetime corresponding to operation at the maximum power point. This would be given by:

Minority carrier density = $(n_i^2/N_A)\ln((qV_{mp})/kT)$.

Typically, this would be evaluated at a maximum power point between 500 and 600 mV, depending on the target efficiency of the solar cell technology.

In cases where the lifetime measurement technique used corresponds to an open-circuit condition, such as with transient photoconductance decay, steady-state photoconductance or OCVD, this can be accomplished directly by evaluating the lifetime at this injection level. If the injection level is not determined explicitly in the measurement, a good approximation would be to use one-twentieth to one-tenth of one sun of light bias.

For measurement techniques corresponding more to a short-circuit condition, such as spectral response measurements, the best strategy would be to perform the measurement at one sun of light bias.

Conclusions:

In order to maximize the impact of fundamental research on solar cell technology, several questions should be asked:

1) What physical model for the effect is currently used in solar cell modeling?

2) Is the model correct?

3) Are there significant deviations for special cases?

4) What form of reporting results is most likely to be incorporated into the device modeling in the most relevant way?

The particular case of the minority carrier lifetime as a function of material, impurity and defect parameters was discussed in more detail. Relevance depends on an accurate knowledge of the minority-carrier lifetime evaluated at the injection level consistent with the target maximum-power voltage. This injection level will be different for each doping level in the substrate material.

References:

1) Paul Basore and Donald Clugston, To be published in the Proc. of the 25th IEEE Photovoltaic Specialist Conference. Washington, D.C., May 1996.

2) J. R. Davis, A. Rohatgi, P. Rai-Choudury, P. Blais, R. H. Hopkins, and J. R. McCormick, Proc. 13th IEEE Photovoltaics Specialist Conference, 1978, pp. 490-495.

3) J. R. Davis et al., IEEE Trans. Elec. Dev. Vol. ED-27, No. 4, April 1980, pp. 677-687.

4) J. P. Kalejs, B. R. Bathey, J. T. Borenstein, and R. W. Storment, Proc. 23rd IEEE Photovoltaics Specialist Conference, 1993, pp. 184-189.

5) K. Graff and H. Pieper, J. Electrochem. Soc.: Solid State Science and Technology, March 1981, pp. 669-674. and Abstracts from the 5th Workshop on the Role of Defects and Impurities in Silicon Device Processing, 1995.

Oxygen, Carbon and Nitrogen in Multicrystalline Silicon

H. J. Möller, D. Yang, S. Riedel
Institute for Experimental Physics, TU Bergakademie Freiberg, Silbermannstr. 1, 09599 Freiberg, Germany

M. Werner
Max-Plank Institute of Microstructure Physics, Weinberg 2, 06120 Halle, Germany

D. Wolf
Institute for Crystal Growth, Rudower Chaussee 6, 12489 Berlin, Germany

1. Introduction

Multicrystalline silicon grown by directional solidification is a low cost material for photovoltaic applications. During recent years improvements of the crystallization process have reduced the influence of grain boundaries and dislocations on the performance of solar cells. The properties of multicrystalline cells are therefore increasingly determined now by intragrain defects such as impurities, small clusters of atoms or precipitates.

Apart from the doping elements the main impurities in multicrystalline silicon are oxygen and carbon. The concentrations are generally higher in ribbon material. Since silicon nitride crucibles are increasingly used nitrogen can also be incorporated in substantial concentrations.

Oxygen is known to affect the conversion efficiency of solar cells. Both for Cz - and multicrystalline silicon an improvement of the solar cell performance as well as a degradation has been reported [1, 2]. Carbon and nitrogen can influence the electrical behavior of oxygen and are thus important as well. In this paper a systematic study is performed to identify intragrain defects in multicrystalline ingot silicon and RGS ribbons and to determine the role of these impurities in the formation of defects and the ramifications on the solar cell performance.

2. Experimental Procedure and Results

2.1 Selective etching of microdefects

Extended defects in multicrystalline silicon can be observed by selective etching. Figure 1 shows a typical example where in addition to the large etch pits from dislocations shallow pits occur. Repeated etching after the removal of a thin surface layer shows that the defects are small precipitates. They occur both in ingot silicon from various suppliers, in RGS ribbons, and in CVD and LPE thin films deposited on multicrystalline silicon substrates. The density of the shallow etch pits varies between 10^5 to 10^8 cm^{-2}.

In general, the preparation of the surface before the selective etching is a crucial step for the identification. Basically two different types of polishing procedures are commonly used : polishing with non-alkaline slurries for instance with diamond paste and chemomechanical procedures with alkaline slurries. We found that after chemomechanical polishing more microdefects become visible by selective etching. A systematic study of the impact of chemomechanical polishing on the etching behavior of swirl defects in Fz - silicon has shown that this effect may be due to the decoration with copper [3]. Intentional decoration of the defects in mc - silicon by in-diffusion of copper, lithium or hydrogen, however, were unsuccessful so far. This is probably due to the much stronger gettering efficiency of dislocations and grain boundaries in the material.

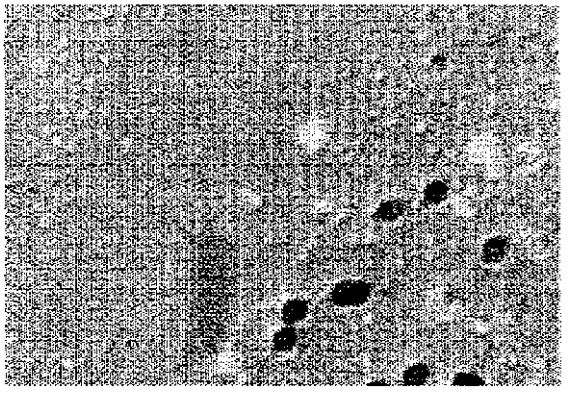


Figure 1 Shallow etch pits of microdefects in multicrystalline silicon after chemomechanical polishing and selective etching. Large etch pits are dislocations. (1 cm ≡ 8 μm).

2.2 FTIR Measurements

Considering the impurities that are present with sufficient concentrations to form precipitates oxygen, carbon and possibly nitrogen are the main candidates. One may also have to take into account transition elements such as iron, chromium, or nickel, and vacancies and interstitials that at least in monocrystalline silicon are known to form swirl defects under certain growth conditions.

During crystal growth and solar cell processing the material experiences several high temperature annealing treatments. The temperature regime around 800 - 1050 °C is particularly important for the diffusion of phosphorous to form the p-n junction. Therefore systematic FTIR measurements were carried out to determine the dissolved oxygen, carbon and nitrogen distribution and their annealing behavior in ingot silicon.

A typical distribution of the impurities in the center of an ingot is shown in figure 2. The concentration of the elements is below the maximum solubility at the melting point. The maximum values for oxygen are comparable to Cz - silicon while the maximum carbon and nitrogen concentrations are usually higher.

2.3 Oxygen

The annealing behavior of oxygen was studied in multicrystalline silicon specimens with various initial oxygen and low carbon concentrations (below the detection limit of 5 x 10^{15} cm^{-3}). The results show that the previous thermal history of

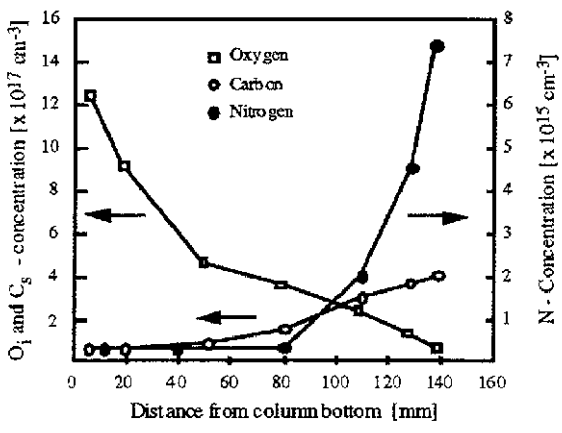


Figure 2 Vertical distribution of oxygen, carbon and nitrogen in an ingot of mc silicon.

the specimens has an influence on the annealing behavior. Therefore the specimens were preannealed at 1260 °C for 1 hour which turned out to be sufficient to eliminate any previously formed nucleation centers that are responsible for an enhanced precipitation of oxygen. The specimens were annealed then at different temperatures between 2 to 24 hours. The results are summarized in figure 3.

The main result is that the oxygen concentration decreases between 750 - 1050 °C. The corresponding FTIR spectra confirm the formation of the SiO_2 phase. In the same temperature regime the number of shallow etch pits increases up to a density of 10^8 cm^{-2}. In addition stacking faults are observed at 1050 °C. Below an oxygen concentration of about 2 x 10^{17} cm^{-3} precipitation does not occur anymore.

The comparison with Cz - silicon with the same oxygen concentration (and no carbon) shows essentially the same precipitation behavior after preannealing at 1260 °C. Therefore it appears that the presence of dislocations and grain boundaries in mc - silicon has no influence on the precipitation process.

2.4 TEM results

TEM investigations of the same specimens were performed to study the structure of defects in the as-grown and annealed specimens. Two different types of precipitates are observed : spherical

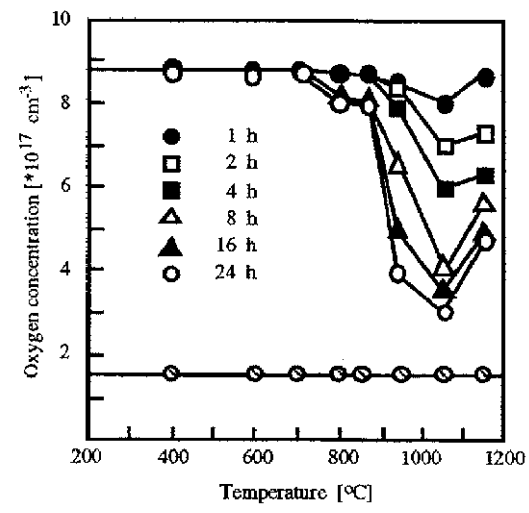


Figure 3 Concentration of interstitial oxygen in multicrystalline silicon for different annealing temperatures. Specimens are preannealed at 1260 °C for 1 hour.

Figure 4 TEM micrograph of a spherical precipitate in as-grown and annealed multicrystalline silicon (950°C for 24 hours).

defects (figure 4) and platelike defects on (111) planes (figure 5). The lattice images so far did not allow to determine the structure of the precipitates uniquely, but we assume that at least the spherical defects are amorphous SiO_2 precipitates.

The results show that above 1050 °C only the platelike precipitates are observed. In the same temperature regime the 1224 cm^{-1} absorbance line in the FTIR spectra disappears. We assume that oxygen rather diffuses now to dislocations than to precipitate in the bulk. Table 1 summarizes the results for the density and corresponding the diffusion length. It appears that at least some of the microdefects can reduce the diffusion length.

Table 1

Density of microdefects as determined by TEM and selective etching for as-grown and annealed specimens. The diffusion length was measured by the SPV method.

Sample	Defect density [cm^{-2}]	Etch pit density [cm^{-2}]	Diffusion length [µm]
as-grown	3×10^6	6×10^6	-
as-grown	$< 10^4$	0	-
as-grown	2×10^5	5×10^6	-
950°C	3×10^8	-	14.5
950°C	3×10^5	-	34.1
1050°C	1×10^6	-	18.3
1050°C	$< 10^4$	-	41.7

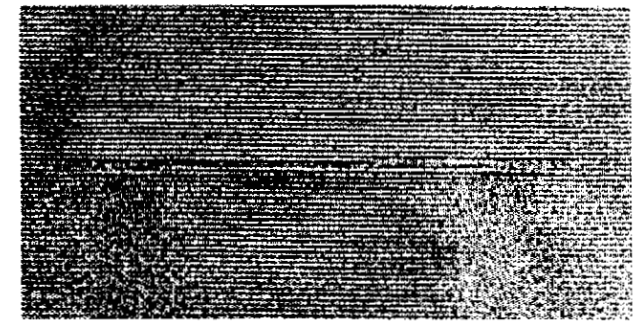


Figure 5 HREM micrograph of a platelike precipitate in as-grown multicrystalline silicon.

2.5 Carbon

The precipitation behavior of oxygen can be enhanced by the presence of carbon. This is depicted in figure 6 where the precipitation of oxygen in a specimen with a carbon concentration of 2.4×10^{17} cm^{-3} is compared to a specimen without carbon (below the detection limit). Oxygen precipitation begins now already in the temperature region 400 - 850°C whereas at higher temperatures no difference can be observed.

Correspondingly the carbon concentration decreases in the same temperature region which indicates that carbon is directly involved in the process. The ratio between the decrease of oxygen and carbon $\Delta O : \Delta C$ is about 10 : 1.

At higher temperatures above 950°C carbon decreases again which is probably due to the formation of SiC precipitates. TEM investiga-

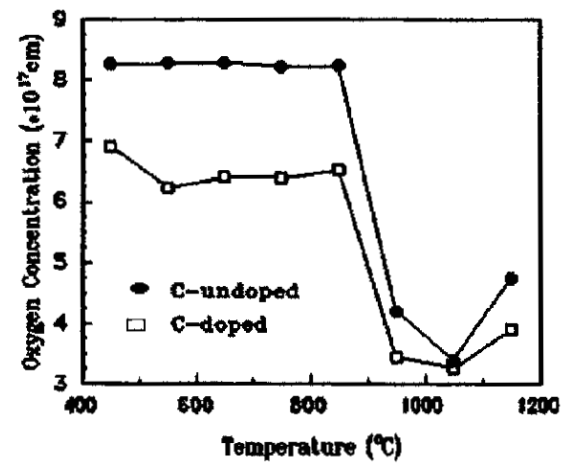


Figure 6 HREM micrograph of a SiC precipitate in as-grown multicrystalline silicon.

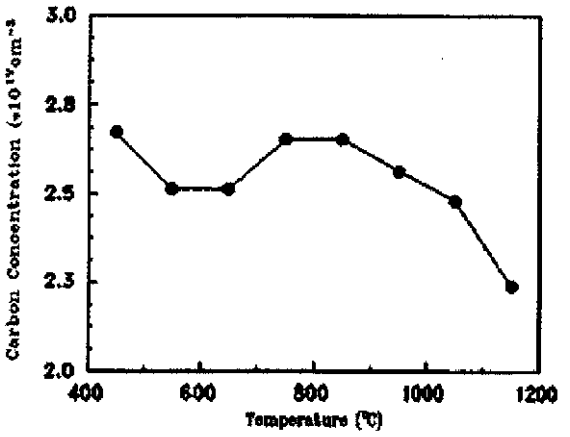


Figure 7 Carbon concentration as function of annealing temperature in mc - silicon. (Annealing time 24 hours).

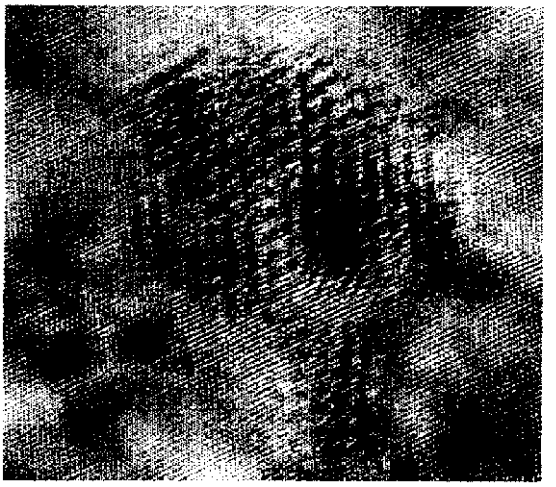


Figure 8 HREM micrograph of a SiC precipitate in as-grown multicrystalline silicon after annealing at 950°C.

tions show in fact 20 - 30 nm size SiC precipitates after annealing (figure 8).

2.6 Nitrogen

Multicrystalline silicon grown in Si_3N_4 crucibles can have nitrogen concentrations in the top region of an ingot above 1 x 10^{15} cm^{-3} (figure 1). In this region the carbon concentrations are also high, but oxygen concentration is low. Nitrogen predominantly exists in silicon in N-N pairs and can be detected by FTIR by an absorption line at 963 cm^{-1}. Annealing experiments were carried out with specimens with high nitrogen and carbon concentrations, but no oxygen (below the detection limit). The results are summarized in figure 9. After 24 hours nitrogen completely disappears below the detection limit above 750°C. At the same time the carbon concentrations remains almost constant. The FTIR spectra in the entire range from 400 - 4000 cm^{-1} show no other lines that could be related to Si_3N_4 precipitates or any other new defect. Considering the high diffusivity for the nitrogen pair that has been reported [4] and the mean distance of dislocations of about 10 µm it is concluded that nitrogen mainly disappears at dislocations above 750°C.

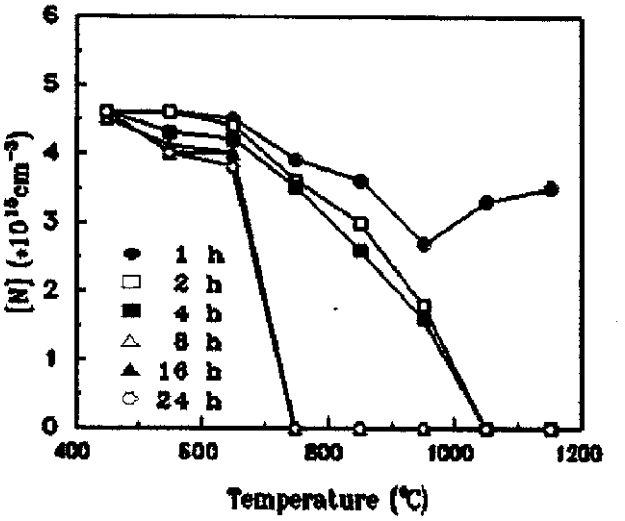


Figure 9 Nitrogen concentration in mc - silicon as a function of the annealing temperature.

3. References

[1] B.L. Sopori, Proc. of 20th IEEE PVS Conf. (1988) 591

[2] J.M. Serra, R. Gamboa, A.M. Valera, A. Eyer, W. Warta, Proc. of 11th EPVSE Conf. (1992) 975

[3] McHugo, S. A. and Sawyer, W. D., Appl. Phys. Lett. 62 (1993) 2519

[4] T. Itoh, T. Abe, Appl. Phys. Lett 53, 39 (1988)

RECENT ADVANCES IN WET CLEANING TECHNOLOGY IN SILICON PROCESSING

Kamal Mishra and I. Malik
OnTrak Systems, Inc.
77 W. Montague, Milpitas , CA 75035

Preparation of defect-free surface has become one of the most important process issues with the increase in the level of device integration. The paper reviews advances in the optimization of the pre-gate oxide cleaning steps: removal of metals, organics, particles and passivation. The deposition of metals on Si/ SiO_2 surface has been described using thermodynamic potential-pH diagrams. An electrochemical model has been presented to elucidate the relationship between the surface roughness and the solution chemistry.

Double-side scrubbing (DSS) has emerged as a preferred cleaning process after Chemical-Mechanical Planarization. Several examples of cleaning efficiency of the DSS in various applications is presented.

INFLUENCE OF DEFECT-IMPURITY INTERACTION ON SILICON SOLAR CELLS

by S. MARTINUZZI - LPDSO - University of Marseilles, France

1. INTRODUCTION

The continuous increase of the solar cell production to a GW scale needs the use of large quantities of low cost silicon wafers, which will be obtained from imperfect monocrystals (probably Cz material) or from multicrystalline ingots and so called solar graded materials. Such materials will contain impurities like oxygen or metallic fast diffusers.

Oxygen atom concentrations higher than the solubility limit are frequently found in Cz wafers and during thermal treatments precipitation can occur and degrade the electrical properties of the single crystals. Fast diffusers are well known to be the source of efficient recombination centres which limit the diffusion lengths of minority carrier.

The conversion efficiency in depending on the value of the diffusion length of the minority carriers as shown by Fig.1 obtained by PC1D software for back surface passivated or non passivated cells which the thickness of the base is 200 µm.

In multicrystalline wafers, extended crystallographic defects like grain boundaries, dislocations and twins introduce additional recombination centres, especially when they have segregated impurities. In such complicated materials, effective values of the minority carrier lifetime (τ_{eff}) as well as of their diffusion length (L_{eff}) must be taken in account. L_{eff} results of the different mechanisms which reduce the lifetime and could be approximately expressed by :

$$L_{eff}^{-2} \cong L_0^{-2} + \sum L_{defects}^{-2} + \sum L_{imp}^{-2} \qquad (1)$$

provided the interaction between defects and impurities is negligeable.

However and especially after thermal treatments, interactions between defects and impurities occur and expression (1) no longer support the comparison with experimental values. In fact, it is clear that the main part of the recombination activity of the defects results of the segregation of impurities.

When the diffusion length L of minority carriers decreases, the photocourrent J_{sc} given by a solar cell is reduced, like the open circuit photovoltage. Indeed using the classical equation :

$$V_{co} \cong \frac{kT}{q} \ln \frac{J_{sc}}{J_o} \qquad (2)$$

and assuming that J_o is a diffusion current i.e.

$$J_0 \cong \frac{q\, D_n\, n_{po}}{L_n} \qquad \text{(in a } N^+\text{-P junction)} \qquad (3)$$

one obtains :

$$V_{co} = \frac{kT}{q} \ln\left(\frac{J_{sc}.L_n}{c}\right) \cong \ln(L_n) \qquad (4)$$

The relation between J_{sc} and L is not so simple, as the sunlight is not absorbed uniformly in the material. Only the near infrared wavelengths induce a current which is proportional to L. However it is well admitted that values of L_{eff} higher than 150 µm are needed to obtain efficiencies in the 15 % range with 300 µm thick silicon wafers.

Presence of precipitates, especially in the space charge region of the junctions are sources of leakage currents in reverse like in forward bias. In this case they have a direct influence on V_{oc} by means of local shunts of the junction.

In the present paper one describes briefly the problems found in single crystalline cells, those (more marked) of multicrystalline cells and some solutions are proposed in order to reduce the deleterious effects of impurities and defects.

Although the free surface recombination strength is of a paramount importance in imperfection free and thin materials, the paper will be focused on the influence of bulk defects.

2. EXPERIMENTAL TECHNIQUES

Conventional techniques are used for photovoltaic devices like current-voltage (I-V) curves in dark and light, capacitance-voltage (C-V) curves and spectral response. These techniques lead to the knowledge of macroscopic informations concerning the device. They cannot be sufficient, essentially because if solar cells are obviously simple devices (a p-n junction with front and back ohmic contacts), a large area is needed and the entire volume on the silicon wafer is utilized for the conversion of photons. So the material must be imperfection free, or local characterization techniques are needed to correlate local electrical and photoelectrical properties with the presence in the investigated area of defects and impurities.

Such techniques are mapping ones, like Electron Beam Induced Current (EBIC), Light Beam Induced Current (LBIC) at different wavelengths, mapping of V_{oc} thanks to array of mesa diodes, Electronic Microscopies and Microanalyses, Scanning Infrared Microscopy (SIRM), etc. Quantified scanning techniques could also be employed like the mapping of minority carrier diffusion lengths and those of lifetime by the use of microwave detected photoconductance decay.

The reduction of the recombination center density could result from special treatments like external getterings or hydrogenations. Low cost external gettering techniques are essentially those resulting of a long phosphorus diffusion from $POCl_3$ at 900°C (several hours), or Aluminium-silicon alloying. These techniques have the main advantage on others to be used currently as conventional processing steps during the solar cell preparation.

3. MONOCRYSTALLINE CELLS

Cz single crystals are considered only. As they do not contain dislocations or grain boundaries, impurities are the major imperfection. Fast diffusers like Fe, Ni, Cu, Cr are normally present at low concentrations, or are introduced by inadvertent contaminations during processings. Conversely oxygen concentration is frequently in the 10^{18} cm^{-3} range, so higher than the solubility limit (due to the reaction of the melted silicon with the silica crucible) and precipitation can occur easily during thermal treatments. Carbon concentration is also as high as few 10^{17} cm^{-3} and influences the precipitations of oxygen, or can give rise to the formation of inclusions [1,2,3].

These precipitates are sources of recombination centers by themselves, and at a larger extend by the formation of associated extended crystallographic defects. As a consequence the lifetime of minority carrier is strongly reduced. Fig.2, from ref.1, shows the degradations observed after several oxydation treatments in the best case. Fig.3, from ref.3, demonstrates clearly the decrease of τ_{eff} when oxygen concentration increase above 1 ppma.

Swirls and striations are also well known defects which characterize the influence of oxygen precipitation and give ring like distributed defects which are well detected by LBIC technique.

The preceding imperfections lead to inhomogeneous wafers and the inhomogeneity tends to increase with the size of the wafers, in fact of the ingot diameter, due to non uniform heating of large crucibles, non uniform convection at the solid liquid interface.

These imperfections reduce the minority carrier diffusion length, and consequently the photocurrent J_{sc}. But even at low densities these defects can affect dramatically V_{oc} by means of shunting paths which result of their presence in the junction region and of their decoration by metallic impurities.

4. MULTICRYSTALLINE SILICON WAFERS AND CELLS

4.1. General features

The first characteristic of these materials is the inhomogeneity. Several kind of defects are spreaded in a given wafer, their nature, density and recombination strength vary markedly on short distances. This is due to a large variety of extended crystallographic defects like grain boundaries (Gbs), and intragrain defects as dislocations, twins, dislocation lineages and tangles.

Obviously, impurities are also present, especially when low quality silicon feedstocks are used. Oxygen, carbon and metallic impurities can interact with the preceding defects and increase dramatically their recombination strength. In addition, as this interaction results generally of a segregation by the defects, the final recombination strength is heterogeneous along a given Gb, as well as for the intragrain defects. Moreover, this recombination strength can be largely enhanced when thermal treatments are applied to the material, which increase the segregation and consequently the recombination activity.

Oxygen and carbon are involved in precipitation phenomena like in monocrystalline materials. Even if their concentration is generally below the solubility limit, segregation at extended defects lead to the formation of precipitates, which in turn trap metallic impurities and degrade the effective diffusion length in the material (this is the key of the so called internal gettering). These problems are longly described, with a large bibliography in ref.4.

In large grained materials usually obtained by directionnal solidification, the grain size is generally higher than few mm and the influence of Gbs is totally hidden by that of a intragrain defects. Fig.4 (from ref.5) shows for highly recombining Gbs the variation of effective diffusion length versus the ratio grain size/intragrain diffusion length. Fig.5 (from ref.5) shows the variation of the conversion efficiency as a function of effective diffusion length for different grain size and for a similar monocrystalline cell. It is clear that for grain sizes larger than 2 mm, the difference between a single crystalline and a multicrystalline wafer is very low.

Twins are normally neutral except when they are decorated by dislocations or by impurity precipitates.

The more deleterious intragrain defects are the dislocations. These defects are sources of recombination centers especially when they are decorated by impurities, in the base of the cell like in the space charge region of the junction. However when they cross the junction they can also induce a parasitic conductivity. Their influence will be extensively described in the next subchapter.

4.2. Influence of dislocations

This influence was studied by several authors [6 ; 7 ; 8] from theoretical and experimental points of vue. The model of El Ghitani [7] computed the dependence of L_{eff} on the density of dislocations (N_{dis}) for different values of the true diffusion length L_n (in the undislocated region of the wafers) and for different values of the recombination strength S_d of the defects. S_d is evaluated by means of an effective interfacial recombination velocity at the edge of the cylindrical space charge region associated to the dislocation core. This effective parameter is depending on the segregation of impurities.

Fig. 6 represents such a variation in the case of Polix material in which $L_n \cong 90$ µm. The fit with experimental points suggests that S_d is in the range between 10^4 and 10^5 cm s^{-1}. Obviously if S_d decreases the influence of N_{dis} is less marked, as shown by Fig.7, for $S_d = 10^3$ cm s^{-1} and different values of L_n.
In addition these results indicate that the improvement of the material could be obtained either by a decrease of S_d or (and) by an increase of L_n.

Fortunately the dependence of the photocurrent versus N_{dis} is not so marked, as in solar cells there are contributions of the emitter and from the space charge region which are irrespective of the bulk properties and escape to the recombinations by bulk defects. These two contributions mitigate the decrease of J_{sc} when N_{dis} increases as shown by the figures 8(a) and 8(b) and the influence of these defects decreases slightly when the thickness of the wafers decreases.

The preceding results are related to an homogeneous distribution of dislocations in grains. However frequently in some restricted areas, dislocation tangles are present in which the density N_{dis} is certainly higher than 10^8 cm^{-2}. The preceding models do not work at a so high density. In these regions the photocurrent is frequently very low due to the high density of recombination centers but new phenomena appear.

When the cells are reverse biased hot spots are detected in such areas which can lead to the burn off of the junction. This could be explained by an anomalous conduction by the dislocation tangles [9] inducing leakage currents which heat locally the device.

In addition, the presence of very large densities of dislocations and subgrain boundaries produces current in excess through the junction and reduces locally V_{oc}. Such studies were recently developped thanks to the use of very sensitive infrared cameras and the comparison of maps of photocurrent obtained by LBIC and map of V_{oc} obtained by arrays of small diodes [10 ; 11]. In some regions V_{oc} is decreased while the photocurrent is not affected substantially by the defects.

It was also proposed by El Ghitani et al. [12] that dislocations which cross the junction can provide currents is excess of the conventional recombination one when the junction is forward biased. These currents might be expressed by :

$$J = A.N_{dis}\left[\exp\left(\frac{qV_f}{2kT}\right) - 1\right] \qquad (5)$$

Such variations were approximately found with mesa diodes made in polix material, probably because dislocations are strongly decorated by impurities.

Notice that the model of El Ghitani for dislocated materials was well verified in a recent material produced by SITIX (Osaka, Japan) by the cold crucible technique. In this material, there is large densities of dislocations in the grains, ranging between 10^5 to 10^7 cm^{-2} but the minority carrier diffusion length is found higher than 120 µm. This could be explained only if S_d is below 10^3 cm s^{-1} for these defects.

5. HOW TO SURVIVE ?

Périchaud and Martinuzzi [13], Schindler [14] and Sopori et al. [15] (and many others) have proposed solutions for the use of imperfect materials.

What is important ? It is needed that oxygen precipitate formation be avoided in sc-Si like in mc-Si. It is needed that extended defects be neutral (as their presence is intrinsic to multicrystalline materials). It is needed that impurities like oxygen and metallic fast diffusers be in low concentrations, or be extracted by external gettering, or be passivated for exemple by interaction with hydrogen.

The most efficient external gettering technique is developped by phosphorus diffusion from a $POCl_3$ source at about 900°C for 1 to 4 hours. Indeed this technique proceeds by 3 basic mechanisms :

- Segregation gettering due to the increase of solubility and the decrease of diffusivity in the heavily doped N^+ region
- Relaxation gettering due to the trapping of impurities by the defects associated to the heavy phosphorus diffusion like the border of SiP precipitates.
- Injection induce gettering due to the injection of self interstitials in the bulk during the growth of SiP precipitates. These self interstitials can interact by the kick out mechanism with substitutional impurities, and also can participate to the dissolution of precipitates.

It is to day recognize that this gettering is able to remove impurities from the bulk and cleans the homogeneous regions of the grains as well as dislocations and grain boundaries, and L_{eff} increases drastically as shown by Fig.9. Such treatments improve the conversion efficiency of solar cells, increasing the photocurrent and the photovoltage, as shown by Fig.10 (from ref.16)

This was fairly well verified by LBIC maps and diffusion length maps [17].

Nevertheless this technique is limited by the presence of a too large density of defects or of oxygen atoms [18 ; 19].

Another low cost technique is the external gettering by Aluminium-silicon alloying which proceeds essentially by the segregation mechanism as the solubility of metallic impurities in the alloyed region is 10^4 (at least) times higher than in silicon. This gettering works is sc-Si like in mc-Si materials.

As for phosphorus diffusion, the gettering efficiency is limited in regions which contain dislocation tangles, or when oxygen concentration is too high.

Indeed, the presence of dense arrays of dislocations induce an internal gettering of impurities which cannot reach the external gettering sites and remain trapped in the bulk. During the thermal treatment associated to the gettering, which the temperature is higher than 700°C oxygen precipitates are formed and degrade the material.

Passivation of the defects, of the impurities and also of the segregated impurities at the extended defects has been obtained by hydrogenation. The most powerful technique is the ion implantation by a Kaufman source.

However due to the instability of hydrogen when the wafer temperature reaches 450°C, hydrogenation can be employed only as a end of range process in the solar cell fabrication (a revue was given in ref.20).

Fortunately solar cells work in sunlight and this illumination has by itself a beneficial effect : some recombination centres are partly saturated. In the worse materials L_{eff} is higher in sunlight than when the cell is illuminated by monochromatic light only. This improvement is equivalent to a phosphorus gettering at 850°C for 2 hours (as shown in ref. 15). Such a variation of the recombination strength at Gbs was investigated successfully by Chen et al [21]. These authors shown that the material is well improved 10 µm below the illuminated surface by the absorbed light and that suffices to increase the effective diffusion length of a 300 µm thick wafer.

6. CONCLUSIONS

The preceding considerations suggest obviously that the use of a material containing few defects and few impurities is certainly the best solution provided this material is cost effective. Such a material does not exist to day. (It could be solar grade FZ).

In single crystals like FZ there is no problem (no defects ; no precipitates). In Cz the situation is worse due to the presence of oxygen, and the wafers must be choosen carefully in order to not contain more than 5.10^{17} cm^{-3} oxygen atoms. Under these conditions, gettering techniques work very well, and contaminants can be extracted from the active area of the wafers.

In multicrystalline material carbon, oxygen and metallic contaminants can react with the extended defects during the solidification of ingots, and also during the thermal treatments.

External gettering is able to improve drastically regions of the material in which the defect density is not too high. This is particularly true for dislocations. However dislocations tangles and lineages must be avoided. Fortunately sunlight mitigates the deleterious influence of all these defects.

REFERENCES

[1] G.H. Schwuttke, Proc. Of 16th IEEE PV Spec.Conf. 1982, p.327.

[2] R.V. D'Aiello, P.H. Robinson and H. Kressel, Proc. of 12th IEEE PV Spec. Conf. 1976, p.15.

[3] S.K. Pang, A. Rohatgi and J.P. Schaffer, Proc. of 19th IEEE PV Spec. Conf. 1987, p.1500.

[4] S. Martinuzzi and S. Pizzini, Large grain polysilicon substrates for solar cells in Advanced Silicon and Semiconducting Silicon alloy based materials and devices ed. By J.F. Nijs, Inst. of Phys. Pub. (Bristol), 1995, p.323.

[5] J. Dugas and J. Oualid, Rev. Phys. Appl. 22, 1987, 677.
[6] M. Yamaguchi, A. Yamamoto and Y. Itho, J. Appl. Phys. 59, 1986, 1751.
[7] H. El Ghitani and S. Martinuzzi, J. of Appl. Phys. 66, 1989, p.1717 and p.1723.
[8] R.P. Lieninger, H. Morikawa and S. Arimoto, Proc. Of 13th EPVSEC, Nice, 1995, p.395.
[9] A. Simo and S. Martinuzzi, Proc. Of 21st IEEE PV Spec. Conf. 1990, p.800.
[10] O. Breitenstein and K. Iwig, Proc. Of 13th EPVSEC, Nice 1995, p.145.
[11] R. Baldner, H. Lautenschlager, C. Schetter, R. Schindler and W. Warta, Proc. of 25th IEEE PV Spec. Conf. Washington 1996, to be published.
[12] H. El Ghitani and M. Pasquinelli, J. de Phys. III, 3, 1993, 1931.
[13] I. Périchaud and S. Martinuzzi, J. de Phys. III, 2, 1992, 313.
[14] R. Schindler, Solid State Phenomena 37, 1994, 343.
[15] B.L. Sopori, L. Jastrzebski, T.Y. Tan and S. Narayanan, Proc. of 12th EPVSEC, Amsterdam 1994, p.1003.
[16] S. Navayanan, S.R. Wehuam and M.A. Green, Appl. Phys. Lett. 48, 1986, 873.
[17] M. Stemmer, Thesis of Doctorate, Univ. of Marseilles, 1994.
[18] I. Périchaud and S. Martinuzzi, Proc. of 24th IEEE PV Spec. Conf.
[19] B.L. Sopori, L. Jastrzebski and T. Tan, Proc. of 25th IEEE PV Spec. Conf. Washington, 1996, to be published.
[20] B.L. Sopori, X. Deng, J.P. Brenner, A. Rohatgi, P. Sana, S.K. Estreicher, Y.K. Park and M.A. Roberson, Solar Energy Materials and Solar Cells 41, 1996, 159.
[21] Z. Chen and L.C. Burton, Proc. of 21st IEEE PV Spec. Conf., 1990, p.731.

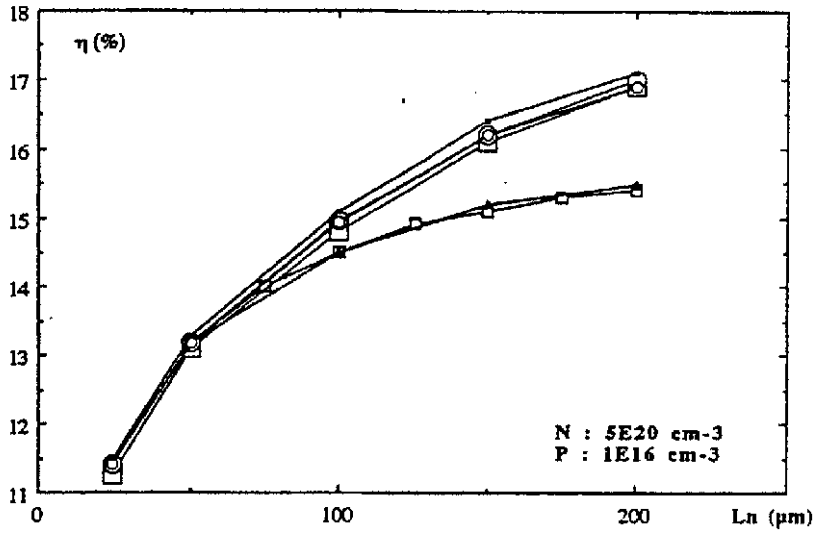


Figure 1. Variation of the conversion efficiency towards the diffusion lengths. The upper curves correspond to passivated back surface of the samples. The thickness of base is 200 μm.

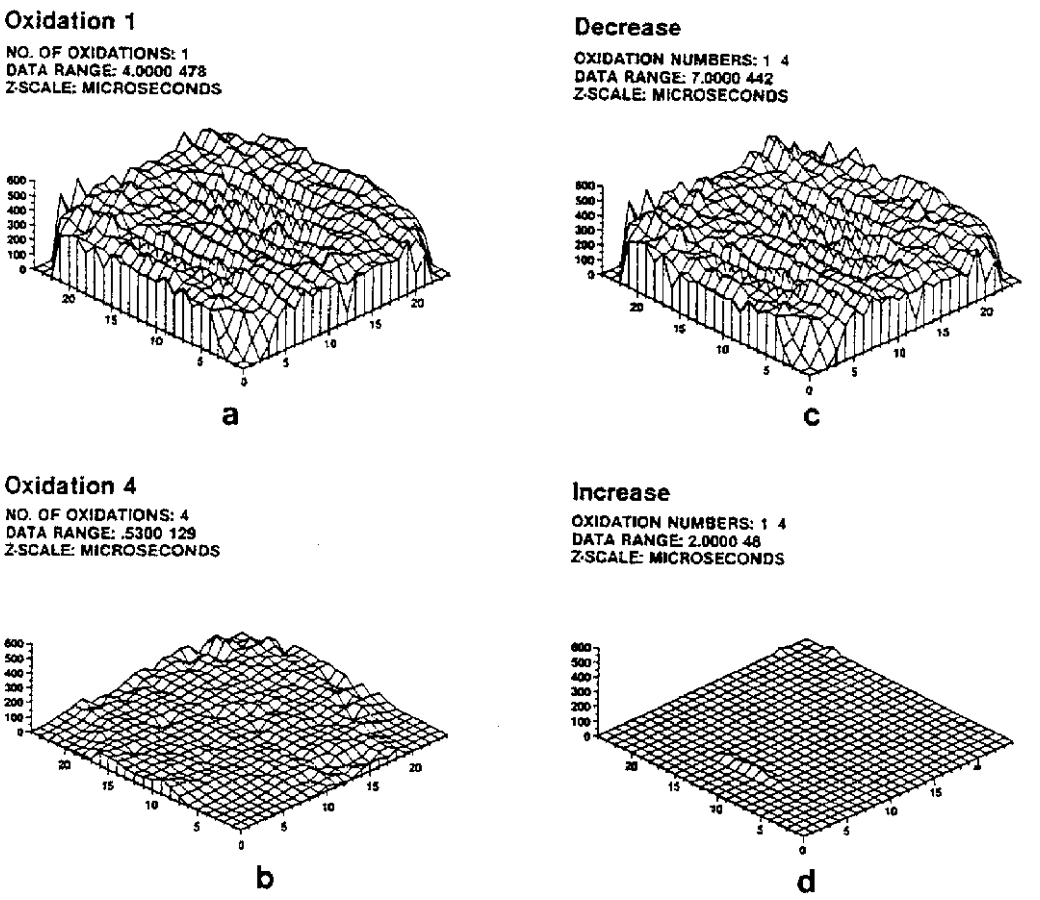


Figure 2. Minority carrier lefetime distribution maps of 100 mm Czochralski silicon wafer. Lifetime values below 1 usec are displayed as zeros (from ref.1) after 1 oxydation (a) ; 4 oxydations (b) ; c) decreases of τ ; d) increases of τ.

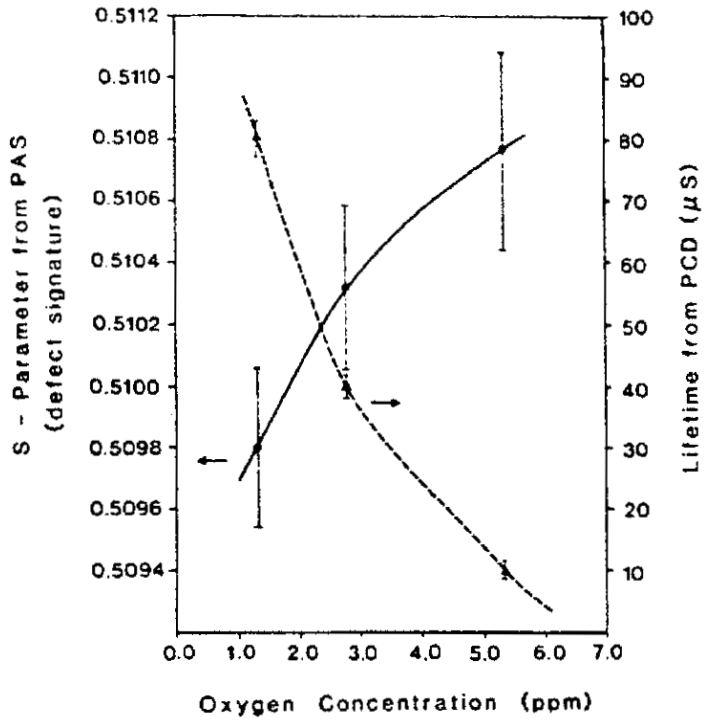


Figure 3. Change in lifetime and S-parameter (Defect signature) as a function of oxygen concentration in high resistivity (> 250 Ω-cm) MCZ Silicon (from ref.3).

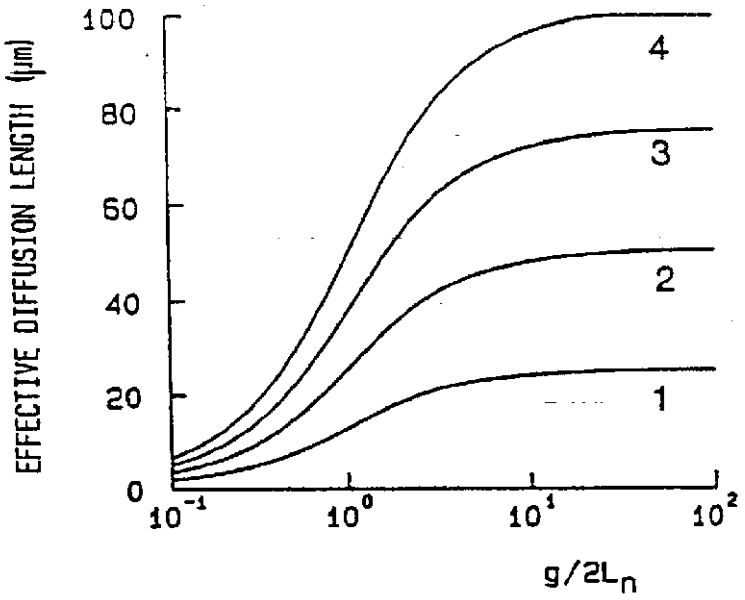


Figure 4 Effective diffusion length vs the ratio grain size/bulk diffusion length. $N_A = 10^{16}$ cm^{-3} ; Grain boundary recombination velocity : 10^6 cm/s.
1) $L_n = 25$ μm ; 2) $L_n = 50$ μm ; 3) $L_n = 75$ μm ; 4) $L_n = 100$ μm [from Dugas (1987)].
(Reproduced by permission of Ed. de Physique)

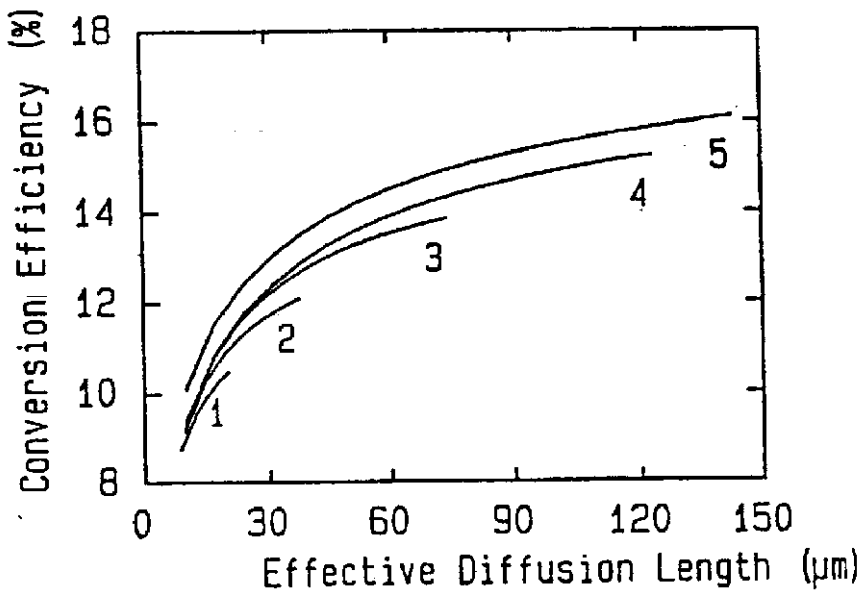


Figure 5 Variation of the conversion efficiency of solar cells as a function of the effective diffusion length, for different grain sizes : 1) g = 100 μm ; 2) g = 200 μm ; 3) g = 500 μm ; 4) g = 2 mm ; 5) equivalent monocrystalline cell.
Base : p-type, $N_A = 10^{16}$ cm^{-3} ; base thickness = 500 μm.
Emitter : n-type , $N_D = 5 \times 10^{19}$ cm^{-3} ; emitter thickness = 0.2 μm.
Grain boundary recombination velocity S = 10^6 cm/s [from Dugas (1987)].
(Reproduced by permission of Ed. de Physique)

$L_{eff} = f(N_{dis}, S_d, L_n)$

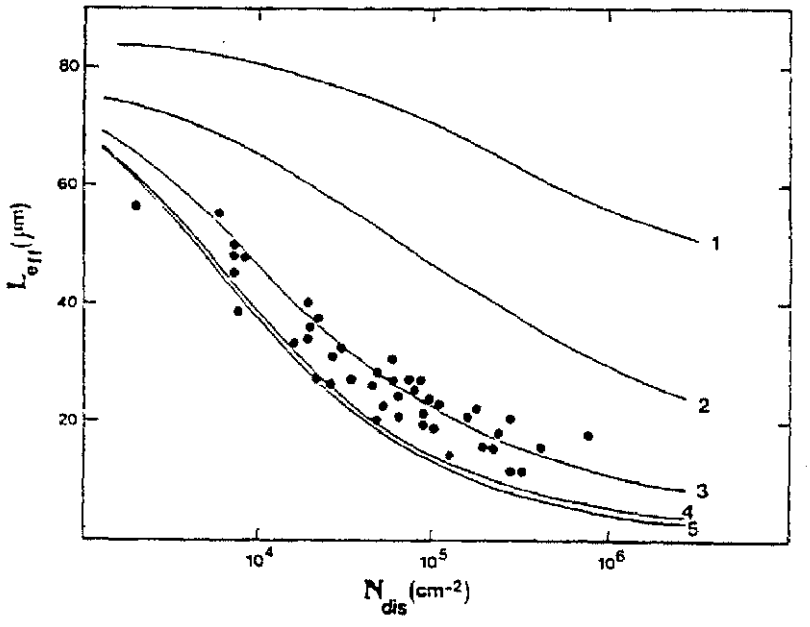


Figure 6 Calculated and experimental variations of the effective diffusion length (L_{eff}) as a function of the dislocation density (N_{dis}). Solid curves have been calculated for different values of dislocation recombination strength (S_d) :

(1) 5 x 10^2 cm s^{-1} ; (2) 10^3 cm s^{-1} ; (3) 10^4 cm s^{-1} ; (4) 10^5 cm s^{-1} (5) 10^6 cm s^{-1}, full circles, experimental results [from El Ghitani (1989 a, b)].
(Reproduced by permission of Mat. Sci. Engineering)

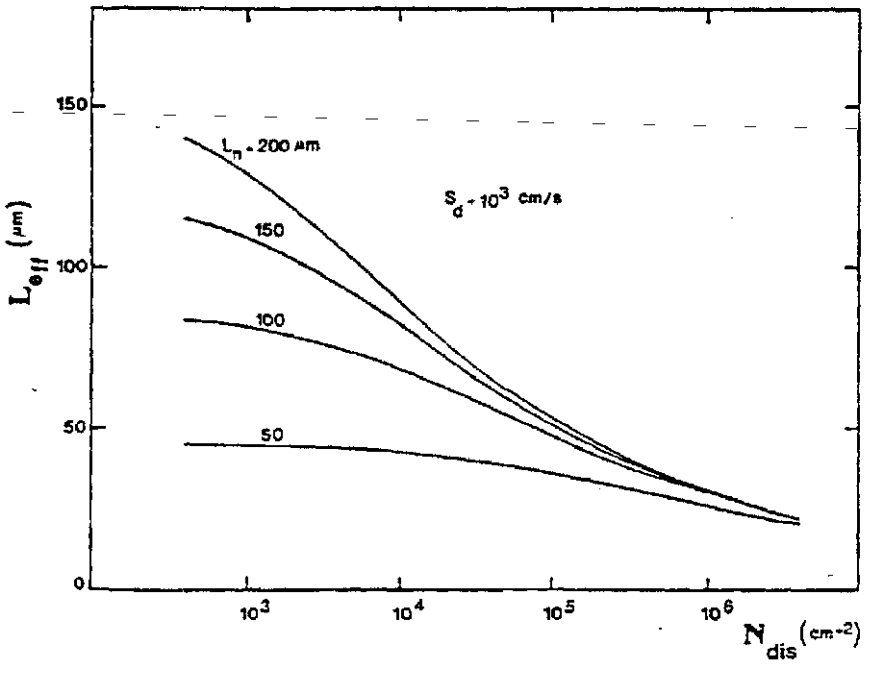


Figure 7 Plot of L_{eff} as a function of N_{dis} for different L_n values in the range between 50 and 200 μm and for $S_d = 10^3$ cm s^{-1} [from El Ghitani (1989c)].
(Reproduced by permission of Mat. Sci. Engineering)

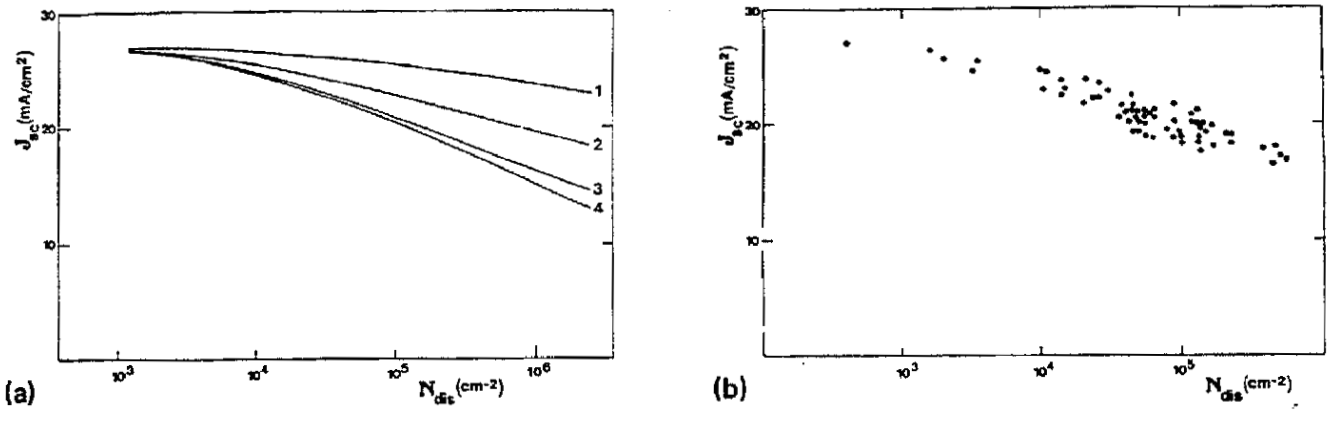


FIG. 8 (a) Calculated variation of photocurrent (J_{sc}) vs dislocation density (N_{dis}) for different values of dislocation recombination strength (S_d): (1) 10^3 s^{-1}; (2) 10^4 cm s^{-1}; (3) 10^5 cm s^{-1}; (4) 10^6 cm s^{-1}. (b) Experimental values determined by means of N^+P mesa diodes.

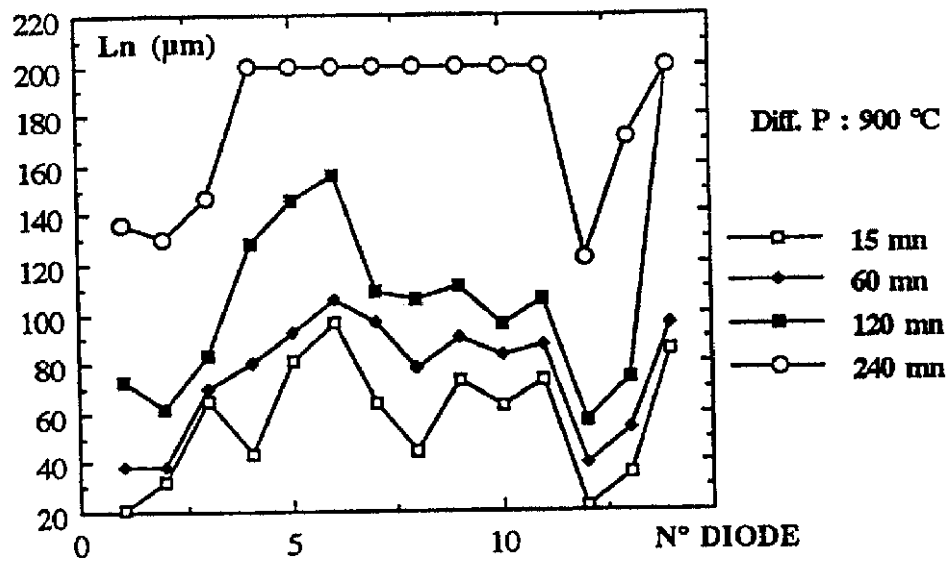


Figure 9 Variations of electron effective diffusion lengths in 14 mesa diodes realized at the same place of matched samples which have been submitted to phosphorus diffusion at 900°C for (□) 15 mn ; (◆) 60 mn ; (■) 120 mn and (○) 240 mn. The values greater than the sample thickness have been arbitrary limited at 200 µm (diode number 4 to 11).

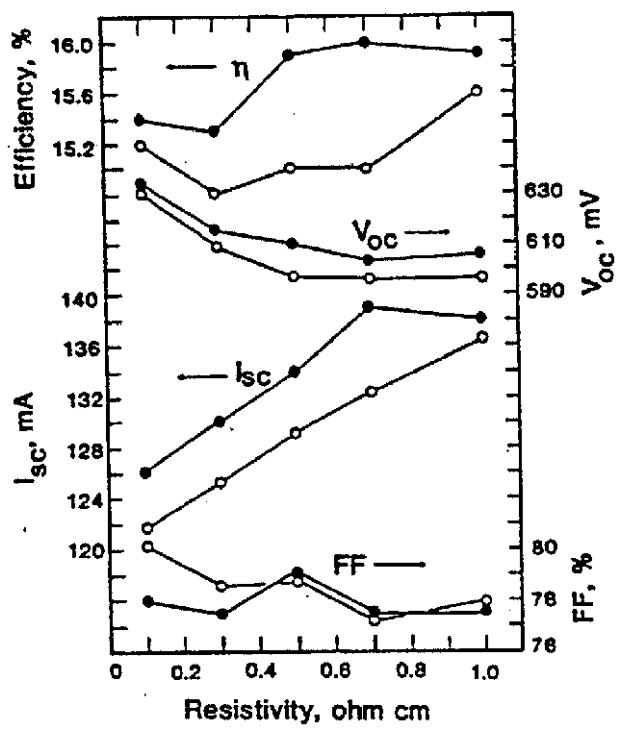


Figure 10. Output parameters of PESC cells fabricated on p-type polycrystalline silicon (Wacker Silso) as a function of substrate resistivity. The open circles show the results without phosphorus pretreatment while the closed circles show the effect of this pretreatment. [from ref. 16].

Investigation of Shunting Regions in Solar Cells by Dynamical Precision Contact Thermography

O. Breitenstein, K. Iwig and I. Konovalov *

Max Planck Institute of Microstructure Physics, Weinberg 2, D-06120 Halle, Germany
* Shevchenko University, Radiophysical Faculty, Vladimirskaja 64, 252017 Kiev-17, Ukraine

The efficiency of multicrystalline solar cells is still significantly below that of CZ-Si solar cells. Since the open circuit voltage (Voc) and the fill factor (FF) are basically governed by the balance between photocurrent and internally back-injected forward current of the cell, it can be assumed that inhomogeneities of the local dark forward I-V-characteristic of multicrystalline solar cells are responsible for their lower Voc and FF. If there are localized points of strongly increased forward current in solar cells, these positions are called local shunts. It is a non-trivial task to measure the local injection current density in large-area solar cells, since all regions are electrically switched in parallel. Thus, while Jsc can be mapped at zero bias using LBIC techniques, a similar optical mapping of Voc would give misleading results, because the local photogenerated current would be balanced by the injection current of the whole cell.

To overcome this problem, Häßler et al. [1] have proposed to divide solar cells into arrays of small diodes using reactive ion etching, and to characterize these small diodes separately. Indeed, Karg et al. [2] have found a good correlation between the Voc-values of these diodes and their dark forward current measured at 0.5 V, whereas the correlation between Voc and the reverse current was much worse (see Fig. 1). This Mesadiode Analysis of Solar Cells (MASC) technique, however, is a destructive and very time-consuming one, and till now it is not applicable to areas below the grid lines and at the edges of solar cells. Moreover, it has been found that the edges of these mesadiodes are not perfectly passivated yet, hence there is some preferential current injection into the etched grooves, probably masking low injection level effects of the diodes.

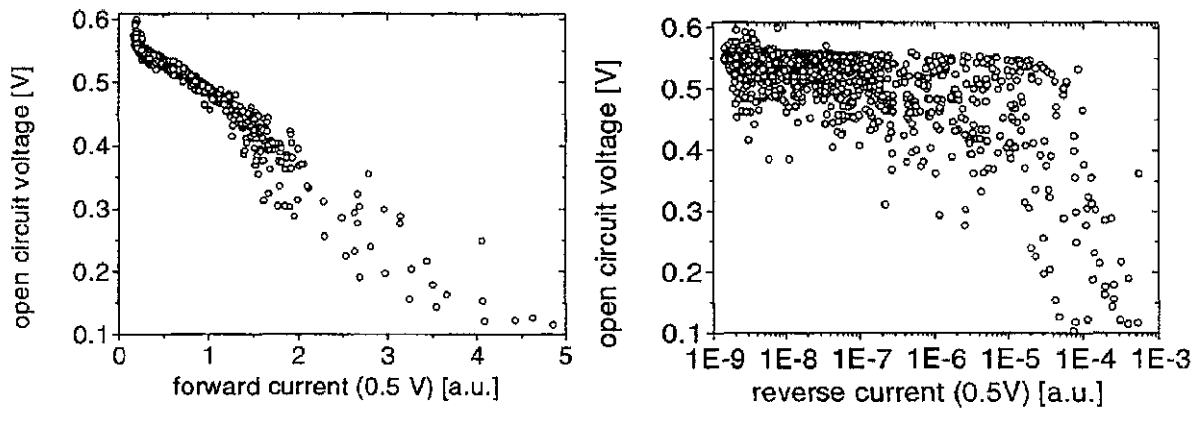


Fig. 1: Correlation of Voc of an ensemble of 600 mesadiodes of 0.4mm^2 size to their forward current (left) and their reverse current (right), both measured at 0.5V in the dark (by friendly permission of Karg et al [3])

Thermography, on the other hand, has the potential to measure the local current density for a given bias, since it detects the amount of the local dissipated power. However, the sensitivity of the usual infrared (IR) thermography technique is too low to detect the local temperature differences in the low mK range expected for a forward biased solar cell near its regular working point and to map its forward current density. IR thermography has been successfully used to map only the reverse current density at reverse biases of many Volts, where the temperature differences are in the order of Kelvins (see, e.g., Simo and Martinuzzi [3]). There it was assumed that shunts are essentially ohmic, so shunts in reverse direction would also be shunts in forward direction. Our investigations, however, show that this is not always the case. Thus, thermography in reverse direction is not able to localize all regions of preferred current flowing in forward direction [4, 5].

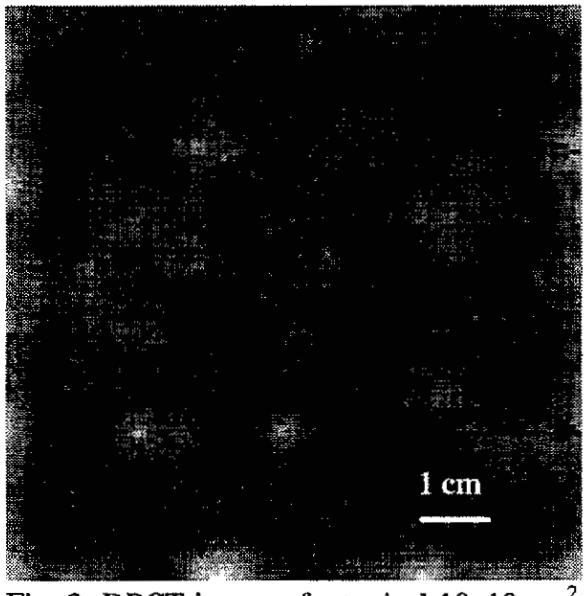


Fig. 2: DPCT image of a typical 10x10 cm^2 multicrystalline solar cell measured at 0.5V forward bias (logarithmic grey scale)

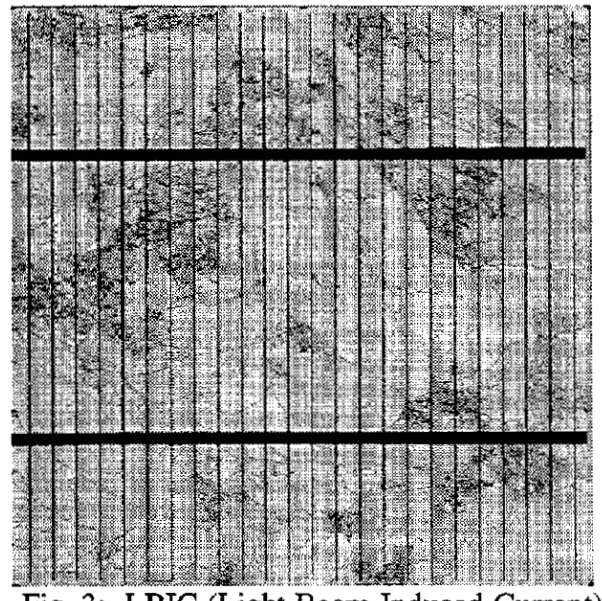


Fig. 3: LBIC (Light Beam Induced Current) image of the sample used for Fig. 2

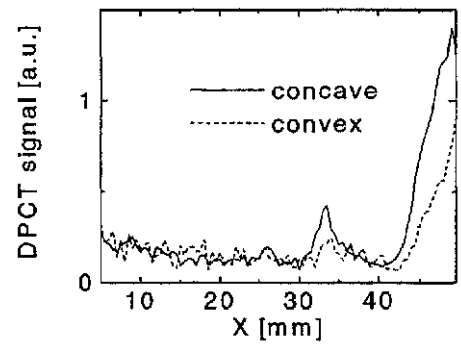
In order to map the dark forward current density of solar cells under realistic operation conditions in a non-destructive way, we have developed a technique called Dynamical Precision Contact Thermography (DPCT, [4]). It relies on the successive mechanical probing of the cell with a small temperature sensor in contact mode. The cell at room temperature in the dark is forward biased not in dc-mode but using bias pulses at a frequency of 3 Hz. Only the temperature modulation at this frequency is measured in lock-in mode to detect the local current density. In first approximation the DPCT-signal can be interpreted as a measure of the local current density. Extended regions of different injection current density can be localized with a resolution of 1...2mm, but for point-like shunts the spatial resolution is about 0.1 mm. Temperature modulations of the sample surface as low as 100 μK can be detected, corresponding to a sensitivity of the forward current density measurement well below 1mA/cm^2. Thus, for the first time the dark forward current density under ordinary operation conditions of solar cells can be mapped in a non-destructive way. This system has been used to characterize 10x10 cm^2 sized solar cells made of block-cast multicrystalline silicon in order to find local shunts and extended regions of locally increased forward current density. At the observed shunt

positions the cells have been investigated in detail using Scanning Electron Microscope (esp. EBIC, Electron Beam-Induced Current) techniques.

Fig 2 shows a thermogram of a typical whole cell measured at 0.50 V forward bias at 25°C, leading to a pulsed forward current of the whole cell of 175 mA. A logarithmic scale of the grey values has been chosen, so that both local shunts, showing a surface temperature modulation of up to 20 mK, and lateral variations of the surface temperature modulation as low as 100 μK can be distinguished. The dominant local shunts are proved to be at the edges of the cell. The edge of the cell generally shows increased current injection, hence it seems to be not well passivated. Also in the cell area some local shunts as well as some extended regions of increased injection density are visible. None of the local shunts are indicated in the Jsc-mapping in the LBIC image of this cell in Fig. 3. The presence of these different shunting regions shows that the physical mechanisms responsible for the shunting action are worth being investigated in detail for understanding all factors reducing the efficiency.

In the following different shunt types will be described separately, and the quantitative influence of all shunting actions on the efficiency of the cells being investigated is estimated.

Fig. 4:
DPCT line scan across a stress-sensitive edge shunt measured under concave (straight) and convex (dashed) bending of the cell to a bending radius of 30 cm



In many cases edge shunts have been found to be the dominating local shunts in the cells, sometimes exceeding the minimum current density by more than a factor of 100. As shown earlier [5], these shunts are often related to dark contrasts in the EBIC image (grain boundaries and / or dark clouds), and there are edge shunts appearing in both bias polarities (forward and reverse) and shunts appearing only in one. Moreover, also certain edge shunts had disappeared when the cell had been cut into pieces in order to make SEM investigations. This has led to the suspicion that those shunts may be induced or affected by internal mechanical stress [5]. Fig. 4 shows a DPCT line scan across a stress-sensitive shunt measured under concave (straight) and convex (dashed) elastic bending of a solar cell to a bending radius of about 30 cm. The data are taken along the edge of the solar cell. Not only the local shunt at x = 33 mm but also the shunt in the corner of the cell at x = 50 mm reacts to the bending. This result clearly shows that elastic stress may influence the activity of certain shunts. Fig. 5 shows a typical strong edge shunt both in thermography and in EBIC imaging. Here only a small fraction of the whole sample area was scanned. The grid line is seen in dark contrast in the thermogram. In the shunting region an accumulation of grain boundaries is visible in the EBIC image. The detailed origin of the shunting action is still under investigation. Besides local accumulation of mechanical stress (probably influenced by grain boundaries), edge shunts may also be caused by mechanical violations like cracks, which sometimes have been observed in shunt positions. The latter

mechanism is supported by the fact that whenever solar cells had been intentionally mechanically violated, these regions have been proven by DPCT to be shunts afterwards.

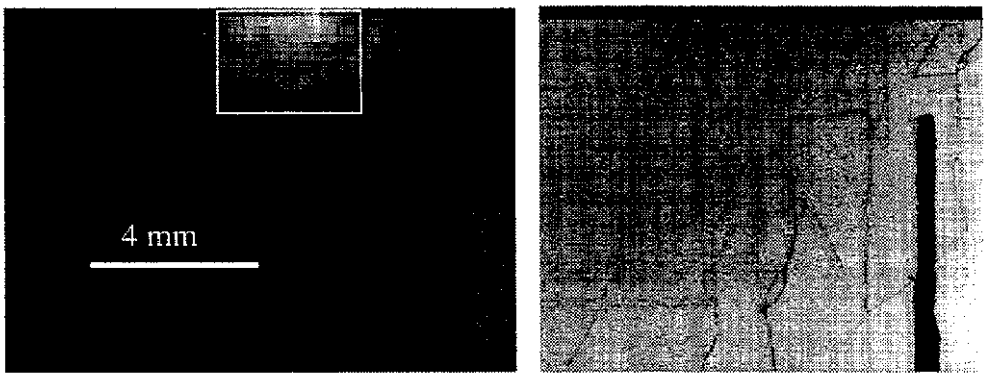


Fig. 5: DPCT image (left) and EBIC image of the framed region (right) of a dominant edge shunt.

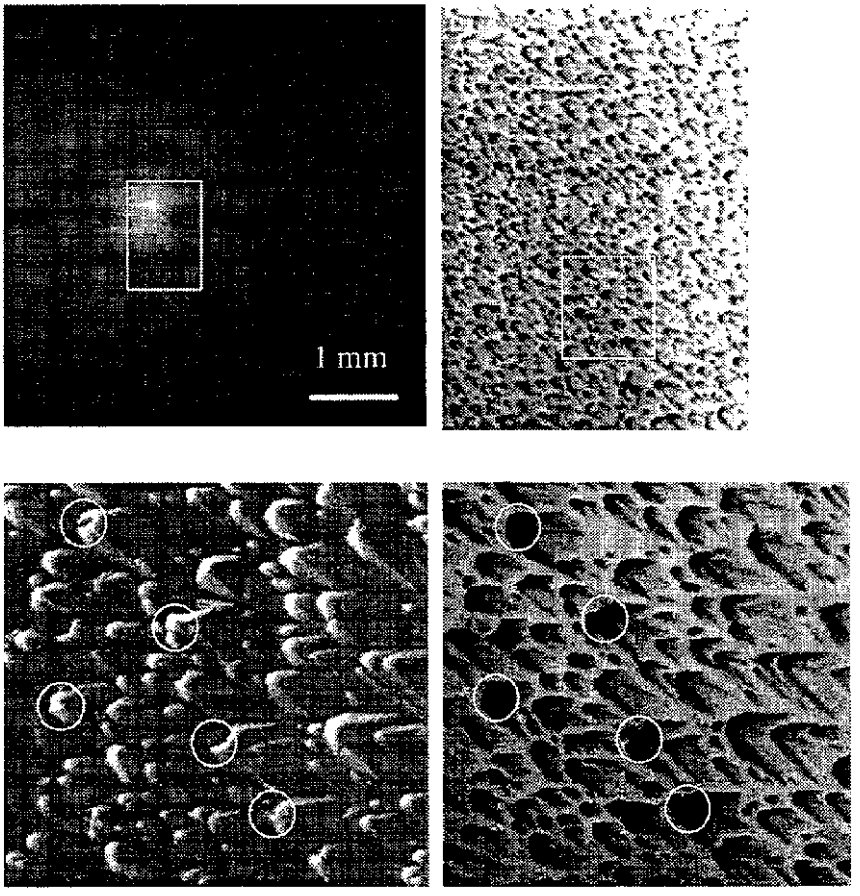


Fig. 6: DPCT image (top left) of a shunt below a grid line and EBIC image of the framed region after dissolving the grid line (top right). Below: SE image (left) and EBIC image (right) of the region framed in the upper right EBIC image.

Not all solar cells show local shunts in the cell area. However, if there are shunts in the cell area, they often lie below grid lines. It had been shown that relatively extended regions (100 µm dia.) with no pn-junction may cause shunts below grid lines [5]. Meanwhile we have found that also smaller regions (some µm dia.) without pn-junction may lead to shunts whenever they are below grid lines. Fig. 6 shows a DPCT image and an EBIC image of a shunting region after having etched away the grid lines using HF. In the thermogram some minor grid lines and the edge of a major grid line are visible as dark lines. The shunt is just above the edge of the major grid line. In the EBIC image besides of the texturization-induced topography contrast there are a

few very dark spots. They have been identified by SE imaging to be mechanically truncated tips of texturization pyramids (marked in the lower part of Fig. 6). Whenever these sites are below metallization lines they are becoming shunts. This shunt type did not disappear after cutting the cell into pieces.

On the other hand, sometimes there are local shunts between grid lines. Fig. 7 shows the EBIC- and the DPCT image of a shunt between grid lines. It is visible that the shunting region is more extended than in the case of Fig. 6. The dark lines besides the grid lines in the DPCT images are grain boundaries. Their DPCT contrast is due to a reduced heat contact to the sensor owing to surface steps caused by the texturization. The EBIC image shows an accumulation of grain boundaries in the shunt region, just like for the edge shunt in Fig. 5. Interestingly, this shunt was visible in a similar position in solar cells made from adjacent wafers in the block. This points to a physical similarity between this shunt type, the edge shunt shown in Fig. 5, and probably even the extended shunting regions to be described below, which are also related to extended regions of bad crystal quality.

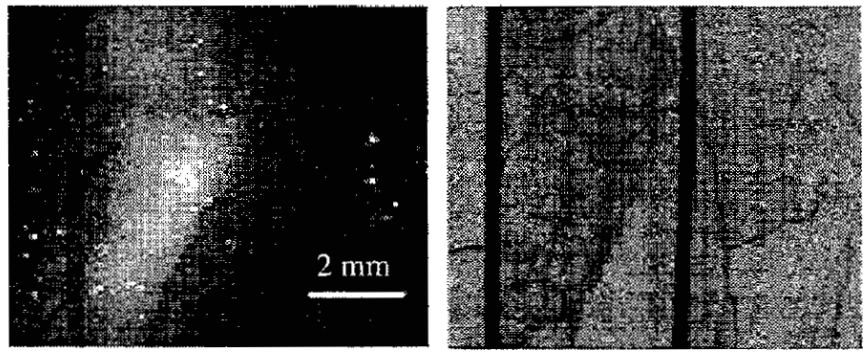
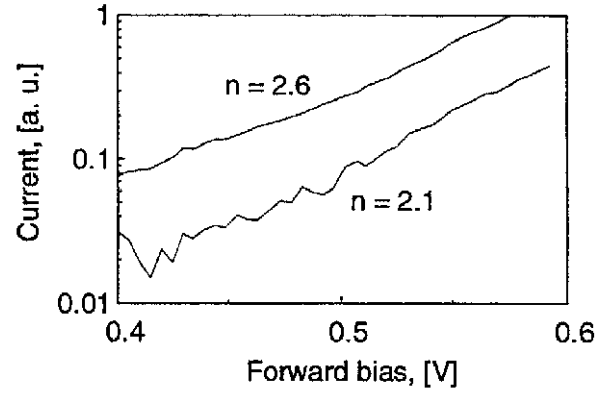


Fig. 7: DPCT (left) and EBIC image (right) of a shunt between grid lines

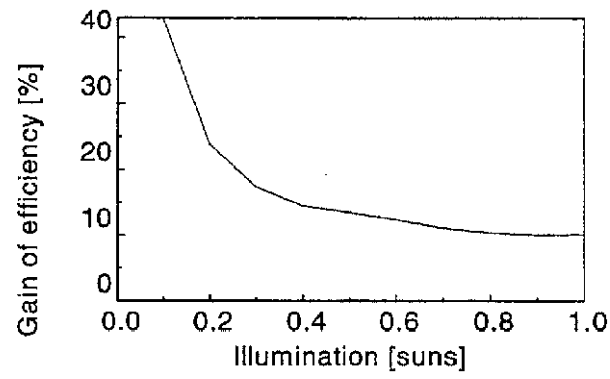
Besides of the local shunts Fig. 2 also shows extended regions of enhanced injection density as bright regions. These regions correlate with dark regions in Fig. 3, hence in positions with a low forward current we have a larger diffusion length. This principally agrees with the predictions of classical Shockley diode theory. However, the correlation is not one-to-one, and especially the regions of dark LBIC contrast appear to be localized more clearly than the bright DPCT contrast ones, more looking like smooth clouds. This smoothness cannot be attributed solely to the limited spatial resolution of DPCT, which is about 2 mm (2 pixels). Another argument for a different physical origin of the DPCT contrast may be derived from local I-V-characteristics measurements. Since the DPCT signal is proportional to the local dissipated power, the quotient of it to the applied bias is proportional to the current at varying biases. Thus, local I-V-characteristics have been measured thermally in positions of local shunts „in circuit" without destructing the cell. The general observation was that local shunts have either a linear or an exponential characteristic with a considerably higher n-factor than undisturbed regions. Detailed results will be published soon. Fig. 8 shows thermally measured local I-V-characteristics of a typical bright region and a typical dark region in Fig. 2. It shows that the current at 0.5 V varies by a factor of 3 and the n-factor is somewhat lower in the dark region. When solar cells had been cut into small pieces of several cm^2 size, these extended regions of increased injection density sometimes also have disappeared, just as it had been reported for edge shunts. This points to a contribution of internal mechanical stress also to this shunting mechanism, which may get released by dividing the cell into small pieces.

Fig. 8:
Thermally measured local I-V- characteristics of a typical bright (top) and a dark region (bottom) in Fig. 2



Based on the local I-V-characteristics of „good" crystal regions in Fig. 4 (bottom) we may calculate the quantitative influence of all shunting regions. First we assume a hypothetical solar cell that would consist only of „good regions". Such a cell would have an n-factor of 2.1 (contrary to 2.35 of the real cell), and at 0.5V forward bias its current would be about a factor of 3 below that of the real cell. Assuming validity of the superposition principle we have estimated the maximum power output both of the real cell and of a hypothetical „good" cell without any shunting regions as a function of light intensity. Fig. 9 shows as a result the calculated gain in efficiency if the real solar cell would be replaced by the hypothetical cell. It shows that the possible improvement is highest for low light intensities. This is a result of the higher n-factor of the I-V-characteristics of all shunting mechanisms, which strongly increases their relative influence for lower biases. A further (illumination-independent) improvement of the efficiency by approx. 10% may be expected regarding the fact that „good" regions of the cell also have a somewhat higher Jsc.

Fig. 9:
Hypothetical improvement of efficiency if all shunting actions could be avoided as a function of light intensity



Contrary to our original expectations, until now single grain boundaries never have been found to act as shunts themselves. Hence, multicrystalline material has the potential to allow fabrication of solar cells with high Voc. However, the multicrystallinity of the material may be responsible not only for losses in Jsc, but also indirectly for certain shunts. So grains of certain orientation may become especially rough due to the chemical texturization, therefore becoming especially sensitive to mechanical violation during wafer handling. These violations may become shunts whenever they are below metallization lines. Also dominant local shunts at the edges of the cells often have been found in positions where grain boundaries accumulate. We have found clear indications that internal mechanical stress may affect or even induce shunts

(see Fig. 4). Probably internal stress during crystal cooling is even responsible for the appearance of regions of bad crystal quality, which have been found to have low Jsc and be correlated with shunts. The quantitative influence of all shunts has been proved by calculation to strongly increase with decreasing illumination intensity from approx. 10% at 1 sun to about 40% at 0.1 sun. This result clearly shows that avoiding shunting actions in these solar cells gives the potential for a considerable improvement of the overall efficiency of a photovoltaic system, especially if it works in regions where the average light intensity is low.

The authors are indebted to D. Karg and G. Pensl (Erlangen) for experimental cooperation and to E. Schaeffer (Freiburg) for carrying out the LBIC investigations. This abstract is an extended version of the paper sent for publication in [6]. This work was supported by the BMBF under contract No. 0329 536 E and, in part, by the International Soros Education Program (ISSEP) through grant No. PSU062050.

References

[1] C. Häßler, S. Thurm, W. Koch, D. Karg, and G. Pensl, „Mesadiode Analysis of Solar Cells (MASC): A New Characterization Technique for Solar Silicon", 13th Eur. Photovolt. Solar Energy Conf. 1995, pp. 1364 - 1367.

[2] D. Karg, C. Häßler, and G. Pensl (Univ. Erlangen), private communication (1996).

[3] A. Simo and S. Martinuzzi, „Hot Spots and Heavily Dislocated Regions in Multicrystalline Silicon Cells", 21st IEEE PVSC, 1990, pp.800-805.

[4] O. Breitenstein, W. Eberhardt, and K. Iwig, „Imaging the Local Forward Current Density of Solar Cells by Dynamical Precision Contact Thermography", First WCPEC, 1994, pp. 1633-1636.

[5] O. Breitenstein and K. Iwig, „Forward Bias Shunt Hunting in Solar Cells by Dynamical Precision Contact Thermography", 13th Eur. Photovolt. Solar Energy Conf., 1995, pp. 145-149

[6] O. Breitenstein, K. Iwig, and I. Konovalov, „Identification of Factors Reducing Voc in MC Silicon Solar Cells", 25th IEEE PVSC, Washington D.C. 1996, in print

Thin film solar cells from crystalline silicon

Jürgen H. Werner[a,b),1], Ralf B. Bergmann[b)], Rolf Brendel[b)], and Uwe Rau[c)]
[a)]Institute for Physical Electronics and Photovoltaics,
University of Stuttgart, Stuttgart, Germany
[b)]Max-Planck-Institut für Festkörperforschung, Stuttgart, Germany
[c)]University of Bayreuth, Bayreuth, Germany

1 Introduction

Thin film cells from crystalline Si on foreign substrates promise further cost reductions in photovoltaics. The indirect band gap of crystalline Si leads to a relatively weak absorbance of near band gap light. However, *even without* light trapping structures, about 30 µm of pure Si suffice to absorb more than 75 % of the sunlight with photon energies hν>1.12eV.

Films of the thicknesses discussed here need mechanical support by a substrate. In contrast to most other groups, that use either graphite or a re-usable Si substrate, we prefer glass. Glass has the following advantages: i) low fabrication cost (several 10 DM/m^2), ii) chemical and mechanical stability, iii) the insulating property allows for integrated connections of cells, and, iv) the high transparency permits the implementation of light trapping structures.

Despite all of these apparent advantages of thin film Si on glass, there are substantial challenges for basic research as well as for technology if one aims at the development of efficient crystalline cells on glass.[1] This contribution flashes some light on recent work of our group.

2 Deposition on glass

Conventional glasses have maximum transformation temperatures of 650 °C. In contrast, deposition processes for high quality Si from the gas phase need temperatures around 1000 °C. This temperature gap of 350°C is the main problem in a technology of Si on glass.

Our first experiments used commercial glasses and aimed at *low-temperature* deposition of Si on glass by liquid phase epitaxy (LPE), which yields large grains of up to several hundred microns.[2] Unfortunately, similar to work of another group,[3] these films were discontinuous and therefore not appropriate for the processing of large area solar cells. Our subsequent experiments were therefore oriented towards the formation of a seeding layer

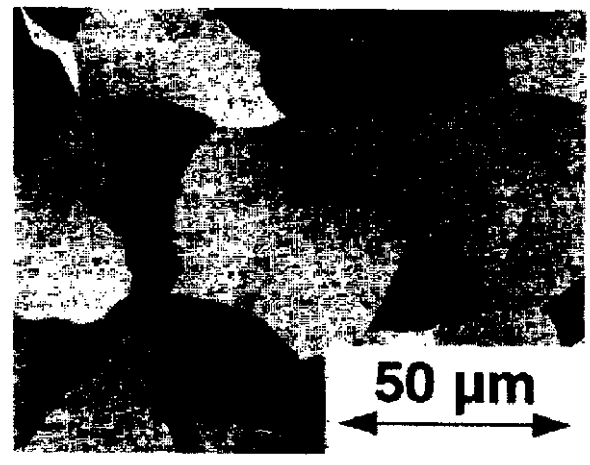


Fig. 1: Optical micrograph of a 150 nm thick $FeSi_2$ seeding layer on glass. Coevaporation of Fe and Si at 400 °C yields a closed film with large grains. These grains appear appropriate to serve as a seeding layer for the subsequent epitaxy of Si.

[1] FAX:++49-711-689-1606, e-mail: werner@quasix.mpi-stuttgart.mpg.de

on glass, which should mediate epitaxy. For the seeding layer, we employed either i) $FeSi_2$ from co-evaporation of the elements Fe and Si, ii) an Al/Si layer formed by a solution growth process, or iii) chemically vapor deposited Si seeding layer.

Fig. 1 presents an optical micrograph of $FeSi_2$.[4] During the co-evaporation of Fe and Si on glass at T=400 °C, large $FeSi_2$ grains form spontaneously, which seem suited as seeds for a subsequent epitaxy of Si to obtain a Si/$FeSi_2$/glass stack. However, despite several experiments of Si deposition on $FeSi_2$ above and below 850 °C, we did not succeed in finding epitaxial relationships between Si and the $FeSi_2$. Obviously, the lattice mismatch of +2% to -5.5% between the cubic Si and the orthorhombic $FeSi_2$ prevents epitaxy.

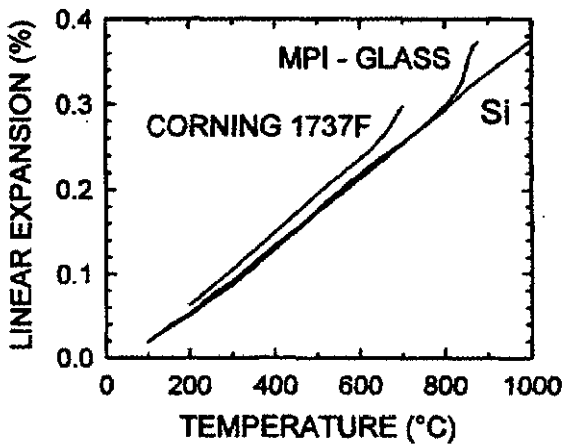


Fig. 2: Expansion coefficient of our new glass in comparison to Si and to the Corning 1737F glass. The transformation temperature of the new high-temperature glass is about 200 °C above the one of the Corning glass. The expansion coefficient matches that of polycrystalline Si.

In case ii) of the Al/Si seeding layers, no continuous films could be obtained. Consequently, at present only case iii), the seeding layers from Si, promise epitaxy of Si.

We prepare the crystalline Si seeds by first depositing amorphous Si form Si_2H_6 and a subsequent solid phase crystallization.[5] The (area-weighted) grain size distribution has a maximum at a grain size of 2.5 μm. On these seeding layers, chemical vapor deposition (CVD) at from $SiHCl_3$ at 1000 °C serves then to form the light absorbing base layers of our Si solar cells.

Fig. 2 shows the thermal expansion coefficient of our newly developed glass, which makes possible the epitaxy at 1000 °C for at least 30 min. Our glass has a transformation temperature T_t=820 °C and exceeds the transformation temperature of commercial glasses by about 200 °C. In addition, the new glass matches closely the expansion coefficient of polycrystalline Si. This glass enables the use of conventional high-temperature processing (such as oxidation, diffusion etc.) for a technology of Si on glass. For example, we are able to perform a systematic comparison of liquid phase epitaxy and chemical vapor deposition on the Si seeds. Both of these techniques require deposition temperatures above 850°C. As a result of these experiments, we find high temperature CVD to be more appropriate then LPE for the deposition of Si on glass.[6]

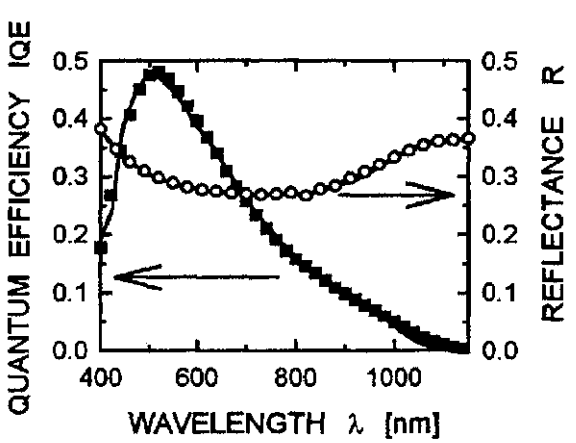


Fig. 3: Internal quantum efficiency (black squares) and reflectance (open circles) of a 10 μm thick test structure. The fit yields an (electron) diffusion length of 1.8 μm.

3 Electronic Properties

First Hall effect measurements on our polycrystalline Si on glass yield majority carrier (hole) mobilities of 68 $cm^2/(Vsec)$ at a boron doping of $7x10^{17}$ cm^{-3}. This mobility exceeds 1/3 of the hole mobility in single crystalline material of the same doping and should therefore be high enough to avoid series resistance problems in solar cells.[7] The measurements of the internal quantum efficiency in **Fehler! Verweisquelle konnte nicht gefunden werden.** reveal a minority carrier diffusion length of 1.8 µm.

4 Light trapping

The light of the sun has to be captured within the thin Si film. Intelligent structuring of the glass substrate before Si deposition permits much higher absorbances than previously thought. Our experiments as well as modeling prove that the structure of Fig. 4 with a 4 µm thick Si film on glass absorbs about 80 % of the sunlight.[8] These thicknesses are comparable to those of conventional thin film materials such as amorphous Si, CdTe or $CuInSe_2$. The recently proposed structure in Fig. 5 is even more effective: With a 4 µm thick Si film, the pyramidal shape of the glass permits to absorb photons which correspond to a current of 37 mA/cm^2. This current corresponds to 85 % of the maximum, theoretical short circuit current of 44 mA/cm^2 of a Si cell under AM1.5G illumination. Light trapping imposes therefore no severe problems to reach high efficiencies with thin films Si on glass.

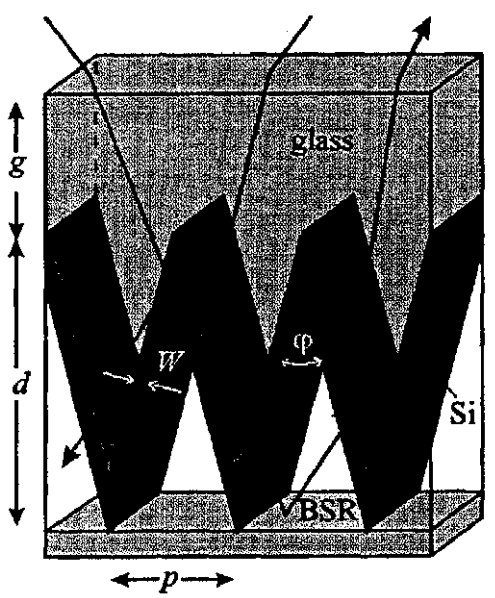


Fig. 4: Light trapping structure with "Encapsulated-V" texture.[8] The back side reflector (BSR) increases the probability for the trapping of light. With a groove angle of φ=30°, a 4 µm thick Si film captures light that corresponds to a current of 35 mA/cm^2. This current represents 80 % of the limiting value for crystalline Si.[8]

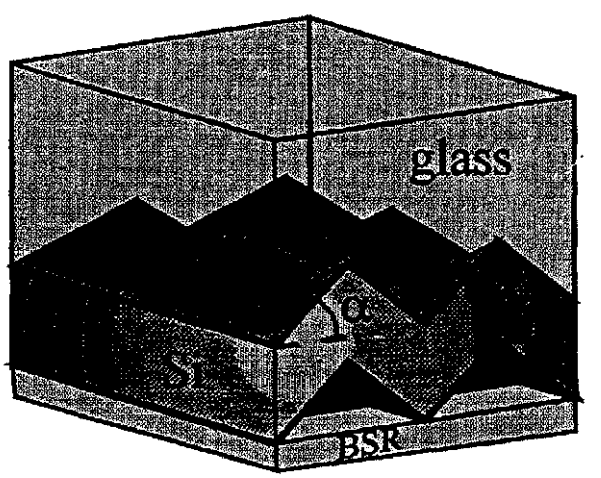


Fig. 5: Light trapping structure with pyramidally structured glass. A film of 4 µm thickness and a texture period of p= 15 µm absorbs photons which correspond to 37 mA/cm^2 short circuit current density under AM1.5G illumination. This current represents 85 % of the limiting value for Si.[5]

5 Efficiency Potential/Modeling

The diffusion lengths in our Si films on high-temperature glass amount up to about 2 µm. This value corresponds to an efficiency potential of 12-15%, if 4 µm thin films are used in a light trapping schema as shown in Fig. 5.[5] At present, shunts prevent us to make full use of this potential.

Our present cells use a single pn-junction. Here, our approach differs from the one of Green and Wenham,[9] who proposed to use the so-called multijunction solar cell, which consists of a *stack* of pn-junctions. In order to investigate the potential of multijunctions, we performed a detailed numerical simulation of solar cells, which are based on the light trapping structure of Fig. 4.[10]

On the one hand, multijunction solar cells promise a high carrier collection efficiency (and therefore a high short circuit current), even if small-grained silicon with low values for the diffusion length is used. On the other hand, the higher the number n of junctions, the higher is the chance for recombination in the space charge region, which limits the cell voltage.[10] Unconventional solar cell structures as those of Fig. 4 and Fig. 5 offer possibilities to keep the number of junctions as low as possible.

The benefit of multiple junctions in combination with the Encapsulated-V structure of Fig. 4, if any, is marginal: Fig. 6 compares the (theoretical) efficiencies of solar cells with different numbers n of junctions and different Si thicknesses d for three different values of the Shockley-Read-Hall lifetime τ_{srh}. These calculations are based on two-dimensional modeling and assume a recombination velocity of 10^4cm/sec for the front and back surface.[10] The higher the thickness d of the Si, the larger is the number n of junctions, that is required, to reach a certain efficiency. Compared to a single junction, one obtains about 1.5 % more efficiency, if n=3 or n=4 junctions are used. These results demonstrate the high capabilities of intelligent structures for light trapping even with a single junction.

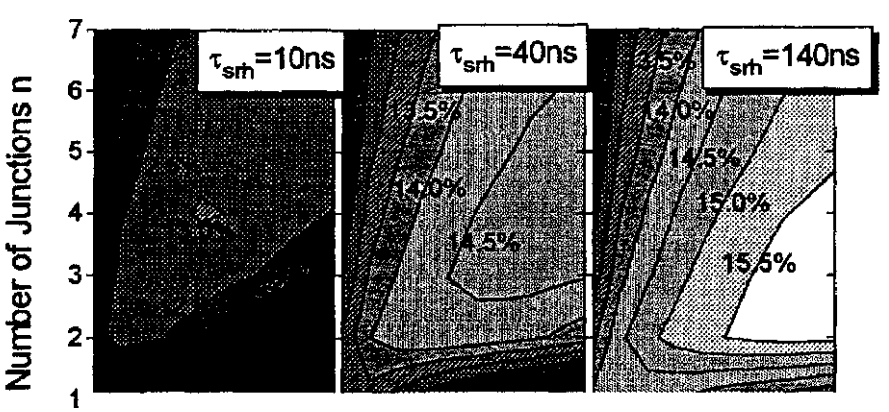


Fig. 6: Efficiency of single (n=1) and multijunction (n>1) cells for the Encapsulated-V structure of Fig. 4 for several lifetimes τ_{srh}. The larger the thickness d, the more layers are required to maintain high efficiencies.[10]

6 Outlook

The new high-temperature resistant glass enables us to process Si on glass with conventional Si technology: Diffusions at 900°C, high temperature oxidation and deposition processes are now possible for Si on glass. These processes are not only interesting for solar cells but also for the technology of thin film transistors for flat panel displays as well as for conventional technology of thick crystalline Si wafers. Bonding Si on glass, SOI techniques as well as mechanical supports could gain from this glass, which is matched to the thermal expansion coefficient of Si.

At present, our Si films on glass (deposited by $SiHCl_3$) have grain sizes of several microns, (hole) mobilities around 70 $cm^2/Vsec$ and (electron) diffusion lengths up to around 2 µm. Together with novel light trapping structures, the present material quality would allow to fabricate solar cells up to about 12-15 % efficiency even with a single pn-junction. The gain of multiple junctions would be very small.

7 References

[1] J.H. Werner, R. B. Bergmann, and R. Brendel, in *Festkörperproblemen/Advances in Solid State Physics*, ed. by R. Helbig (Vieweg, Braunschweig/Wiesbaden, 1994), Vol. 34, p.115

[2] S.H. Lee, R. Bergmann, E. Bauser, and H.J. Queisser, Mat. Lett. **19,** 1 (1994)

[3] Z. Shi and M. A. Green, J. Electrochem. Soc. **140,** 3290 (1993)

[4] R. Bergmann, J. Kühnle, J.H. Werner, S. Oelting, M. Albrecht, H.P. Strunk. K. Herz, and M. Powalla, in *Proc. 1st World Conf. Photovolt. Energy Conv.* (IEEE, New York, 1994), p.1398

[5] R.B. Bergmann, R. Brendel, M. Wolf, P. Lölgen, J.H. Werner, J. Krinke, and H.P. Strunk, in *Proc. 25th IEEE Photovolt. Spec. Conf.* (IEEE, New York, 1996), in press

[6] J. Kühnle, R.B. Bergmann, J. Krinke, and J.H. Werner, Mat. Res. Soc. Symp. Proc. **126,** xxx (1996) in press

[7] U. Rau, unpublished

[8] R. Brendel, in *Proc. 13th Europ. Photovolt. Solar Energy Conf.* (Stephens &Assoc., Bedford, UK, 1995), p.436

[9] M.A. Green and S. Wenham, Appl. Phys. Lett. **65,** 2907 (1994)

[10] U. Rau, T. Meyer, M. Goldbach, R. Brendel, and J.H. Werner, in *Proc. 25the IEEE Photovolt. Spec. Conf.* (IEEE, New York, 1996), in press

MULTICRYSTALLINE SILICON SOLAR CELLS BY LIQUID PHASE EPITAXY

A.W. Blakers and K.J. Weber

Department of Engineering, The Australian National University, Canberra, ACT 0200, Australia

Abstract

We have investigated the growth of thin silicon films by liquid phase epitaxy (LPE) on single crystal and multicrystalline silicon substrates. It is found that high lifetimes (>10 μsec) can be achieved under a range of growth conditions. The main difference between growth on multicrystalline substrates and growth on single crystal wafers is the development of grooves in the epitaxial layers in the vicinity of grain boundaries in the former case.

The optical properties of thin grown–silicon structures on opaque substrates has been studied. It is concluded that the presence of an opaque substrate that does not contribute to the photocurrent is not necessarily a serious problem. Reflection control and light trapping have been studied and a suitable low cost method identified that yields results at least as good as with randomly textured (100) single crystal wafers.

Low cost, low quality silicon substrates are a good substrate choice compared with non–silicon alternatives.

1. INTRODUCTION

Since the advent of photovoltaics, silicon has been the most widely used material for the fabrication of solar cells for terrestrial applications, and both its advantages (abundance, near – ideal bandgap for photovoltaic energy conversion, non toxicity) and its disadvantages (high cost of high quality, single crystal or multicrystalline silicon, weak absorption of infra-red light) are well documented. Since the cost of the silicon substrate represents are large fraction of the cost of a photovoltaic module, it has been recognised that a reduction in silicon materials cost, without a concomitant reduction in cell efficiency, is a necessity in order to reduce the cost of silicon cells.

In principle, thin film silicon cells, in which the active layer is 20–100 μm in thickness, can meet these demands. As the layer thickness is reduced, lower quality silicon can be tolerated while still maintaining adequate cell efficiencies. Further, material consumption is reduced. Consequently, thin film silicon deposition techniques such as liquid phase epitaxy (LPE), chemical vapour deposition (CVD) and zone melt recrystallization (ZMR) have attracted considerable attention. Impressive results have been achieved by several groups for solar cells fabricated on single crystal epitaxial layers grown by LPE [Blakers et al. (1995), Werner et al. (1993), Zheng et al. (1994)] and by CVD [Werner et al. (1994)]. However, obtaining good results on cheaper substrates is considerably more challenging.

An efficiency of 16% was reported by ZMR [Ishihara et al. (1995)]. Although these authors used single crystalline silicon substrates, the silicon surface was oxidised and no seeding windows were required. Therefore, it should be possible to obtain similar efficiencies on very low quality polycrystalline silicon substrates. However, the process involves a comparatively large number of steps.

Recently, several authors have investigated silicon LPE on multicrystalline silicon substrates [Ciszek et al. (1993), Wang and Ciszek (1994), Wagner and Steiner (1994)]. Growing on multicrystalline silicon rather than a foreign substrate such as glass, graphite or ceramics avoids the problems of thermal mismatch, substrate wetting and very small grain size, provided the grain size of the substrate is reasonable large. Growth on heavily doped substrates allows effective surface passivation of the active silicon layer through the formation of a high–low junction.

2. CHOICE OF SUBSTRATE

The growth of thin layers of high quality silicon on a low cost substrate requires the definition of a suitable substrate. Choice of substrate is bound up with choice of silicon deposition and recrystallisa-

tion temperature. The use of a high temperature deposition process has the advantage of improved crystal quality and the ability to use standard processing techniques for diffusions and surface passivation. However, high temperature processing probably eliminates glass as a viable option. Other substrates under consideration are opaque. Many substrates have been suggested for the high temperature deposition of silicon layers, including low cost silicon sheet, metal, graphite and ceramics. These substrates are likely to have minimal photovoltaic activity.

Loss of light from the grown silicon into an opaque substrate is a potentially serious problem. The insertion of a dielectric layer between the grown silicon layer and the substrate can reduce the loss by reflection at the high/low refractive index interfaces. It is certainly possible to remove the substrate after processing by chemical or mechanical means if the cell is attached to a strong superstrate. Whether this is practical on a large scale at low cost remains to be seen. The easiest approach would be simply to increase the thickness of the active layer and tolerate the loss of light.

An analysis using PC1D [Basore, 1996] was made of the optical effect of an opaque substrate on cell efficiency. The substrate was assumed to be heavily doped silicon with a minority carrier diffusion length of 2.6 microns ($\tau = 10$ nsec). In one case the substrate was assumed to be 150 μm thick, which approximates the minimum thickness that could be handled in an industrial environment at low cost with adequate yield. In the other case the substrate was assumed to be 5 μm thick, which approximates the cases where the substrate is physically removed after silicon growth or where a dielectric layer is interposed between the substrate and the grown silicon layer (or where the silicon is deposited on glass). A texturing scheme (random texturing of (100) silicon) was included to model the benefits of light trapping. The results are shown in figure 1.

The optimum thickness of the grown layer is approximately equal to the diffusion length in the case of a cell with a thick substrate attached, and half the diffusion length in the case of a cell without a substrate. However, it is a broad optimum, and thicknesses half the optimum would yield cell efficiencies of at least 95% of the efficiency of the optimum cell.

If the grown silicon layer is much thicker than a diffusion length then cell efficiencies are only slightly reduced if the substrate is still attached. In contrast, the performance advantage of a cell without a substrate diminishes markedly if the grown layer is thicker than optimum. If, for example, a buffer layer of silicon needs to be grown on a foreign substrate prior to high quality silicon growth, then the buffer layer should be thin to avoid interference with optical properties.

The angled coupling of light provided by surface texturing causes a current increase of a few percent. Some texturing schemes cause the light to be coupled in at a much larger angle than is the case with random pyramid texturing of (100) silicon, and would cause a larger current increase.

Attainable efficiencies in industrial practice are unlikely to be more than 80–90% of those shown in figure 1. If a minimum industrial efficiency of 15% is required then the minimum acceptable diffusion length in the grown silicon is about 50 μm.

The advantage of avoiding loss of light into the substrate diminishes as the diffusion length in the grown silicon layer improves. The reason for this is that the optimum thickness of the grown silicon layer increases, which increases light absorption in the grown layer. The performance advantage of a cell without substrate ranges from 5% for a diffusion length in the grown layer of 200 μm to 16% for a diffusion length of 20 μm. Relaxation of the idealities assumed in figure 1 (eg poorer quality texturing or lower back surface reflection) reduces the advantage of removing the substrate.

In summary, acceptable solar cell efficiencies can be obtained from silicon layers of modest quality grown on poor quality opaque substrates even if no steps are taken to reduce loss of light into the substrate. The additional cost of avoiding loss of light into the substrate must be set against the performance benefits to be obtained by so doing.

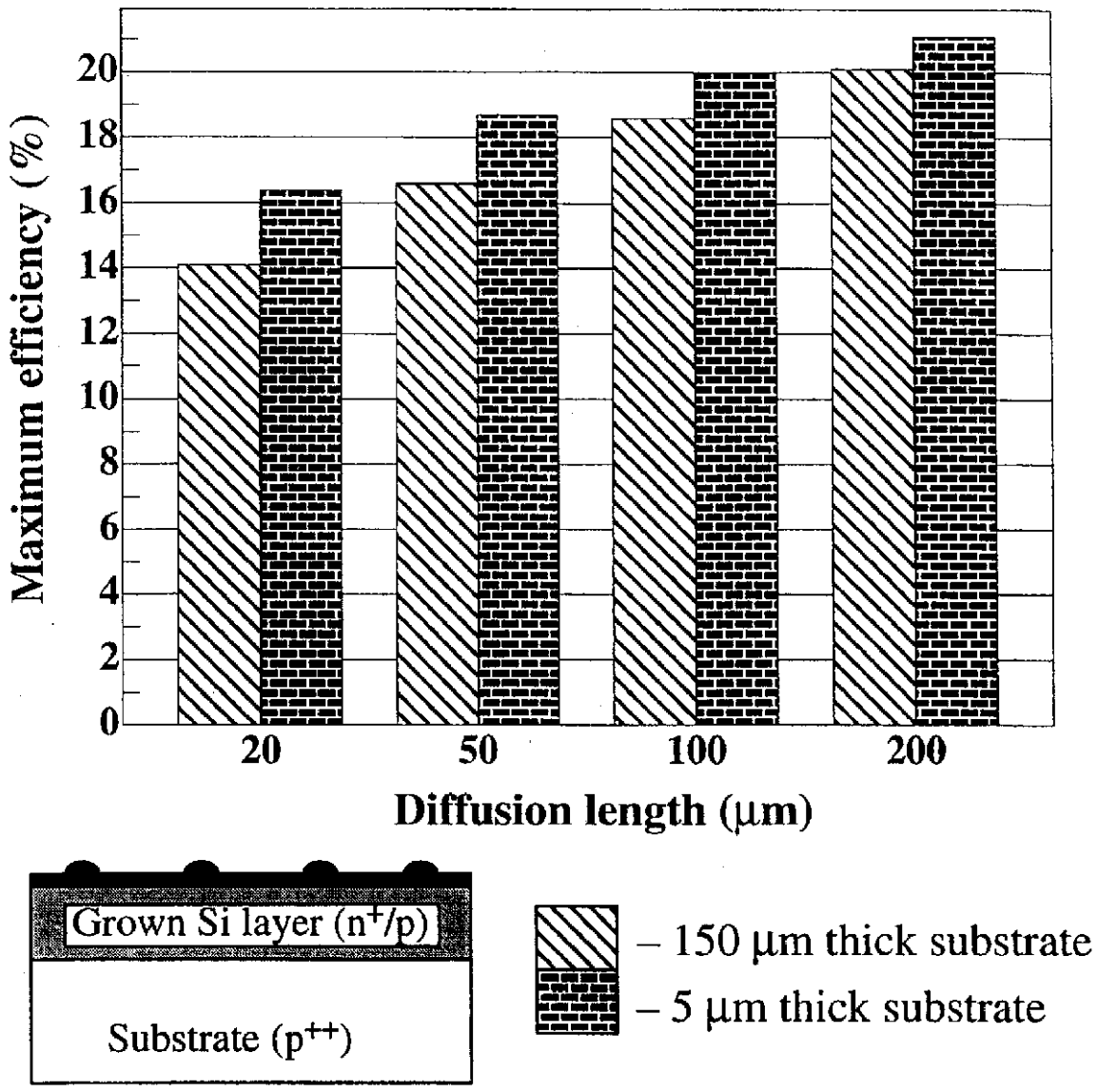


Figure 1: Maximum efficiency as a function of diffusion length for cells grown on a 5 μm or a 150 μm thick low quality p^{++} silicon substrate. Analysis uses PC1D and assumes zero top surface and 99% rear surface reflectivity; random (100) pyramid texturing; zero surface recombination; and a 1 Ω–cm epitaxial layer grown on a p^{++} substrate ($5x10^{18}$ cm^{-3}, τ=10 nsec, L=2.6μm)

Silicon has many advantages over non–silicon substrates and few disadvantages. Advantages include the elimination of thermal mismatch (which is particularly important in high temperature processing) and the pre–existence of a crystal template for the epitaxial process. As a result the quality of silicon grown on a silicon substrate (or a dielectric coated silicon substrate) is likely to be better than silicon grown on a foreign substrate. This will compensate for the modest optical advantage that a foreign substrate such as glass might have.

Silicon substrates can certainly be manufactured in a low cost manner if constraints on electronic quality are relaxed. Metallurgical grade silicon substrates are a suitable option. The problem of diffusion of impurities into the growing silicon layer can be controlled by soaking the substrates prior to growth in a chlorine ambient at a temperature 200° or so above the silicon growth temperature. Fast diffusing impurities will be removed by the chlorine while slow diffusing impurities will not migrate into the silicon layer during growth at a lower temperature. This is somewhat akin to work in the

1970s and 1980s on upgraded metallurgical silicon wafers for direct use, with the difference that the grown silicon layer will contain neither the fast nor the slow diffusing impurities.

3. CONTROL OF OPTICAL LOSSES

Texturing reduces reflection losses from the top surface of a cell and usually leads to light trapping within the cell. Low cost cells are likely to be multicrystalline, which means that pyramid texturing used for (100) single crystal cells is not very effective. A number of other approaches have been tried, such as using dicing saws or lasers to groove the surface. However, if the grown silicon layer is thin then these approaches are inappropriate.

The quality of a texturing scheme can be assessed by using a spectrophotometer with attached integrating sphere. The resulting reflection vs wavelength data can be convoluted with solar photons/m^2/μm vs wavelength data to obtain the photons lost by reflection in each wavelength band. Integration over the wavelength range 300–1100 nm then yields the loss in short circuit current compared with a hypothetical zero reflection solar cell (the 'weighted photon loss').

One approach to shallow texturing is to use an isotropic acid etch to produce 3–5 μm deep 'tubs' in the surface (Stocks et al, 1994). The process is rather similar to producing 'inverted pyramids' which are used in highest performance silicon cells. In conjunction with an antireflection coating, reflection losses can be reduced to low levels. Importantly, the light trapping quality of such a structure is better than for textured (100) wafers. A weighted photon loss over the wavelength range 300–1100 nm from *encapsulated* multicrystalline wafers of < 4% have been measured with such structures. Most of this reflection loss is from the top surface of the glass (which has an MgF_2 coating). Excellent results have recently been obtained using a greatly simplified process that dispenses with the photolithography. A weighted photon loss over the wavelength range 300–1100 nm from encapsulated multicrystalline wafers of 3.8% have been measured, with a minimum reflectivity of 2.4% at 645 nm. The structure is shown in figure 2.

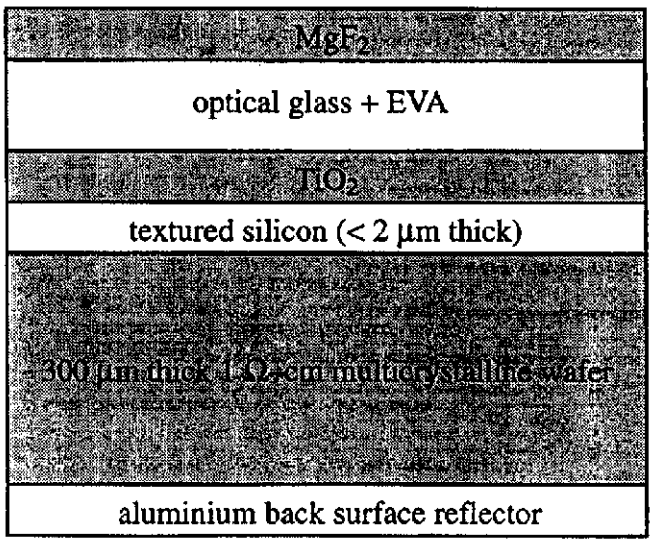


Figure 2: Structure for assessing the quality of shallow texturing processes.

The light trapping quality of a texturing process can be assessed by looking at reflection data in the wavelength range 1100–1400 nm where silicon does not absorb to create electron–hole pairs. A polished wafer will have a large reflectance (>80%) in this wavelength range because photons will reflect from the rear surface mirror and exit from the top surface. A small reflection loss from a structure such as figure 2 means that most of the photons must be trapped for a sufficient time to be lost to the weak parasitic processes of free carrier absorption and absorption in the aluminium reflector, EVA and glass. The simplified texturing process has a reflection in this region of < 15%, which is indicative of excellent light trapping. Reflectivity curves are shown in figure 3.

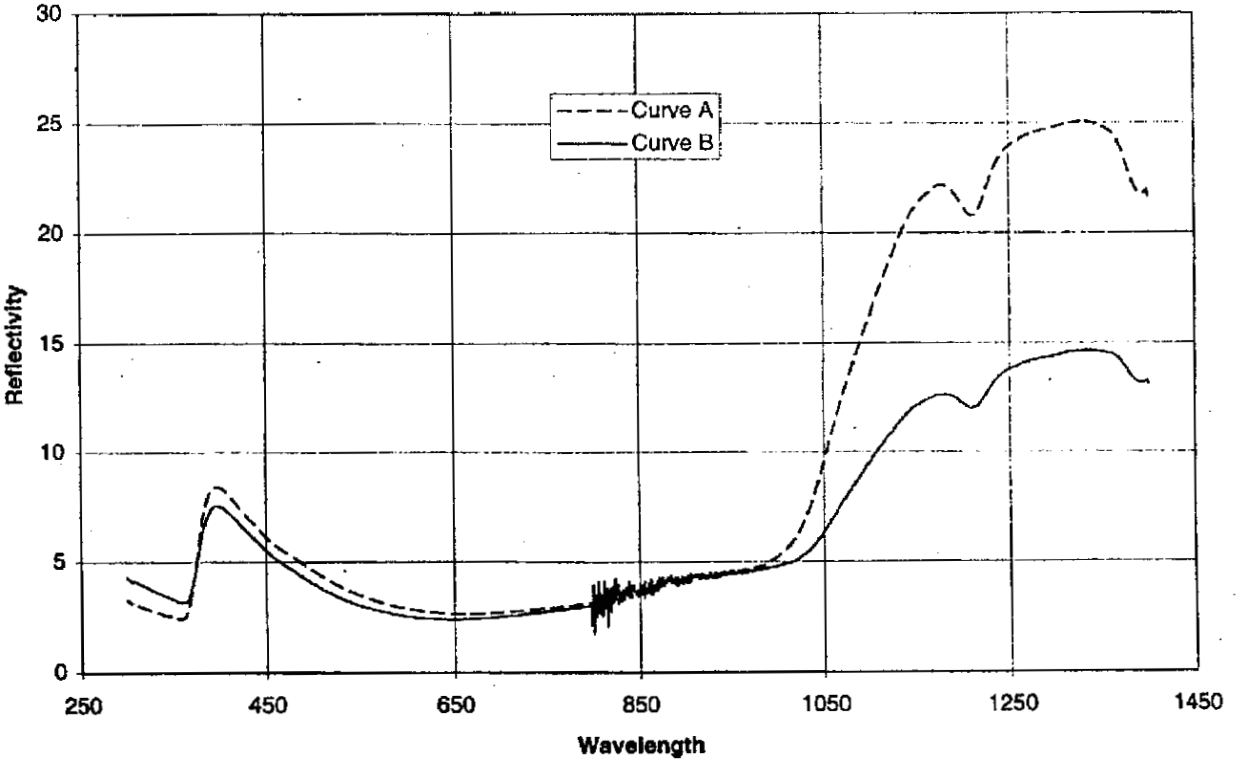


Figure 3: Reflectivity versus wavelength for encapsulated multicrystalline wafers (figure 2).
Curve A: photolithographically defined 'tubs'
Curve B: simplified texturing process

4. THE LIQUID PHASE EPITAXIAL GROWTH PROCESS

Thin silicon films of 30 to 50 μm thickness were grown by LPE using a tipping boat apparatus, as described previously [Weber et al. (1994)]. 60 gm of In were saturated with silicon at a temperature of 970^{0}C. A small amount of Ga was added to the melt to obtain p type epitaxial layers in the doping range 10^{16} to 10^{17} cm^{-3}. The melt was then supersaturated by cooling to 965 or 945 ^{0}C. Following supersaturation, the melt was brought in contact with the silicon substrate and cooled. Three different cooling rates were employed, namely 0.3, 0.7 and 2^{0}C/min.

The substrates used for the experiments were cast multicrystalline silicon wafers by Wacker Chemitronic, B doped to a resistivity of 0.015Ω–cm. The wafers were supplied as sawn and were mechanically polished with 1μm paste, followed by a chemical etch in an HF/HNO_3 solution in order to remove mechanical damage. Some of the wafers were only given a chemical etch in order to determine the influence of surface preparation on the epitaxial layer properties.

Retarded growth near grain boundaries in multicrystalline substrates was observed. This groove formation can be explained by the fact that LPE is a near equilibrium growth process, in which silicon atoms attach themselves to the most energetically favourable sites on the growing crystal. The higher energy required for attachment near a grain boundary thus makes grain boundaries unfavourable growth sites. The development of these grooves is in general undesirable as the resulting increased roughness of the layers makes further processing more difficult.

5. ELECTRONIC QUALITY OF EPITAXIAL LAYERS

For photovoltaic purposes, an important parameter of the epitaxial material is the minority carrier lifetime. For a high efficiency solar cell, the minority carrier diffusion length, given by $L=(D\tau)^{1/2}$

where D is the diffusion coefficient and τ the minority carrier lifetime, should be at least twice the active layer thickness. For a typical thin film silicon cell with a thickness W=50μm, the diffusion length should be at least 100μm. For D=20cm^2/s this gives τ=5μs.

The minority carrier lifetime of the epitaxial layers was determined by the photoconductive decay (PCD) method. Epitaxial layers were grown on heavily doped, 0.015 Ω–cm Cz or cast multicrystalline silicon wafers. In the case of growth on the multicrystalline substrates, two layers were grown on top of each other to obtain a thicker epitaxial layer. The multicrystalline substrates were selected from the same part of the growth ingot and so had nearly identical grain structures. Following growth, the heavily doped substrate was completely removed by chemical etching. Surface passivation was achieved either using an iodine/ethanol solution in the case of the single crystal epi layers or by a light phosphorus diffusion on both sides of the layer followed by growth of a thin oxide, in the case of the multicrystalline epi layers.

Tables 1 and 2 show the values for the effective minority carrier lifetime, τ_{eff}, obtained by PCD. It can be seen that high minority carrier lifetimes can be obtained, independent of cooling rate. The last column in table 2 is for an epitaxial layer grown on an unpolished substrate. In this case the wafer had only been given a short chemical etch to remove remove sawing damage. From the result it is apparent that mechanical polishing is not a necessary substrate preparation step in order to obtain high quality epitaxial layers. This result is important due to the high cost associated with wafer polishing, which is incompatible with a low cost solar cell process.

	Epi layer number and cooling rate		
	K147 0.3^{0}C/min	K145 0.7^{0}C/min	K150 2^{0}C/min
Effective lifetime, τ_{eff} (μs)	9.6	10.0	7.6

Table 1: Effective minority carrier lifetimes of single crystal epitaxial layers

	Epi layer number and cooling rate			
	K175 0.3^{0}C/min	K176 2^{0}C/min	K178 0.7^{0}C/min	K179 0.7^{0}C/min
Effective lifetime, τ_{eff} (μs)	9.5	7.5	9.1	11.0

Table 2: Effective minority carrier lifetimes of multicrystalline epitaxial layers

The actual minority carrier lifetime, τ_b, is related to the effective lifetime through

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{2S}{W}$$

where S is the surface recombination velocity (assumed equal on both surfaces) and W is the layer thickness. Thus the measured lifetime gives a lower bound on the bulk lifetime. For the single crystal epitaxial layers in particular, τ_b is likely to be substantially higher than τ_{eff}, because the layers were very thin (around 20μm). The values for the lifetimes in the multicrystalline layers are higher than the average lifetimes usually obtained in the Wacker silicon we used for the substrates, despite the relatively high doping levels in the epitaxial films. This can be attributed to the fact that the purity of layers grown by LPE is usually high and the defect density can be considerably lower than that in the substrate [Albrecht et al. (1994)]. These authors have also reported that the electrical activity of grain boundaries in the epitaxial layer is less than that in the substrate.

Solar cells made on heavily doped (5x10^{18} boron cm^{-3}) multicrystalline Silso wafers have displayed encouraging performance. Efficiencies of over 10% have been achieved without any antireflection

coating, which translates to about 15% after addition of an antireflection coating. Current work is aimed at incorporating the texturing process mentioned in section 3.

6.CONCLUSION

We have analysed substrate options for the growth of a thin high quality layer of crystalline silicon on a low cost substrate. We conclude that low quality, low cost silicon has many advantages over alternatives and no serious disadvantages.

We have investigated the influence of growth parameters for silicon epitaxial layers grown by LPE from an indium melt on a silicon substrate. We found that high minority carrier lifetimes can be achieved under a range of growth conditions. Solar cells made to date indicate that an efficiency of 16% should be readily achievable on heavily doped multicrystalline (Silso) silicon substrates. The challenge is to achieve such efficiencies in silicon grown on low quality but inexpensive silicon substrates.

ACKNOWLEDGEMENTS

We would like to thank other members of the photovoltaics group at the ANU for their contributions to this work. The financial assistance of the Energy Research and Development Corporation, the Australian Research Council and the NSW Office of Energy is gratefully acknowledged.

REFERENCES

•M. Albrecht, B. Steiner, T. Bergmann, A Voigt, W. Dorsch, H.P. Strunk and G Wagner, Proceedings of the Materials Research Society Meeting, Boston, 1994

•P. Basore, PC1D version 4, University of New South Wales, 1996

•A.W. Blakers, K.J. Weber, M.F. Stuckings, S Armand, G Matlakowski, A.J. Carr, M.J. Stocks, A. Cuevas and T Brammer, Progress in Photovoltaics **3**, 193 (1995)

•T.F. Ciszek, T.H. Wang, X. Wu, R.W. Burrows, J. Alleman, C.R. Schwerdtfeger and T. Bekkedahl, in the Conference Record of the 23rd IEEE Photovoltaics Specialists Conference, Louisville, Kentucky (1993) p. 65.

•T. Ishihara, S. Arimoto, H. Kumabe and T. Murotani, Progress in Photovoltaics **3**, 105 (1993)

•G. Wagner and B. Steiner, Solid State Phenomena **37/38** (1994) 427.

•M. Stocks, A. Carr and A.W. Blakers, Conf Record 1st World Conf on PVEC, p1551, Hawaii, 1994

•T.H. Wang and T.F. Ciszek, in the Conference Record of the 1st World Conference on Photovoltaic Energy Conversion, Hawaii (1994), p. 1250.

•K. J. Weber, A.W. Blakers and G. Matlakowski in the Annual Conference Record of the Australia and New Zealand Solar Energy Society (Ed. G. Morrison, D. Prasad and N. Watt) 1994, p. 476

•J.H. Werner, S. Kolodinski, U. Rau, J.K. Arch and E. Bauser, Applied Physics Letters **62**, 2998, (1993)

•J.H. Werner, J.K. Arch, R. Brendel, G. Langguth, M. Konuma, E. Bauser, G. Wagner, B. Steiner and W. Appel in the Conference Record of the 12th European Community Photovoltaic Solar Energy Conference (Ed. R. Hill, W. Palz and P. Helm) 1994, p.1823

•G. Zheng, W. Zhang, Z. Shi, S. Ghaemi, M. Gross, S. Wenham and M. Green in the Annual Conference Record of the Australia and New Zealand Solar Energy Society (Ed. G. Morrison, D. Prasad and N. Watt) 1994, p. 482

Light-Trapping in Thin Crystalline Silicon Layers

James A. Rand
Jeffery E. Cotter
AstroPower, Inc.
Solar Park
Newark, DE 19716-2000

Abstract

Enhancing the performance of thin crystalline silicon layers with light-trapping has been actively discussed in the literature for over two decades. The majority of these discussions have focused on the theoretical aspects of light-trapping, i.e. developing models and estimating the limits to which light-trapping can influence performance. The gap between experimental work and theory has recently begun to narrow.

Light-trapping has been incorporated in structures with thicknesses ranging from less than 1 micron to 400 microns with varying degrees of success. Assessing the effectiveness of light-trapping schemes is complicated by other losses, such as bulk or surface recombination. In ideal structures, the short-circuit current is the ultimate figure of merit for comparisons. In real devices, however, spectral response and reflection data, analyzed by different methods, are used to extract information about light-trapping. These techniques require assumptions that limit their usefulness in predicting final cell performance.

The talk that accompanies this paper will review recent publications regarding crystalline silicon experimental devices (significantly greater than 1 μm thick) and their light-trapping effectiveness. Measurement methods and potential pitfalls will be reviewed.

Introduction

Light-trapping offsets the relatively weak absorption of light in the near-bandgap region of silicon by maximizing the optical path length of light within the device. In general, optical path lengths greater than the thickness of the device are obtained by texturing one or both surfaces, and maximizing the reflection at the back surface. Texturing results in oblique paths for internally confined light and maximizes total internal reflection at the illuminated device surface.

Methods of light-trapping can be grouped into three categories.

Random Texturing. Random texturing holds promise due to the resulting performance potential and the hope that it can realized on substrates with differing physical properties. For Lambertian optical distributions, Goetzberger [1981] showed that the fraction of light reflected by total-internal-reflection at the illuminated surface is equal to $1-1/n^2$, where n is the refractive index of silicon (approximately 3.4). He pointed out that the front surface is highly reflective to Lambertian distributions of light, reflecting about 92% of exiting light by total internal reflection. Yablonovitch [1982] then showed that weakly-absorbed light of a Lambertian distribution travels

an effective path-length of $4n^2$ times the physical thickness of a dielectric layer. He pointed out that this path-length enhancement factor is about 50 for silicon.

Random textures can be achieved by a number of methods including sand blasting, natural lithography [Deckman, 1983], porous etching [Skryshevsky, 1996], rapid thermal processing of an aluminum-silicon interface [Cudzinovic, 1996], or by the use of random-textured ancillary dielectric layers such as ZnO [Gee, 1996; Hegedus, 1996] or SnO_2 [Hegedus, 1996], for example.

Geometrical Textures. Geometric textures are relatively easy to form on single crystal silicon surfaces by taking advantage of the orientation dependent etch rates generated by alkaline solutions. This approach has been used to fabricate the majority of light-trapping structures demonstrated to date. Common textures include 54 degree pyramids, inverted pyramids, slats, and perpendicular slats. A similar result can be achieved in multicrystalline substrates (with much more effort) with the use of mechanical sawing or laser ablation. An option for very thin layers is conformal growth on a textured substrate.

Analysis of geometrical textures is often carried out by computer-aided ray tracing techniques. Ray tracing analysis makes no assumptions about the distribution of light within the absorber layer. Instead, the path of any incident ray of light is traced out using knowledge of reflection and refraction at surfaces and absorption in the bulk regions. This technique is useful for the analysis of geometrically textured surfaces [Campbell, 1987] and other highly-complex geometries such as the Spheral Solar™ Cell [Bisconti, 1995], for example.

External Light Engineering. This final category includes all methods of redirecting light back to the solar cell after it has escaped. External reflectors and optical cavities are two examples of this technique. Miñano, et.al. [1992], have analyzed light-confining cavities for concentrator solar cells, for example.

Measurements of Light-trapping

Short Circuit Current. Ultimately, short circuit current is the best figure of merit for light-trapping effectiveness. The effect of light-trapping becomes more pronounced as the device thickness is reduced and surface interactions increase. Several analyses have been performed to establish the magnitude of the effect as a function of device thickness. The results of three different theoretical analyses are shown in Figure 1. The *no light-trapping* case was computed with PC-1D [Basore,1990] assuming no recombination losses, perfect anti-reflection coating, and perfect transmission out the back for light not absorbed on the first pass. Theoretical analysis of Green [1995] and Tiedje [1984] are included in Figure 1 and set the "best case" limit for perfect light-trapping. The analysis of Green appears to predict perfect collection for all thickness (J_{sc} = 44 mA/cm^2 independent of thickness). The method of Tiedje assumes random texture, Lambertian reflection, and realistic losses through the front surface loss cone on each interaction.

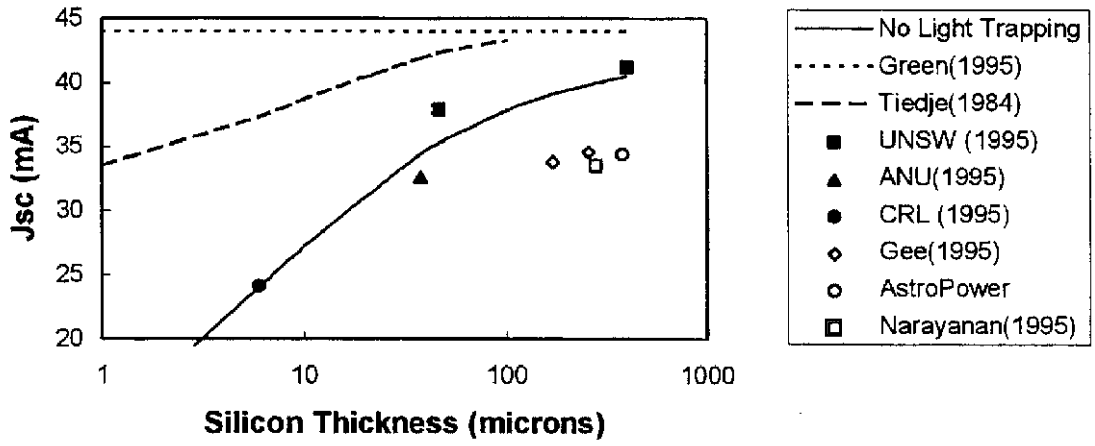


Figure 1. *Short circuit current density for silicon solar cells of varying thickness (AM1.5G, 100 mw/cm^2). Theoretical analyses are shown as lines. Recent laboratory results are shown as solid symbols. Commercial results are shown as open symbols.*

The use of short-circuit current as the figure of merit for comparisons allows the least complicated view of light-trapping effectiveness. The experimental results shown in Figure 1 indicate that most laboratory and on commercial devices have not yet exceeded the threshold current level capable of the ideal *no light-trapping* case. Losses due to imperfect anti-reflection coatings, bulk recombination rates and emitter losses offset gains from light-trapping. Short circuit current is dominated by other factors. This has prompted researchers to investigate analysis methods to measure the level of light-trapping obtained in a device with otherwise poor current collection properties [Rand,1991]. These methods have focused on the analysis of the spectral response and reflection data.

Extended Spectral Response. The extended spectral response method was developed by Basore [1993] to extract an effective optical pathlength for near-bandgap light. The method utilizes the data from a plot of $1/\alpha$ vs. 1/IQE, where α is the absorption coefficient for silicon and IQE is the internal quantum efficiency. An example of such a plot from the recent literature is shown in Figure 2. The inverse of the slope of the curve for the strongly absorbed light reflects the effective diffusion length of the device (when certain simplifying assumptions exist). For the data in Figure 2, an effective diffusion length of 10.8 microns is calculated. The second linear region (absorption lengths greater than 500 microns in this case) contains information regarding the optical properties of the structure. It is tempting, but incorrect to associate meaning to the slope alone.

The effective optical pathlength generated by the analysis proposed by Basore utilizes the information in the slope of the $1/\alpha$ vs. 1/IQE curve, an estimate of the collection efficiency of near-bandgap light, and the detailed reflection data, to generate an effective optical path length. This analyses requires that light be uniformly absorbed in the device, therefore limiting the results of the analysis to pertain to only weakly absorbed light. This limits the usefulness of this method for predicting the current generating properties. For current generating purposes, the response in the wavelength range of 800 to 1100 nm is critical due to the relatively high absorption coefficient and relatively high solar energy available, however the requirement for uniform absorption will

not be met. Examples will be given in the talk of the cases that require special interpretation of the results of the extended spectral response analysis technique.

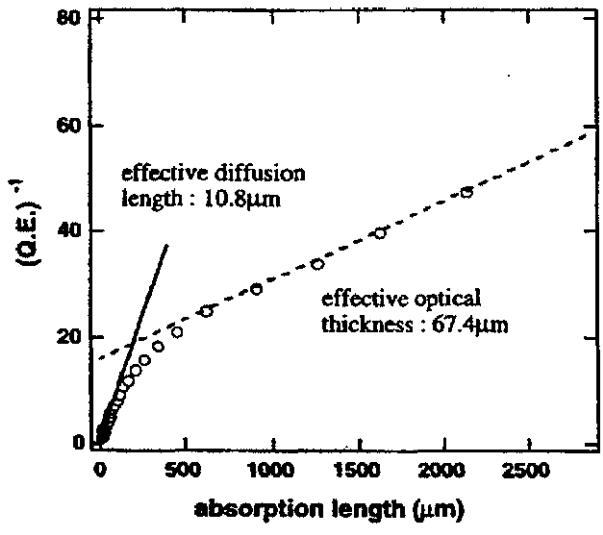


Figure 2. Plot of 1/α vs. 1/IQE for a recently reported textured 4 micron thick silicon device (after Yamamoto et al.[1996]).

Long Wavelength Reflection. Effects of the optical design of a structure can be seen in the long wavelength reflection. Escape reflection, defined as light initially transmitted into the structure that later escapes out the front surface, reaches significant levels in devices with reflective back surfaces. Escape reflection reaches a wavelength independent value in the limit of non-absorbed long wavelength light. An expression for the total reflection in this regime can be stated as

$$R_{Total} = \frac{R_{Front}(1-\rho_B)+\rho_B(1-\rho_{FI})}{1-\rho_B \cdot \rho_{FI}}$$

where ρ_B is the internal reflection of the back surface, ρ_{FI} is the internal front surface reflection, R_{Total} is the measured external reflection, and R_{front} is the reflection off the front surface alone. In this form, the measured reflection contains no explicit information regarding the light-trapping nature of the device under test. With an independent measurement of ρ_B, a value for the effective internal front surface reflection can be generated. However, this internal front reflection data can be used to imply only that *some* level of randomization of the light is occurring after the entering the device. No detailed information is available about the optical distribution within the solar cell. Examples will be given in the talk of cases that require special interpretation of the results of the long wavelength reflection analysis technique.

Conclusions

Significant interest in light-trapping structures has been found in the literature. The increased level of interest may in part be due to the heightened awareness of the potential of thin silicon layers as a major photovoltaic device option. Experimental laboratory devices are

demonstrating light-trapping within 10% of theoretical limits using orientation dependent texture-etching schemes. Commercial structures are still awaiting break-through level changes in thickness, bulk recombination, and surface recombination before sophisticated light-trapping techniques become a priority.

References

P.A. Basore, "Numerical Modeling of Textured Silicon Solar Cells Using PC-1D" IEEE Trans. on Electron Devices, ED-37, (1990), p. 337.

P.A. Basore, "Extended Spectral Analysis of Internal Quantum Efficiency", *Proceedings 23rd IEEE Photovoltaic Specialists Conference*, (May, 1993).

R. Bisconti and H.A. Ossenbrink, "Light Trapping in Spheral Solar™ Cells", *Proceedings 13th European Photovoltaic Solar Energy Conference*, (October, 1995), p. 386-389.

A.W. Blakers, et.al., "17% Efficient Thin-Film Silicon Solar Cell by Liquid-phase Epitaxy", *Progress in Photovoltaics: Research and Applications*, Vol. 3, (March, 1995), p. 193-195.

P. Campbell and M.A. Green, "Light Trapping Properties of Pyramidally Textured Surfaces", *Journal of Applied Physics*, (July, 1987), p. 243-249.

T.I. Chappell, "The V-Groove Multijunction Solar Cell", *IEEE Transactions on Electron Devices*, Vol. ED-26, (July, 1979), p. 1091-1097.

M. Cudzinovic and B. Sopori, "Control of Back Surface Reflectance from Aluminum Alloyed Contacts on Silicon Solar Cells", *Proceedings 25th IEEE Photovoltaic Specialists Conference*, (May, 1996) , to be published.

H.W. Deckman, C.R. Wronski, H. Witzke and E. Yablonovitch, "Optically Enhanced Amorphous Solar Cells", *Appl. Phys. Lett.*, Vol. 42(11), (1983), p. 968-970.

P. Fath, et.al., "Multicrystalline Silicon Solar Cells Using a New High-Throughput Mechanical Texturization Technology and a Roller Printing Metallization Technique", *Proc. 13th EPVSEC*, (October, 1995).

J.M. Gee, R.R. King, and K.W. Mitchell, "High-Efficiency Cell Structures and Processes Applied to Photovoltaic-Grade Czochralski Silicon", *Proceedings 25th IEEE Photovoltaic Specialists Conference*, (May, 1996), to be published.

J.M. Gee, R. Gordon and H. Liang, "Optimization of Textured-Dielectric Coatings for Crystalline-Silicon Solar Cells", *Proceedings 25th IEEE Photovoltaic Specialists Conference*, (May, 1996.), to be published.

A. Goetzberger, "Optical Confinement in Thin Si-Solar Cells by Diffuse Back Reflectors", *Proceedings 15th IEEE Conference*, (1981), p. 867-870.

M.A. Green, et.al., "Enhanced Light-Trapping in 21.5% Efficient Thin Silicon Solar Cells", *Proceedings 13th European Photovoltaic Solar Energy Conference*, (October, 1995), p. 13-16.

S.S. Hegedus and X. Deng, "Analysis of Optical Enhancement in a-Si n-i-p Solar Cells Using a Detachable Back Reflector", *Proc. 25th IEEE PVSC*, (May, 1996), to be published.

J.C. Minano, A. Luque and I. Tobias, "Light-Confining Cavities for Photovoltaic Applications Based on the Angular-Spatial Limitation of the Escaping Beam", *Applied Optics*, Vol. 31, No. 16, (1992), p. 3114-3122.

J.A. Rand and P.A. Basore, "Light-Trapping Silicon Solar Cells Experimental Results and Analysis", *Proceedings 22nd IEEE Photovoltaic Specialists Conference*, (October, 1991).

D. Redfield, "Multiple-Pass Thin-Film Silicon Solar Cell", *Applied Physics Letters*, Vol. 25, No. 11, p. 647-648.

V.A. Skryshevsky, et.al., "Effect of Porous Silicon Layer Re-Emission on Silicon Solar Cell Photocurrent", *Proceedings 25th IEEE Photovoltaic Specialists Conference*, (May, 1996.) , to be published.

D. Thorp, P. Campbell and S.R. Wenham, "Absorption Enhancement in Conformally Textured Thin-Film Silicon Solar Cells", *Proceedings 25th IEEE Photovoltaic Specialists Conference*, (May, 1996.) , to be published.

T. Tiedje, E. Yablonovitch, G.D. Cody, and B.G. Brooks, "Limiting Efficiency of Silicon Solar Cells", *IEEE Transactions on Electron Devices*, Vol. ED-31, (May, 1984), p. 711-716.

E. Yablonovitch and G. D. Cody, "Intensity Enhancement in Textured Optical Sheets for Solar Cells", *IEEE Transactions on Electron Devices*, Vol. ED-29, (February, 1982), p. 300-305.

K. Yamamoto, T. Suzuki, M. Yoshimi, and A. Nakajima, "Low Temperature Fabrication of Thin Film Polycrystalline Si Solar Cell on the Glass Substrate and Its Application to the a-Si:H/Polycrystalline Si Tandem Solar Cell", *Proceedings 25th IEEE Photovoltaic Specialists Conference*, (May, 1996.) , to be published.

J. Zhao, A. Wang, S.R. Wenham, and M.A. Green, "21.5% Efficient 47μm Thin-Layer Silicon Cell", *Proceedings 13th European Photovoltaic Solar Energy Conference*, (October, 1995), p.1566-1569.

Gettering of Defects and the Impurities in Solution Grown Silicon

Z Shi

Pacific Solar Pty Ltd
82-86 Bay Street, Botany NSW 2019 Australia
Telephone: (61-2) 316 6811; Facsimile: (61-2) 666 4079

1. Abstract

This paper reports the advantages of using the solution growth technique to produce high quality Si materials at low temperatures, either epitaxially on multicrystalline Si (mc-Si) substrate or on glass, due to its unique capability of gettering defects and impurities during crystal growth. The improved quality of liquid phase epitaxial (LPE) layer over that of the mc-Si substrate is confirmed by EBIC measurements. High quality large grain polycrystalline Si (pc-Si) layers were successfully grown on glass using solution growth techniques.

2. Introduction

Thin film polycrystalline silicon (pc-Si) is potentially an important material for low cost solar cell applications. Its lower cost potential than single crystalline silicon and superior electronic properties and stability compared to hydrogenated amorphous silicon (a-Si:H) have stimulated considerable R&D work in this area. A number of techniques have been investigated to produce pc-Si materials. These techniques include zone melt re-crystallisation (ZMR) using a strip heater, electron or laser beams [1], solid phase crystallisation (SPC) [2], and liquid phase epitaxy and/or solution growth [3]. ZMR is a higher temperature process (above the melting point of silicon) which is capable of producing pc-Si with grain size of hundreds of microns wide and millimetres long. In contrast, SPC is a low temperature (about 600°C) technique with pc-Si grain size of a few microns being demonstrated. Solution growth has unique advantages over these techniques such as low growth temperature, large grain size and low level of defects and impurities in the grown materials. These properties have been demonstrated by the improved material quality of silicon epitaxial layer by LPE over the multicrystalline Si (mc-Si) substrate, as presented in this paper, as well as large grain pc-Si prepared by solution growth at low temperatures.

3. LPE Growth of Silicon

Liquid phase epitaxy has been frequently used to produce epitaxial silicon layer on heavily doped single crystalline silicon wafers for thin film silicon solar cell applications. A variety of growth facilities were used to produce LPE silicon layers, such as tipping and dipping system, horizontal sliding boat and the centrifugal system. Figure 1 shows a schematic of the horizontal sliding boat mechanism.

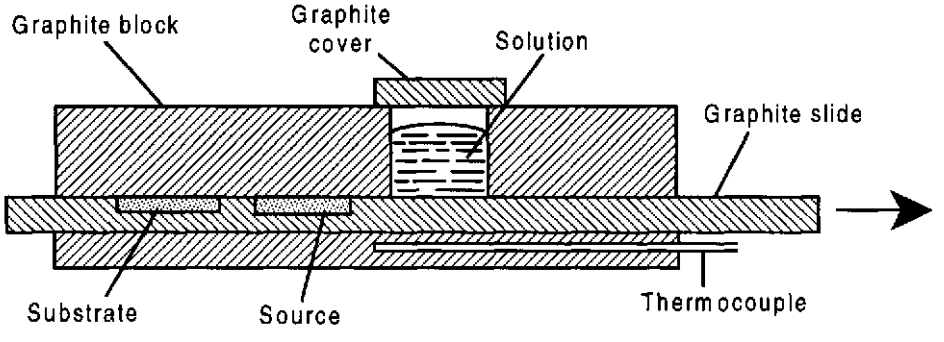
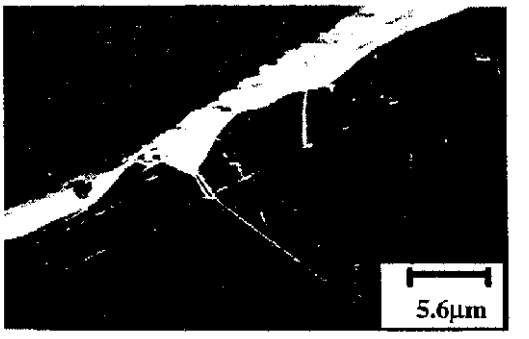


Figure 1 Sliding boat apparatus with arrangement for pre-saturation with silicon.

The metal solution is initially in contact with a source silicon wafer and subsequently is brought into contact with the growth substrate after the molten metal is saturated or super-saturated with silicon. The epitaxial growth proceeds as the metal solution is cooled at a specific cooling rate over a predetermined temperature range. The substrate is separated from the solution by the sliding action after LPE growth is completed. Low cooling rate is usually used to ensure the growth process is close to the equilibrium condition and thus high quality epitaxial film can be obtained. As the segregation coefficient of most impurities is smaller than one, the impurities remain in the metal solution rather than being incorporated into silicon crystals. The metals often used as the solvent for LPE growth are those which form an eutectic system with silicon. These include Sn, Ga, Al, In, Au, Cu and their alloys. Sn and In are often used to prepare LPE Si layer on heavily doped single crystalline silicon substrate for thin film solar cell fabrication because Sn is an isoelectric element with silicon and the solubility of In in silicon is fairly low (about $10^{16}/cm^2$ at 900°C). Hence, the incorporation of either into silicon does not introduce a high background doping level. The thin film silicon solar cells prepared in this way have demonstrated energy conversion efficiency above 17% [4], indicating a higher quality epitaxial material because the substrate is electronically inactive due to heavy doping, only serving as a crystal template.

LPE growth of silicon on cast multicrystalline silicon (mc-Si) substrate has also been investigated recently. Quite interesting results have been observed in this work. Figure 2 shows SEM cross-section images along grain boundary areas. The epi-layer/substrate interface can be clearly observed. The orientation of any given grain boundary in the epi-layer changes in three different ways from that of their counterpart in the substrate, namely; the orientation can follow the direction of the grain boundary in the substrate as shown in (2a); it can change direction to close to the normal to the substrate (2b) and it can turn away from the normal to the substrate as compared to that in the substrate (2c).

2a



2b

2c

Figure 2 SEM cross-section micrographs around grain boundary areas: the orientation of grain boundaries in LPE layer can follow its original in the substrate (a); move closer to the normal to the substrate (b) and move away from the normal to the substrate (c).

As the substrate material (mc-Si) was prepared at a much faster growth rate, a lot of crystal defects and impurities are frozen in the material. The location and orientation of grain boundaries thus are not necessarily in the lowest energy situation whereas LPE growth proceeds in an equilibrium condition and thus the orientation of grain boundaries can be rejustified in the epitaxial silicon layer during LPE growth.

Both the defect and the impurity levels are also significantly reduced in the LPE layers as compared to the mc-Si substrate. The improved quality in the LPE layers has been demonstrated by comparing the recombination activity of the dislocations and the grain boundaries in the layers and the substrates using electron beam induced current (EBIC) measurements [5].

It was reported that the grain boundary recombination showed much smaller effect in the LPE layers than in the mc-Si substrates [5], indicating a rather high collection efficiency and thus a comparatively higher electrical quality of the epitaxial layer as expressed, for example, by a longer diffusion length.

The improved electrical properties of the LPE layers on mc-Si substrates are a result of three effects: a reduced defect density, a reduced impurity content and a reduced electrical activity of dislocations and the grain boundaries of the layer. The lower impurity content in the layer is due to the gettering effect of the growth solution for most elements with a segregation coefficient smaller than one. A further contribution to the higher electron quality has resulted from the lower density of intrinsic atomic defects in the LPE layer as compared to the substrate. The near equilibrium growth method results in a thermo-dynamic equilibrium distribution of intrinsic point defects in contrast to that of the substrate.

4. Growth of Silicon on Foreign Substrate

Solution growth technique has been successfully used to produce large grain (above 100μm) high quality pc-Si thin films on foreign substrates such as glass at temperatures below 750°C. It is most difficult to prepare the pc-Si material of this quality using other techniques. Although pc-Si materials can be produced by SPC technique at the low temperature (about 600°C), neither grain size nor crystal quality is comparable to those of pc-Si prepared by solution growth technique.

Two experimental features were found to be crucial for obtaining successful crystal growth: good wetting of the substrate by the solution and supersaturation to provide a driving force for nucleation. With these two features well controlled during the experiments, continuous polycrystalline silicon thin films were successfully grown on glass substrates. Figure 3 shows a SEM picture of a continuous polycrystalline silicon thin film deposited on glass from Sn/Al alloy solution at a growth temperature of 700°C.

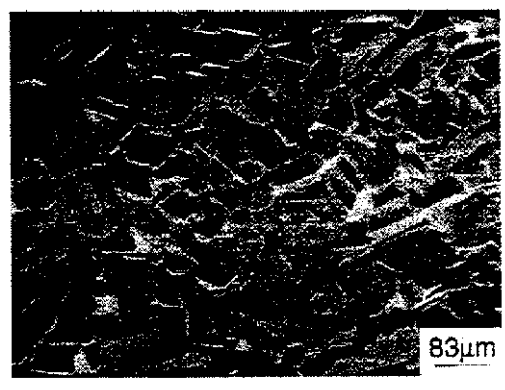


Figure 3 A SEM micrograph of a continuous pc-Si thin film on glass from Sn/Al alloy solution at a temperature of 700°C.

The film has a thickness of about 20μm and average grain size of larger than 100μm with the largest grains being up to 5mm² in area. The morphology of silicon thin films on glass is quite similar to that of silicon LPE layers deposited on polycrystalline silicon substrates.

Figure 4 shows an SEM micrograph of the cross-section of a silicon thin film on glass.

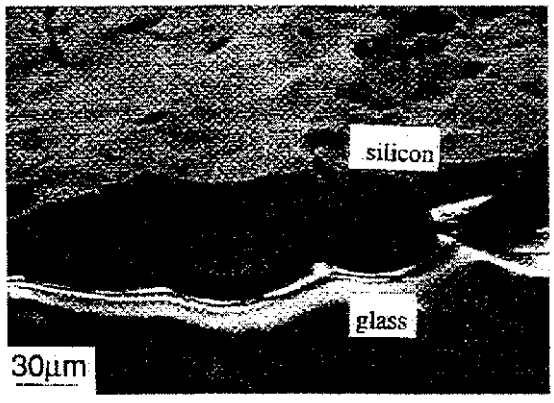


Figure 4 A SEM micrograph of the crosss-section of a pc-Si thin film on glass.

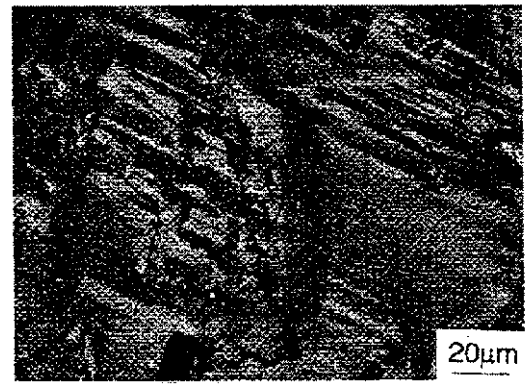


Figure 5 A micrograph of a Secco etched (30 secs) pc-Si thin film on glass.

X-ray diffraction spectra indicated that the orientation distribution of a silicon thin film changes with solution cooling rate and film thickness. (111) preferred orientation was obtained for slow cooling rate and thinner film thickness, while (110) oriented films were obtained using higher cooling rates and greater film thicknesses. Secco etchant was used to delineate crystal defects in the polycrystalline silicon films. As shown in Figure 5, few etch pits were observed on the facets of individual grains except twinned crystals. Twinned crystals, either flattened or elongated, are often observed in the growth of semiconductor crystals from molten metal solutions [6]. They are also often observed in silicon crystals pulled directly from molten silicon melt [7]. It is proposed that the re-entrant corner at a twin junction is a preferential site for nucleation of new layers [6]. Twinned grain boundaries do not harm silicon solar cell performance significantly [7].

The achievement of high quality pc-Si material at low temperatures is attributed to the high mobility of Si atoms and crystallites provided by the presence of the molten metal medium. The high mobility of Si atoms results in a low nucleation density, thus large grain size as well as low level of defect formation.

5. Conclusion

The potential of solution growth for producing high quality Si materials has been demonstrated by the improved electronic properties of LPE layers grown on mc-Si substrates and the large grain continuous pc-Si grown on glass at low temperatures. The gettering of the impurities is due to the fact that the segregation coefficient of most element is smaller than one. The low defect level in solution grown materials results from the equilibrium growth condition as well as the high mobility of Si atoms in a molten metal medium.

6. Acknowledgement

The author acknowledges the provision of facilities by the Centre for Potovoltaic Devices and Systems at the University of New South Wales where some of this work was conducted.

7. Reference

1) A. Takami, S. Arimoto, H. Naomoto, S. Hamamoto, T. Ishihara, H. Kumabe and T. Murotani; Proc. of the first world Conference on Photovoltaic Energy Conversion, Hawaii 1994, p.1394
2) T.Baba, M. Shima, T. Matsuyama, S. Tsuge, K. Wakisaka and S. Tsuda; Proc. of 13th European Photovoltaic Solar Energy Conference October 1995, Nice France, p.1708
3) Z. Shi, T.L. Young and M.A. Green; Proc. of the first world Conference on Photovoltaic Energy Conversion, Hawaii 1994, p.1579
4) Blackers, K.J. Weber, M.F. Stuckings, S. Armand, G. Matlakowski, M.J. Stoks and A. Cuevas; Proc. of 13th European Photovoltaic Solar Energy Conference October 1995, Nice France, p.33
5) Steiner, G. Wagner, A. Voigt, W. Dorsch and H.P. Strunk; Polyse '95, September 1995, Gargnarno, Italy
6) Trust, Jr. and H.F. John; J.Phys. Chem. Solids Vol. 25 (1964), p.1407
7) Schwuttke, K.Yang and T.F. Cizek; J.Cryst. Growth 43 (1978), p.329

Hydrogen Passivation in Silicon Solar Cells

Stefan Estreicher
Texas Tech University, Lubbock, TX
and
Bhushan Sopori
National Renewable Energy Laboratory
1617 Cole Boulevard, Golden, CO

Hydrogen passivation is being extensively used in multicrystalline silicon solar cells to improve the minority carrier diffusion length, and hence the cell performance. In theory, hydrogen easily diffuses through the bulk and passivates dangling and weak Si bonds at vacancies, vacancy aggregates, grain boundaries, dislocations, and other defects. In practice, things are much more complicated. These complications occur both in the diffusion of hydrogen as well as how it passsivates defects and impurities. For example, the diffusion of H through the material varies considerably in samples from different vendors, some dislocations are efficiently passivated while others remain strong traps for charge carriers despite hydrogenation.

In this talk, we will summarize the issues and discuss the results of recent theoretical and experimental studies. Theoretical work on vacancy-vacancy interactions shows that some vacancy aggregates are much more stable than others are have no deep levels in the gap. It is likely, however, that they are gettering centers for a variety of impurities. In O-rich material, there is now abundant evidence (both theoretical and experimental) that hydrogen is not only strongly attracted to the interstitial oxygen, but greatly enhances its diffusivity. This suggests that hydrogenation of CZ-type material would enhance the precipitation of O. If this precipitation occurs at dislocations, it may transform "good" dislocations into "bad" ones (the ones that cannot be passivated or annealed out).

On the experimental side, evidence of more macroscopic nature is being collected. The differences in H diffusivity in samples from different vendors have been measured. It is found that H diffusivity is lower in O-rich material and higher in C-rich material. Furthermore, in the case of silicon ribbons, an increased growth rate also increases H diffusivity. These results are consistent with variations in the degree of improvement in solar cells from different vendors. The mechanism(s) responsible for these characteristics remain to be resolved. The observed improvement in the cell performance following a forming gas treatment raises questions as to the mechanisms responsible for H diffusion from a molecular ambient. Likewise, mechanisms associated with passivation during nitridation need futher attention. A model for diffusion mechansims is begining to emerge that might suggest involvement of a vacancy-enhanced diffusion of hydrogen and surface damage assisted dissociation of molecular hydrogen.

One of the practical concerns is how passivation can improve the spatial uniformity of the cell response. It is interesting that passivation is not uniform within the material or cell. In fact, passivation appears to be weakest in the regions of already low response which are known to contain dislocation clusters. This suggests two possible reasons — (i) dislocation clusters are decorated with impurity precipitates (a mechanism that also prevents effective gettering in these regions) which cannot be passivated by H , and (ii) hydrogen segregates at dislocation nodes making it difficult to diffuse into the bulk of the material. While our understanding of the various processes taking palce is still incomplete, more and more pieces of the puzzle are being identified and put into place.

Defect passivation by means of PECVD-nitride and hydrogenation for crystalline Si solar cells

Authors : J. Poortmans, J. Szlufcik, F. Duerinckx, K. Declercq, J. Horzel, T. Vermeulen, O. Evrard, J. Nijs and R. Mertens

Abstract

This paper is subdivided in 2 main sections. In the first part a broad review will be given on the application of SiN_x-layers in the production of low-cost crystalline Si solar cells and its main aspects. Recent results will be given with emphasis on new cell concepts which become possible by the use of PECVD-nitride. Attention will also be devoted to new techniques like remote-plasma deposition of SiN_x which allow record low surface recombination velocities. In the second part, attention will be focused on remote plasma hydrogenation of thin-film cells. The base layer of the thin-film cells was epitaxially grown on highly doped p-type defected Si substrates (ribbons and SILSO-substrates). A hydrogenation treatment leads in the thin-film cells to considerable improvement of the cell characteristics. Specificly for thin-film cells, boron desactivation by hydrogen has been found to influence considerably the effect of remote plasma hydrogenation. These effects have to be taken into account when optimizing the treatment.

1. PECVD-nitride for low cost crystalline Si solar cells

PECVD-silicon nitride (SiN_x will be used as the abbreviation throughout the whole text, although, to be fully correct, one should write SiN_xH_y) is usually deposited at temperatures between 250 and 400°C and can contain a high concentration of hydrogen, in some cases up to 40%. Advantages of PECVD-SiN, compared to LPCVD-SiN, are the higher deposition rate and the possibility to tune the refractive index over a wider range. This can be done by changing the power of the glow discharge or the relative flow rates of ammonia and silane. The use of PECVD-nitride in Si solar cells is driven by three effects : the PECVD-nitride acts as a anti-reflective coating [1] but also is a source of hydrogen which leads to improved surface [2] and even bulk passivation [1, 3, 4, 5]. We will deal with this apects in some detail in the following sections. After the short discussion on these properties we will review some relevant efficiency results, reported on the last 3 years.

1.a PECVD-nitride as an antireflective coating

The refractive index of SiN_x can be varied by means of of the SiH_4/NH_3-ratio in a broad range between 1.8 and 2.3. The higher the Si/N-ratio, the higher n. For single layer ARC's, a refractive index of 2 is preferred. When used in a double-layer ARC-configuration (thin $SiO_2/SiN_x/SiO_2$) the refractive index is preferably around 2.3. In the latter case, however, absorption in the high-energy part of the spectrum sets in [6]. This defines a trade-off between minimization of reflection and reduction of energy losses by absorption in the passivation layer. Detailed optical measurements revealed that the refractive index of SiN only changes slightly (2%) after firing in contrast to the one of TiO_x which changes substantially (20%) after firing at the same temperature. This is

accompanied by a drastic change of the thickness (40%) for the latter. The SiN_x absorbs at short wavelengths, but this loss is reduced after firing.

The anti-reflective properties are however not the main driving force for their application in solar cells, because TiO_x would be an equal optical equivalent without the need of expensive vacuum systems.

1.b. PECVD-nitride as a surface passivation layer

The main reason for the strong interest in SiN_x stems from the fact that there is overwhelmingly strong evidence for the good surface passivation properties of the SiN_x-layer [1, 7, 8, 9]. The best passivation effect is most often reached when the SiN_x-layer is combined with a thin layer of SiO_2 (thermally grown [8] or plasma-deposited [1]) at the surface of the cell. This statement is valid for a broad range of Si-substrates [7], going from monocrystalline Fz-Si substrates to electromagnetically casted material.

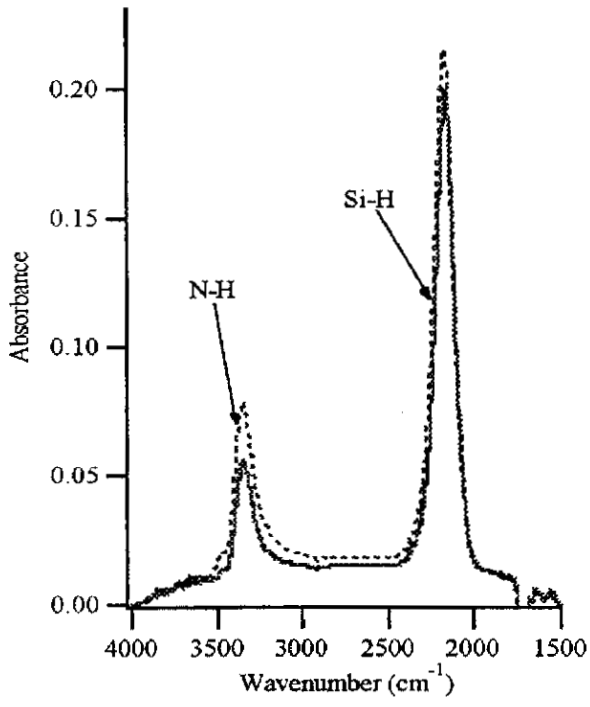


Figure 1 : Absorbency spectra of a 110 nm thick SiN_x-layer as-deposited : 380°C, 50 KHz (dashed line) and fired at 800°C (solid line). Taken from ref. 12

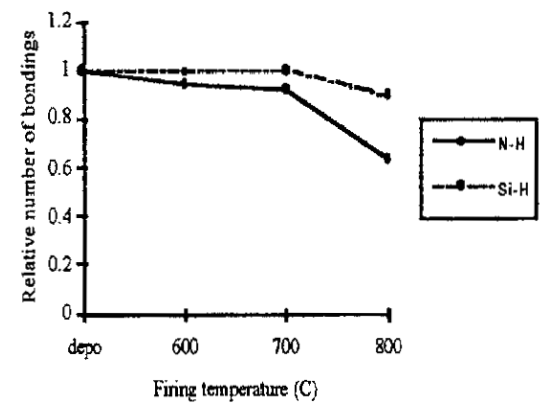


Figure 2 : Relative decrease of Si-H and N-H bondings as a function of firing temperature (taken from ref. 12)

On all these materials the use of SiN_x-layers for surface passivation of the solar cell allows values of the internal quantum efficiency of over 80% at 400 nm [7, 8]. This corresponds to a typocal surface recombination velocity of less than 5000 cm/s. It must be noted however that the low surface recombination velocity is mostly obtained after an additional treatment (photoassisted anneal in forming gas [1], sintering in forming gas [8], the firing treatment after screenprinting the metal contacts [3], hydrogen radical annealing [11]).

Firing of the metal contacts can lead to substantial changes in the Si-H and N-H bond configuration

in the layer. This was witnessed in [12] by means of FTIR-measurements (see fig. 1). The lowest surface recombination velocity was found after a treatment at 650°C [3] which corresponds with the temperature range where the number of Si-H-bonds starts to decrease (see fig. 2)

The exact cause of the surface passivation effect is still a matter of discussion [9]. Whether the surface passivation effect is to be attributed to the H-atoms, passivating the dangling bonds at the surface, or to the formation of positively charged defects during growth or the post-growth treatment remains largely an open question. Recently it was reported [10] that the surface passivation effect of SiN_x-layers shows a similar behaviour as thermal oxides with S being smallest on (100)-material and largest on (111) material. This was only observed for p-type wafers. In addition it was found that the passivation effect was also a strong function of the HF-treatment before the deposition. The best results were obtained with a diluted HF-dip (in accordance with analogue results for thermal oxide).

1.c PECVD-nitride as a source of hydrogen for bulk passivation

The use of PECVD-nitride becomes even more attractive when looked at in conjunction with its use as a source ofhydrogen for bulk passivation. This is especially important for the passivation of grain boundaries and intra-grain defects in multicrystalline Si-materials (although also on Cz-Si improvements are witnessed in the characteristics after hydrogenation [13]). There is ample evidence for the beneficial effect of hydrogen on multicrystalline materials. The hydrogen can be brought in the bulk by various methods (rf-plasma [14], remote plasma [15, 16]). Hydrogenation requires however an extra step and the use of a hydrogen plasma is often not compatible with screenprinted contacts when it is applied after the contact formation because of a degradation of the fill factor.

However, the use of SiN_x in the process leads to comparable improvements in the bulk properties as hydrogenation and therefore avoids the need for a separate hydrogenation step. SiN_x can serve as a reservoir for the hydrogen needed for the bulk passivation. Hydrogen can diffuse in the substrate during the deposition, but as in the case of the surface passivation, one gets the maximum benefit when combined with an additional post-treatment. When contacts are screenprinted on a structure where the SiN_x-layer is already deposited, the firing can serve as a post-deposition anneal. EBIC-images gave ample evidence of a bulk passivation effect after this firing step [3]. The increase in bulk lifetime has been specifically studied in [1], where it was found that this increase can be as high as factor of 2. The improvement of the bulk lifetime by SiN_x-deposition (+ post-deposition treatment) is however material specific [1, 17]. The oxygen content of the Si-substrate has a strong influence on the indiffusion of hydrogen ; low-oxygen content material is more susceptible to efficient hydrogenation [18].

1.d Effect of SiN_x-layers on the efficiency of low cost Si solar cells made with screenprinting

In Table 1 (taken from ref. 3) a comparison is made between several firing and deposition sequences. The process was executed on 100 cm^2 Wacker multicrystalline substrates (1 ohm-cm, thickness of 350 micron). All the cells in this study had homogeneous emitters with a sheet resistance of about 45 ohm/square. The benefit compared to the non-passivated cells and the cells

with TiO_x is obvious.

Sequence	Jsc [mA/cm^2]	Voc [mV]	FF [%]	Efficiency [%]
ref. (no ARC)	22.5	570	76.3	9.8
Metal. + TiO_x	28.4	580	76.2	12.5
Metal. + SiN_x	29.3	591	71	12.3
SiN_x + Metal.	30.0	601	76.1	13.7

Table 1 : Effect of PECVD-nitride on solar cell output characteristics

A basic process flow for a simple homogeneous emitter process is shown in fig. 3a. In fig. 3b the cross-section of this cell-type is shown.

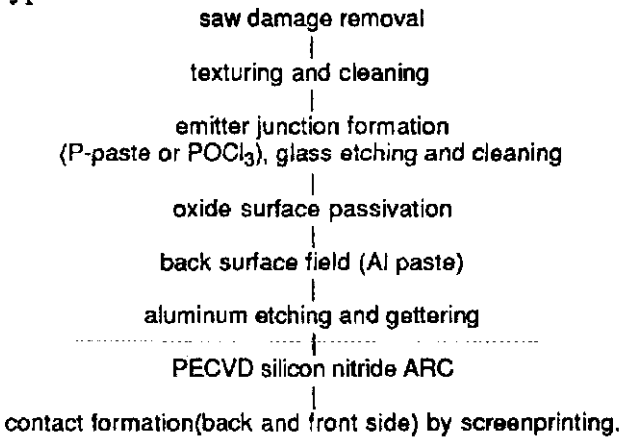


Figure 3a : Flow chart of a screenprinting pilot-line solar cell process for cells with homogeneous emitter.

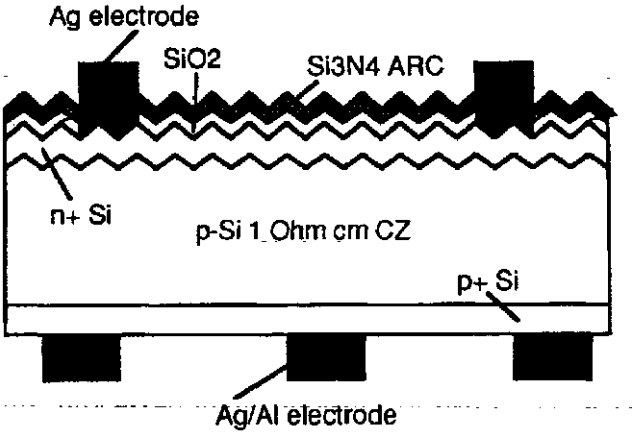


Fig. 3b Schematic cross-section of a homogeneous emitter cell

These processes were optimized for mono- and multicrystalline large-area cells. In table 2 there is a summary of best cell results, processed in the pilot-line of IMEC. These cells have a screenprinted emitter and contacts.

Material	J_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	Efficiency [%]
mono-Cz	34.1	617	79	16.6
multicrystalline, mechanically textured (i.c. Un. Konstanz)	34.3	609	76.4	16

Table 2: Parameters of screenprinted solar cell with homogeneous emitter, as measured at FhG-ISE in Freiburg. The cell area is 96 cm^2 for mono-Si and 100 cm^2 for multi-Si. Mechanical texturing was done by the university of Konstanz, Germany [20] (Taken from ref. 19)

n view of the excellent surface passivation properties (see above), the use of SiN_x-layers in solar cells with selective emitters is a logical extension (for a schematic cross-section see fig. 4). Much efforts are being spent over the world to make a selective emitter structure by means of a low-cost technique like screenprinting [21]. In [19] first results are reported for monocrystalline large-area cells with selective emitter, the whole being realized by screenprinting techniques. The surface of the emitter between the fingers was passivated by SiN_x. The efficiency reached a value larger than 17%, clearly confirming the good surface passivation properties of the layer even when used within the frame of a screenprinting process. In [21] an encapsulated cell efficiency of 15.7% is reported for a screenprinted multicrystalline cell with selective emitter and SiN_x-passivation. These values are certainly not to be considered as the end of the development.

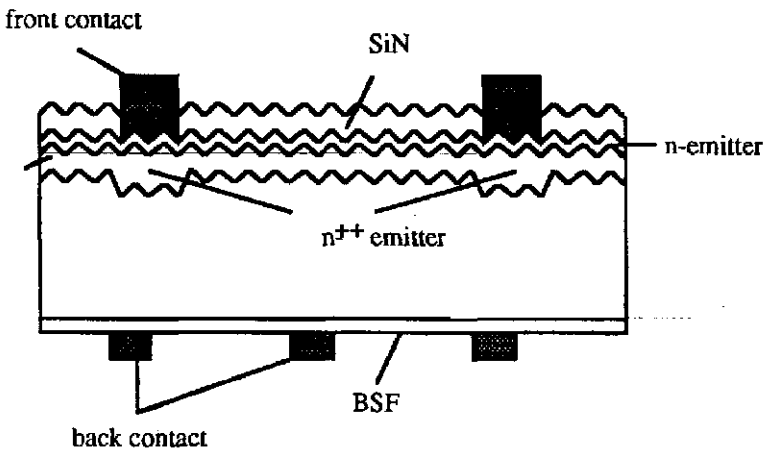


Fig. 4 Schematic cross-section of a selective emitter cell

1.e New developments

As stated above, SiN_x-layers are especially attractive because of their passivation properties. Recently, there was a report [22] about SiN_x-layers grown in a remote plasma environment. On Fz-Si wafers coated with these layers, extremely low surface recombination velocities were extracted. A value as low as 15 cm/s was found for layers deposited at 350°C, a value of 7 lower than obtained on layers, grown in a direct-plasma environment (see fig.5). Record efficiencies of 19.4% on bifacial 4 cm^2 cells give further evidence of the excellent surface passivation properties of the layer. The question remains however to which extent this technique is upscalable towards larger batches.

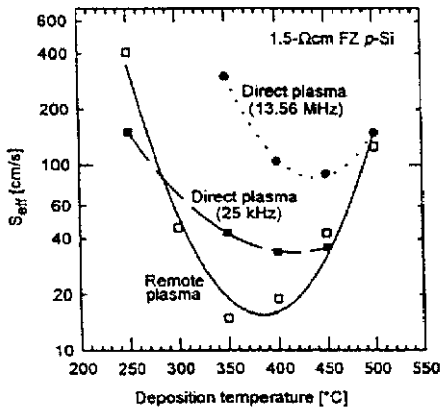


Fig. 5 Surface recombination velocity of remote plasma SiN_x as a function of injection level [22]

2. Hydrogenation and thin-film crystalline Si solar cells

It was mentioned in section 1.c that hydrogenation is often most efficient on a low oxygen-content material. This is the link to the second part of this paper which deals with hydrogenation issues of thin-film crystalline Si solar cells. The layers for the thin-film cells were epitaxially grown on a defected highly doped substrate (which acts as a Back surface field) at a high temperature. Due to the temperature and the highly reducing character of the CVD-environment (SiH_2Cl_2 and H_2) the layers contain only a low amount of oxygen. This makes them more susceptible for improvement by hydrogenation.

Thin-film crystalline Si solar cells carry a large potential for further cost reduction in Si-based photovoltaics. When this layer is grown on a highly doped ribbon the cost reduction is twofold : the use of high quality material is restricted to a minimum and the wafering cost is avoided. Although the long-term objective for the research on thin-film crystalline cells is to go finally to Si-layers on cost-effective non-Si substrates (e.g. ceramics), the use of these highly doped ribbons represents an interesting intermediate step before further development. The basic scheme for the solar cells discussed in the subsequent part of this paper is represented in fig. 6.

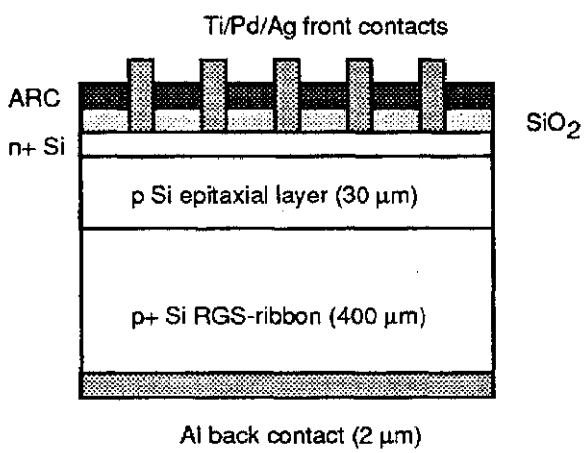


Fig. 6 : Schematic view on the thin film structure .

2. a Solar cell process in epitaxial films on highly doped defective Si substrates

Epitaxial silicon layers were grown on highly doped p-type substrates (ribbons or SILSO-substrates) using dichlorosilane and diborane at temperatures between 1050 and 1130°C. The emitter was formed in the epitaxial layer by means of a 30 minutes P_2O_5 solid source diffusion at 900°C. The emitter was etched back to 80 Ω/square. Next, a thin thermal oxide or PECVD-oxide was grown during 6 minutes at 900°C for, surface passivation. An Al back contact was deposited and sintered in forming gas during 30 minutes at 450°C. Further on, Ti/Pd/Ag front contacts were evaporated after lithographical patterning and lift-off. Finally, 2x2 cm^2 cells were diced from the ribbons and a double layer ARC (110 nm ZnS, 56 nm MgF_2) was deposited. Fig.6 shows the resulting elementary thin film structure. More details can be found in [23, 24].
Although this process is certainly not be considered as a low-cost process, it allows us to study the effects of hydrogenation in depth.

2.b Passivation by microwave induced remote plasma hydrogenation.

A microwave induced remote plasma hydrogenation (MIRP-) system was used as a hydrogen source. Fig. 7 shows a schematic view of the set-up. Details of the system can be found in [25],.

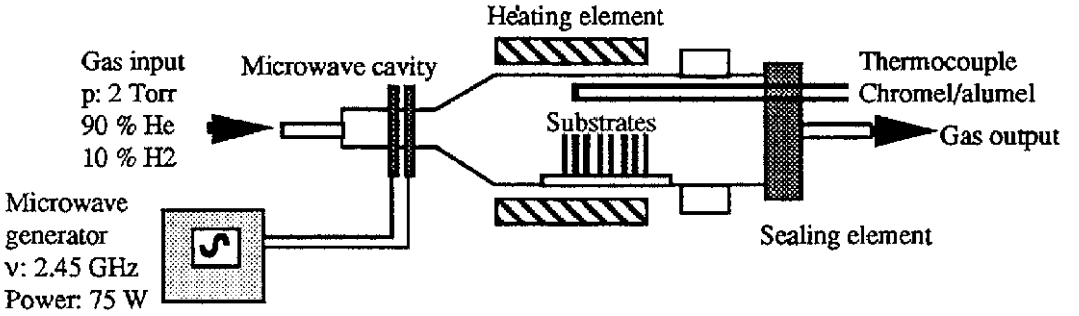


Fig. 7 Schematic representation of the remote plasma hydrogenation system

In this system, atomic hydrogen is present in the afterglow of a H_2-plasma. Several hydrogenation times and temperatures were tested at a total pressure of 2 Torr. The incoming gas flow had a velocity of 0.5 m/s and contained 10% H_2 and 90% He. In the coming sections we will discuss the dependence of the hydrogenation efficiency on temperature, time and surface passivation.

2.c Relation between hydrogenation efficiency, hydrgenation time and temperature

In this part of the study no oxide was present during the hydrogenation treatment. Any interference of an oxide with the hydrogenation mechanism is then also excluded. This is the subject of section 2.d. Thin Si-solar cells in a 0.2 Ωcm, 27±2 μm thick epitaxial layer on SILSO mc-Si substrates were processed. The uncertainty on the thickness stems from the growth rate dependence on grain orientation. MIRP-hydrogenations were performed during 0.5, 1, and 2 hours at temperatures of 350, 375 and 400°C. The resulting averaged AM1.5 illuminated IV-parameters are shown in table 4. All thin-film Si-cells have a PECVD-SiN_x-layer on top, deposited directly after the PECVD-oxidation in the same reactor. The PECVD-oxide and nitride were deposited after the hydrogenation.

Hydrog. conditions	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Eff. (%)
350°C, 0.5 h	21.2	491	71.0	7.4
350°C, 1 h	24.1	523	72.8	9.2
350°C, 2 h	24.2	520	74.6	9.4
375°C, 0.5 h	20.3	484	73.0	7.2
375°C, 1 h	20.8	494	72.8	7.5
375°C, 2 h	20.5	485	71.8	7.1
400°C, 0.5 h	20.7	484	71.4	6.7
400°C, 1 h	25.6	567	75.7	11.0
400°C, 2 h	22.0	502	73.1	8.1

Table 3 : Average AM1.5 illuminated IV-parameters of thin-film Si-cells on SILSO mc-Si for different hydrogenation temperatures and times [26].

Table 3 illustrates that the optimal hydrogenation time at all temperatures for this type of substrate is about 1h. Especially in the case of 400°C this optimum hydrogenation is quite critical. Further Refinement of the timescale (MIRP-hydrogenations were performed during 0.75 and 1.25 hours) confirmed this optimal hydrogenation time of 1 hour. Another striking feature is the relatively bad performance of cells hydrogenated at 375°C, compared to their equivalents at 350 and 400°C. An efficiency of 11.0% is reached when a hydrogen treatment was implemented at 400°C for 1h.

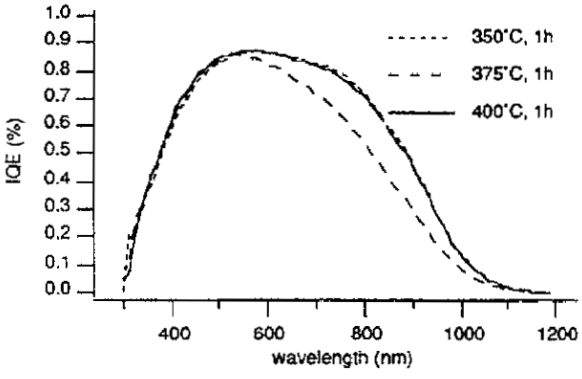


Fig.8 : IQE-curves of TF-cells on SILSO mc-Si hydrogenated at different temperatures [26].

The IQE-analysis reveals (see fig. 8) the underlying details of the observed behaviour. The better performance at 400°C is caused by the somewhat better blue response, whereas the red response is slightly lower. The red response at 375°C is clearly lower than for 350 and 400°C. The diffusion length which was extracted from the IQE-curves is in the best case about 20 micron. This is about the double of the diffusion length for the non-hydrogenated cell.

The question arises to the reason of the observed degradation of the cell for longer hydrogenation times. The answer to that question is partially revealed in fig. 9, which shows the active carrier profiles in the base layer of the thin-film cell.

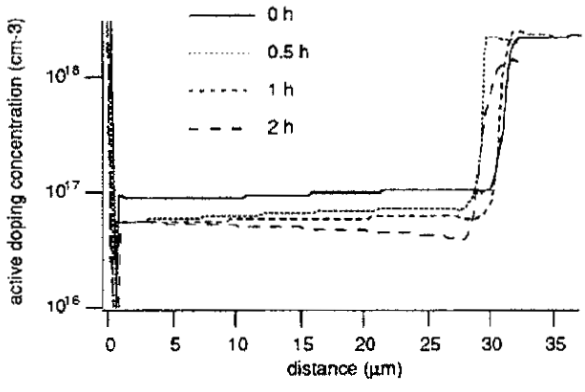


Fig.9 : SRP-profiles of the epitaxial layers of hydrogenated thin--film Si-solar cells on SILSO mc-Si substrates [26].

It is seen that the active carrier concentration in the base is reduced after hydrogenation. The fact that B is desactivated by hydrogen is not surprising on itself. The desactivation of boron by hydrogen has been suggested to result from the Coulomb-interaction between negatively charged B-ions and positively charged H-atoms [26], according to the reaction :

$$B^- + H^+ \rightarrow (BH)^0$$

The most surprising is however the evolution of the profile. After 30 minutes, more boron is passivated closer to the surface, while after 1 hour the boron profile is flat and shifted to 60% of its original value. After 2 hours the boron dopant level is lower at the interface between the epitaxial layer and substrate, introducing an electric field that hinders the transport of minority carriers (electrons) towards the junction. A first order calculation showed that the electric field, which has a magnitude of about 4 V/cm, gives rise to a drift current (under AM1.5 the excess electron concentration will be around 10^{13} cm^{-3} in the base when the lifetime is 0.5 microseconds) in the order of 2 mA/cm^2. This agrees well with the observed decrease in short circuit current of the cells

Obviously, the active carrier profile after an extended MIRP-hydrogenation cannot result from a simple diffusion mechanism of hydrogen into the epitaxial layer. The evolution of the carrier profile shows however a striking resemblance with observations about the hydrogen profile in an epitaxial layer. SIMS-measurements of deuterium-profiles in epitaxial layers give evidence of the interface between epitaxial layer and substrate being a "sink" for hydrogen. This is shown in fig. 10, where a comparison is made of the deuterium-profile in a Eurosolare multicrystalline wafer and an epitaxial layer grown on a Eurosolare wafer from the same location in the ingot.

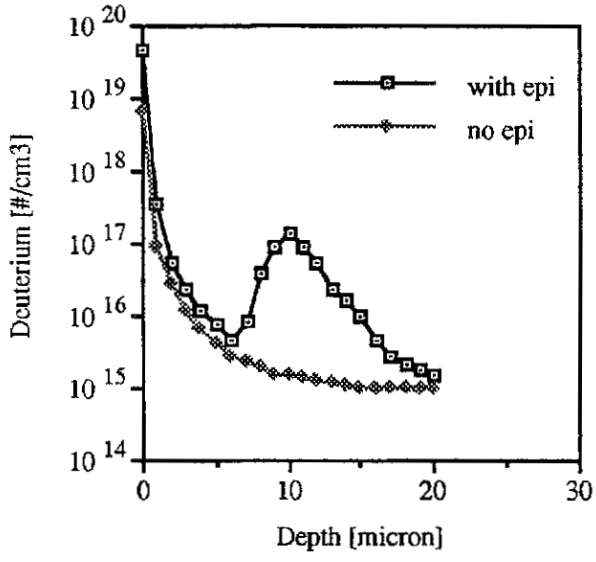


Fig. 10 SIMS-profile of Deuterium after H-plasma (4h, 350°C) in a Eurosolare substrate and in an epitaxial layer, grown on this type of substrate [18]

The most striking feature in fig. 10, besides the higher total amount of hydrogen in the epitaxial layer is the pile-up of hydrogen at the interface between epitaxial layer and substrate. From fig. 9 it is obvious that this pile-up of H in that region might be related desactivation of boron in that region, leading to the observed degradation. Experiments to check whether this "sink" effect at the interface is due to specific defects at the interface are actually ongoing. By means of growing a p^+ epitaxial layer between base and substrate, it is hoped to get more insight in this behaviour. In this way the p^+-p-trannsition is moved away from the substrate-epi interface.

2.d Relation between hydrogenation, surface passivation and type of substrate

An important issue is the optimal hydrogenation condition in relation to the surface passivation method. More specificly, the question is to which extent a thin oxide layer influences the kinetics and efficiency of the hydrogenation. For this purpose a comparison was made between a thermal oxide grown before the hydrogenation and a PECVD-oxide deposited after the hydrogenation (growing a thermal oxide after hydrogenation has obviously no sense).

Two types of highly doped carrier substrates, on which the epitaxial layer is grown, were compared : p^+ribbons and p^+-SILSO-substrates. The effect of the hydrogenation time is shown in fig. 11 (thin-film cells on p^+-SILSO-substrates) and 12 (thin-film cells on p^+-ribbons). In fig. 11 one finds again an optimal hydrogenation time of 1h, irrespective of the presence of an oxide. For hydrogenation times longer than the optimal time a decrease sets in, as discussed in the previous section. For the thin-film cells on the ribbon, we do not observe the degradation for longer hydrogenation times and the hydrogenation of the cell with thermal oxide proceeds obviously much slower. This can be analyzed in depth when looking to the internal quantum efficiency (IQE-) curves in fig.13. Before MIRP-hydrogenation, the red responses of the thin-film Si-cells with thermal and PECVD-oxide coincide. After hydrogenation, the red response of the thin-film Si-cells with PECVD-oxide increases faster and is clearly higher. Whereas the diffusion length in the base

of the PECVD-oxide cells is increased by 80%, compared to the non-hydrogenated case, the diffusion length in case of the thermal oxide is only enhanced by 25 to 30% after the whole cycle. The best values of diffusion length were around 20 micron, as in section 2.c. It is also seen that there is no degradation in the blue part of the spectrum for the thermal oxide after the hydrogenation.

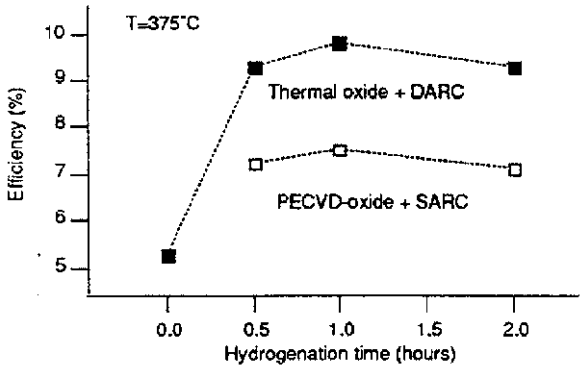


Fig.11 :: Interaction between surface passivation and MIRP-hydrogenation time for thin-film Si solar cells on SILSO mc-Si.

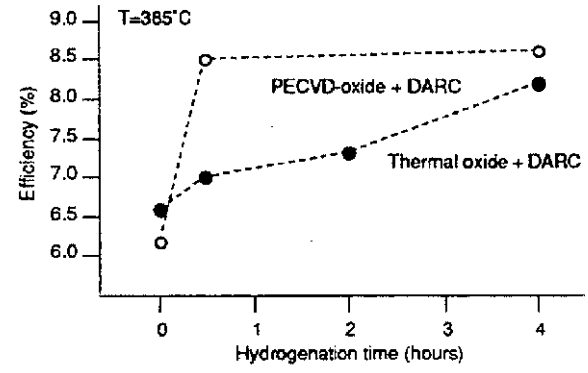


Fig 12. : Interaction between surface passivation and MIRP-hydrogenation time for TFSi-cells on ribbons

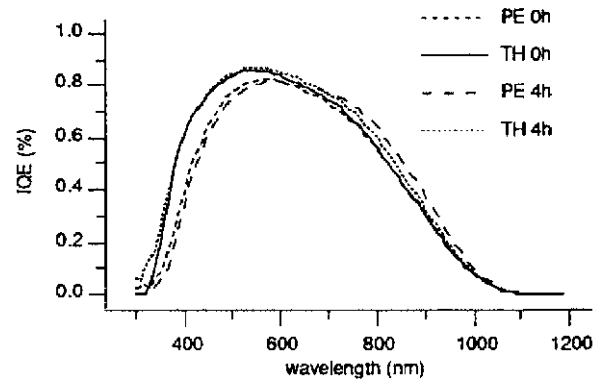


Fig.13 : Internal quantum efficiency curves of thin-film Si-cells on ribbon substrates (PE=PECVD, TH=thermal oxide)

From the evolution it is clear the in-diffusion of hydrogen is clearly hindered by the presence of the thermal oxide and the bulk passivation of the epitaxial layer is delayed.The reason for the absence of the degradation effect for longer hydrogenation times in the thin-film cells on ribbon with PECVD-oxide is less clear. A possible explanation is the higher defect density in the thin-film cells on ribbon compared to the thin-film cells on SILSO ($> 10^7$ cm^{-2} compared to 10^6 cm^{-2}). The longest hydrogenation times used in this experiment might not be sufficient to passivate all the defects in the layer which prevents excess hydrogen (= hydrogen concentration not needed for defect passivation) from accumulating at the substrate-epi interface. This explanation needs further validation however.

3. Conclusions

A broad overview is given about the growing importance of PECVD-nitride in low-cost processes based on screenprinting. All the aspects (optical properties, bulk and surface passivation properties) have been looked at in conjunction with this type of process, with special attention to the effects occurring in the SiN_x-layer during the contact firing. It is clearly seen that optimized nitride-layers will play an increasingly important role in many advanced cell types (selective emitters, MIS solar cells).

In relation with bulk passivation by hydrogenation, we have also discussed in detail the results of a hydrogenation optimization study. This study revealed the existence of an optimal hydrogenation time for a material with reasonably low defect level. The degradation for periods longer than the optimal hydrogenation time can be explained by boron desactivation, leading in the end to an unfavourable drift field in the base. In materials with a higher defect density (e.g. ribbons) this optimal time is extended. No degradation was found for even the longest hydrogenation time of 4 hours. In the latter case, the presence of a thermal oxide also slows down considerably the hydrogenation process.

Acknowledgements

The authors would like to acknowledge the JOULE II project SICRYT (contract number JOU2-CT93-0398) and MULTICHESS (contract number JOU2-CT92-0179) which made possible this study.

References

1. Z. Shen, A. Rohatgi, R. O. Bell and J. P. Kalejs, Appl. Phys. Lett. 65 (16), 2078 (1994)
2. T. Lauinger, J. Schmidt, A. G. Aberle, Proceedings of the 13th European Photovoltaic Solar Energy Conference, Nice, 1291 (1995)
3. J. Szlufcik, K. De Clercq, P. De Schepper, J. Poortmans, A. Buczkowski, J. Nijs and R. Mertens, Proceedings of the 12th European Photovoltaic Solar Energy Conference, Amsterdam, 1018 (1994)
4. D. S. Ruby, W. L. Wilbanks, C. B. Fleddermann, J. I. Hanoka, Proceedings of the 13th European Photovoltaic Solar Energy Conference, Nice, 1415 (1995)
5. C. Schetter, H. Lautenschlager and F. Lutz, Proceedings of the 13th European Photovoltaic Solar Energy Conference, Nice, 407 (1995)
6. Multichess II final report, Topic 8 (1996)
7. K. Shirasawa, H. Takahashi, Y. Inomata, K. Fukui, K. Okada, M. Takayama and H. Watanabe, Proceedings of the 12th European Photovoltaic Solar Energy Conference, Amsterdam, 757 (1994)
8. S. Sivoththaman, J. Poortmans, J. Nijs and R. Mertens, Proceedings of the 13th European Photovoltaic Solar Energy Conference, Nice, 1428 (1995)
9. C. Leguyt, Ph.D. Thesis, University of Utrecht, (1995)
10. F. M. Schuurmans, A. Schönecker, J. A. Eikelboom and W. C. Sinke, to be published in the Proceedings of 25th IEEE Conference, Washington (1996)

11. H. Nagayoshi, M. Ikeda, T. Saitoh, K. Kamisako, T. Uematsu, Proceedings of the 13th European Photovoltaic Solar Energy Conference, Nice, 1546 (1995)
12. F. Duerinckx, J. Szlufcik, K. De Clercq, P. De Schepper, W. Laureys, J. Nijs and R. Mertens, Proceedings of the 13th European Photovoltaic Solar Energy Conference, Nice, 1493 (1995)
13. J. Poortmans, M. Rosmeulen, J. Vanhellemont, MRS Spring Proceedings Vol. 378, 399 (1995)
14. S. Sivoththaman, M. Rodot, J. C. Muller, B. Hartiti, M. Ghannam, H. E. Elgamel, J. Nijs and D. Sarti, Appl. Phys. Lett. 62 (24), 317 (1993)
15. H. E. Elgamel, M. Caymax, M. Ghannam, J. Poortmans, P. De Schepper, J. Nijs and R. Mertens, Proceedings of the 12th European Photovoltaic Solar Energy Conference, Amsterdam, 724 (1994)
16. M. Spiegel, P. Fath, K. Peter, B. Buck, G. Willeke and E. Bucher, Proceedings of the 13th European Photovoltaic Solar Energy Conference, Nice, 421 (1995)
17. M. Rosmeulen, H. Elgamel, J. Poortmans, M. A. Trauwaert, J. Vanhellemont, J. Nijs and R. Mertens, Proceedings of the First World Conference on Photovoltaic Energy Conversion (WCPEC), Hawaii, December, (1994)
18. H. E. Elgamel, Ph. D. Thesis Katholieke Universiteit Leuven (1994)
19. J. Nijs, E. Demesmaeker, J. Szlufcik, J. Poortmans, L. Frisson, K. De Clercq, M. Ghannam, R. Mertens and R. Van Overstraeten, Proceedings of the 1st World Conference on Photovoltaic Energy Conversion (WCPEC), Hawaii, 1242 (1994)
20. P. Fath, C. Marckmann, E. Bucher and G. Willeke, J. Szlufcik, K. De Clercq, F. Duerinckx, L. Frisson, J. Nijs and R. Mertens, Proceedings of the 13th European Photovoltaic Solar Energy Conference, Nice, 29 (1995)
21. L. A. Verhoef, P. P. Michiels, R. J. C. Van Zolingen, H. H. C. De Moor, A. R. Burgers, R. A. Steeman, W. C. Sinke, Proceedings of the 1st World Conference on Photovoltaic Energy Conversion (WCPEC), 1547, Hawaii, (1994)
22. A. G. Aberle and R.Hezel, to be published in the Proceedings of 25th IEEE Conference, Washington (1996)
23. T. Vermeulen, O. Evrard, W. Laureys, J. Poortmans, M. Caymax, J. Nijs, R.Mertens, Proceedings of the 13th European Photovoltaic Solar Energy Conference, Nice, 1501 (1995)
24. T. Vermeulen, J. Poortmans, K. Said, O. Evrard, W. Laureys, M. Caymax, J. Nijs, and R. Mertens, to be published in the Proceedings of 25th IEEE Conference, Washington (1996)
25. C. Vinckier and S. De Jaegere, Reactivity of Solids, 7, 61-65 (1989).
26. S.J. Pearton, J.W. Corbett, T.S. Shi, Appl. Phys. A 43, p. 153-195 (1987).

Charge State Control of Hydrogenation in Silicon

by C. H. Seager and R. A. Anderson

Sandia National Laboratories, Albuquerque, N.M.

ABSTRACT

We demonstrate that periodic exposure to zero bias during in-situ hydrogenation of reverse-biassed p-type Schottky barrier structures has dramatic effects on H penetration. H influx can be slowed or even stopped by such protocols. By contrast, similar pulsing techniques produce almost no changes of penetration in n-type barriers during hydrogenation; this latter observation is in sharp contrast to the expectations that charge conversion from H^+ to H^- would reverse the drift of H species. We suggest that these effects are caused by the charge conversion of relatively immobile H-related defects. In the p-type barriers this results in a weakening or reversal of the near surface electric field, effectively stopping the drift of H^+ into the bulk.

New trends in defects passivation

S. Pizzini, M. Acciarri, S. Binetti, D. Narducci, C. Savigni
Istituto Nazionale di Fisica della Materia
Department of Physical Chemistry and Electrochemistry
Via Golgi, 19 20133 Milano Italy
Tel/Fax. ++39 2 26603 204 e-mail matlab@imicilea.cilea.it

1 Introduction

External and internal gettering and hydrogen passivation (generally carried out in radiofrequency (RF) or microwave-driven plasma) are well established techniques in microelectronic and photovoltaic (PV) devices processing, respectively. The main difference between the two techniques is that in the case of passivation, hydrogen interacts chemically with the species responsible of the lifetime degradation, shifting the corresponding energy level out of the gap [1]. Gettering, instead, is based on the interaction of impurity (metallic) species with suitable sinks, thus inducing a chemical potential field inside the material which drifts the impurities towards the sinks, possibly up to their exhaustion [2]. Once gettered, the impurities might remain electrically active or deactivated, as in the former case.

Gettering and passivation are therefore very complementary techniques, their aim being in the first case that of maintaining the metal impurities at an acceptable level in the active area of the device, even in the case of unwanted contamination, and of reducing the density of recombination centres associated to point or extended defects in the second case.

While in microelectronics external and internal gettering is a customary practice, considering that only the front surface of the wafer must be depleted from impurities, in the case of PV cells both passivation and external gettering are of great value, because the entire volume of the device is electrically active. A further problem arising in polycrystalline cells is the internal self-gettering of metallic and non metallic impurities at grain boundaries (GB) and dislocations . Therefore, in the case of PV materials external gettering must provide more efficient metallic impurity sinks than those provided by GB and dislocations.

In spite of the major importance of defect gettering engineering in microelectronics, hydrogen incorporation is well recognized to be an unavoidable by-process in wet wafer cleaning and device etching procedures, performed by dipping silicon in diluted HF (DHF), although DHF dipping can be used to obtain a semi-permanent passivation of a silicon surface by reaction of hydrogen with dangling bonds. For this reason, it can not excluded that hydrogen passivation might play a different role also in microelectronics.

Aim of this paper is to show that in addition to conventional plasma hydrogenation and internal gettering, some new techniques can be used to minimize both the effect of bulk deep levels and surface states in microelectronic and in PV devices. These techniques are based on the use of molecular hydrogen, oxygen and transition metals (TM) and are shown to be of possible, widespread use for defect (point and extended, including surfaces) passivation purposes.

2 Passivation and passivation methodologies

As passivation has a strong influence on the surface recombination rate of minority carriers v_s, the determination of v_s is a measure of the passivation achieved after a certain chemical process. In alternative to the determination of the recombination rate, attenuated total reflectance (ATR) measurements could be however performed, to monitor both the details of surface chemistry associated to passivation and the passivation kinetics [3]. This Section will be therefore devoted to the illustration of the passivation techniques and of passivation measurement techniques.

2.1 Hydrogen passivation

Hydrogen passivation can be conducted both using an RF Plasma system and by catalytically dissociating molecular hydrogen directly onto the semiconductor surface [4]. In both cases the hydrogenation temperature should be kept higher than 250-300 °C , to avoid the formation of B-H complexes which are known to be stable up to 200 °C [5]. For the catalytical dissociation Pt metal was used, which was deposited onto the semiconductor surface by sputtering or by spray-pyrolysis of a suitable metallorganic precursor.

2.2 Passivation of surface states by transition metals

Surface passivation techniques based on the use of transition and noble metals were introduced at a laboratory scale only recently [6] and need an appropriate presentation, also because transition metals are known to passivate the surface states of compound semiconductors, while their effect is practically unknown in the case of silicon surfaces. It is to be reminded, under this respect, that surface states of compound semiconductors are of extrinsic nature and come from the decomposition of the surface oxide of the non metallic species (As in the case of arsenides, P in the case of phosphides) by the metal, with a reaction of the type

$$2Ga_{Ga} + As_2O_3 \rightarrow Ga_2O_3 + 2As_{Ga} \tag{1}$$

and it is supposed that the passivation of the surface is associated to the capability of TM to make stable bonds with the antisites. It has been shown [6],[7],[8], as an example, that Ru^{3+} induces the partial passivation of the GaAs, InP and CdTe surfaces, making the photoluminescence yield twice. In the case of silicon, surface states are instead intrinsic in nature and originate from dangling bonds of unreconstructed or partially reconstructed

surfaces and it was shown with computational methods that TM (Pd) should have only a negligible effect on the surface passivation [9].

2.3 Molecular oxygen passivation

Although this method is really an (external relaxation) gettering procedure [10], it might fall among the passivation techniques as it is based on a mild oxidation of a silicon surface in air at 700 °C for times ranging within 4 and 16 hrs. The strained Si/SiO_2 interface behaves as a sink for metallic impurities and as source of selfinterstitials, which favor metallic impurities diffusion. It was shown [11] that a temperature of 700 °C optimizes the gettering yield and that oxide films grown in an air atmosphere are more efficient impurity sinks than oxide film grown in pure oxygen.

3 Electrical measurements: determination of the diffusion length (L_d) and of the surface recombination rate

While the surface photovoltage technique (SPV) in its standard configuration does allow the quantitative determination of the diffusion length L_d (provided the sample thickness is at least $4L_d$), both the diffusion length and the recombination velocity can be determined by the Light-Beam-Induced-Current (LBIC) [12] technique. In fact, as shown by Marek [13] the LBIC technique in its standard configuration ($p-n$ junction parallel to the surface scanned by the beam) gives the diffusion length in the bulk and the recombination velocity at defects, provided the absorption coefficient, the thickness of the space-charge layer and the beam diameter are known or measured independently.
These limitations could be however overcome using LBIC in lateral configuration, where the sample has the $p-n$ junction perpendicular to the surface scanned, using the Flohr [12] model which assumes (see Fig. 1), that the sample is semi-infinite in the y and z directions while the thickness of the n-zone along the x direction is x_1 and is confined the space charge region and the n^+ zone at $x=0$ and $x=x_1$ respectively.
The expression for the light beam induced current j is given by the following equation:

$$j(x_o,z_o) = j_s(x_o,z_o) + \sum_{n=1}^{+\infty}(-1)^n\left[j_s(2nL_d+x_o,z_o) - j_s(2nL_d-x_o,z_o)\right] \tag{2}$$

where

$$j_s(x,1/\alpha) = \frac{2G_o\alpha}{L_d\pi}\frac{x}{L_d}\Big[\frac{v_s/D}{\alpha(v_s/D-\alpha)}\int_0^\infty e^{-\alpha z}\frac{K_1(\sqrt{x^2+z^2}/L_d)}{\sqrt{x^2+z^2}/L_d}dz - \frac{1}{(v_s/D-\alpha)}\int_0^\infty e^{-\frac{v_s}{D}z}\frac{K_1(\sqrt{x^2+z^2}/L_d)}{\sqrt{x^2+z^2}/L_d}dz\Big] \tag{3}$$

G_o is the generation rate at the surface, α is the absorption coefficient, K_1 is the modified Bessel function of the first kind, v_s is the surface recombination velocity and D is the diffusion coefficient and L_d is the diffusion length.

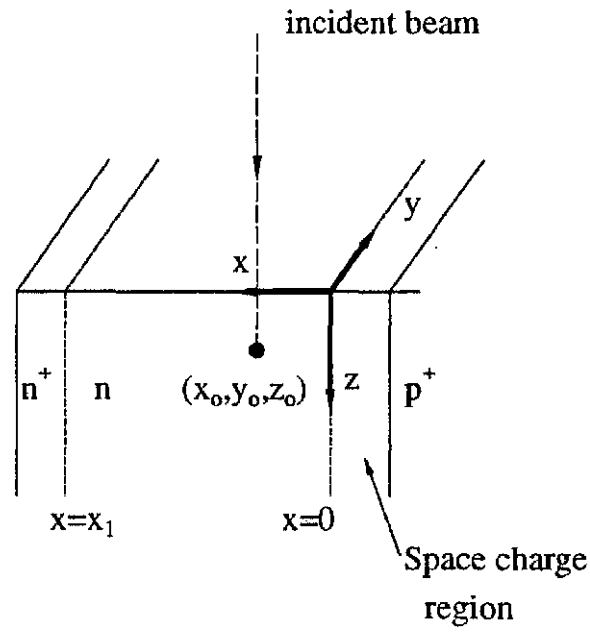


Figure 1: LBIC in the lateral configuration.

If $v_s = 0$ we can simplify eq. 3 as:

$$j_s(x) = G_o e^{-\frac{x}{L_d}} \tag{4}$$

which is absorption coefficient independent. In this case the diffusion length may be directly obtained from the slope of the measured current in a $ln[j_s(x)]$ vs x plot.

4 Experimental details

4.1 Silicon samples selection and /or preparation

Two kinds of polycrystalline samples, used as substrates for solar cells, were considered in details, both exhibiting low or very low diffusion length values in as-grown conditions and thus requiring passivation or gettering to improve the photovoltaic yield.
The former were grown by the Edge Film Growth Technique (EFG) [14] and chosen in view of their ability to show a large increase of diffusion length after plasma hydrogen passivation [15].
The latter, supplied by Eurosolare SpA (Nettuno, Roma), were grown by the directional solidification method [16] and cut from the middle part or edge regions of a 150 Kg multicrystalline silicon ingot. As already shown in a previous paper [17], the diffusion length of minority carriers in the edge region of these Eurosolare (EU) ingots is largely in defect over the bulk average and associated to the presence of precipitates and dislocations, arising from the interaction of the silicon charge with the crucible walls

during the solidification. The diffusion length of wafers cut from the middle part of the ingots is, instead, exclusively dominated by iron impurities.
As a consequence of the different growth techniques used, the morphology, the microstructure and the impurity content of EFG and EU samples are very different.
As reference, we used single crystalline samples, cut from high-oxygen ($[O_i]$= 1.1 $10^{18} cm^{-3}$), boron doped (ρ = 1- 2 Ω cm) CZ-grown 4 " diameter silicon wafers. As obtained by the supplier, the wafers are dislocation free. On these samples dislocation sources are nucleated by scratching the surface of the samples along the $\langle 011 \rangle$ direction with a diamond tip loaded with a 0.3 N weight (other details are reported in [18],[19]).
The dislocation density, determined via etch pit counting and X-ray topography, is shown to vary from $10^6 - 10^8 cm^{-2}$ near the high stressed end of the scratch (maximum resolved shear stress 35 MPa) to $10^4 - 10^5 cm^{-2}$ near the low stressed end (maximum resolved shear stress 4MPa).

4.2 In-depth hydrogen profiles determination

To determine the spatial extent of passivation, deuterium was diffused instead of hydrogen, using as the source a deuterium plasma. The deuterium diffusion profiles were then determined using the SIMS (Secondary Ions Mass Spectrometry) technique[20].

4.3 Microstructural characterization

Microstructural characterization was carried out by TEM (for microprecipitates), XR topography (for dislocations) and SEM (for etch pit counts after Yang etching (1HF:1 (solution 1.5M CrO_3 in H_2O)).

4.4 Measurements of the diffusion length and surface recombination rate

Details about the system developed and tested are given elsewhere [21]. To analyze the data quantitatively, using eq.2-4, a fitting program (FORTRAN language) was elaborated using MINUIT [present in the CERN library] for the minimization and error analysis. The system was shown to work properly using as reference samples silicon- and InP-based diodes. The p^+nn^+ silicon diodes were manufactured by the International Rectifier Corporation Italiana S.p.A. while the $InP(n) - InP(p)$ diodes were obtained by CSELT SpA of Torino.

5 Experimental results

5.1 In-depth deuterium diffusion profiling

A systematic investigation was carried out on several types of polycrystalline and dislocated, single crystalline samples, in order to get information about the deuterium diffusion mechanism. We report here only the in-depth profile of a EFG sample (see figure 2) which has a carbon concentration of 15.6 ppma, an oxygen concentration of 2.2

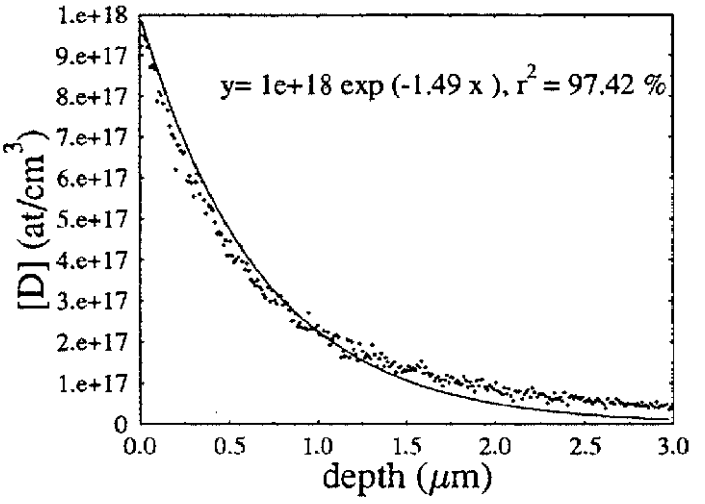


Figure 2: Deuterium diffusion SIMS profiles in an EFG sample. Solid lines: fits with the equations reported on the top of the figures, with r^2 as the correlation coefficients.

ppma and an initial diffusion length of 25 μm and the in-depth profiles of a dislocated sample, in two neighbor regions presenting a different dislocation densities (see fig. 3). As the experimental results could not be fitted by the standard erfc profiles, they were fitted using an equation proposed by Corbett [1], by assuming that the diffusion process occurs by a mechanism of multiple trapping at unsaturable traps

$$[D] = [D_o]exp(-\alpha x) \tag{5}$$

where $[D_o]$ is the surface concentration of deuterium, $\alpha = \sqrt{4\pi R_o[T]}$ where R_o is the capture radius, [T] is the trap concentration and x is the depth. For dislocated single crystals the experimental points could be fitted only for a depth larger than about 500 nm, as some deuterium back-diffusion occurred during the cooling down stage after the hydrogenation. It is well evident that the same mechanism of diffusion is occurring in dislocated single crystals and in EFG samples, the latter presenting in fact a very large density of dislocations (about $10^9 cm^{-2}$). As the diffusion length of both the dislocated samples and the EFG samples incraes after hydrogenation (see table 1) we have to argue that the passivation mechanism involves the passivation of deep levels associated to dislocations.

5.2 Effect of catalytic and plasma hydrogenation on EFG samples

The experimental results, as average values before and after the hydrogenation and post annealing processes of EFG samples are reported in tables 1 and 2.
It is apparent (see table 1) that the catalytic hydrogenation induces an increase of diffusion length of the EFG samples which reaches values comparable with those obtained only after a 450 °C annealing of the RF plasma pre-hydrogenated samples (see table 2). No

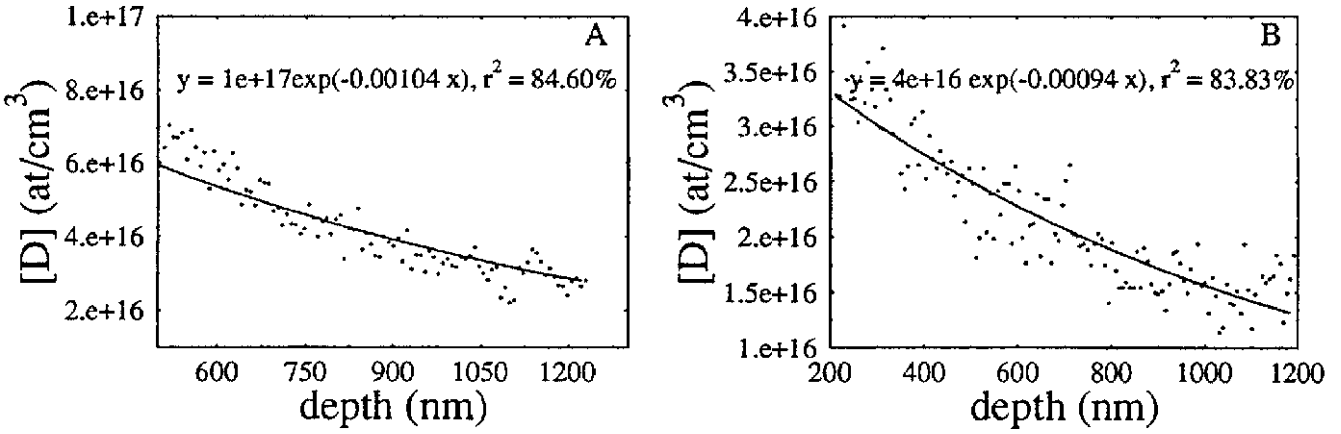


Figure 3: Fit of the deuterium diffusion profiles in dislocated samples A) $N_d = 10^8$ cm^{-2} B) $N_d = 10^6$ cm^{-2}

Sample	L_{D1} (μm)	L_{D2} (μm)	L_{D3} (μm)
CS2	28 ± 3	52 ± 5	45 ± 5
CG2	33 ± 3	47 ± 5	41 ± 4
LS2	26 ± 3	42 ± 4	41 ± 4
LG2	21 ± 2	60 ± 6	52 ± 5
Sample	L_{D1} (μm)	L_D (plasma) (μm)	
DIS	6 ± 1	50 ± 5	

Table 1: SPV measurements on EFG samples. L_{D1}, L_{D2} e L_{D3} are, respectively, the average diffusion length of the as-grown, catalytically treated and post-annealed samples. On each sample, a minimum of three measurements in different position were carried out. DIS is the monocrystalline dislocated sample before and after plasma hydrogenation.

Sample	L_{D1} (μm)	L_{D2} (μm)	L_{D3} (μm)
CS1	37 ± 4	36 ± 4	52 ± 5
CG1	23 ± 2	17 ± 2	67 ± 7
LS1	27 ± 3	30 ± 3	41 ± 4
LG1	27 ± 3	31 ± 3	39 ± 4

Table 2: SPV measurements on EFG samples. L_{D1}, L_{D2} e L_{D3} are, respectively, the average diffusion length of the as-grown, plasma treated and post-annealed samples. On each sample, a minimum of three measurements in different position were carried out.

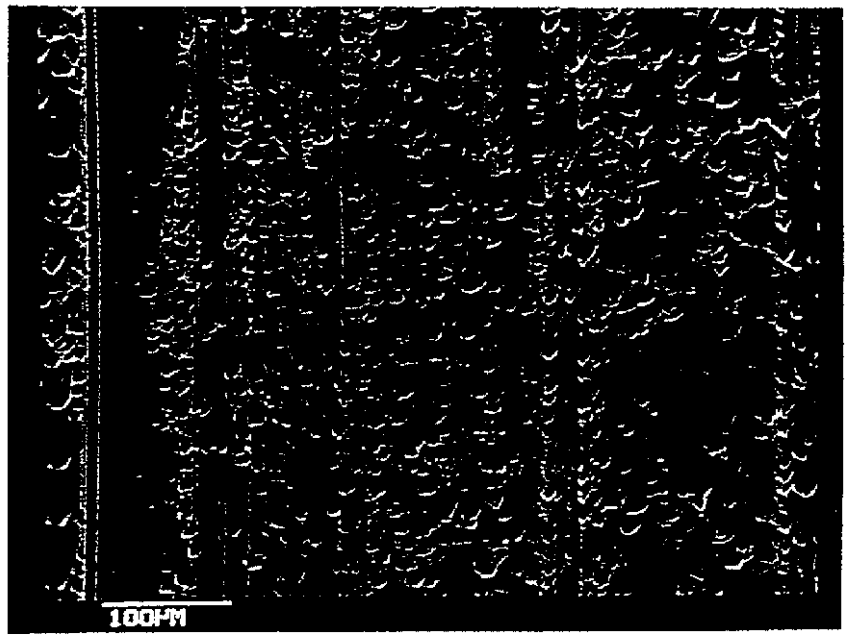


Figure 4: SEM micrography of EFG sample (CS1) submitted to plasma hydrogenation and post annealing. Magnification 200x

significant improvement of the diffusion length is instead observed in the case of EU material, taken as reference and having approximately the same composition, but not the same microstructure, both in plasma and catalytically hydrogenated samples neither after the hydrogenation or after the post-hydrogenation annealing.

To understand whether the different effect on the EFG samples of the catalytical and plasma hydrogenation process would be associated to a different density of defects which can be decorated by Pt and then made preferential of sites for dissociative chemisorption, we have measured the dislocation density by the etch pit count technique on the EFG material before and after the catalytic hydrogenation.

The results of these measurements, carried out on SEM (Scanning Electron Microscope) pictures (see figures 4, 5), after purple etch ($10\%HF$: $48\%HNO_3$: $42\%CH_3COOH$ saturated with I_2) at room temperature for 15s for the removal of the massive Pt deposits, show that after the catalytic hydrogenation the apparent number of etch pits is drastically reduced. As the hydrogenation temperature is too low to allow dislocation movement, one has to conclude that some emerging dislocation segments are not more selective etching sites, due to Pt decoration. Apparently, these decorated dislocations are preferential hydrogen diffusion paths, with Pt which behaves as localized dissociation center of the molecular hydrogen adsorbed on it.

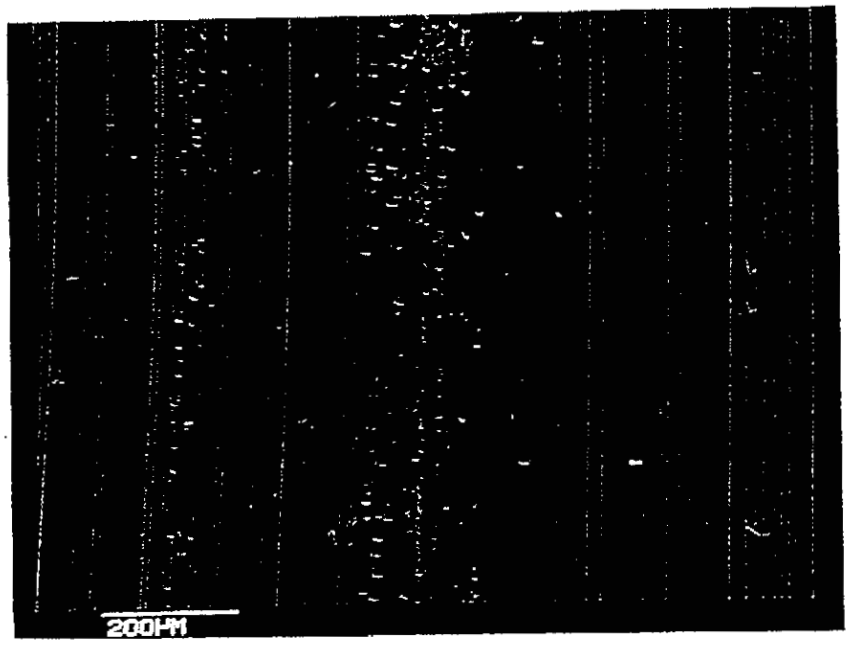


Figure 5: SEM micrography of EFG sample (CS2) submitted to catalytic hydrogenation. Magnification 200x

5.3 Effect of surface oxidation on the diffusion length of polycrystalline silicon wafers

This procedure was used on polycrystalline silicon samples, cut from blocks of DS crystallized ingots. The effect of thermal treatments at 700 °C on L_d are summarized in table 3. It shows that the diffusion length increases systematically, being the increase larger for samples presenting the lower initial values. When applied to edge region wafers, the procedure results inappropriate as the electrical properties of the wafers remain almost unchanged. Considering that the lifetime of these wafers is dominated by deep levels associated to iron in supersaturated conditions and to iron silicide precipitates [17], this result supports the assumption reported in the Introduction, that external gettering might be effective only when the surface sinks are deeper than the internal ones. In this case, even if iron is gettered at the surface, the solution is continuously replenished by iron silicide precipitates dissolution.

5.4 Effect of Ru^{3+} passivation on InP and Si

The experiments were carried out using the SPV and LBIC technique in the lateral configuration on a InP diodes and Schottky diodes prepared by depositing Al on MCZ silicon. In both cases, the junction is perpendicular to the exposed surface. The Ru^{3+} solution was 0.01 M in $RuCl_3$ in which the devices were dipped for 30" and then gently rinsed with water. Before dipping the silicon samples in $RuCl_3$ solution, they were submitted to a series of cleaning steps (APM+DHF+HPM+DHF [22]). The results for InP and Si are reported in Fig. 6 and Fig. 7. Considering the results concerning the

Wafer	Sample	L_D [μm]	
		As grown	4h 700 °C air
3	O/B	35 ± 3	106 ± 11
6	C/B	53 ± 5	52 ± 5
7	O/C	21 ± 2	44 ± 4
7	O/A	57 ± 6	118 ± 12
		As grown	16h 700 °C air
5	O/C	33 ± 3	80 ± 8
10	O/A	53 ± 5	79 ± 8
10	O/AS	65 ± 6	71 ± 7
10	O/BS	34 ± 3	72 ± 7
14	C/BS	97 ± 10	103 ± 10

Table 3: Diffusion length of Eurosolare samples before and after annealing in air at 700 °C for different times

InP samples, it appears that the photocurrent increases after dipping the sample in the Ru^{3+} solution. As for a surface recombination rate close to zero the dependence of the photocurrent on the distance from the junction is linear (see eq. 4), the surface passivation induced by Ru^{3+} is well evident. In the case of silicon, while a passivating action of DHF is well evident, that ofRu^{3+} is almost undetectable, thus confirming the theoretical predictions about the poor or negligible passivating capability of noble metals.

6 Discussion and Conclusions

The experimental results reported in the previous Sections well support that passivation and gettering are complementary techniques.
About the first topic considered, the increase of the diffusion length in EFG samples after catalytic hydrogenation supports a preliminary conclusion that the catalytic process not only is competitive with the plasma one, but presents also the advantage of being effective without a post-hydrogenation anneal.
However, the results of our experiments about hydrogen diffusion enlighten also some still undiscovered features of the hydrogen passivation, which seem to fit with the multiple trapping model of Corbett and al.[1], by assuming that dislocations are unsaturable traps and, then, preferential paths for hydrogen diffusion and secondary hydrogenation sources. The need of a post-hydrogenation anneal in the plasma hydrogenated samples, moreover, indicates that in this latter case the hydrogen is ubiquitously diffused in a thin subsurface layer during the hydrogenation process, but that it is allowed to diffuse deep into the material by the high temperature post-hydrogenation stage. This conclusion is well supported and implemented by the effect of hydrogenation on minority carrier properties in a dislocated single crystal, see table 1, which demonstrates that a substantial increase of the diffusion length L_d can be obtained by plasma hydrogenation of dislocation-induced recombination centres.
If dislocations are both traps for hydrogen and (at least partially) passivable recombination

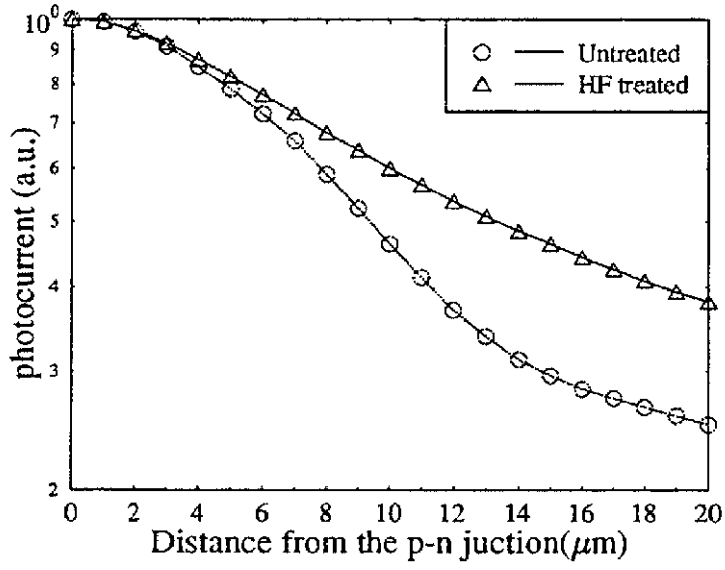


Figure 6: Photocurrents curves of InP samples before and after dipping in the $RuCl_3$ solution.

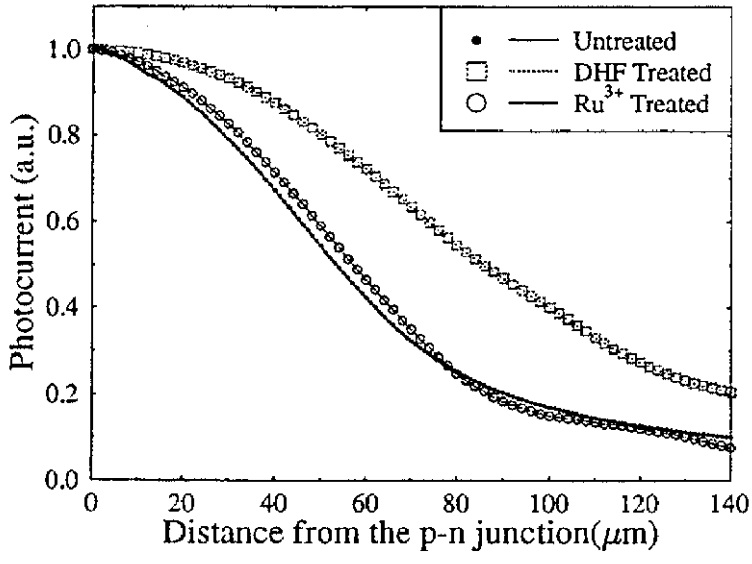


Figure 7: Comparison between the spectral responses of MCZ samples in as-grown conditions and after dipping in HF and in $RuCl_3$.

centres, the interpretation of the results concerning the Eurosolare samples which were shown almost insensitive to hydrogen passivation, is definitely simpler. Actually, although the EFG and DS samples were chosen very close in composition, they present large microstructural differences depending on the type of charge, furnace and growth cycle.

For these particular DS samples, due to their relatively low dislocation density the hydrogen passivation, catalytic or plasma, has no effect, as the defects responsible for the electrical degradation are bulk recombination centers (iron in supersaturation conditions and silicon nitride and iron silicide precipitates [17]) cannot be easily reached and passivated by hydrogen.

About the second topic, concerning low temperature oxidation gettering, we have shown that impurity gettering engineering presents still undiscovered, but theoretically well based, opportunities, which however depend significantly, like in the former case, on the materials properties. Eventually, the fact that TM passivation was shown to be effective only in the case of III-V semiconductors, does not mean that further progresses in defect passivation and gettering could be achieved by a careful choice of experimental conditions and passivation tools, based on the already available theoretical knowledge on defect properties.

References

[1] S.J. Pearton, J.W. Corbett, M. Stavola "Hydrogen in Crystalline Semiconductors" Springer Verlag (Berlin) 1992

[2] M. Kittler, H. Richter. H.G. Grimmeis "Proceedings of the Gadest Conferences 1989, 1991, 1993, 1995 "TransTech and SciTech Publ. Ltd., Zug (Switzerland)

[3] Chabal Y. J. *Physica B* **170** (1991) 447

[4] S. Binetti, M. Acciarri, C. Savigni, S. Pizzini and S. Basu, accepted at EDS'96 and to be published in. J. de Physique (Paris)

[5] Zundel T., Weber J. *Phys. Rev. B* **39** (1989) 13549

[6] Lee H.H. *Appl. Phys. Lett.* **54** (1989) 724

[7] Mandal K. C., Basu S., Bose D. N. *J. Phys. Chem.* **91** (1987) 4011

[8] Bose D. N., Ramprakash Y., Basu S. *J. Electrochem. Soc.* **131 (4)** (1984) 850

[9] Xie Xide, Zhang Kaiming, *Progr. Surf. Sci.* **28-2** 1988, pp.71-179

[10] W. Schroeter, M. Seibt, D. Gilles: In "Materials Science and Technology Vol.4" ed R.W. Cahn, P. Hasen, E.J. Kramer VCH Publ. (Weinheim,1991) pp. 539-579

[11] Savigni C., Acciarri M., Binetti S. Proc. of Polyse '95 Polycrystalline Semiconductors IV in "Solid State Phenomena" (S. Pizzini, H.P. Strunk Wand J. H. Werner eds. Trans. Tech. Publ. Zug. Switzerland 1995)

[12] Th.Flohr, R. Helbig *J.Appl. Phys.*, **66** (1989) 3060

[13] Marek J. J. Appl. Phys. **55** (1984) 318

[14] Wald F.V. *Solar Energy Materials* **23** (1991) 175

[15] S. Binetti S., Ratti S., Acciarri M., Pizzini S., Proc. 12th European Photovoltaic Solar Energy Conference, (Amsterdam 11-15 April 1994) 709

[16] Pizzini S., Gasparini M. and Rustioni M., Fr. Patent 82, July 1982, 12588

[17] Binetti S., Acciarri M., Savigni C., Brianza C., Pizzini S., Musinu A. *Materials Science and Engineering* **B36** (1996) 68

[18] Mariani J.L., Pichaud B., Minari F., Martinuzzi S. *J. Appl. Phys.* **71**, (1992) 1284

[19] Acerboni S., Pizzini S., Binetti S., Acciarri M., Pichaud B. *J.Appl.Phys.* **76** (1994) 2703.

[20] Herrero C. P., Stutzmann, Breitschwerdt P., Santos P. V. *Phys. Rev.* **B** (1990) 1054

[21] Acciarri M., Binetti S., Garavaglia M., Pizzini S. *Materials Science and Engineering* (1996) in press

[22] Binetti S., Acciarri M., Brianza A., Savigni C. and Pizzini S. *Materials Science and Technology* **11**. (1995) 665

Physical and Numerical Modeling of Impurity Precipitation, Precipitate Dissolution, and Gettering of Precipitated Impurities in Silicon

Teh Y. Tan, R. Gafiteanu, and U. Gösele

Department of Mechanical Engineering and Materials Science
Duke University
Durham, NC 27708-0300
USA

Gettering of unwanted impurities away from the device active regions has already been an integral part of manufacturing integrated circuits (IC) using Czochralski (CZ) Si wafers [1,2], and is becoming increasingly important in Si solar cell fabrications for improving the cell efficiency [3-12]. Gettering consists of the creation of suitable gettering regions, and the gettering processes of contaminants. In the past, associated with IC applications utilizing the intrinsic gettering (IG) scheme [1,2], emphasis has been placed upon the study of the IG site/region properties [1]. Efforts in studying the impurity gettering processes either experimentally or theoretically were quite limited [13,14]. The process of gettering the contaminating metals to the gettering region involves the metal atom dissolution from precipitated state, the metal atom diffusion to, and the stabilization at the gettering sites. We have recently implemented a program to model the impurity gettering process physically and numerically. Some results of such studies have been reported previously [15]. This includes the gettering of fast diffusing interstitial (i) species and substitutional-interstitial (s-i) species as the model impurities. The modeled gettering techniques include the use of a wafer backside Al layer; wafer frontside indiffusion of P; indiffusion of P together with an Al layer (P+Al). The primary purpose of the present talk is to report modeling results on precipitated impurities using a wafer backside Al layer as the gettering region. These results are relevant to solar cell applications.

The monolithic IC devices are fabricated using single crystal CZ Si containing dissolved metal atoms with very small concentrations, but no metal precipitates and no dislocations. The main contamination sources are processing equipment and materials, irrespective of the fact that IC fabrication facilities are maintained at very clean states at very high costs. Thus, gettering in the IC case is to guard against the processing introduced contaminants. Because of the monolithic nature of the IC devices, these contaminants can be gettered to the wafer bulk IG sites. The involved metal diffusion distance is short, on the order of only 10 μm or less. In solar cell fabrications a variety of Si substrates are used, including single crystal FZ and some CZ wafers for high efficiency cells fabricated using clean facilities, and low cost CZ wafers and large grain polycrystalline ribbons and wafers for commercial cells. The polycrystalline Si ribbons and wafers contain grain boundaries, dislocations, precipitated as well as dissolved metals. Moreover, the commercial solar cell are fabricated in low cost (hence not clean) facilities. Thus, gettering is essential for commercial solar cell fabrications, for purposes of improving the starting Si substrate quality as well as guarding against contamination during processing. To improve the substrate quality, metal precipitate dissolution is involved, and the dissolved metal atom diffusion distance is very long, on the order of 100-200 μm.

Stabilization of impurities in the gettering region may be due to either the impurity segregation property between the gettered and gettering regions, or due to preferential precipitation of the impurity in the gettering region. Gettering of Fe by the IG technique relies upon preferential precipitation in the IG region during cooling [14]. On the other hand, an Al layer on the Si wafer surface can provide a gettering effect because of the segregation effect. Al is a dopant in Si, and not a metallic contaminant. The solubility of other metals in Al is very high, reaching 1 at% in the temperature range below the eutectic temperature of 577°C. Above the eutectic temperature at which a liquid Al-Si alloy forms, the solubility of a typical metal can exceed 10 at%, i.e., on the order of $5x10^{21}cm^{-3}$. Since the solubility limit of metals in Si does not exceed $\sim 10^{17}$ cm^{-3}, the segregation

coefficient of the metal between the Al liquid and Si is $>10^4$, reaching 10^{10} in some cases. This provides a tremendously large driving force for the metal to segregate into the liquid. It is obvious that the elementary process involved in Al gettering is impurity diffusion and segregation. It is expected that Al gettering should be highly effective for interstitially dissolved metal atoms because of their large diffusivity values in Si, and because of the large segregation coefficient between Si and Al.

To mathematically model/simulate the gettering process of an atomically dissolved impurity species in Si, it is necessary to calculate the impurity diffusion and segregation processes simultaneously. For the simplest case of gettering an interstitially dissolved metal species by Al, the standard diffusion equation

$$\frac{\partial C}{\partial t} = D \frac{\partial^2 C}{\partial x^2} \tag{1}$$

can be used to simulate the diffusion processes in both the Al layer and the Si matrix. The empirical boundary condition of Antoniadis and Dutton [16], in the more detailed form of

$$F_S = \frac{D^{eff}}{\lambda} (C_1 - \frac{C_2}{m_2}) , \tag{2}$$

arrived at recently via a derivation [17], can be used as a computational criterion at the Al-Si interface to describe the segregation process. In Eq. (2) F_S is the impurity flux at the interface; C_1 is the impurity concentration at the computational grid point 1 in the bulk of region 1 (e.g., Si) nearest to the interface (which should in principle be the last Si lattice plane at the interface); C_2 is the same in region 2 (e.g., Al), m_2 is the equilibrium segregation coefficient of the species in region 2 relative to region 1 (m_1=1); λ is the atomic plane spacing; D^{eff} is an effective diffusivity given by $D^{eff} = \Gamma_{1\rightarrow 2}\lambda^2$ with $\Gamma_{1\rightarrow 2}$ being the atom jump frequency from region 1 to 2. Except for this simplest case, Eqs. (1) and (2) cannot be used to simulate the impurity gettering process. In general, the impurity diffusion process may be coupled to also the Si native point defect diffusion processes, leading to the need of additional diffusion equations and the existence of appropriate coupling terms in each of the equations. To treat the general case, a flux equation of diffusion-segregation (FEDS) and a diffusion-segregation equation (DSE) have been derived [18,19]:

$$J = -D\left(\frac{\partial C}{\partial x} - \frac{C}{m}\frac{\partial m}{\partial x}\right), \tag{3}$$

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial x}\left[D\left(\frac{\partial C}{\partial x} - \frac{C}{m}\frac{\partial m}{\partial x}\right)\right]. \tag{4}$$

In Eqs. (3) and (4) the segregation coefficient m of a species may be regarded as either a continuously changing or fairly abruptly changing quantity. That is, insofar as the impurity or point defect segregation properties are concerned, the use of Eq. (4) is sufficient for all gettering problems. It is easy to see the similarity between Eqs. (2) and (3), and it has been shown [20] that Eq. (3) reduces to Eq. (2) upon discretization at an abrupt interface. Indeed, it has been demonstrated using model problems that Eqs. (2) and (4) yielded the same results [15].

Solar cell grade multicrystalline Si substrates contain bad regions wherein the minority carrier diffusion lengths are extremely low, and cannot be significantly improved by a normal gettering treatment such as P indiffusion. These regions contain dislocations and metal silicide precipitates to high densities. The reason that the quality of these regions is difficult to improve by gettering treatments is that now the gettering process involves also precipitate dissolution which requires more extensive treatment. To model the impurity gettering process involving both precipitated and

dissolved metal atoms in Si, a basic set of expressions has been written by assuming that the precipitate dissolution process is limited by diffusion of the dissolved impurity atoms. The reason for regarding the precipitate dissolution process as diffusion limited is for the purpose of obtaining a best case estimate of the effectiveness of a gettering process, which should be the fastest. This means that no kinetic barrier against the dissolution of the precipitate is assumed. Most silicide precipitation and precipitate dissolution processes are associated with a precipitate-matrix volume misfit, which leads to a kinetic barrier slowing down the process. However, the diffusion limited precipitate dissolution assumption should be fairly realistic for solar cell grade Si, because the high density of dislocations can serve to eliminate the kinetic barrier incurred by the volume misfit via mediations of point defects (this will not be the case in single crystal Si substrates containing no dislocations). Accounting for segregation processes that may also be involved, these expressions are

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial x}\left[D\left(\frac{\partial C}{\partial x} - \frac{C}{m}\frac{\partial m}{\partial x}\right)\right] + 4pr\rho D(C^{*}-C)\,, \tag{5}$$

$$C^{*} = C^{eq}\exp\left(\frac{2\Omega\sigma}{rk_BT}\right), \tag{6}$$

$$\frac{dr}{dt} = -\,\Omega\, D\,\frac{C^{*}-C}{r}\,. \tag{7}$$

In Eqs. (5)-(7) C is the (metal) impurity atom concentration in the matrix, C^{*} is the impurity dynamic equilibrium concentration at the interface of Si and the precipitate with radius r, C^{eq} is the thermal equilibrium concentration of the impurity, ρ is the precipitate density, Ω is the volume of one impurity atom in the precipitate, σ is the precipitate-matrix interfacial energy density, and k_B is Boltzmann's constant. It is noted that Eqs. (5)-(7) also apply to the precipitate growth process.

Equations (5)-(7) have been used to numerically model the processes of impurity precipitation, of dissolution of impurity precipitates, as well as of gettering in the simultaneous presence of dissolved and precipitated impurities by a wafer backside Al layer. The chosen model impurity is Fe, with its thermal equilibrium concentration and diffusivity in Si given by

$$C^{eq} = 1.82\text{x}10^{26}\exp\left(-\frac{2.94\text{ eV}}{k_BT}\right)\text{cm}^{-3}\,, \tag{8}$$

$$D = 1.3\text{x}10^{-3}\exp\left(-\frac{0.68\text{ eV}}{k_BT}\right)\text{cm}^{2}\text{s}^{-1}\,. \tag{9}$$

No precipitate-matrix volume misfit is assumed, which should be fairly realistic for solar cell grade multicrystalline Si substrate cases. For simplicity, the surface energy density σ is assumed to be zero. This assumption has the effect of speeding up the precipitation process, while slowing down the precipitate dissolution process and the gettering process involving also precipitated impurities. We believe, however, that the effect is small, for two reasons. First, the effect of σ is inherently small for larger precipitates. Second, the work of Gilles et al. [14] seems to indicate that the magnitude of σ in the case of Fe cannot be very large, or else the observed effect of gettering of Fe by precipitation on IG sites cannot have occurred as effectively.

Figure 1 shows a set of results of Fe precipitation, which will be valid if there exists no nucleation barrier. The condition is probably satisfied fairly well in multicrystalline solar Si and in CZ Si by IG. In both cases there is an abundance of dislocations which are heterogeneous nucleation sites with low activation energy barriers. In the simulation, the Si wafer was assumed to have been satu-

rated by interstitial Fe atoms at 900°C and subsequently precipitated at 700°C for various ρ values. It is found that the precipitate density ρ played the most critical role in determining the precipitation rate. For the case of $\rho=10^{11}$ cm^{-3}, it takes a time of ~1.5 min to complete the precipitation process to 99%. This 99% precipitation-completion time is increased to ~7 and ~32 min respectively for the $\rho=10^{10}$ and 10^{9} cm^{-3} cases. Figure 2 shows a set of results of precipitate dissolution, which is exactly the reverse process of that shown in Fig. 1. That is, the precipitated wafer shown in Fig. 1 is now brought to 900°C for an annealing so as to dissolve the Fe precipitates. The needed 99% dissolution-completion time for the $\rho=10^{11}$ cm^{-3} case is ~0.7 min, which is faster than the corresponding precipitation time shown in Fig. 1, because the dissolution temperature is higher and hence D is larger. As with the precipitation case, the dissolution time also becomes longer for lower ρ values: the 99% dissolution-completion times are ~4 and ~16 min respectively for the $\rho=10^{10}$ and 10^{9} cm^{-3} cases. The basic reason for the ρ dependence of the completion times in both the precipitation and precipitate dissolution cases is that a higher ρ value provides a larger total capturing/dissolution surface area for Fe atoms.

To model the gettering process of both dissolved and precipitated Fe, a 200 μ thick Si wafer was assumed to have been saturated with Fe at 900°C and precipitated at 700°C to ~100% completion, and then gettered by a 2 μ thick Al layer situated at the backside of the wafer at different temperatures. Note that *completion* means that no precipitation (or dissolution) further goes on, which is a condition satisfied in the present case when the Si matrix Fe concentration has reached its thermal equilibrium value of ~10^{11} cm^{-3} at the precipitation temperature of 700°C. Figure 3 shows the simulation results at the gettering temperature of 700°C for the $\rho=10^{11}$ cm^{-3} case. From Fig. 3, three outstanding features are noticed: (i) it takes ~60 h for the gettering process to reach the steady state for which the Fe concentration dropped to ~10^{7} cm^{-3}; (ii) to reduce the Fe concentration everywhere in the Si wafer to below 99% of the 700°C Fe solubility value of ~10^{11} cm^{-3}, it has taken already ~59 h of gettering time, and in the mean while precipitates existing in the wafer frontside are still not totally dissolved; (iii) for shorter times, the Si wafer dissolved Fe concentration is not spatially uniform, and neither is the precipitate size: concentrations of Fe existing in both dissolved and precipitated forms increase monotonically from the backside to the frontside of the wafer. As the assumed precipitate density ρ is decreased, the needed gettering times increase. For example, the gettering time is increased to ~260 h for the $\rho=10^{10}$ cm^{-3} case. For comparison, we have also simulated the cases for which Fe introduced at 900°C are completely existing in solution, which may be obtained by quenching. Figure 4 shows the simulation results of such a case for which the gettering temperature is 700°C. It is seen from Fig 4 that it takes less then 2.7 h to reach the same steady state and to gettering Fe to a concentration everywhere in the Si wafer to below 99% of the 700°C Fe solubility value of ~10^{11} cm^{-3} needs slightly more than 1 h. For the results shown in Fig. 4 to be valid, it is assumed that the Si substrate is perfect, so that via the existence of a nucleation barrier, the rapid Fe precipitation process illustrated in Fig. 1 is not occurring. In both the case shown in Fig. 3 and the case shown in Fig. 4, the total amount of Fe is the same, but for the case of Fig. 4, all the Fe atoms exist in solution and are hence available to be gettered at any time. For the case shown in Fig. 3, long gettering times are needed, because of three factors, in descending order of importance: (i) the assumed gettering temperature is lower than the Fe introduction temperature, which limits the amount of dissolved Fe to be gettered to a value corresponding to the gettering temperature C^{eq} value-which is much lower than the total amount of Fe introduced; (ii) the total Fe precipitate dissolution surface is small, irrespective of the assumed high precipitate density; (iii) the dissolved Fe diffusivity is small. Thus, it will be quite ineffective to getter precipitated im-

purities at a temperature much lower than an effective temperature at which the impurity solubility corresponds to the total amount of the impurity present in the Si wafer. This suggests that a higher temperature may be more effective, since for a given precipitate density and size the needed gettering time is decreased, see Fig. 5 for a summary of data. We believe that the present simulation results have provided a plausible explanation to the experimental results that gettering by Al of multicrystalline Si substrates may be ineffective, or may even has an inverse effect: it is because the gettering time is too short and hence the gettering process is hardly complete. In addition, the substrate dissolve impurity concentration may actually also have increased due to precipitate dissolution at a higher gettering temperature, while the gettering process has not yet been effective due to the short gettering times used. One should also be aware of the problem of further contamination in using an unclean furnace at a fairly high temperature, e.g., 1000°C.

We believe that most of the basic physics and expressions for modeling the gettering process of a given impurity species, from the dissolution of the impurity precipitates to the diffusion and segregation (stabilization) of the impurity atoms, now exist. Accurate modeling parameters, such as the impurity charge states, level positions, solubilities, diffusivities, and interfacial energy densities between the silicide precipitates and Si are needed. Furthermore, we need also a realistic treatment of the precipitate nucleation problem.

1. *Semiconductor Silicon 1994*, edited by H. R. Huff, w. Bergholz, and K. Sumino (The Electrochem. Soc., Pennington, NJ, 1994).
2. T. Y. Tan, E. E. Gardner, and W. K. Tice, Appl. Phys. Lett. 30, 175 (1977).
3. T. M. Bruton, A. Mitchell, L. Teale, and J. Knobloch, *Proc. 10th European Photovoltaic Solar Energy Conference*, 1991 (Kluwer Academic Publishers, Dordrecht, 1991) p. 667.
4. B. Hartiti, A. Slaoui, J. C. Muller, and P. Siffert, Appl. Phys. Lett. 63, 1249 (1993).
5. R. Sundaresan, D. E. Burk, and J. G. Fossum, J. Appl. Phys. 55, 1162 (1984).
6. R. Janssens, R. Mertens, and R. Van Overstraeten, *Conference Record of the 15th IEEE Photovotaic Specialists Concerfence* (IEEE, 1981) p. 1322.
7. S. Narayanan, S. R. Wenham, and M. A. Green, IEEE Trans. Electron Dev. ED-37, 382 (1990).
8. A. Rohatgi, P. Sana, and J. Salami, *Proc. 11th European Photovoltaic Solar Energy Conference*, 1992 (Harwood Academic Publishers, Switzerland, 1992) p. 159.
9. M. Pasquinelli, S. Martinuzzi, J. Y. Natoli, and F. Floret, in Proceedings of the 22nd IEEE PV Specialists Conference, Las Vegas, NV, 1991 (IEEE, New York, 1991), p. 1035.
10. M. Loghmarti, R. Stuck, J. C. Muller, D. Sayah, and P. Siffert, Appl. Phys. Lett. 62, 979 (1993).
11. B. Hartiti, A. Slaoui, J. C. Muller, and P. Siffert, Appl. Phys. Lett. 63, 1249 (1993)e governing expressions are. Kalejs, and R. O. Bell, Appl. Phys. Lett. 64, 97 (1994).
13. W. Schröter, M. Seibt, D. Gilles, Ch. 11 of "Electronic Structure and Properties of Semiconductors", Vol. 4 of "Materials Science and Technology: A Comprehensive Treatment" eds. R. W. Cahn, P. Haasen, and E. J. Kramer, Vol. 4 ed. W. Schröter (1991), p. 576.
14. D. Gilles, E. R. Weber, and S. Hahn, Phys. Rev. Lett. 64, 196 (1990).
15. T. Y. Tan, R. Gafiteanu, and U. Gösele, NREL 5th mtg.
16. D. A. Antoniadis and R. Dutton, IEEE Trans. Electron. Devices ED-26, 490 (1979).
17. T. Y. Tan and R. Gafiteanu, Second Annual Report, NREL Subcontract No. XD-2-11004-1 (1994), Chapter II.
18. H.-M. You, U. Gösele, and T. Y. Tan, J. Appl. Phys. 74, 2461 (1993).
19. T. Y. Tan, R. Gafiteanu, and U. M. Gösele, in *Semiconductor Silicon 1994*, edited by H. R. Huff, W. Bergholz, and K. Sumino (The Electrochem. Soc., Pennington NJ, 1994) p. 920.

20. R. Gafiteanu, U. Gösele, and T. Y. Tan, in *Defect and Impurity Engineered semiconductors and Devices*, eds. S. Ashok, I, Akasaki, J. Chevallier, N. M. Johnson, and B. L. Sopori, Mater. Res. Soc. Proc. 378 (Mater. Res. Soc., Pittsburgh, PA, 1995) p. 297.

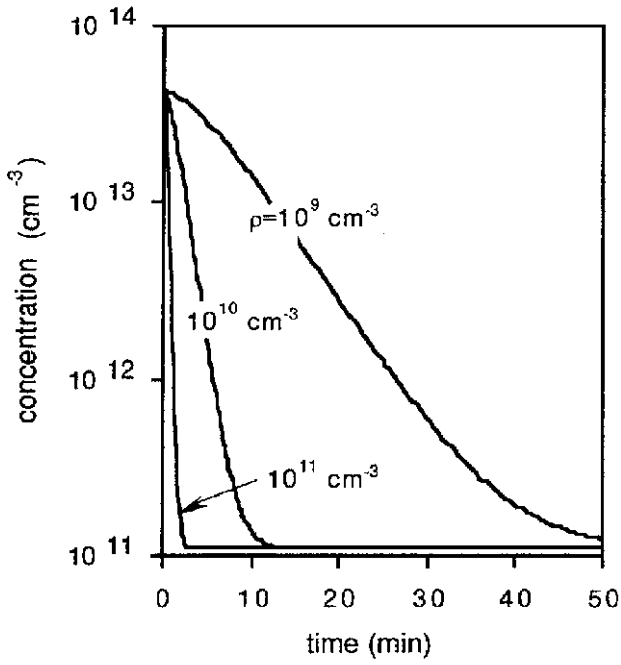


Fig. 1 Calculated concentration of Fe in Si during Fe precipitation. ρ indicates the assumed precipitate density. The initial Fe concentration is assumed to be the thermal equilibrium value at 900°C, and the precipitation temperature is assumed to be 700°C. Precipitate growth is assumed to be controlled by Fe diffusion, which yields the upper limit of the precipitation rate for a given ρ at a given precipitation temperature.

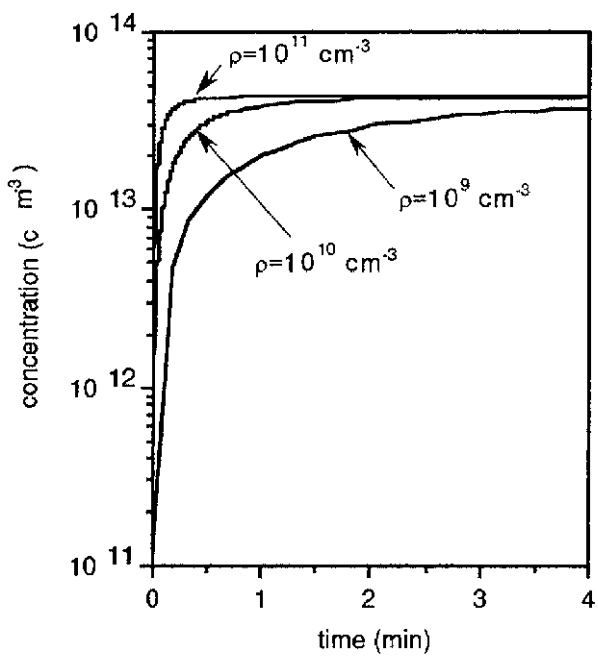


Fig. 2 Calculated concentration of Fe in Si during Fe precipitate dissolution. This is the inverse case of that shown in Fig. 1. That is, the Fe precipitation process according to conditions leading to the results shown in Fig. 1 was carried out to completion, and then the Si wafer was annealed at 900°C to dissolve the precipitates.

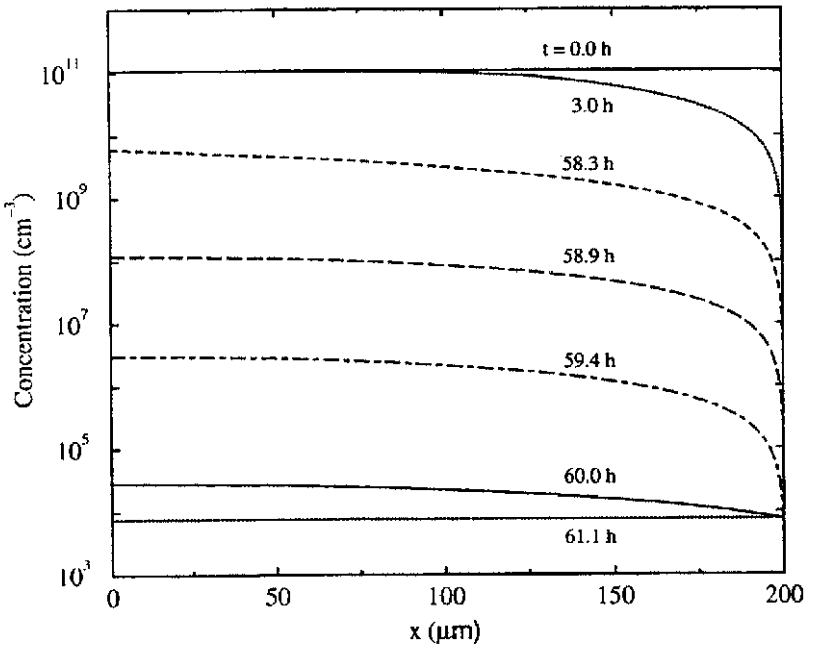


Fig. 3 Calculated results of gettering by a Si wafer backside Al layer of Fe existing both in solution and in precipitates. The initial Fe concentration is assumed to be the thermal equilibrium value at 900°C, and was precipitated at 700°C to completion. The gettering annealing was assumed to be at also 700° C. The assumed Si wafer and Al layer thicknesses are 200 and 2 μm, respectively.

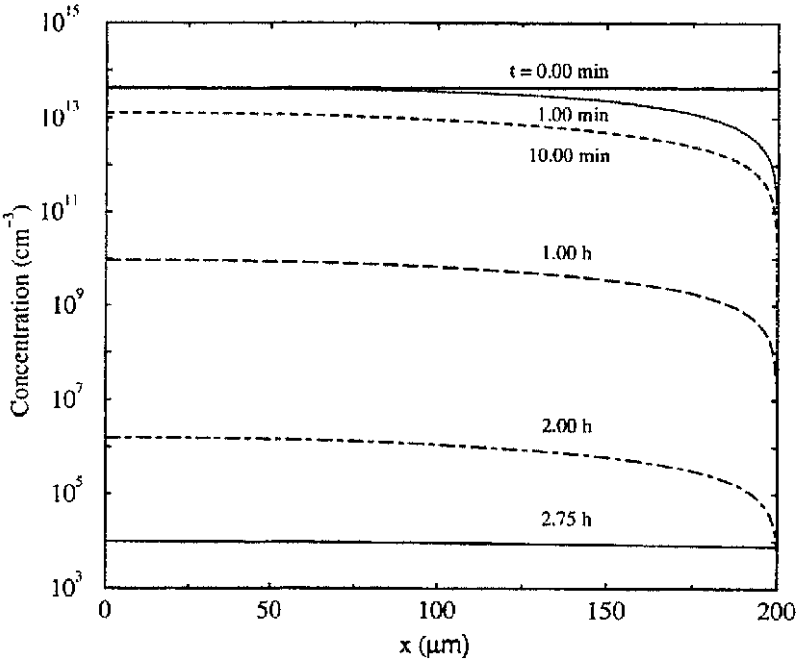


Fig. 4 Calculated results of gettering by a Si wafer backside Al layer of Fe existing in solution only. The total amount of Fe is the same as in the case shown in Fig. 3. That is, the initial Fe concentration is assumed to be the thermal equilibrium value at 900°C, which can be quenched-in, and the gettering annealing was assumed to be at also 700° C. Other conditions are the same as the case shown in Fig. 3.

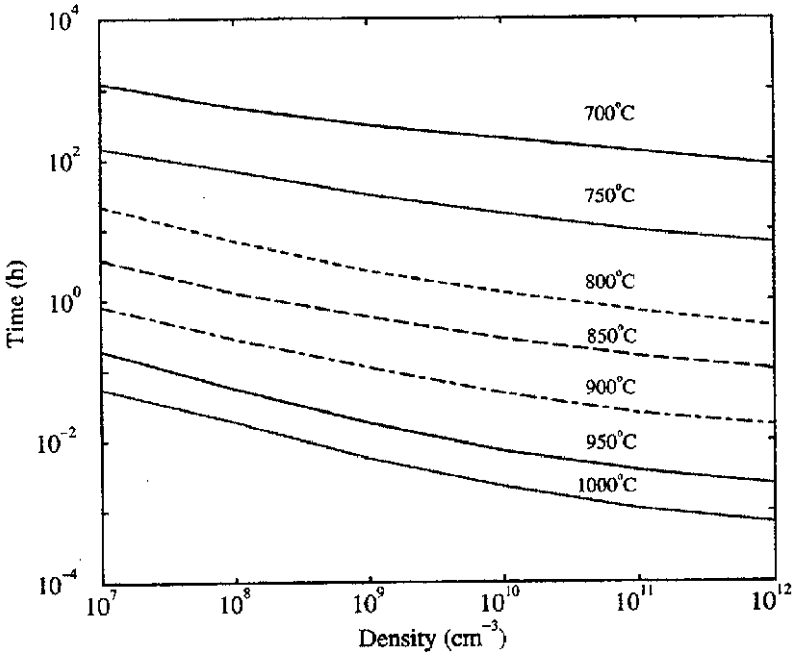


Fig. 5 Calculated completion times of gettering by a Si wafer backside Al layer of Fe existing both in solution and in precipitates. Various precipitate density ρ and gettering temperature T values have been included. Other conditions are the same as for the case shown in Fig. 3.

REDISTRIBUTION KINETICS OF METAL IMPURITIES IN MULTICRYSTALLINE SILICON

M.Seibt, M.Apel, I.Hanke and W.Schröter
IV.Physikalisches Institut der Universität Göttingen
Bunsenstr.13-15, D-37073 Göttingen
Germany

1 Introduction

The technological importance of transition metal impurities in silicon device fabrication has initiated intensive research of their physical properties. As a result, there is now profound knowledge of their solubility and diffusivity, their precipitation behavior as well as their electrical properties in silicon (for reviews c.f. [1] ,[2] ,[3]). It is well-known that the technologically most relevant 3d transition metal impurities in intrinsic silicon are predominantly dissolved on interstitital sites at high temperatures. At room temperature, however, they are obtained as isolated interstitials (e.g. Fe_i) [1], as complexes or pairs (e.g. FeB-pairs) [4], or as metal silicide precipitates [2] depending on type and concentration of the impurity, cooling conditions as well as the density and type of defects present in the silicon.

For illustration, consider Fe and Ni representing moderately and extremely mobile metal impurities in silicon, respectively. On the one hand, Fe is observed as Fe_i in defect-free FZ- and Cz-Si after rapid cooling from high temperatures (e.g. [3]). For p-type silicon, storage at room temperature will result in the formation of FeB pairs. On the other hand, heterogeneous precipitation of Fe occurs in the presence of extended defects like bulk stacking faults, SiO_x- or transition metal precipitates. Fast diffusing transition metals like Co, Ni and Cu predominantly precipitate even in defect-free silicon unless the material is highly doped with shallow acceptor atoms like B [5]. For these metal impurities, cooling conditions and the presence of crystal defects will mainly determine the distribution and size of silicide precipitates [2]. For example, fast quenching of Ni-diffused FZ-Si results in a homogeneous distribution of thin $NiSi_2$ platelets with diameters of 20-500nm [7] [8], whereas slow cooling leads to $NiSi_2$ precipitates up to $10\mu m$ in size predominantly formed at wafer surfaces giving rise to the well-known phenomenon of haze formation [9].

Transition metal contaminations may affect the electrical properties of silicon materials in different ways. For illustration, let us again consider the cases of Fe and Ni in silicon in the absence of extended defects, which may serve as examples for isolated and pecipitated metal impurities, respectively. Interstitial iron is known to introduce a deep donor level into the silicon band gap and acts as a lifetime killer in p-type material (for a detailed discussion, c.f. [3]). For modern p-type, as-grown Cz-Si for integrated

circuit applications, the minority carrier diffusion length is controlled by the amount of Fe contamination predominantly in the form of FeB pairs [10]. For Ni in Si, Electron Beam Induced Current (EBIC) investigations of structurally well-defined $NiSi_2$ precipitates exhibited extremely large EBIC contrasts of up to 40% proving these defects to be efficient recombination centers which may control the minority carrier diffusion length [11].

In contrast to single crystal FZ-Si and unprocessed Cz-Si, multicrystalline silicon (mc-Si) contains extended defects like grain boundaries, dislocations and microdefects ([12], [13]). There is now strong evidence that the electrical activity of these defects is related to transition metal decoration. Experimental and theoretical work show that the electrical activity of grain boundaries is due to impurity segregation and is not of intrinsic origin [14]. Extensive EBIC investigations indicate that dislocations in silicon intrinsically give rise to shallow levels, whereas deep levels controlling their recombination activity at room temperature result from transition metal contamination ([15]).

From the point of view of mc-Si materials for solar cell applications the effect of transition metals on the minority carrier diffusion length L_D is most important, and – as follows from the above considerations – is related to their distribution which in turn critically depends on the *density of extended defects* and the *cooling conditions* during crystal growth and processing. In a first set of experiments, we have studied the influence of different cooling conditions on the average diffusion length $\langle L_D \rangle$ of mc-Si materials after annealing at high temperatures. We show that fast quenching always results in a decrease of $\langle L_D \rangle$ by about one order of magnitude, whereas slow cooling only slightly reduces or even improves the minority carrier diffusion length. This behavior is attributed to the release of impurities from metal silicide precipitates during annealing leading to cooling rate dependent levels of accumulation at extended defects.

Gettering processes in mc-Si for solar cell applications must be operative at high temperatures, i.e. they must be segregation-induced or injection-induced following the classification scheme given in [2]. There are two gettering processes used in solar cell production, namely phosphorus diffusion gettering (PDG) and aluminium gettering (AlG) (for a more detailed discussion, see [16]) and recent theoretical work has been devoted to quantitatively simulate impurity redistribution during gettering [16],[17],[18],[19],[20]. Basically, there are two time scales involved in gettering kinetics, i.e. the formation of the gettering layer and the impurity transport from the bulk to the gettering region. For a given impurity, the latter depends on the amount of mobile and immobile species which for 3d transition elements are interstitial and precipitated metal atoms, respectively. In a second set of experiments, we have measured *in-situ* the outdiffusion of radioactive ^{57}Co from mc-Si during AlG. We find that the rate-limiting step is the dissolution of $CoSi_2$- precipitates and that AlG for long times still leaves contaminated regions in the bulk. Autoradiography shows the residual ^{57}Co to be located in 'bad regions' of the mc-Si materials.

2 Results and Discussion

2.1 Metal impurity redistribution during annealing and cooling

We used cast mc-Si of two different manufacturers, called material A and B. For each material and annealing temperature ($900°C$ and $1100°C$) we prepared three samples out of neighbouring wafers. Due to the directional solidification during crystal growth we obtained three samples with comparable grain structure and about the same local dislocation density which is sufficient for comparison of the L_D values measured in each of the three samples. All samples were polished and RCA cleaned [21]. One of the three samples was not annealed and used as reference sample. The second sample was annealed for $60min$ at $900°C$ or $45min$ at $1100°C$. The third sample was annealed and quenched in the same way, followed by annealing at the same temperature for $15min$ and subsequent slow cooling.

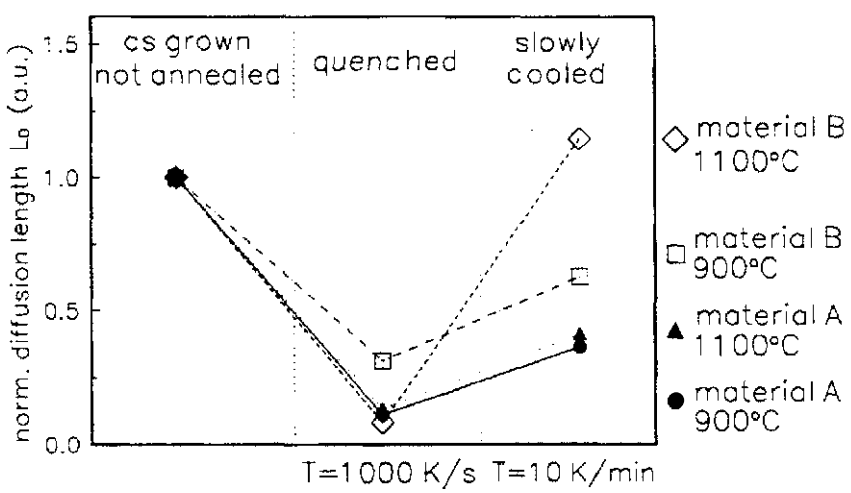


Fig. 2.1 *Averaged minority carrier diffusion lengths $\langle L_D \rangle$ for as-grown, quenched, and slowly cooled samples of different mc-Si materials (A and B) annealed at $900°C$ or $1100°C$. $\langle L_D \rangle$ values are normalized with respect to the as-grown material.*

Minority carrier diffusion lengths were measured by means of the Spectral Response method which utilizes the wavelength dependend absorption coefficient of light in Si [22]. The used light spot was $1mm$ in diameter. On each sample L_D was determined at 10 to 15 different positions which were the same on each of the three samples. The results of our measurements can be seen in Fig.2.1 [23]. The values there were obtained by averaging all L_D values of one sample and normalizing with respect to the as-grown

reference sample. As a result, high cooling rates lead to a dramatic reduction of $\langle L_D \rangle$ by a factor of up to 12 with respect to the reference material. In contrast, cooling down slowly reduces $\langle L_D \rangle$ by a factor of 2.8 at maximum or even leads to a slight *increase* with respect to the reference material. In all cases, $\langle L_D \rangle$ is at least a factor of two higher after slow cooling compared to fast cooling.

We interprete these results in terms of a redistribution of fast diffusing metal impurities which exist in the as-grown material in precipitates of low density with negligible influence on L_D. Annealing leads to dissolution of those precipitates and after quenching the impurities accumulate at extended defects or form small precipitates with high density due to a high supersaturation and the short time during the cooling period. In contrast, slow cooling again leads to a small density of precipitates at those positions at extended defects or at the wafer surface which offer the strongest reduction of the nucleation barrier.

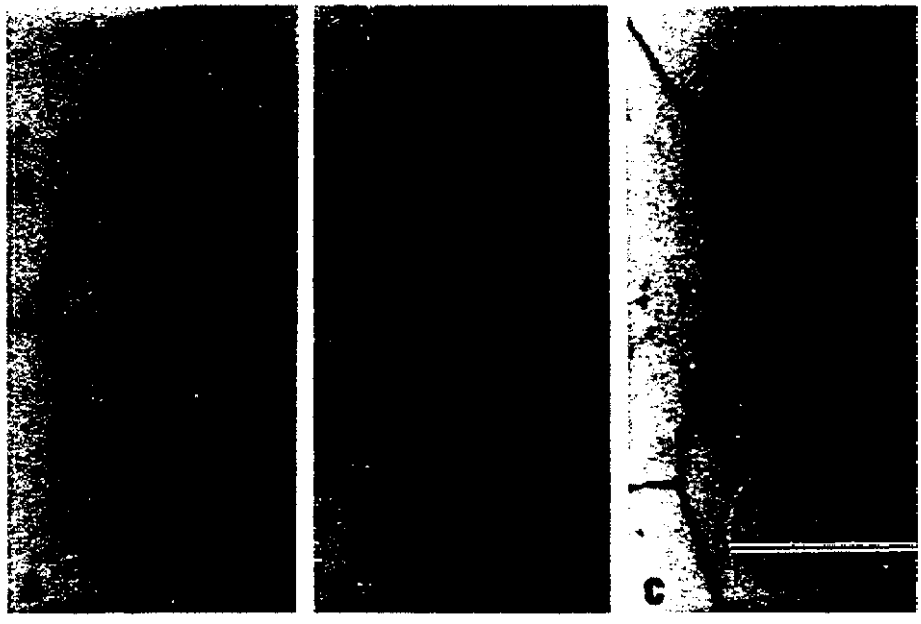


Fig. 2.2 : *EBIC images of the same parts of material B-samples (electron energy 30keV). (a) as-grown, not annealed; (b) annealed at 1100°C and quenched; (c) annealed at 1100°C and cooled down slowly. Dark areas represent regions of reduced current and therefore lower local L_D.*

This hypothesis is further supported by EBIC investigations of the same samples as shown in Fig.2.2 in the case of material B annealed at 1100°C. In EBIC dark regions mean regions of reduced short circuit current and therefore lower L_D. Fig.2.2 shows the same crystal regions in (a) the not annealed reference sample, (b) the annealed and quenched sample, and (c) the annealed and slowly cooled sample. In the as-grown

material there are partly recombination avtice grain boundaries and no EBIC contrasts within the grains. This picture changes fundamentally after annealing and quenching (Fig.2.2(b)). In addition to grain boundaries, we observe recombination active defects with a density of 10^3 up to $10^5 cm^{-2}$ within the grain. These contrasts are tentatively attributed to dislocations decorated with those impurities which were released from precipitates in the as-grown material during the annelaing step. Indeed, after cooling down the sample slowly all contrasts within the grains vanish. This means that different cooling conditions lead to defect configurations in mc-Si with different influence on the diffusion length L_D. Hence, in the case of mc-Si the cooling process can be understood as a kind of internal gettering with slow cooling selecting those heterogeneous nucleation centers which offer the highest reduction of the nucleation barrier.

2.2 Kinetics of Al-gettering of cobalt in mc-silicon

Phosphorus diffusion gettering and aluminum gettering (AlG) are widely used in solar cell manufacturing. From a physical point of view, AlG bases on the segregation induced mechanism [24], i.e. impurity redistribution is driven by an enhanced solubility of these atoms in the liquid Al:Si layer compared to the silicon bulk which leads to a flux of impurity atoms into the liquid layer.

We use AlG together with radioactive tracer methods for an *in-situ* observation of the redistribution of Co atoms during the gettering process. Together with results from Mössbauer spectroscopy and autoradiographic (AR) images we conclude that the dissolution process of the $CoSi_2$ precipitates determines the redistribution kinetics and also the finally achieved gettering efficiency.

Before presenting the results, we briefly describe the experimental procedure and the numerical model used for simulations.

The nuclear transitions $^{57}Co \xrightarrow{270d} {}^{57}Fe^* \xrightarrow{98ns} {}^{57}Fe$ ($^{57}Fe^*$: excited state of ^{57}Fe) lead to photon emission at energies of 123 keV, 14.4 keV, and 6.4 keV, whose absorption coefficients λ_E in silicon are 0.038 mm^{-1}, 2.65 mm^{-1}, and 28.0 mm^{-1}, respectively. The measured intensities I_E of each radiation are proportional to:

$$I_E \sim \int_{x=0}^{x=d} c(x,t) \cdot \exp(-\lambda_E x) dx, \tag{1}$$

where d denotes the sample thickness and c(x,t) the depth profile of radioactive tracers in the sample. Due to the small absorption coefficient one can determine the average concentration of Co in the specimen from the intensity of the 123 keV-radiation, I123, whereas I6 and the ratio I6/I14 contains information about the depth distribution of the Co atom [25]. In our experimental setup we can simultaneously measure both intensities – I6 and I14 – which allows to calculate the Co distribution *at gettering temperature* with a time resolution of about 30s.

Eqn.1 can be evaluated by comparing the measured intensity with simulated $c(x,t)$. In this work, we calculate the evolution of $c(x,t)$ with the following one dimensional model which contains diffusion of the mobile interstitial species with concentration c_i and a reaction term describing the dissolution of $CoSi_2$ precipitates containig Co atoms corresponding to a concentration c_p.

$$\frac{\partial c_i(x,t)}{\partial t} = D_i \frac{\partial^2 c_i(x,t)}{\partial x^2} - \frac{\partial c_p(x,t)}{\partial t} \tag{2}$$

$$\frac{\partial c_p(x,t)}{\partial t} = k \cdot c_p(x,t)^{2/3}(c_i(x,t)) - c_i^{eq}) \tag{3}$$

The boundary condition at the Si–Al:Si ($x = 0$) interface is:

$$S \cdot c_i(x = 0, t) = c_{Al:Si}(t), \tag{4}$$

where $c_{Al:Si}(t)$ denotes the average Co concentration within the Al:Si layer and S the segregation coefficient. Eqn. 3 holds for spherical precipitates. Within this approximation the reaction parameter k depends on the density ρ_p of the precipitates and on the reaction barrier ΔH as

$$k \sim \rho_p^{1/3} \exp(-\Delta H / k_B T) \tag{5}$$

In this first approach, we assume the equilibrium concentration $c_i^{eq} = const$ to be independent from the size of the precipitates and also assume that the density ρ_p is constant. Furthermore, we start with $c_p(x, t = 0) = const$ as the initial concentration which is in accordance with measured I6/I14 ratios. By fitting the measured data we gain the model parameters e. g. k or the diffusion coefficient D_i [26].

The lateral ^{57}Co distribution were measured by autoradiographic images which are obtained simply by exposing X-ray film to the radiation leaving the ^{57}Co doped sample. The atomic configuration of the Co atoms, in our case $CoSi_2$ precipitates or CoB–pairs, were identified by Mössbauer spectroscopy.

The experiment were carried out as follows: samples were doped by in–diffusion of ^{57}Co followed by quenching ($\dot{T} \approx 500 K s^{-1}$) resulting in a uniform Co concentration of $1.7 \cdot 10^{14} cm^{-3}$ except for accumulations at grain boundaries which are estimated as $\approx$10% of the total amount. After chemical etching of a $60 \mu m$ thick layer to remove near–surface precipitates samples were annealed at 600°C for 1h in Ar atmosphere leading to a transformation of thermaly unstable Co–species like CoB–pairs and metastable $CoSi_2$- platelets into more stable $CoSi_2$ precipitates [27] but leaving the macroscopic Co distribution unaffected. Subsequently, a 130 nm thick Al film was evaporated on one side of the sample followed by the gettering anneal at 830°C for 150min. Finally, the Al:Si gettering layer was removed by chemical etching. By comparing the I123 intensities, we measured a gettering efficiency of $1 - \langle c(x, t = t_g) \rangle / \langle c(x, t = 0) \rangle = 0.93$.

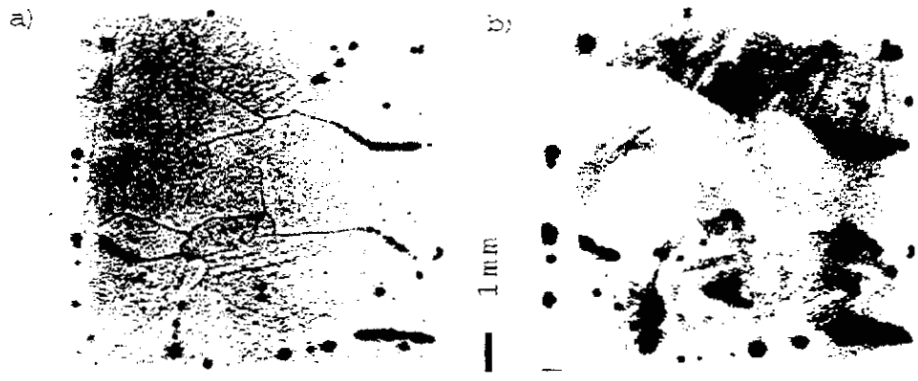


Fig. 2.4 : *Autoradiograhic images of the lateral Co distribution within the multicrystalline Si sample a) after preparation and b) after the AlG for 150min at 830°C and chemical removal of the Al:Si layer. Please notice the different exposure time: a) 4h and b) 24h which leads to broadening of the dark spots in Fig.2.4b*

be detected within the grains after Co diffusion and quenching (Fig.2.4a). Furthermore, a homogenous Co accumulation at grain boundaries is present. These grain boundaries are surrounded by a depleted zone ($< 150\mu m$) providing evidence for an accumulation during quenching. Another striking feature are the dark spots which are not surrounded by a depleted zone. This indicates growth at high temperature during Co indiffusion.

After AlG (Fig.2.4b) the residual Co distribution reveals concentration variations between neighbouring grains and at the grain boundaries. The vast majority of the dark spots remain stable during AlG. A rough estimation gives for the total Co concentration in this dark spots $8 \cdot 10^{12} cm^{-3}$. The Mössbauer spectrum taken from the sample after AlG is identical to the one from $CoSi_2$ platelets.

Obviously, there are some crystal features – grain boundaries and also defect configurations within some grains — which generates stable Co species. The concentration of this stable species determines the gettering efficiency. Structural investigations are needed to identify these 'bad regions' in mc-Si.

References

[1] E.R.Weber, *Appl.Phys.A* **30**, 1 (1983)

[2] W.Schröter, M.Seibt and D.Gilles, in: *Materials Science and Technology* **Vol.4**, R.W.Cahn, P.Haasen and E.J.Kramer (eds), W.Schröter (vol.editor), (VCH Weinheim, 1991), p.539

[21] W. Kern und D.A. Puotinen, RCA Review **31** (1970)187

[22] J.W. Orton und P. Blood, *The Electrical Characterisation of Semiconductors: Measurement of Minority Carrier Properties*, vol. 13, series *Techniques of Physics*, Academic Press, London 1990

[23] I. Hanke, M. Apel and W. Schröter, to be publ.

[24] M.Apel, I.Hanke, R.Schindler, and W.Schröter, *J. Appl. Phys.* **76** (7), 4432 (1994)

[25] W.Bergholz, *Physica* **116B**, 312 (1983)

[26] It should be noted that, apart from simulations, I6 can be directly interpreted as proportional to the amount of gettered ^{57}Co if the latter exceeds the amount of Co in a 50μm thick layer below the surface.

[27] J.Utzig, *J.Appl.Phys.* **64**, 3629 (1988)

[28] J.Utzig and D.Gilles, *Materials Science Forum* **Vol.39-41**, 729 (1989)

[29] M.Apel, I.Hanke, and W.Schröter, to be published

[3] K.Graff, *Metal impurities in silicon-device fabrication* , (Springer Series in Materials Science **Vol.24**) (1995)

[4] H.Feichtinger, in:*Materials Science and Technology* **Vol.4**, R.W.Cahn, P.Haasen and E.J.Kramer (eds), W.Schröter (vol.editor), (VCH Weinheim, 1991), p.185

[5] For Co in Si high B-doping leads to CoB pair formation in FZ-Si whereas precipitation at extended defects is observed in processed Cz-Si [6]

[6] H.Ewe, D.Gilles, S.K.Hahn, M.Seibt, and W.Schröter, in: *Semiconductor Silicon 1994* H.R.Huff, W.Bergholz, and K.Sumino (eds.) (The Electrochem.Soc., Pennington 1994), p.796

[7] M.Seibt and W.Schröter, *Phil.Mag.A***59** 337 (1989)

[8] F.Riedel, J.Kronewitz, U.Gnauert, M.Seibt, and W.Schröter, *Solid State Phenomena***47-48** 359 (1995)

[9] M.Seibt and K.Graff, *J.appl.Phys.***63**, 4444 (1988)

[10] R.Falster and D.Gambaro, *Solid State Phenomena***32-33** 359 (1993)

[11] M.Kittler, J.Lärz, W.Seifert, M.Seibt, and W.Schröter, *Appl.Phys.Lett.*58 911 (1991)

[12] H.J. Möller, Solid State Phen. **47-48**, 127 (1996)

[13] J. Bailey and E.R. Weber, phys.stat.sol.(a) **137**, 515 (1993)

[14] J.Thibault, J.L.Rouviere, and A.Bourret, in: *Materials Science and Technology* **Vol.4**, R.W.Cahn, P.Haasen and E.J.Kramer (eds), W.Schröter (vol.editor), (VCH Weinheim, 1991), p.322

[15] M. Kittler and W. Seifert, *Mat.Sci.Forum***196-201** 1123 (1995)

[16] T.Y.Tan, R.Gafiteanu, and U.Gösele, this volume

[17] W.Schröter, E.Spiecker, and M.Apel, *Fifth Workshop on the Role of Impurities and Defects in Silicon Device Processing 1995*,p.85

[18] T.Y.Tan, R.Gafiteanu, and U.Gösele, ibid, p.93

[19] E.Spiecker, M.Seibt, and W.Schröter, submitted for publication

[20] T.Y.Tan, R.Gafiteanu, and U.Gösele, in: *Semiconductor Silicon 1994*, H.R.Huff, W.Bergholz,and K.Sumino (eds.) (The Electrochem.Soc., Pennington 1994), p.920

High-Efficiency Cell Fabrication on Low-Defect Density Materials

A. Rohatgi and S. Narasimha
University Center of Excellence in Photovoltaic Research and Education
Georgia Institute of Technology, Atlanta, GA. 30332-0250

Section I. *Introduction*

Low-cost and high-efficiency are the keys to large scale acceptability of PV systems. However, no material or technology has yet achieved the cost and efficiency targets simultaneously to make PV attractive for peek shaving or utility scale applications. Silicon is a strong contender because it has the advantage of a huge technology base and a proven track record. Almost 80% of the PV modules shipped today are made from crystalline silicon. However, today's crystalline silicon modules are somewhat expensive because of the high cost of materials and manufacturing. Moreover, the production cell efficiencies are generally less than 15%. Silicon cells can become more cost-effective by developing manufacturable, high-efficiency processes for low defect density (LDD) materials and by engineering these processes so that their throughput capacity is increased. The objective of this paper is three-fold: 1) to describe the role of defects in LDD materials, 2) to review the quality enhancement techniques used to mitigate the impact of these defects, and 3) to discuss the integration of these techniques to achieve high efficiency solar cells on LDD materials.

1.1. *Role of Defects in Low Defect Density Silicon Materials*

LDD silicon includes a broad class of photovoltaic materials. Essentially, this category includes any material which can be grown in a cost-effective manner and sustain high-efficiency devices. Growth methods for these materials generally fall into three categories: cast ingot, ribbon, and LPE or CVD based films. Even though these growth techniques have been improved over the years, they are still the source of most of the performance limiting defects contained in the finished solar cells. In general, these defects can be classified as impurities/point defects, precipitates, and extended defects. The major impurities in LDD silicon are carbon, oxygen, and the various transition metals. Common precipitates (material clusters which are not chemically bonded to the rest of the lattice) include SiO_x or SiC inclusions. A large precipitate density can degrade materials in two ways. First, stress induced by precipitates can generate harmful extended defects like stacking faults and dislocations. Secondly, precipitates decorated with metallic impurities can drastically reduce carrier lifetime in silicon. The most common type of extended defects in LDD materials are dislocations and grain boundaries. Dislocations are usually the result of stresses experienced during the material growth process. Grain sizes in LDD mc-Si generally range from 1.0 mm^2 to 1.0 cm^2. Table 1 lists features of certain LDD silicon materials which are currently being used for photovoltaic applications. Before discussing high efficiency cell fabrication on LDD material, a brief review of the major defects present in these materials and their influence on carrier lifetime will be given.

Table 1. Some low defect density materials and their characteristics.

Material/ References	Thickness (μm)	Resistivity (Ω-cm)	Dislocations (cm^{-3})	Carbon (cm^{-3})	Oxygen (cm^{-3})	Metals (cm^{-3})	Lab Eff. (%)
CZ	200 to 400	1-3 p-type	500 avg	0.5e17 to 2.5e17	0.1e18 to 2e18	1e10 to 1e14	21.7%
Cast mc-Si (HEM)	300	0.8 to 1.5 p-type	1e6 max 1e5 avg	< 5e17	< 2.5e17	1e12 (Fe, Cr)	18.6%
Cast mc-Si (Solarex)	300	1 to 1.5 p-type	1e4 to 1e5	3.5e16 to 4.2e17	2.5e17 to 1.2e18	equal to CZ levels	17.2%
Ribbon (EFG)	300	1-2 p-type	1e6 max	1e18	2.4e17 to 4e17	1e15	15.0%
Ribbon (String)	300	1-3 p-type	5e5 avg	3.5e17 to 4.5e17	< 5e16	below detection	14.5%
Ribbon (D-web)	100	10-50 n-type	1e4 avg	below detection	1e18	below detection	17.3%
Silicon Film™ (AstroPower)	100	1-3 p-type	1e4 to 1e5	2e17 to 7e17	1e17 to 8e17	not available	13.8%

1.2. *Transition Metals*

Transition metals can be found in most LDD materials either dissolved in silicon or in precipitate form. For example, Cu and Ni exist almost exclusively in precipitate form. Significant concentrations of Fe and Cr can be found dissolved in interstitial positions in the silicon lattice, whereas impurities like Au and Pt are typically found in substitutional sites. Harmful transition metals generally give rise to specific DLTS spectra. Davis et. al. found threshold concentrations of transition metals in silicon above which solar cell performance begins to degrade due to lifetime reduction [1]. Fig. 1 shows the impact of several transition metals on the performance of CZ silicon solar cells. DLTS was used to determine the activity coefficients and energy levels of each species. Fig. 1 indicates that impurities like Cu, Ni, and Al can be tolerated in concentrations near 1e15 cm^{-3} before degrading device performance. Other metals, like Ti, have degradation threshold concentrations of only 3e11 cm^{-3} and can reduce cell performance by 50% at concentrations of 1e14 cm^{-3}. Therefore, gettering of transition metals is vital for improving the performance of cells fabricated on LDD materials.

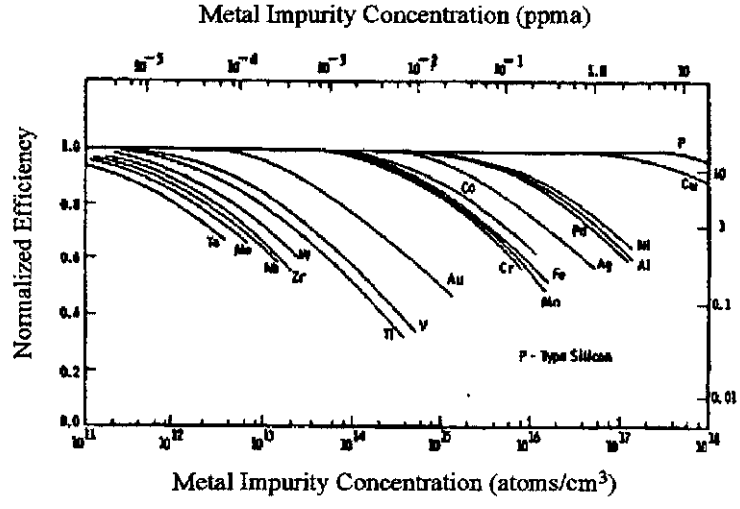


Fig. 1. The effects of transition metals on solar cell performance [1].

1.3. *Oxygen and Carbon*

Significant quantities of oxygen can be found in most LDD solar cell materials. The effects of oxygen on device performance are quite complex, mainly because it can exist in multiple configurations in silicon. Oxygen can be found dissolved in interstitial sites in the lattice, precipitated as SiO_2 (or other SiO_x complexes), behaving as a thermal donor, or interacting with point defects to form vacancy-oxygen complexes. Sopori has shown that when interstitial oxygen concentrations below 5e17 cm^{-3} are measured by FTIR, the amount of precipitated oxygen in the material is small and does not have an appreciable effect on solar cell performance. When interstitial oxygen concentrations exceed 5e17 cm^{-3}, oxygen precipitates form [2]. These precipitates can, in turn, generate dislocations and stacking faults in the material which can severely degrade device performance, especially if they become decorated with metallic impurities. Pang et. al. have shown that increased oxygen concentration in the range of 5-15 ppma results in process-induced degradation of lifetime in silicon [3]. Their experimental findings are shown in Fig. 2. Oxygen is also known to segregate to regions of extended defects (dislocations or grain boundaries).

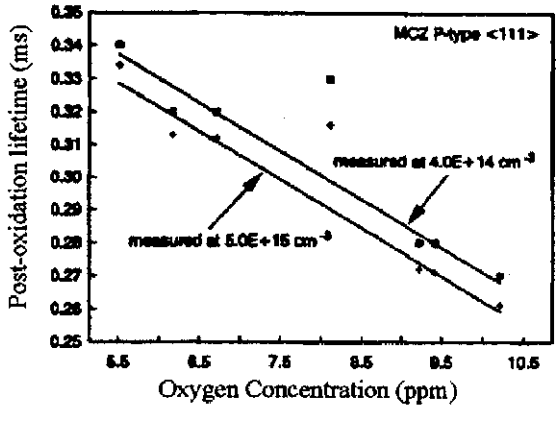


Fig. 2. The relationship between oxygen concentration and the processed lifetime in silicon [3].

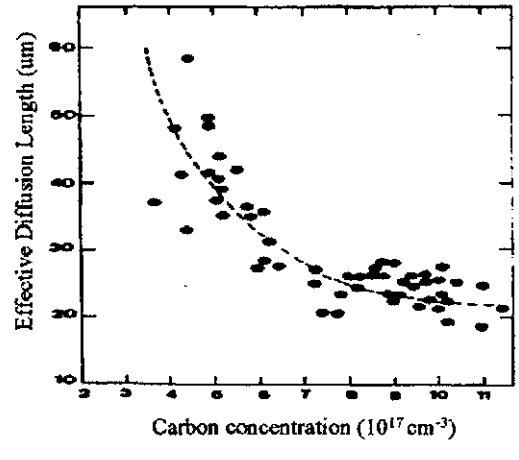


Fig. 3. Variation in L_{eff} with increasing carbon concentration [4].

Carbon is electrically inactive when dissolved in moderate quantities at substitutional positions in the silicon lattice. However, excessive concentrations of carbon in the material can influence the formation of extended defects. Ammor et. al. have shown that carbon concentrations in cast mc-Si have a direct effect on material parameters such as precipitate size and density, grain boundary size, and dislocation density [4]. Increasing the carbon concentrations above 2e17 cm^{-3} monotonically degrades the bulk diffusion length (Fig. 3) and lowers the solar cell performance.

1.4. *Dislocations and Grain Boundaries*

Extended defects in silicon are defined as long range structural disruptions in the lattice periodicity. This loss of periodicity results in a local collapse in the energy band structure which leads to a continuum of energy states within the forbidden gap. It is this distribution of energy states (DOS) which determines the electrical activity of the extended defects. The DOS varies with the type of extended defect (dislocations, grain boundaries, stacking faults, etc.), and with the impurities (transition metals, SiO_x or SiC precipitates) which decorate the extended defects. In their study of dislocation effects on solar cell performance, Ghitani and Martinuzzi were able to correlate increased dislocation density in Wacker mc-Si to a reduction in photocurrent (Fig. 4) [5]. Comparison to theoretical calculations showed that recombination velocities at the dislocations were approximately 1e4 cm/s.

Impurity segregation to extended defects largely determines the recombination at these defects. In general, metal segregation to extended defects, such as dislocations, is deleterious to solar cell performance. However, a moderate amount of oxygen segregation to grain boundaries can result in reduced recombination when compared to grain boundaries in oxygen-lean materials. Evidence of this is shown by an EBIC study of EFG material (Fig. 5) conducted by Doolittle [6]. The improvement due to oxygen content is attributed to the modification of the DOS to a parabolic profile, which has a lower density of states near midgap than uniform or Gaussian DOS profiles.

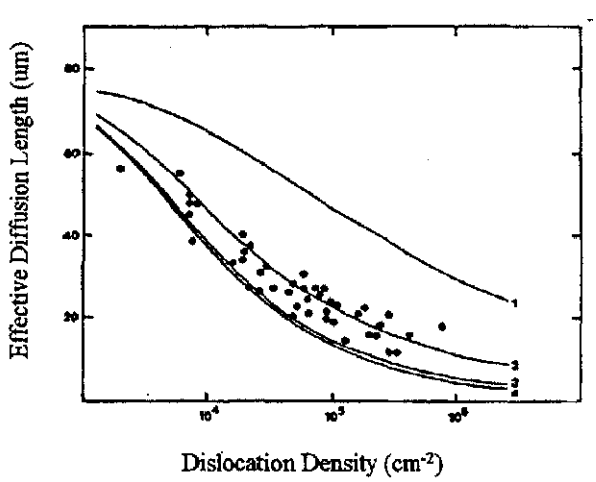


Fig. 4. L_{eff} versus dislocation density and dislocation recombination velocity [5].

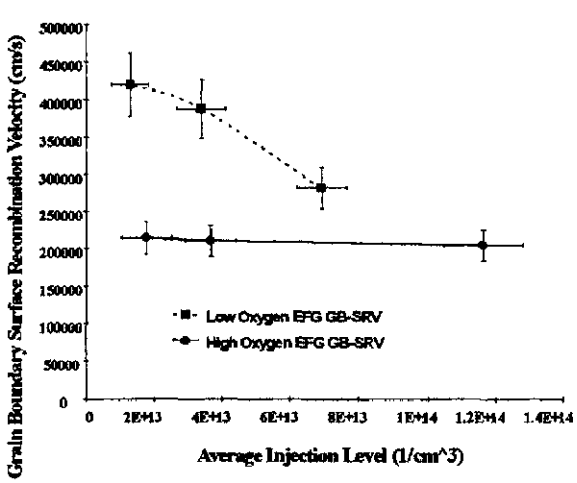


Fig. 5. Grain boundary recombination velocity versus injection level for low and high oxygen concentration materials [6].

Section II. *Quality Enhancement Techniques for LDD Materials*

2.1. *Gettering and Bulk Passivation*

The as-grown lifetimes in low defect density silicon materials can generally be improved by process induced gettering or passivation. Gettering is the process by which impurities are removed from the device active area to a gettering region. Passivation is the process by which electrically active trap states in the silicon bandgap are rendered inactive. Gettering can be accomplished by a number of techniques which include dopant diffusion, metal film deposition, mechanical damage, chlorine oxidation, or laser damage. In solar cell fabrication sequences, the most viable forms of gettering are phosphorus diffusion gettering (PDG) and backside aluminum

gettering. Bulk passivation of defects in silicon can be accomplished with hydrogen treatments. The most common methods of hydrogenation are via PECVD coatings, annealing in a forming gas ambient, or exposure to high-energy hydrogen plasmas.

2.1.1. *Phosphorus Diffusion Gettering*

The mechanisms behind PDG have been investigated at length in the literature. The general consensus is that PDG is due to impurity segregation from bulk silicon to the phosphorus diffused region [7]. In the event that the impurity occupies a low-mobility, substitutional site, the injection of silicon-self interstitials (SSI) during phosphorus diffusion enhances gettering through the "kick-out" mechanism [8]. A number of investigators have reported the effects of PDG on specific metallic impurities. Kang and Schroder showed that optimum phosphorus gettering temperatures usually exist for transition metals like Au, Cu, Fe, and Ni [7]. Rohatgi et. al. used DLTS analysis to show that PDG can effectively getter fast-diffusing impurities like Cr, but is less effective in removing slow diffusers like Ti, V, and Mo [9]. The results of this work are shown in Fig. 6. The injection of SSI during PDG has been shown to aid in the gettering of Au [8] and Pt [10].

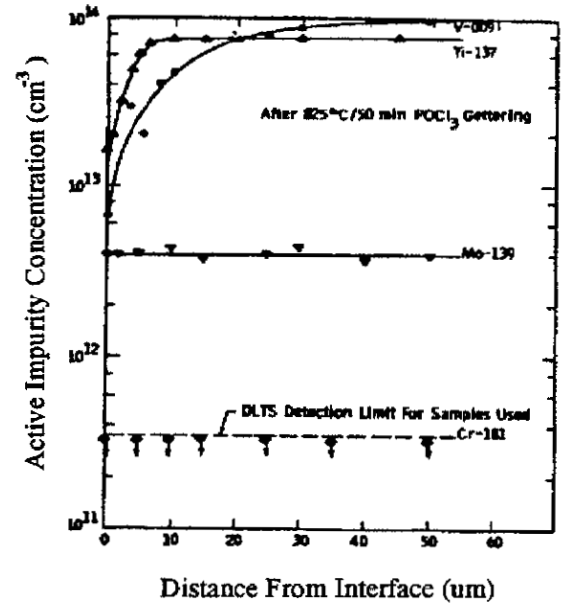


Fig. 6. Electrically active impurity profiles for certain species after PDG [9].

Typical solar cell processes employ some sort of PDG. There is generally an optimum gettering temperature for LDD materials because of the tradeoff between increased gettering efficiency and the formation of lifetime limiting defects and complexes as the gettering temperature is increased. As an example, an optimal PDG treatment at 900°C for 30 minutes on HEM material resulted in the fabrication of the record high 18.6% efficient small area mc-Si solar cell [11]. The bulk lifetime was observed to increase from 10 μs to the range between 35-135 μs at this temperature. However, at temperatures above 900°C, lifetime degradation was observed in the bulk material. Because the gettering time used was relatively short, it is evident that the primary impurities in the as-grown HEM are fast diffusing metallic species. Narayanan et. al. attributed a 1% (absolute) increase in the solar cell efficiency of 0.7 Ω-cm Wacker mc-Si to PDG [12].

Although 30 minutes to 1 hour is short on a gettering time scale, it is excessively long from the standpoint of high-throughput processing. Moreover, lengthy PDG necessitates either etching away and re-diffusing the phosphorus emitter or etching the emitter back to a reasonable sheet resistance in order to avoid heavy doping effects. The feasibility of these long, additional steps in high-volume processing is presently questionable. Therefore, there is a need to develop rapid gettering techniques for LDD materials.

2.1.2. *Aluminum Gettering*

Numerous effects of aluminum on photovoltaic materials and devices have been observed over the years. Among these, the most important are aluminum gettering and aluminum BSF formation. The latter will be discussed in the section concerning surface treatments.

Aluminum gettering is typically carried out by applying a layer of aluminum onto a silicon wafer (by evaporation or screen-printing) and then annealing at elevated temperatures. Below the Al-Si eutectic temperature (577°C), the solubility of certain metals in aluminum can be quite high (1 at. %), allowing for effective low temperature aluminum gettering [13]. Thompson and Tu showed that Cu, which is a fast diffusing impurity in silicon (D@540°C = 9.1×10^{-6}), can be effectively gettered by aluminum at 540°C [14]. However, at low temperatures, slow diffusing substitutional impurities like Au are difficult to remove as the gettering process becomes release/diffusion limited. This is because, unlike PDG, aluminum gettering does not generate SSI which cause the kick-out of slow diffusing, substitutional impurities.

At temperatures above the Al-Si eutectic, an Al-Si liquid alloy forms. The segregation coefficient for impurities between the liquid alloy and solid Si can be on the order of 10^4 [13]. This provides an excellent segregation potential for metallic impurities into the gettering region. Sundaresan et. al. have shown that high temperature aluminum alloying can raise the intragrain diffusion lengths in mc-Si material. They concluded that an aluminum gettering process at 800°C for 1 hour reduced the intragrain defect density by an order of magnitude in cast Wacker mc-Si material [15]. Fig. 7 shows that at high temperatures, aluminum treatments can getter slow diffusing species like V. Rohatgi et. al. have shown that high temperature aluminum gettering (850°C for 35 minutes) can increase the cell performance of small area OTC and EFG solar cells by 1-2% (absolute) [16].

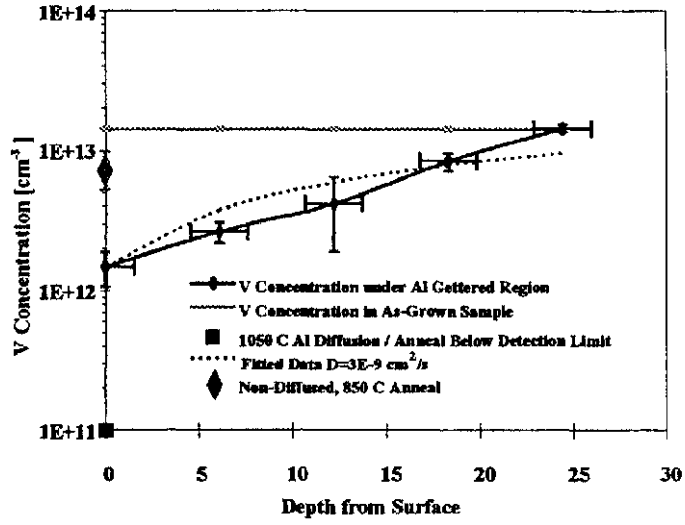


Fig. 7. Aluminum gettering effectiveness of slow-diffusing Vanadium [6].

The effect of aluminum gettering on dislocated silicon has also been the subject of investigation. Martinuzzi et. al. have shown that low temperature aluminum treatments in cast mc-Si materials can increase minority carrier diffusion lengths in regions where dislocation densities are between $1x10^4$-$5x10^5$ cm^{-2} [17]. The authors postulated that the gettering was accomplished by the enhanced diffusion of the decorating impurities (iron or oxygen) along the dislocation paths. Rohatgi et. al. have also shown that aluminum gettering effectiveness is increased in the presence of modest dislocation densities [16]. However, in regions where the dislocation density approaches or exceeds 10^6 cm^{-2}, Sopori et. al. have shown evidence that aluminum, phosphorus, and chlorine gettering are all ineffective in improving the material quality [18]. In their experiments, cast mc-Si materials with iron and chromium concentrations between 10^{11} cm^{-3} and 10^{12} cm^{-3}, were gettered using aluminum at temperatures between 700-900°C. Gettering treatments increased the minority carrier diffusion length in low-defect, intragrain regions of the material but not in highly dislocated regions.

2.1.3. *Hydrogen Passivation*

The isoelectronic structure and highly reactive nature of hydrogen have proved very useful for passivating defects in silicon. However, the degree of passivation can be quite material-specific. Although much is still not understood about the interaction of hydrogen with silicon and its defects, recent extensive model calculations by Estreicher [19] have led to the understanding of three stable states of hydrogen in silicon: 1) trapped at dangling bonds, 2) existing in molecular form, and 3) unbound in atomic form [20].

Hydrogen can be effectively introduced as part of the solar cell processing sequence via PECVD deposition of anti-reflection coatings. These coatings have proven to be effective in passivating bulk and extended defects. Fig. 8 shows the results of a study on EFG ribbon silicon in which the application of a PECVD SiN layer, followed by a low temperature anneal using a tungsten-halogen light source, effectively passivated intragrain defects in the material [6]. This is evident from the increased EBIC response after the hydrogen treatment.

Rohatgi et. al. attributed a 2.6% (absolute) increase in the efficiency of small area EFG solar cells to a forming gas anneal at 400°C. A further improvement of 1.2% (absolute) due to the forming gas anneal in the presence of aluminum was observed [16]. It was concluded from IQE

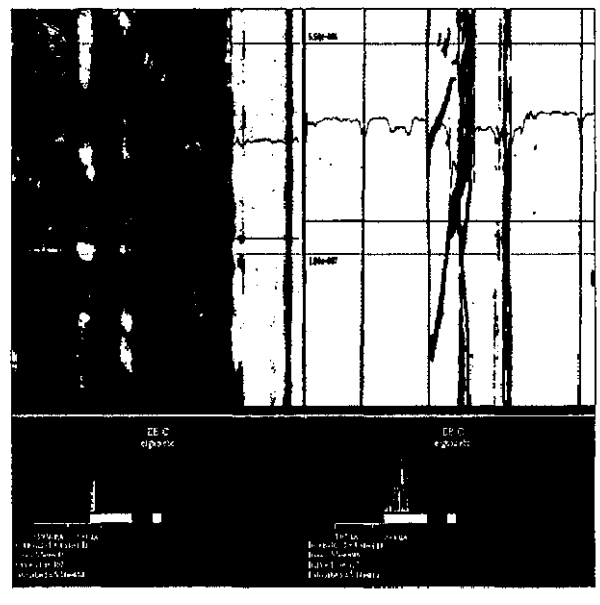


Fig. 8. Bulk and extended defect passivation by PECVD/RTA treatment [6].

measurements that the efficiency improvements were caused by hydrogen bulk passivation of defects in the material.

Elgamel et. al. attributed an efficiency improvement of 0.7% and 1.7% (absolute) on Eurosolare mc-Si and Sitix-EMC, respectively, to a backside RF hydrogen plasma treatment. An additional gain of 0.4% in both cases was observed after exposing the front faces of the samples to a microwave-induced remote plasma source [21]. It was observed that remote plasma treatments do not damage the silicon surface, which is often the concern when using direct plasma sources.

2.2. *Surface Treatments for High-Efficiency LDD Cells*

In addition to the bulk quality enhancement, surface recombination velocity (S) must also be reduced for achieving high efficiency cells on LDD materials. Some of the most effective techniques for reducing S are discussed below.

2.2.1. *Thermal Oxide Passivation*

Emitter passivation by thermal oxidation is one of the most widely used passivation schemes in high-efficiency solar cell fabrication sequences. As will be pointed out in Section IV, the most efficient mc-Si cells reported to date implement this particular method of emitter passivation. The passivating quality of thermal oxides is largely dependent on the doping concentration of the underlying silicon surface. Cuevas et. al. determined the following empirical relationship between the surface recombination velocity for oxide passivated n^+ emitters as a function of surface doping concentration:

$$S = S_O \quad \text{for } N_D < N_{ref}, \qquad (1)$$

$$S = S_O\left(\frac{N_D}{N_{ref}}\right) \quad \text{for } N_D > N_{ref}$$

where S_O=70 cm/s and N_{ref}=7e17 cm^{-3} [22]. Eades and Swanson showed that the surface recombination velocities of p-type substrates with thermal oxide passivation are one to two orders of magnitude higher than those of n-type substrates [23]. This variation was attributed to the difference in the capture cross section of holes and electrons at the surface. Using Equation 1 in conjunction with PC-1D model calculations, we have found that front oxide passivation can account for a 0.9-1.1% (absolute) increase in efficiency for devices with 100 Ω/sq. emitters and surface concentrations of 5e19 cm^{-3}. This is fairly consistent with studies on OTC mc-Si in which a 1% (absolute) increase in efficiency was attributed to emitter passivation by thermal oxide [24].

2.2.2. *Surface Passivation by PECVD Films*

Passivation by PECVD films has proven to be an attractive alternative to thermal oxide passivation since it can be accomplished at low temperatures. SiN or SiO_2 films have been shown to provide effective emitter passivation on solar cells. PECVD SiN passivation gives about a factor of two higher J_{oe} compared to emitter passivation by thermal oxide. J_{oe} values in the range of 100-200 fA/cm^2 have been achieved for 100 Ω/sq. emitters passivated with SiN films, a reduction of a factor of five in J_{oe} compared to unpassivated emitters. [25]. An added advantage of SiN passivation is that it can also act as an AR coating for silicon solar cells [26].

Besides emitter passivation, PECVD films can be effective in passivating the undiffused back surface of a solar cell. Chen et. al. have measured surface recombination velocities as low as 2 cm/s on high-resistivity (> 500 Ω-cm) n-type silicon passivated with direct PEVCD SiO_2 coatings [27]. Recently, Schmidt et. al. reported surface recombination velocities as low as 4 cm/s on 1.5 Ω-cm silicon resulting from remote PECVD SiN passivation [28].

2.2.3. *Back Surface Fields*

When minority carrier diffusion lengths exceed half the wafer thickness, recombination losses at the back surface begin to limit the solar cell performance The most practical way to reduce the recombination velocity at the rear of the device (S_b) is to implement a back surface field (BSF) structure (high-low junction). A BSF provides a potential barrier for minority carriers such that they are repelled from the back surface of a device. In

the case of p-type substrates, BSFs are formed by aluminum alloyed regions or by boron diffused junctions. In the case of n-type substrates, BSF junctions are typically formed by phosphorus diffused regions. The attractive feature of aluminum alloyed BSFs (Al-BSFs) is that they can be realized at low temperatures in short firing times, whereas effective boron BSFs require high process temperatures and extended diffusion times. Furthermore, it has been shown that thick Al-BSFs (which can result from implementing screen-printing technology) can provide better BSF action than ideal boron BSFs [29]. Lolgen et. al. measured S_{eff} values as low as 200 cm/s resulting from screen-printed Al-BSFs formed on 3 Ω-cm CZ material [30]. Other studies on EFG mc-Si [31] and CZ [32] have also shown the beneficial effects of screen printed Al-BSFs on device performance.

2.3. *Surface Texturing*

Surface texturing is a commonly implemented method of improving solar cell performance. Texturing serves three primary purposes. First, it reduces the front surface reflectance by promoting multiple bounces. Second, texturing can increase the path length of the light through the device. This improves the collection efficiency of carriers generated by the absorbed light. Third, textured front surfaces can trap the light reflected from the back surface by the process of total internal reflection. This feature becomes significant for thin substrates.

Surface texturization can be accomplished in a number of ways, some of which have been reviewed by Green and Campbell [33]. Inverted pyramid structures defined on (100) silicon can provide very low reflectance surfaces. However, the process of forming inverted pyramids is slow and tedious because of the photolithographic steps required. Random pyramids can be realized on (100) surfaces by using an anisotropic etch. This process is quite simple and is currently being implemented by certain manufacturers who use single crystalline CZ as their basic substrate [34]. Anisotropic etching is not as effective in texturing mc-Si materials which exhibit different crystollographic orientations in different grains. For such materials, mechanical texturing by V-grooving has proven to be quite useful. The improvements in cell efficiency afforded by the different texturing geometries have been calculated by Smith and Rohatgi using a Monte Carlo based numerical technique [35].

Experimentally, Nunoi et. al. showed that implementing a V-groove texturing scheme on cast mc-Si material can improve the efficiency of large area solar cells by 1% (absolute) over non-grooved cells (from 14.5% to 15.5%) [36]. Similar results have been reported by Fath et. al. who measured a 1.1% (absolute) increase in 100 cm^2, V-grooved mc-Si solar cells over identically processed devices without mechanical texturing (14.1% to 15.2%) [37].

Section III. *High-Throughput Processes for LDD Solar Cells*

3.1. *RTP versus Conventional Furnace Processing*

The emitter diffusion steps are usually the most severe bottleneck for high-throughput solar cell fabrication. Rapid thermal processing (RTP) provides an attractive alternative to conventional furnace processing (CFP) because emitters and BSFs can be formed in a matter of seconds as opposed to hours. The resulting RTP junctions usually exhibit higher surface concentrations (heavy doping effects) and shallower junction depths (shunting problems) than CFP junctions. Another drawback of RTP sequences is the difficulty of growing a rapid, high-quality passivating oxide on the emitter. Experimental work by Rohatgi et. al. has shown that efficiencies of RTP cells are roughly 1.5-2.0% (absolute) lower than CFP cells fabricated on 0.2 Ω-cm FZ [38]. The difference was largely attributed to heavy doping effects in the emitter and the difference in surface passivation quality. Research is in progress to improve the RTP emitters and the quality of rapidly grown thermal oxides to bridge the gap between RTP and CFP cells.

As discussed in Section 2.1, most mc-Si materials need to be effectively gettered in order to maximize cell efficiency. Sparks et. al. showed that rapid thermal anneal cycles using tungsten-halogen lamps can provide the activation energy necessary to getter certain metallic impurities [39]. However, incomplete phosphorus or aluminum gettering could be of some concern due to short RTP temperature cycles. Also, inherent to RTP processing is the fast temperature ramp-up and cooldown rates. While these rates have little effect on FZ materials, they can adversely affect some LDD materials by quenching in defects. Considerable research needs to be done in this area to optimize RTP for appropriate emitter formation and effective gettering in LDD materials.

Doshi et. al. have demonstrated high-efficiency RTP cells of 17.1%, 16.4%, and 14.8% on FZ, CZ, and mc-Si, respectively [40]. Recently, RTP has been effectively used in the fabrication of p^+nn^+ solar cells on dendritic

web silicon. Efficiencies as high as 17.3% have been reported for devices in which the emitter and BSF junctions were both formed simultaneously during a single RTP diffusion cycle. Analysis of the 17.3% cell revealed that the efficiency result was due to a combination of high bulk lifetime in the thin substrate (>100 μs for 100 μm material) and effective BSF action from the n^+n phosphorus diffused BSF (10 cm/s on 10 Ω-cm material).

3.2. *Screen-Printed Contacts*

Even though the best silicon solar cells to date have been made using photolithography (PL) contacts, a production line must implement screen-printing (SP), or some equivalent technology, in order to accomplish high-throughput processing. The use of SP makes it necessary to change certain aspects of device fabrication. First of all, in order to minimize the contact resistance, the n^+ emitter region must be doped more heavily for SP contacts (40 Ω/sq.) than for PL contacts (100 Ω/sq.). Secondly, SP contacts generally provide more shading than PL contacts. Finally, the resistive losses in SP contacts are generally higher than those in PL metallization. Analysis by Doshi et. al. has shown that the combination of these loss mechanisms leads to 1.5-2.0% (absolute) difference between PL and SP cells [41]. SP technology needs to be improved to the point where fine-line printing (< 60 μm feature size) can be achieved. Furthermore, selective emitters, with heavy doping beneath the gridlines and lighter doping in the field regions, must be implemented in order to maximize the efficiency of SP solar cells. In spite of some of the current drawbacks of RTP and SP, efficiencies approaching 16% have been achieved on CZ silicon by integrating these two techniques into one fabrication process [41].

Section IV. *High-Efficiency Solar Cells on LDD Materials*

4.1. *Progress in mc-Si Solar Cell Efficiency (1976-1996)*

Mc-Si solar cell efficiencies have increased steadily over the past 20 years. These gains have been brought about by improved material quality and improved material processing. In Fig. 9, the efficiency progress for mc-Si solar cells is shown over time. In order to place the results in perspective, the efficiencies are divided into three categories: small area cells, large area cells, and very large area cells. The highest reported efficiencies in these categories are 18.6%, 17.2%, and 16.4%, respectively. Process sequences employed in the fabrication of these devices will be discussed in order to highlight the steps most critical in achieving high efficiency.

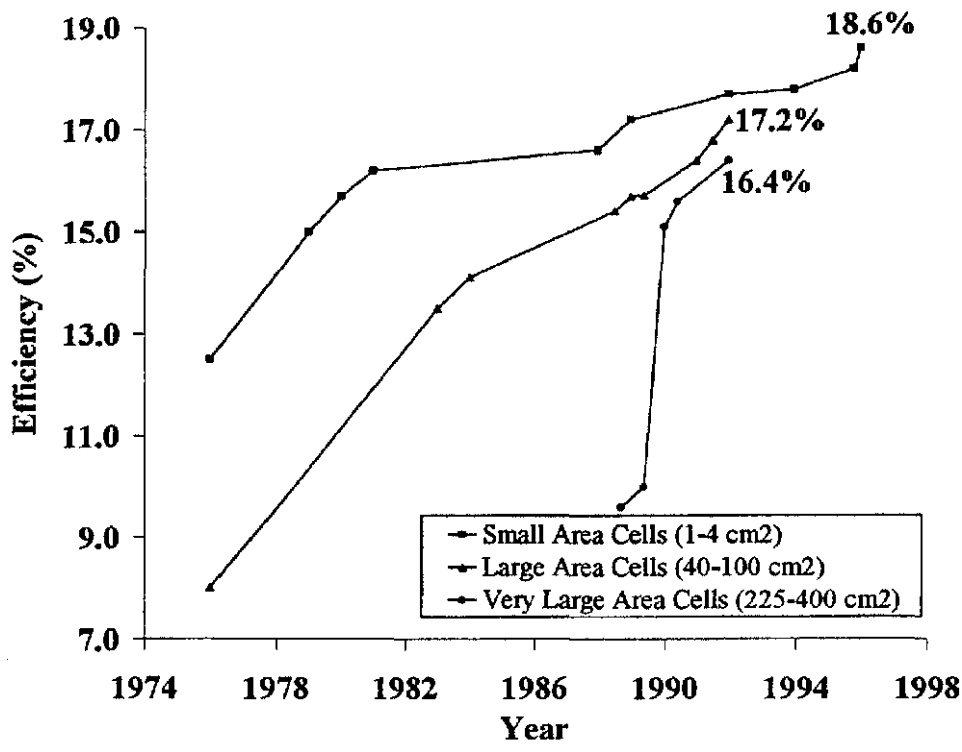


Fig. 9. Efficiency progress of mc-Si solar cells over the past 20 years.

4.1.1. *Small Area Cells*

The baseline process used to fabricate high-efficiency mc-Si solar cells at Georgia Tech involves the following steps. The emitter is formed by a phosphorus diffusion at 900°C for 30 minutes. This time and temperature have been shown to produce an optimal gettering effect on HEM mc-Si [42]. The emitter diffusion is followed by an etch-back step in order to lower the surface concentration and reduce heavy doping effects. Next, an Al-BSF is formed by evaporating 1 μm of aluminum onto the rear side of the wafer and then alloying at 850°C for 30 minutes. During the first 10 minutes of this anneal, the ambient gas is switched to oxygen in order to grow a passivating oxide on the emitter. Then, the ambient gas is switched back to nitrogen for the remaining 20 minutes of the alloying treatment. At the end of the anneal, the temperature is ramped down to 400°C at which time a forming gas anneal is done in order to provide atomic hydrogen for interface and bulk passivation. Front contacts to the solar cells are formed by PL. Finally, a DLAR coating consisting of ZnS and MgF_2 is applied to the front surfaces.

Solar cells with efficiencies as high as 18.6% (1 cm^2 area) have been achieved on 0.65 Ω-cm HEM mc-Si by the above process sequence. Photoconductance decay analysis revealed that process-induced gettering raised the bulk lifetime in the HEM material from an as-grown level of 10 μs to 135 μs. This increased the impact of S_b on solar cell performance. By incorporating a deeper Al-BSF than that described in the baseline sequence, the S_b for solar cells in this study was lowered from 10,000 cm/s to 2,000 cm/s on HEM mc-Si. This corresponded to an efficiency change of 0.4% (absolute), raising the cell efficiency from 18.2% to 18.6%. Model calculations revealed that reducing S_b further (to the 1,000 cm/s range) would increase the efficiency of similar HEM mc-Si solar cells beyond 19%.

In one of the wafers processed in this experiment, eight adjacent devices had an efficiency range of 16.8% to 18.2% with an average efficiency of 17.6%. This suggested a nonuniform distribution of electrically active defects in the material. Light beam induced current (LBIC) scans were carried out on high and low efficiency devices in order to determine the role of extended defects on cell efficiency. A comparison between the LBIC response of an 18.1% and a 16.8% cell are shown in Fig. 10. The scan of the 18.1% device reveals that the active area is free from electrically active defects. Furthermore, the high bulk lifetimes measured in the processed material indicate that phosphorus gettering was effective in removing impurities from the as-grown silicon. On the contrary, the LBIC response of the 16.8% cell shows the presence of a significant density of electrically active defects. The PDG and aluminum treatments did not improve the current response in these defective regions. Forward biased current-voltage analysis of this device showed that the defects lowered the cell performance by increasing both bulk and depletion region recombination. However, the efficiency degradation was primarily due to the bulk recombination, or the J_{o1} component of the total reverse saturation current.

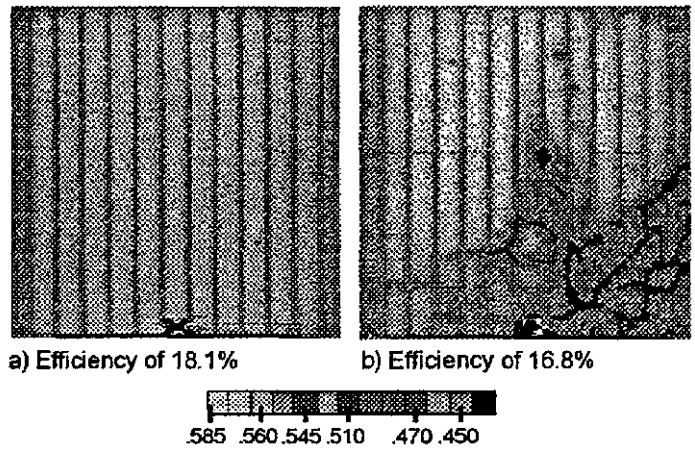


Fig. 10. LBIC scans revealing the effects of electrically active defects in HEM mc-Si solar cells [42].

4.1.2. *Large Area Cells*

Listed in Table 3 are significant results of various studies that resulted in high-efficiency cells on large area mc-Si materials. The Table also shows the key processing steps used in fabrication. All of these cells have the following three features in common: 1) SiO_2 emitter passivation, 2) front surface texturing, and 3) an AR coating. These processes serve to maximize J_{sc} since the current response is not as dependent on localized regions of electrically active defects as the voltage response.

The process sequence for the 17.2% cell (fabricated by Sharp Corporation) begins with mechanical texturing of the front surface. The emitters are formed by a phosphorus diffusion cycle (at 850°C) and then passivated by

an ensuing oxidation (at 800°C). Next, the first AR coating layer (TiO_2) is deposited by an atmospheric CVD process. The front and back contacts are applied by SP techniques. Fine line printing is used in order to keep the grid shading to a minimum. During the SP contact firing cycle, a BSF is formed. Finally, a second AR coating (MgF_2) is applied to the front surface [43]. It is noteworthy that such a highly efficient large area mc-Si solar cell was achieved using SP contacts.

Table 2. High efficiency large area mc-Si solar cells and process characteristics.

Cell	Area	Source	Eff.	Process Characteristics
1	100	Sharp/ OTC	17.2	SiO_2 Emitter Pass, Text. (Mech.), SP Cont., DLAR, Al BSF
2	100	Kyocera/ OTC	16.5	SiO_2 Emitter Pass, Text. (Chem.), PL Cont., DLAR, Al BSF, Selective Emitter
3	225	Kyocera/ OTC	16.4	SiO_2 Emitter Pass, Text. (Chem.), PL Cont., DLAR, Al BSF, Selective Emitter
4	100	Sharp/ OTC	16.4	SiO_2 Emitter Pass, Text. (Chem.), SP Cont., DLAR, Al BSF
5	42	Sandia/ HEM	16.4	SiO_2 Emitter Pass, Text. (Chem), PL Cont., DLAR, Al BSF, Al Gettering
6	100	IMEC-Konstanz	16.0	SiO_2 Emitter Pass, Text. (Mech.), SP Cont., DLAR, Al BSF, Al Gettering
7	100	IMEC-Konstanz	15.7	SiO_2 Emitter Pass, Text. (Mech.), SP Cont., DLAR, Al BSF
8	230	Solarex	14.7	SiO_2 Emitter Pass, Text. (Mech.), SP Cont., SLAR, Al BSF, Al Gettering, Selective Emitter

4.1.3. *Very Large Area Cells*

Significant throughput gains can be realized by increasing the silicon wafer size. Attempts are being made to fabricate larger solar cells than the standard 100 cm^2. By moving to wafers which can support device areas greater than 200 cm^2, the power produced can be increased by a factor of two for the same production time. In this paper, such cells are deemed *very large area* devices. Two of these devices are described in Table 2. As Fig. 9 indicates, the maximum reported very large area cell efficiency to date is 16.4% (fabricated by Kyocera Corporation).

The fabrication sequence for the 16.4% involved surface texturing of Sitix mc-Si by PL, followed by a double phosphorus diffusion. The resulting selective emitter was diffused to 20 Ω/sq. under the gridlines and 80 Ω/sq. in the field. Then, a p^+ BSF was formed by screen-printing and annealing aluminum. A SiN coating was deposited on the front and back surfaces, followed by a thermal treatment. This accomplished surface passivation of the emitter and back surface, bulk passivation of defects in the material, and provided the first layer in a DLAR coating. Front and back contacts were formed using PL and metal evaporation techniques. Finally, a MgF_2 film was deposited as the second layer in the DLAR coating.

Low fill factors (0.759 for this 16.4% cell [44]) are of some concern for very large area devices because of the increased resistive losses due to metallization. As contact extent becomes longer, the metallization materials and techniques will become more critical to attaining the maximum power output from very large area solar cell.

Section V. *Conclusions*

LDD materials have become promising candidates for reducing the cost of silicon PV. Significant progress has been made in the efficiency of LDD cells in the laboratory. To date, the highest reported efficiencies for small, large, and very large area LDD cells are 18.6%, 17.2%, and 16.4%, respectively. The real challenge is to reduce the impact of defects in these materials by developing low-cost gettering and passivation techniques which lend themselves to large-scale production. Phosphorus and aluminum gettering, as well as hydrogen passivation by PECVD and forming gas, are especially attractive because the can be included in the basic cell process sequence. With improvements in the silicon bulk quality, surface passivation will become critical. To further boost the efficiency of LDD cells, cost-effective surface texturing procedures must be introduced. Finally, emphasis should be placed on improving high throughput techniques such as RTP and SP to achieve the cost and efficiency goals simultaneously.

Acknowledgments

The authors would like to acknowledge A. Doolittle and P. Doshi for their input and helpful discussions.

References

[1] J.R. Davis, A. Rohatgi, R.H. Hopkins, P.D. Blais, P. Rai-Choudhury, J.R. McCormick, and H.C. Mollenkopf, "Impurities in Silicon Solar Cells," *IEEE Trans. on Electron Devices*, vol. Ed-27, pp. 677-687, 1980.

[2] B.L. Sopori, "Influence of Oxygen on the Performance of Silicon Solar Cells," in *Proc. 20th IEEE Photovoltaic Specialists Conf.*, September 1988, pp. 591-596.

[3] S.K. Pang and A. Rohatgi, "Effect of Oxygen Concentration on Lifetime in Magnetic Czochralski Silicon," *J. Elechtrochem. Soc.*, vol. 138, pp. 523-527, 1991.

[4] L. Ammor, S. Martinuzzi, and H. Amzil, "Influence of Carbon in Excess on Crystallographic and Photovoltaic Properties of Cast Polycrystalline Silicon Cells," in *Proc. 19th IEEE Photovoltaic Specialists Conf.*, September 1987, pp. 1064-1068.

[5] H.E. Ghitani and S. Martinuzzi, "Influence of Dislocations on Electrical Properties of Large Grained Polycrystalline Silicon Cells. II. Experimental Results," *J. Appl. Phys.*, vol. 66, pp. 1723- 1726, 1989.

[6] A. Doolittle, "Fundamental Understanding, Characterization, Passivation and Gettering of Electrically Active Defects in Silicon," *Ph.D. Thesis*, Georgia Institute of Technology, 1996.

[7] J.S. Kang and D.K. Schroder, "Gettering in Silicon," *J. Appl. Phys.*, vol. 65, pp. 2974-2985, 1989.

[8] G.B. Bronner and J.D. Plummer, "Gettering of Gold in Silicon: A Tool for Understanding the Properties of Silicon Interstitials," *J. Appl. Phys.*, vol. 61, pp. 5286-5298, 1987.

[9] A. Rohatgi, J.R. Davis, R.H. Hopkins, and P.G. McMullin, "A Study of Grown-in Impurities in Silicon by Deep-Level Transient Spectroscopy," *Solid-State Electron.*, vol. 26, no. 11, pp. 1039-1051, 1983.

[10] R. Falster, "Platinum Gettering in Silicon by Phosphorus," *Appl. Phys. Lett.*, vol. 46, pp. 737-739, 1985.

[11] A. Rohatgi, S. Narasimha, and S. Kamra, "Record High 18.6% Efficient Solar Cell on HEM Multicrystalline Material," in *Proc. 25th IEEE Photovoltaic Specialists Conf.*, 1996.

[12] S. Narayanan, S.R. Wenham and M.A. Green, "17.8% Efficiency Polycrystalline Silicon Solar Cells," *IEEE Trans. Electron Devices*, vol. ED-37, pp. 382-384, 1990.

[13] T.Y. Tan, R. Gafiteanu, and U.M. Gosele, "Toward Understanding and Modeling of Impurity Gettering in Silicon," in *Fifth Workshop on the Role of Impurities and Defects in Silicon Device Processing: Extended Abstracts*, 1995, pp. 93-100.

[14] R.D. Thompson and K.N. Tu, "Low Temperature Gettering of Cu, Ag, and Au Across a Wafer of Si by Al," *Appl. Phys. Lett.*, vol. 41, pp. 440-442, 1982.

[15] R. Sundaresan, D.E. Burk, and J.G. Fossum, "Potential Improvement of Polysilicon Solar Cells by Grain Boundary and Intragrain Diffusion of Aluminum," *J. Appl. Phys.*, vol. 55, pp. 1162-1167, 1984.

[16] A. Rohatgi, P. Sana, M.S. Ramanachalam, J. Salami, W.B. Carter, "Investigation of the Effects of Aluminum Treatment on Silicon Solar Cells," in *Proc. 23rd IEEE Photovoltaic Specialists Conf.*, May 1993, pp. 52-57.

[17] S. Martinuzzi, H. Poitevin, M. Zehaf, and C. Zurletto, "Improvement of Electron Diffusion Lengths in Polycrystalline Silicon Wafers by Aluminum," *Revue Phys. Appl.*, 22, pp. 645-648, 1987.

[18] B.L. Sopori, L. Jastrzebski, and T. Tan, "A Comparison of Gettering in Single- and Multicrystalline Silicon for Solar Cells," in *Proc. 25th IEEE Photovoltaic Specialists Conf.*, May 1996.

[19] Estreicher, S.K. "Hydrogen-related Defects in Crystalline Semiconductors: A Theorist's Perspective," *Mat. Sci. Eng. Reports*, R14, pp. 319-412, 1995.

[20] H.J. Moller, *Semiconductors for Solar Cells* (Boston: Artech House, 1993).

[21] H.E. Elgamel, C. Vinickier, M. Caymax, M. Ghannam, J. Poortmans, P. De Schepper, J. Nijs, and R. Mertens, "High Efficiency Multicrystalline Silicon Solar Cells Using Hydrogen Remote Plasma Passivation, in *12th European Photovoltaic Solar Energy Conference*, April 1994, pp. 724-727.

[22] A. Cuevas, G. Giroult-Matlakowski, P.A. Basore, C. DuBois, and R. King, "Extraction of the Surface Recombination Velocity of Passivated Phosphorus-Doped Silicon Emitters," in *Proc. 24th IEEE Photovoltaic Specialists Conf.*, May 1994, pp. 1446-1449.

[23] W.D. Eades and R.M. Swanson, "Calculation of Surface Generation and Recombination Velocities at the Si-SiO_2 Interface," *J. Appl. Phys.*, vol. 58, pp. 4267-4276, 1985.

[24] P. Sana, J. Salami, and A. Rohatgi, "Fabrication and Analysis of High-Efficiency Polycrystalline Silicon Solar Cells," *IEEE Trans. on Electron Devices*, vol. 40, pp. 1461-1468, 1993.

[25] Z. Chen and A. Rohatgi, "Silicon Surface and Bulk Defect Passivation by Low Temperature PECVD Oxides and Nitrides," in *Proc. 24th IEEE Photovoltaic Specialists Conf.*, May 1994, pp. 1331-1334.

[26] Z. Chen, P. Sana, J. Salami, and A. Rohatgi, "A Novel and Effective AR Coating for Si Solar Cells," *IEEE Trans. on Electron Devices*, vol. 40, pp. 1161-1165, 1993.

[27] Chen, S.K. Pang, K. Yasutake, and A. Rohatgi, "Plasma-Enhanced Chemical-Vapor-Deposited Oxide for Low Surface Recombination Velocity and High Effective Lifetime in Silicon," *J. Appl. Phys.*, vol. 74, pp. 2856-2859, 1993.

[28] J. Schmidt, T. Lauinger, A.G. Aberle, and R. Hezel, "Record Low Surface Recombination Velocities on Low-Resistivity Silicon Solar Cell Substrates," in *Proc. 25th IEEE Photovoltaic Specialists Conf.*, May 1996.

[29] S. Narasimha, J. Mejia, and A. Rohatgi, "Screen Printed Aluminum Back Surface Fields for Silicon Solar Cells," this Workshop.

[30] P. Lolgen, C. Leguijt, J.A. Eikelboom, R.A. Steeman, W.C. Sinke, L.A. Verhoef, P.F.A. Alkemade, and E. Algra, "Aluminum Back-Surface Field Doping Profiles with Surface Recombination Velocities Below 200 cm/s," in *Proc. 23rd IEEE Photovoltaic Specialists Conf.*, 1993, pp. 1064-1068.

[31] J.A. Amick, F.J. Bottari, and J.I. Hanoka, "The Effect of Aluminum Thickness on Solar Cell Performance," *J. Electrochem. Soc.*, vol. 141, pp. 1577-1585, 1994.

[32] R.R. King, K.W. Mitchell, and J.M. Gee, "Back Surface Cell Structures for Reducing Recombination in CZ Silicon Solar Cells, in *Proc. 24th IEEE Photovoltaic Specialists Conf.*, May 1994, pp. 1291-1294.

[33] M.A. Green and P. Campbell, "Light Trapping Properties of Pyramidally Textured and Grooved Surfaces," in *Proc. 19th IEEE Photovoltaic Specialists Conf.*, 1987, pp.912-917.

[34] RESPV Ltd. (India), Seimens Solar Industries.

[35] A.W. Smith and A. Rohatgi, "A New Texturing Geometry for Producing High-Efficiency Solar Cells with No Antireflection Coatings," *Solar Energy Mat. and Solar Cells*, 29, pp. 51-65, 1993.

[36] T. Nunoi, S. Okamoto, K. Nakajima, S. Tanaka, N. Shibuya, K. Okamoto, T. Nammori, H. Itoh, "Cast Polycrystalline Silicon Solar Cells with Grooved Surface," publication not available.

[37] P. Fath, E. Bucher, G. Willeke, "A Comparative Study of Buried Contact and Screen-Printed Polycrystalline Silicon Cells with a Mechanically V-Grooved Surface Texturiztion," in *Proc. 24th IEEE Photovoltaic Specialists Conf.*, May 1994, pp. 1543-1546.

[38] A. Rohatgi, Z. Chen, P. Doshi, T. Pham, D. Ruby, "High-Efficiency Silicon Solar Cells by Rapid Thermal Processing," *Appl. Phys. Lett.*, 65, pp. 2087-2089, 1994.

[39] D. Sparks, R. Chapman, and N. Alvi, "Anomalous Diffusion and Gettering of Transition Metals in Silicon," *Appl. Phys. Lett.*, 49, pp. 525-527, 1986.

[40] P. Doshi, A. Rohatgi, M. Ropp, Z. Chen, D. Ruby, and D.L. Meir, "Rapid Thermal Processing of High-Efficiency Silicon Solar Cells with Controlled *in-situ* Annealing," in *Proc. 24th IEEE Photovoltaic Specialists Conf.*, May 1994, pp. 1299-1302.

[41] P. Doshi, J. Mejia, K. Tate, S. Kamra, A. Rohatgi, S. Narayanan, and R. Singh, "High-Efficiency Silicon Solar Cells by Low-Cost Thermal Processing, Screen Printing, and Plasma-Enhanced Chemical Vapor Deposition," in *Proc. 25th IEEE Photovoltaic Specialists Conf.*, May 1996.

[42] S. Narasimha, S. Kamra, and A. Rohatgi, "The Optimization and Fabrication of High-Efficiency HEM Multicrystalline Silicon Solar Cells," in *Proc. 25th IEEE Photovoltaic Specialists Conf.*, May 1996.

[43] T. Machida, M. Nishida, T. Nammori, T. Nunoi, and H. Sawai, "High-Efficiency Polycrystalline Silicon Solar Cells," in *Proc. 4th Sunshine Workshop on Crystalline Solar Cells*, 1992, pp. 99-102.

[44] K. Shirasawa, H. Takahashi, Y. Inomata, S. Ogasawara, K. Fukui, K. Okada, M. Takayama and H. Watanabe, "Over 16% Efficiency Large Area Multicrystalline Silicon Solar Cell," in *Proc. 23rd IEEE Photovoltaic Specialists Conf.*, 1993, pp. 256-259.

A Review of Recent Advances in MIS Solar Cells

Rudolf Hezel

Institut für Solarenergieforschung Hameln/Emmerthal (ISFH)
D-31860 Emmerthal, Germany

Abstract

By the elimination of the high temperature diffusion step Metal-Insulator-Semiconductor (MIS) type solar cells have an inherent cost advantage compared to p-n junction solar cells. First generation MIS-inversion layer (MIS-IL) solar cells, already successfully produced in an industrial pilot line, are restricted to efficiencies of 15 % - 16 %.
With the second generation MIS-IL silicon solar cells, based on drastically improved surface passivation by PECVD silicon nitride, simple technology can be combined with very high efficiencies. A 17.1 % efficiency could already be achieved with the novel point-contacted „truncated pyramid" MIS-IL cell. A new surface-grooved line-contact MIS-IL device using unconventional processing steps applicable for large scale fabrication is discussed. By the mechanical grooving technique contact widths down to 2 µm can be homogeneously achieved over large wafer areas. Bifacial sensitivity is included in most of the MIS type solar cells.
For a bifacial 98 cm^2 Cz Si MIS-contacted p-n junction solar cell with a random pyramid surface texture and Al as grid metal efficiencies of 16.5 % for front and 13.8 % for rear side illumination are reported. 19.5 % efficiency could be obtained with a mechanically grooved MIS n^+p solar cell with Al metallization.
MIS type silicon solar cells are able to significantly lower the costs for solar electricity due to the simple technology and the potential for efficiencies well above 20 %.

I. Introduction

The Metal-Insulator-Semiconductor (MIS) type solar cells have received much attention in the past due to their simple low temperature fabrication process and the potential for high efficiencies. They are promising candidates for drastically reducing the cost-per-Watt-ratio of solar electricity.
The high temperature junction diffusion step is completely eliminated in these devices. In an early version, consisting of a continuous low work function metal on top of a p-type semiconductor with an insulating layer in between, a collecting barrier is induced at the semiconductor surface due to the difference in work function. Whereas the minority charge carriers are able to flow through the insulating layer by quantum mechanical tunnelling, if this layer is sufficiently thin, the majority carriers are blocked. It's the main disadvantage of these transparent metal MIS cells, that very thin metal layers have to be used with their thickness being a compromise between transparency and voltage drop caused by series resistance.

To overcome this problem, the MIS configuration was restricted to the contact grid, whereas the active area between the grid fingers was covered by a transparent dielectric (grating type MIS solar cells). If an inversion layer is induced by the presence of insulator charges, the device is called MIS-Inversion Layer (MIS-IL) solar cell. As transparent dielectrics for inversion layer formation at the silicon surface thermal SiO_2 /1/, TiO_x and CVD SiO_2 /2/, SiO /3/ and Ta_xO_y /4/ have been used.
A major shortcoming of these early inversion layer solar cells was that they were suffering from rapid degradation of the inversion layer. The degradation could be overcome by the introduction of silicon nitride as charged dielectric and antireflection layer, with its stable high positive charge densities achieved by incorporation of alkaline species /5-9/.
The silicon nitride MIS-IL solar cells could be successfully transferred to an industrial pilot production line for 10 x 10 cm^2 cells /10/. Since early 1994, the cells encapsulated in novel large-area modules are installed in many places, only to mention the German-Spanish 1 MW photovoltaic power plant in Toledo-Spain with an output power of more than 400 kW provided by MIS-IL cells /11/. They are reported to work without any problem up to now. In April 1995 even additional MIS-IL modules were installed in the Toledo plant in order to replace conventional p-n junction modules because of delamination problems /12/. The technologically very simple processing sequence provides energy conversion efficiencies of up to 15.3 % on 10 x 10 cm^2 CZ silicon and 15.7 % on 2 x 2 cm^2 FZ wafers /13/. The hidden primary energy in monocrystalline MIS-IL cells was estimated to be 35 % lower compared to conventional screen-printed p-n junction solar cells /14/. In addition to this, MIS-IL solar cells have several further advantages compared to diffused p-n junction devices /10, 15/.
It`s the main purpose of the present review paper, after a brief discussion of the above mentioned first generation silicon nitride MIS-IL cells, to point out the importance of surface passivation for further improvement and to introduce the second generation of this promising cell type. Two dimensional numerical modelling revealed, that inversion layer solar cells can basically achieve the same high efficiencies (> 23 %) as p-n junction solar cells /15/. Novel approaches with the potential for very high efficiencies are presented, all based upon the excellent surface passivation properties of the plasma-enhanced-chemically-vapor-deposited (PECVD) silicon nitride. Finally, two recent high efficiency versions of MIS contacted p-n junction solar cells are discussed.

II. First Generation MIS-Inversion Layer Solar Cells

The cross section of the first generation MIS-IL solar cell, including bifacial sensitivity, is shown in Fig 1. As an induced-junction device the inversion layer cell is based upon the formation of an inversion layer at the silicon surface, which provides a conducting path to the adjacent MIS grid fingers for the minority charge carriers generated by the impinging light. The inversion layer is induced by fixed positive charges present in the transparent insulator film which, as a characteristic feature of the first generation MIS-IL cells, covers both the silicon surface and the MIS contacts. This film also has to serve as passivation and antireflection layer. As already mentioned, silicon nitride has been proven to be particularly suitable for this crucial part of the device /10/.
The electrical properties of the cell are determined by two main regions: (i) The tunnel MIS contacts and (ii) The thin film system and its interfaces in the active area between the

collecting contacts. For an ideal Al/SiO_x/p-Si tunnel MIS contact the band bending at the silicon surface is given by the work function difference of the metal and the underlying silicon. For 0.8 Ωcm p-Si and aluminum a barrier height of 0.87 eV is resulting, indicating that in thermal equilibrium the silicon surface beneath the metal is strongly inverted /16/. The ultrathin oxide layer ($d_{ox} \approx 1.3$ nm) blocks majority carrier (hole) currents injected into the

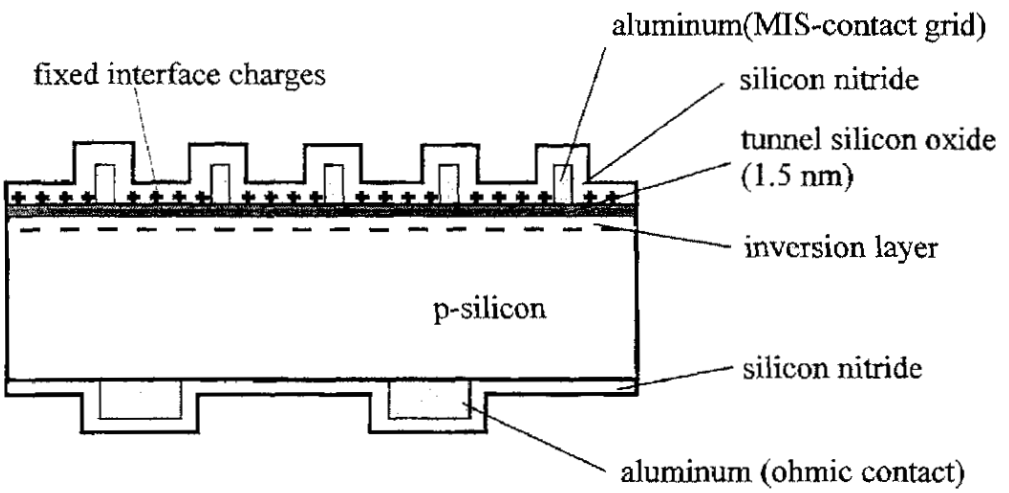


Figure 1: Schematic cross section of the first generation MIS inversion layer solar cell with bifacial sensitivity. The silicon nitride is deposited after the MIS grid formation.

metal at forward bias and reduces surface recombination. Therefore very high open-circuit voltages should be achievable using MIS contacts /17, 18/. The charge distribution and energy band diagram for the system silicon nitride/tunnel oxide/p-Si in the active area of the solar cell is discussed elsewhere /5, 8/.

Details about the theory of MIS contacts as well as about modelling of inversion layer solar cells are published in /19, 20/ and /21-24/, respectively. The fabrication process both for one-sided and bifacial solar cells is outlined elsewhere /10/. Only the following few steps are required: (i) Surface texturing, (ii) Rear surface metallization and sintering simultaneously with tunnel oxide growth (500 °C), (iii) Front grid Al evaporation through a metal mask, (iv) Cesium dip to increase fixed charge density and (v) Deposition of PECVD Si nitride onto the entire front surface (250 °C). The technically simple rear side configuration shown in Fig 1 is based upon excellent surface passivation by plasma Si nitride deposited at about 400 °C after the metal contacts have been formed /25/. Thus, in contrast to thermal oxide passivation, no complex photolithography is required for contact opening. This structure, by which also the light impinging on the rear side can be utilized, is incorporated in most solar cell types presented in this review paper. With this non-diffused back surface design, remarkably high rear efficiencies of 18.1 % could already be achieved, demonstrating the outstanding quality of the surface passivation by plasma silicon nitride, as further discussed below /26, 27/. A gain in output power up to 50 % is possible by simply arranging the bifacial cell module in front of a white wall /10/.

III. Second Generation MIS-Inversion Layer Solar Cells

1. Importance of surface passivation

Fast surface states at the silicon/insulator interface are known to reduce the efficiency of inversion layer solar cells by increasing the surface recombination velocity and by affecting the inversion layer properties, particularly its sheet resistance /28, 29/. Thus excellent passivation of the silicon surface via reduction of the interface state density is required for further improvement of MIS-IL solar cells.

As shown in Fig 2, the effective surface recombination velocity S_{eff} and the open-circuit voltage V_{oc} were calculated with PC-1D as a function of the front surface recombination velocity So, which is given by $S_o = \sigma \cdot V_{th} \cdot D_{it}$, where σ is the capture cross section, V_{th} the thermal velocity, and D_{it} the interface state density. The calculations were performed for 0.5 Ωcm p-Si with a diffusion length of 825 μm. The doping profile was chosen to simulate an inversion layer induced by a fixed surface charge density D_{it} of 1×10^{13} cm^{-2} /30/.

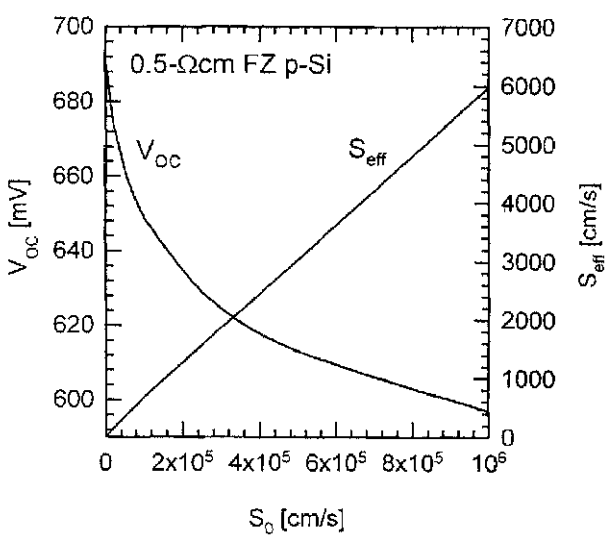


Figure 2: Calculated V_{oc} and effective recombination velocity S_{eff} of the inversion layer emitter of MIS-IL solar cells on 0.5 Ωcm Fz p-Si as a function of the surface parameter $S_o = \sigma \cdot D_{it} \cdot V_{th}$.

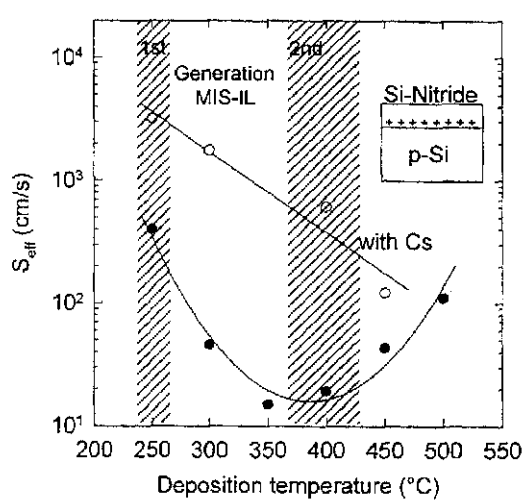


Figure 3: Surface recombination velocity S_{eff} as a function of the plasma-silicon-nitride deposition temperature (0.5 Ωcm Si). The temperature regions characteristic for 1st and 2nd generation MIS-IL solar cells are indicated.

It's evident from Fig 2 that a drastic increase in V_{oc} of MIS-IL solar cells can be achieved by decreasing the front surface recombination velocity. For comparison, p-n junction silicon solar cells are much less sensitive to the front surface recombination velocity /27/. Recently extremely low values of the effective surface recombination velocity S_{eff}, as determined by the microwave-detected photoconductance decay (MW-PCD) technique, could be achieved by the deposition of remote-plasma silicon nitride on silicon /27, 31/. In Fig 3 S_{eff} is plotted as a function of the nitride deposition temperature, both with and without incorporation of

cesium. As can be seen, the lowest S_{eff} value is obtained at temperatures of about 400 °C, whereas at lower and higher temperatures S_{eff} is considerably increasing /25/. Very high insulator charge densities achieved by a CsCl treatment are required in order to provide a high electron density within the inversion layer as well as efficient charge-induced passivation /25/. However, despite of the interface contamination by cesium, S_{eff} should be as low as possible /10, 32/. According to Fig 3 even with cesium S_{eff} is also significantly reduced with increasing the nitride deposition temperature from 250 °C to 400 °C, but the values are higher than those of the not Cs-contaminated samples. The drastic increase of the fixed positive insulator charge density Q_n/q with the cesium concentration of the alcoholic CsCl solution in which the wafers are dipped prior to the nitride deposition is shown in Fig 4 /10, 32/.

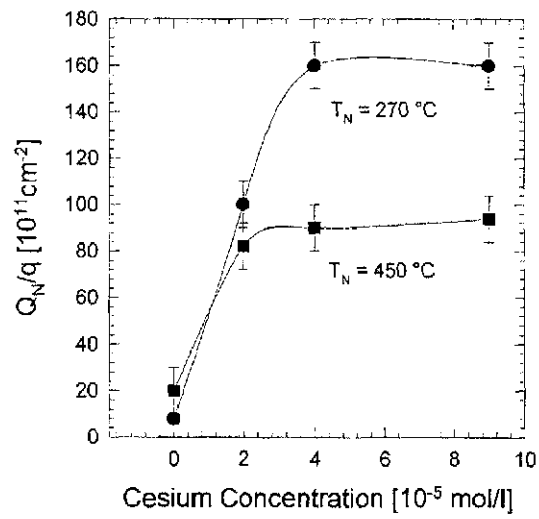


Figure 4: Fixed insulator charge density as a function of the concentration of a cesium-containing solution for structures of plasma silicon nitride on thin-oxide-covered p-silicon (100), 0.5 Ωcm. Nitride deposition temperatures are T_N = 270 °C and T_N = 450 °C, respectively.

As can be seen, the saturation charge density is lower for the films deposited at 400 - 450 °C compared to those prepared at 270 °C, but the value of about 10^{13} cm^{-2} is still sufficiently high /10/. According to Fig 3, for Cs-contaminated interfaces with plasma silicon nitride deposited at 250 °C (1st generation MIS-IL cells) an S_{eff} of about 4000 cm/s, for 400 °C (2nd generation MIS-IL solar cells) an S_{eff} value of about 400 cm/s is resulting. In the latter case, as deduced from Fig 2, a V_{oc} of about 670 mV, for the first case only about 610 mV is achievable.

Thus, in order to improve cell efficiency, the plasma silicon nitride film has to be deposited at about 400 °C. However, at this temperature the MIS contacts are degrading in so far, as the tunnel oxide is reduced by the overlying aluminium /33, 34/. A considerably improved thermal stability of the MIS contacts could be achieved by replacing the thermal tunnel silicon oxide by silicon oxynitride prepared by plasma nitridation of silicon /35, 36/. However, these contacts are also degrading during the nitride deposition at 400 °C. As a consequence, in contrast to the first generation MIS-IL solar cells, the plasma nitride film has

to be deposited prior to the MIS contact formation. For this purpose, cell processing has to be considerably modified, leading to the second generation MIS inversion layer solar cells.

In addition to the low surface recombination velocity, however, stability of both surface passivation and inversion layer properties under ultraviolet radiation is another vital prerequisite for MIS-IL solar cells. Perfect UV stability for both first and second generation inversion layer cells was confirmed by several investigations /9, 37/. Novel cell concepts and first promising results for the 2nd generation MIS-IL cells are discussed in the following.

2. Novel solar cell concept

In a first attempt to realize 2nd generation MIS-IL solar cells with deposition of the plasma silicon nitride layer at temperatures of 400 °C - 450 °C prior to the MIS grid formation, the grid was subsequently defined by photolithography and chemical etching /32/. As expected, improved open-circuit voltages have been obtained, however, the application of photolithography and alignment, which is difficult to perform far large wafer areas, is in contradiction to the low-tech strategy pursued by the MIS-IL approach.

An innovative concept was recently introduced by which highly efficient solar cells should be attainable by high-temperature as well as low-temperature processing, including simple large-area fabrication methods /38/. The basic principle of this approach is as follows:
(i) Formation of specific elevations on the semiconductor surface, (ii) Excellent surface passivation by high- or low-temperature films after the junction has been fabricated, (iii) For contact window opening removal of the passivation layer (and possibly some semiconductor material) from the tips and/or from the upper part of the elevations, and (iv) Selective metal deposition upon the elevated regions.
According to the above-mentioned concept novel point- and line- contact solar cells can be realized. As to the point-contact device, pyramids on monocrystalline silicon are chosen as elevations, resulting in the so-called "truncated-pyramid solar cell /38/. With the line contact solar cells, the ridges of parallel grooves are serving as elevations. Since step (iii)-Removal of the passivation layer- is the most characteristic feature, this cell type is designated as "Abrased-Ridge-Top" (ART) solar cell /39/. MIS-IL cells of the "truncated pyramid" as well as of the ART type are discussed below.

2. 1. Truncated Pyramid MIS-IL Solar Cells

In Fig 5 a specific type of the truncated pyramid solar cell as a novel point-contact device is shown. It has to be emphasized that this structure is completely different from the sophisticated point contact cell designed particularly for concentrator applications /40/. The surface of the device is characterized by passivated pyramids whose tops have been removed to a certain extent. One of the most significant advantages of this design concerns the metal grid. As can be seen, the main part of the metal finger is running over the passivated side walls of the pyramids, while the metal-silicon contact occurs only via small dots on top of the truncated pyramids. The size of the metal-silicon contact area can be precisely controlled by the tip removal depth. Not shown in Fig 5, the truncated-pyramid concept can also

advantageously be applied to the rear surface contact region in order to get a well passivated surface combined with small-sized metal contacts.
As to the fabrication process, the (100) oriented surface is randomly textured by anisotropic etching and the metal grid lines are preferentially formed by vacuum evaporation through a mechanical mask /30, 38/. For passivation plasma silicon nitride deposited at 400 °C and for pyramid truncation chemical-mechanical polishing (CMP) is used /30/.
In Fig 6 a SEM top view of a randomly textured and nitride-passivated silicon surface after pyramid truncation is shown. As can be seen, various differently sized upper surfaces of the truncated pyramids are formed, depending both on the individual height of each particular pyramid and on the silicon removal depth. Very small point-contacts, including many in the submicron range, could easily be fabricated by this novel pyramid truncation technique.

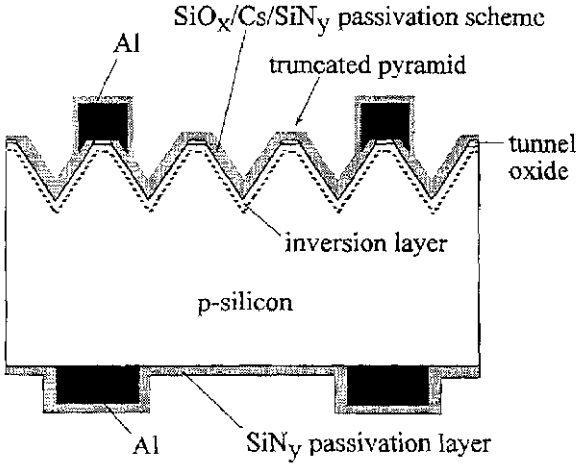


Figure 5: Schematic of the truncated-pyramid MIS-inversion layer silicon solar cell. The nitride passivation layer is deposited prior to the MIS grid formation (2nd generation MIS-IL cell).

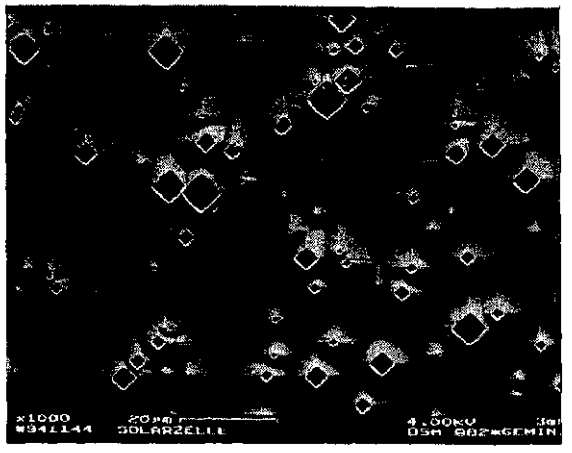


Figure 6: SEM top view of a randomly textured and silicon-nitride-passivated silicon surface after pyramid truncation. Several micron and submicron sized point contact windows are to be seen.

Only recently, a independently confirmed 17.1 % efficient truncated pyramid MIS-IL solar cell, 2 x 2 cm^2 in size, could be obtained /30, 41/. This is the highest efficiency ever reported for an inversion layer silicon solar cell. Bifacial MIS-IL cells of the truncated pyramid type are reported to have independently confirmed one-sun efficiencies of 16.7 % and 14.8 % for the front and rear side, respectively /30/. In these preliminary experiments the improvement compared to the first-generation MIS-IL cells is mainly due to an increase in the open-circuit voltage of about 40 mV. This is attributed to the drastically reduced effective recombination velocity of the inversion layer emitter achieved by the higher plasma nitride deposition temperature of 400 °C and to the reduction of the metallized area, since the silicon is point-contacted only at the tips of the pyramids. However, in the present structure the pyramids are also truncated in the area between the front grid lines which has a negative impact on the dark saturation current due to insufficient passivation of the tip areas /30, 41/. There is plenty of scope for further efficiency improvement well above 18 % by restricting the truncation of the elevations only to the metallized areas. By the following line contact approach the unintended

truncation in the active cell area during the chemical-mechanical polishing step is completely eliminated.

2. 2. Surface-Grooved MIS-IL Solar Cells

In Fig 7, a schematic representation of the novel MIS-inversion layer solar cell of the ART (Abrased-Ridge-Top") -type is shown. The surface is characterized by a set of parallel grooves, which are covered by a passivation layer. An inversion-layer induced by positive charges present in the passivating film is located at the semiconductor surface.

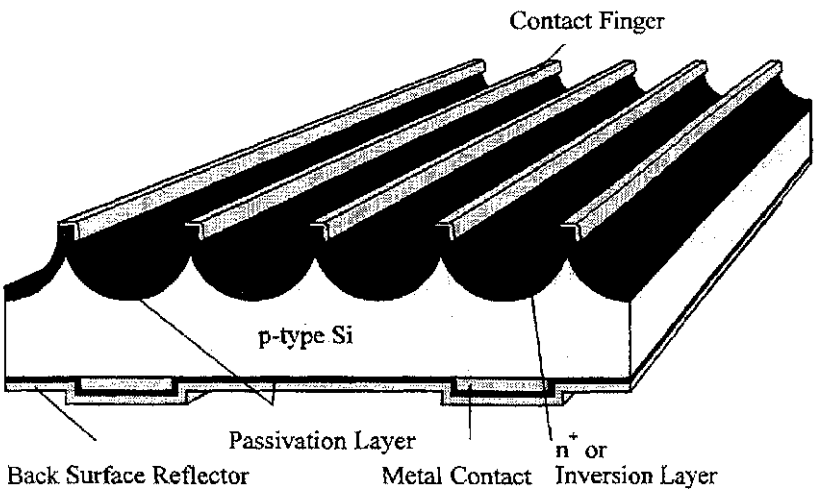


Figure 7: Schematic diagram of a wire-grooved ART (Abrased-Ridge-Top) solar cell for one sided (with BSR) and bifacial (without BSR) operation. The passivating silicon nitride is deposited prior to the MIS grid formation (2nd generation MIS-IL cell).

From the groove tops the passivation layer is removed for contact opening, and the contact metal is deposited, both on top and along the flanks, by a self-aligned process. For the rear side various configurations can be chosen. A simple design already discussed above for bifacially sensitive solar cells is selected /10, 25, 27/.

The novel device provides the following high efficiency features:
(i) Optimization of surface passivation, either by high temperature or low temperature steps, can be performed before contact preparation,
(ii) Very small metal-semiconductor contact areas, since the main part of the grid finger is running upon the passivation layer. Groove top dimensions down to 2 μm are homogeneously achievable on large wafer areas,
(iii) Large finger width combined with low effective shadowing, since the metal fingers are running along the steep flanks of the grooves. Reflection of light occurs from the metal into the opposite face of the grooves,
(iv) Low surface reflectance, increased optical absorption and light trapping,
(v) Enhanced carrier collection due to the generation of charge carriers close to the p-n junction,
(vi) The semiconductor substrate can be made relatively thin due to the mechanical support provided by the ridges. Perpendicular grooving of the rear side is also possible,

(vii) The concept is equally well suited for mono- and polycrystalline semiconductors, as well as for ribbon material. Since the grid lines can easily be made both closely spaced and relatively wide without significantly increasing obscuration, the present concept using mechanical grooving is also suitable for high efficiency concentrator solar cells.
As a special feature, the concept allows to use the elevations not only for simple local opening of small area contact regions and for self-aligned metallization by shallow angle-evaporation, but also for selective contact doping. Thus, as another option for the attainment of very high efficiencies, a combination of heavily doped contact regions (either with or without a tunnelling oxide) with high quality inversion layers are easy to fabricate.
For somewhat lower efficiencies, the extremely small contact area obtained by ridge-top abrasion may not be required, since heavily doped contacts are generally of high quality. Thus, as an alternative, the grid finger can be placed exclusively on one or both flanks of the ridge, either before or after the passivation layer has been formed.

As to the fabrication of the surface-grooved MIS-IL solar cells, four basic steps are required: (i) Surface structuring, (ii) Surface passivation, (iii) Local removal of the passivation layer, (iv) Self-aligned metallization. This is illustrated in Fig 8 together with the appropriate techniques.

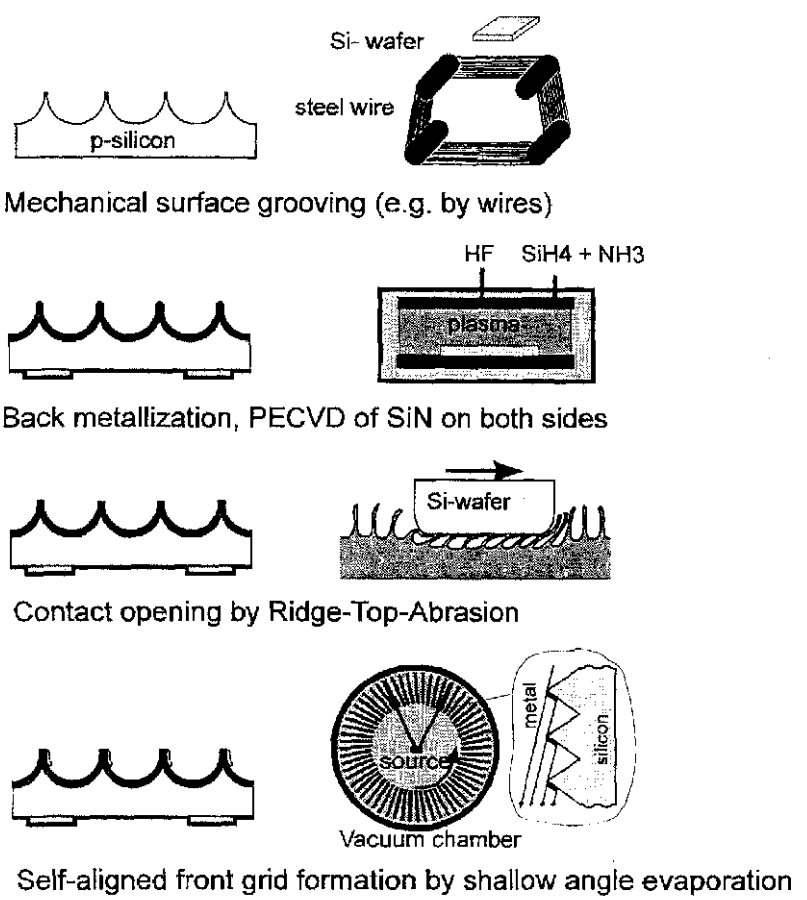


Figure 8: Basic fabrication steps of ART solar cells.

Since steps (ii) and (iii) are identical with those of the truncated pyramid cell, only steps (i) and (iv) are discussed in some detail.
Surface structuring is preferentially performed by mechanical means. Conventional dicing saws normally used in microelectronics for chip separation have already been successfully applied for V-grooving of multicrystalline silicon surfaces in order to improve their antireflection behaviour /42, 43/. Ultrathin self-supporting bifacial solar cells on single- and multicrystalline silicon were fabricated by mechanical structuring, whereby the silicon base thickness could be reduced to 20 µm /44, 45/. In all cases, thin dicing blades consisting of diamond particles (1-5 µm in diameter) embedded in a Ni matrix have been used. This technique is well suited for preparing the surface structure required for the new solar cells, particularly if multiblade dicing wheels for higher throughput are available.
A completely new technique of mechanical surface structuring, the so-called wire-grooving, is introduced, which causes less surface damage and may be more cost-effective due to the large area available for grooving /39, 46/. It's based on the wire-sawing technique, well known in photovoltaics for cutting the silicon rods into thin wafers. A conventional steel wire of about 180 µm in diameter and 120 km in length is guided by four grooved rollers to form a homogeneous web with a certain wire distance (Fig 8). Perfectly grooved silicon surfaces can routinely be manufactured, as is demonstrated by the SEM-picture in Fig 9. Extremely narrow ridges with top dimensions in the submicron range are resulting (Fig 10). It could be demonstrated that very small metal-silicon contact areas, comparable in size to those obtained by complex photolithographic procedures can be prepared homogeneously by ridge-top abrasion /39/.
No difference is observed between monocrystalline, multicrystalline and ribbon-shaped (EFG) silicon with respect to the high precision of wire grooving. It should finally be mentioned that the application of a diamond-coated wire could be another choice for surface grooving, however, surface damage may possibly be more pronounced.

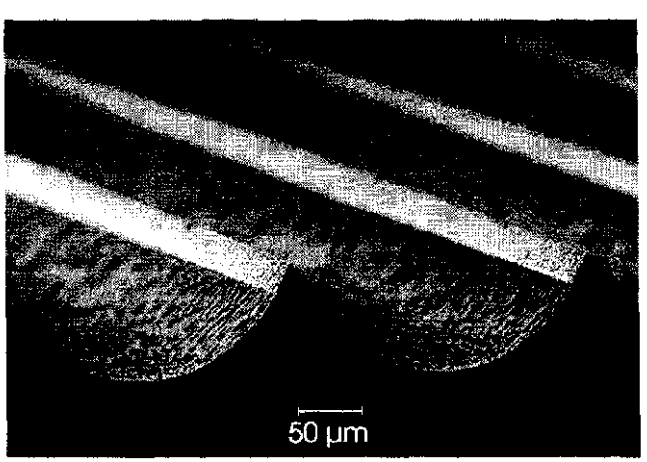


Figure 9: SEM picture of a wire-grooved silicon surface with shallow-angle-evaporated line contacts.

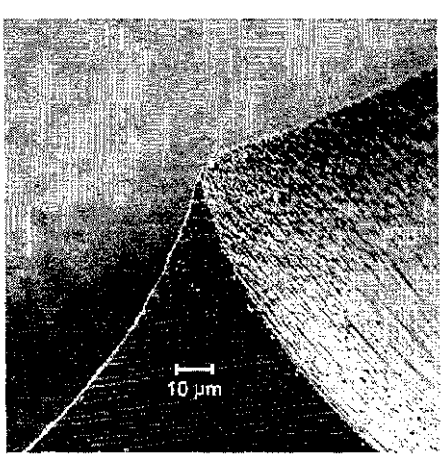


Figure 10: Extremely narrow ridges (submicron dimensions) for contact preparation obtained by the wire grooving technique on silicon. (SEM picture)

Self-aligned metallization by shallow-angle evaporation is based upon the shadowing effect of the ridges. Without any mask or alignment it is possible to deposit a relatively thick metal finger along one flank, whereas simultaneously a thin layer is formed on the truncated top contact region. The width of the finger can be adjusted by variation of the evaporation angle. The finger width can be increased to a certain extent without significantly affecting light obscuration and metal-silicon contact area. Hence, metal thickness and thus the amount of metal is reduced. A large conductor cross section is possible which makes the cells suitable for high concentration levels. As to the economy of the shallow angle evaporation technique, the throughput of wafers is drastically increased (at least by a factor of 10) compared to conventional vacuum evaporation, since the wafers can be arranged closely spaced on a rotating cylinder (Fig 8). Preventing wastage of metal is another big advantage of the angle evaporation. Nearly all the metal evaporated is used for the grid fingers only, so that even more expensive high-quality metal combinations like TiPdAg may come into consideration for mass production of cost-effective high efficiency solar cells. With conventional vacuum evaporation, more than 90 % of the metal is lost and additional processing is required to remove this surplus metal either from shadow masks or from the wafer itself.

IV. MIS-Contacted P-N Junction Solar Cells

1. Random-pyramid-surface-textured bifacial cells

An improvement in cell performance could be achieved for p-n junction solar cells, if, in addition to the plasma silicon nitride surface passivation, an ultrathin tunnelling oxide was incorporated into the metal contacts, resulting in a hybrid MIS- n^+p type solar cell /47/. In particular, it could be demonstrated for the first time, that in this case aluminium can be used for the front contact of phosphorous-diffused p-n junction silicon cells. Compared to the presently applied expensive silver-based metallization, the use of aluminum for both the front as well as the rear contact is a significant advantage with respect to costs for mass production. By the thin oxide contact passivation occurs via reducing the effective surface recombination velocity in the contact area. This passivation effect is most probably enhanced by the low work function of aluminum, creating an accumulation layer in the underlying silicon. Apparently, the thin oxide also prevents aluminium from degrading the p-n junction properties. With the simple MIS-n^+p bifacial cell structure depicted in Fig 11, for the front side efficiencies of 16.5 %, for rear side illumination 13.8 % was obtained on 98 cm^2 textured remelt 1 Ωcm CZ-silicon wafers with 150 μm in thickness. The reliability has already been proven on an industrial pilot production scale.

The tunnelling oxide was prepared in the same way as for MIS-IL cells. The relatively high short-circuit current density and open-circuit voltage for front and rear side illumination is a result of the excellent back surface passivation provided by the plasma silicon nitride deposited onto the ohmic back contacts /25/. This latter configuration was already introduced for the inversion layer type solar cells in an earlier work /10/.

Similar cell structures, using a much more complex technology including photolithography are reported in the literature /48/. The high-efficiency design features of these so-called MINP cells (area 20 x 20 mm^2) include the use of thermal SiO_2 to passify the noncontacted regions of the front surface, a double-layer AR coating and MIS-front contacts made up of Ti/Pd/Ag.

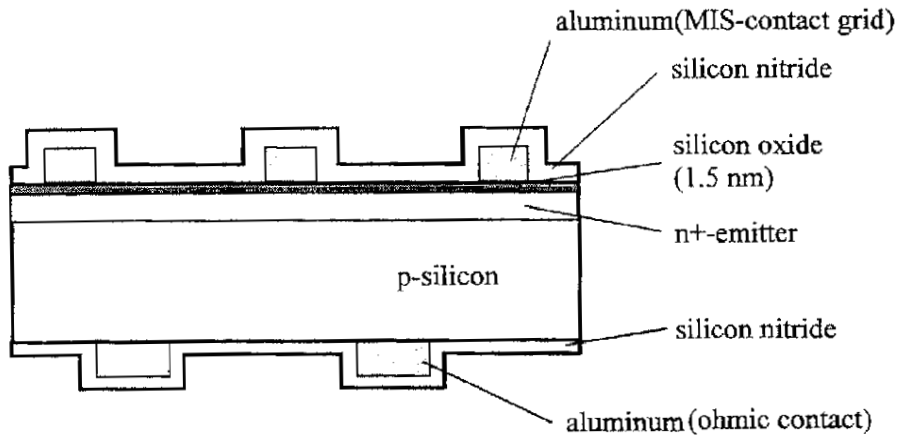


Figure 11: Schematic cross section of the bifacial MIS n^+p solar cell

2. V-Grooved MIS n^+p Solar Cells With Self-Aligned Metallization

In order to eliminate aluminum vacuum evaporation through a shadow mask, as used in the previous case, MIS contacted p-n solar cells are reported taking advantage of the self-aligning metallization technique of shallow angle vacuum evaporation /49/. As already mentioned, a much higher throughput and better utilization of the metal is achieved by this maskless method compared to the conventional perpendicular evaporation. However, a prerequisite for the shallow angle evaporation method is a grooved front surface, which simultaneously reduces light reflection. The cross section of this cell which is characterized by a mechanically grooved, mask-free metallized and low-temperature plasma-silicon-nitride passivated front surface, is shown in Fig 12.

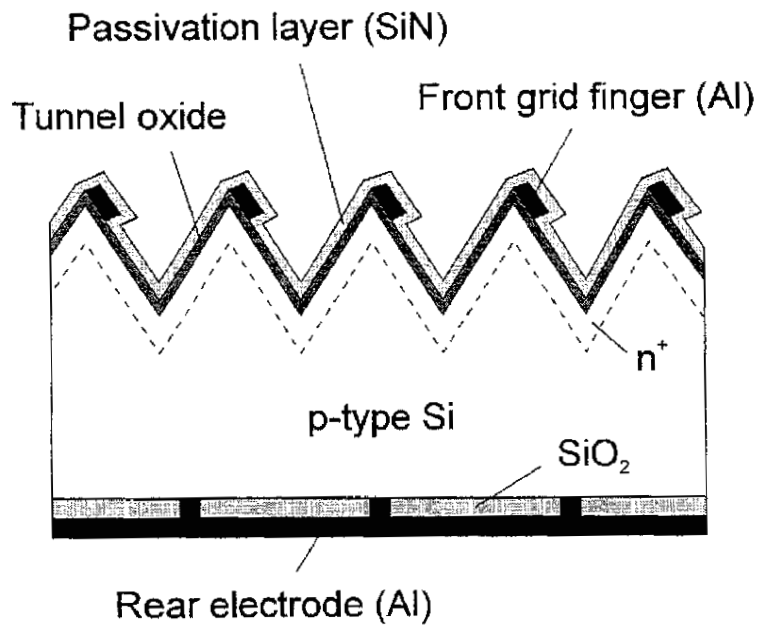


Figure 12: Schematic diagram of the MIS n^+p solar cell with mechanically grooved, mask free metallized and low-temperature passivated front surface.

Mechanical structuring of the wafers is performed using a conventional dicing saw, followed by a chemical etch. The tunnel oxide is grown at 500 °C for 15 min in an oxygen/nitrogen atmosphere. The rear surface was well passivated by thermal oxide in which point-like openings are etched.
As to the results, an independently confirmed one-sun efficiency of 18.6 % for the obliquely evaporated 4 cm^2 MIS-contacted solar cells could be achieved using float zone silicon. If a shadow mask was used for Al-metallization, an efficiency of 19.5 % was resulting, the highest value ever reported for MIS-contacted p-n junction cells using only aluminium for both front and rear electrodes. The higher efficiency is mainly due to the fact, that a finger spacing of 500 µm was used, whereas the shallow-angle evaporated cell had a higher shading loss due to a grid spacing of only 340 µm.

V. Conclusion

The high costs are presently the main obstacle for a world-wide increased utilization of electric power provided by photovoltaic solar cells. Since mass production with the present techniques is not sufficient to reach the cost level required to become competitive with the conventional energy sources, new concepts have to be introduced combining very high cell efficiencies with simple short-time processing, including cost effective materials.
Despite the progress achieved with thin film solar cells, crystalline silicon will keep its dominant role for a long time. Very high efficiencies up to 24 % have been achieved in the past with silicon solar cells, however, undoubtedly it`s evident that the sophisticated process required for these cells is not suitable for a cost-effective mass production. The MIS solar cells reviewed in this paper are, due to their simple time and energy saving fabrication process and their potential for very high efficiencies very promising candidates to make photovoltaics more economic.
As an important milestone clear evidence could be given by large scale application, that the basic elements for the MIS technology such as ultrathin tunnel oxide preparation and induced junction formation by positive insulator charges can reliably be fabricated on an industrial scale. For simple reasons outlined in this paper, efficiencies of the first generation of silicon MIS inversion layer solar cells are limited to values between 15% - 16 %. By the drastically improved surface passivation applicable with the novel concept of second generation MIS inversion layer solar cells, the way is open to reach efficiencies at least up to 20% using large scale fabrication methods. In addition, the MIS technology has been proven to be particularly suitable for using thinner wafers and efficiently utilizing also the light impinging on the rear side of bifacial solar cells. Thus, together with the price reduction for silicon wafers hopefully occurring along with mass production, MIS type silicon solar cells are very promising for drastically lowering the costs of solar electricity.

References

/1/ G.C. Salter and R.E. Thomas, Solid St. Electron. **20**, 95 (1977)

/2/ P. van Halen, R.P. Mertens, R.J. van Overstraeten, R.E. Thomas and J. van Meerbergen, IEEE Trans. Electron. Devices, **ED-25**, 507 (1978)

/3/ R.B. Godfrey and M.A. Green, Appl. Phys. Lett. **34**, 790 (1979)

/4/ R.E. Thomas, C.E. Norman and R.B. North, Conf. Record 14th IEEE Photovoltaic Specialists Conf., San Diego, 1980, p. 1350

/5/ R. Hezel, Solid St. Electron. **24**, 863 (1981)

/6/ R. Hezel and R. Schörner, J. Appl. Phys. **52**, 3076 (1981)

/7/ R. Schörner and R. Hezel, IEEE Trans. Electron. Devices, **ED-28**, 1466 (1981)

/8/ R. Hezel, Conf. Record 16th IEEE Photovoltaic Specialists Conf., 1982, p. 1237

/9/ K. Jaeger and R. Hezel, IEEE Trans. Electron. Devices, **ED-32**, 1824 (1985)

/10/ R. Hezel, W. Hoffmann and K. Jaeger, Proc. 10th European Photovoltaic Solar Energy Conf., Lisbon, 1991, p. 511

/11/ M. Alonso, R. Pottbrock, R. Voermans, J.J. Villard and B. Yordi, Proc. 12th European Photovoltaic Solar Energy Conf., Amsterdam, 1994, p. 1163

/12/ K. Mukadam, F. Chenlo, A. Matas, L. Rebello, M. Alonso, R. Pottbrock, R. Voermans, Proc. 13th European Photovoltaic Solar Energy Conf., Nice, 1995, p. 1770

/13/ ISE PV Charts, 30th Nov. 1994, Fraunhofer Institute FHG-ISE, Freiburg, Germany

/14/ G. Hagedorn, E. Höllriegel, BMFT Report No. 426-3590-PL/141, Forschungsstelle für Energiewirtschaft, München 1992, Germany

/15/ A.G. Aberle, B. Kuhlmann, R. Meyer, A. Hübner, C. Hampe and R. Hezel, Progress in Photovoltaics 4, 1996 (in press)

/16/ S.M. Sze, Physics of Semiconductor Devices, J. Wiley, New York 1981

/17/ M.A. Green and A.W. Blakers, Solar Cells **8**, 3 (1983)

/18/ R.B. Godfrey and M.A. Green, IEEE Trans. Electron. Devices, **ED-27**, 737 (1980)

/19/ M.A. Green, F.G. King, J. Shewchun, Solid St. Electron. **17**, 551 (1974)

/20/ J. Shewchun, R. Singh and M.A. Green, J. Appl. Phys. **48**, 765 (197)

/21/ C.E. Norman and R.E. Thomas, IEEE Trans. Electron. Devices, ED-27, 731 (1980)

/22/ P. de Visschere, IEEE Trans. Electron. Devices, **ED-30**, 840 (1983)

/23/ E.C. Heasell, Solid St. Electron. **27**, 475 (1983)

/24/ B. Kuhlmann, A.G. Aberle, and R. Hezel, Proc. 13th European Photovoltaic Solar Energy Conf., Nice, 1995, p. 1209

/25/ R. Hezel and K. Jaeger, J. Electrochem. Soc. **136**, 518 (1989)

/26/ A. Hübner, A.G. Aberle and R. Hezel, Conf. Record 25th IEEE Photovoltaic Specialists Conf., Washington DC, 1996

/27/ A.G. Aberle and R. Hezel, Conf. Record 25th IEEE Photovoltaic Specialists Conf., Washington DC, 1996

/28/ K. Jaeger and R. Hezel, IEEE Trans. Electron. Devices, **ED-32**, 1824 (1985)

/29/ R. Hezel and K. Jaeger, Solid St. Electron. **26**, 993 (1983)

/30/ M. Grauvogl, A.G. Aberle and R. Hezel, Conf. Record 25th IEEE Photovoltaic Specialists Conf., Washington DC, 1996

/31/ T. Lauinger, J. Schmidt, A.G. Aberle and R. Hezel, Appl. Phys. Lett. **68**, 1232 (1996)

/32/ W. Bauch and R. Hezel, Proc. 9th European Photovoltaic Solar Energy Conf., Freiburg, 1989, p. 390

/33/ R. Brendel and R. Hezel, J. Appl. Phys. **71**,(9), 4377, (1992)

/34/ R. Hezel, Technical Digest of the 1st PVSEC, Kobe 1984, p. 145

/35/ R. Bartels, A. Bierhals, A.G. Aberle and R. Hezel, Proc. 13th European Photovoltaic Solar Energy Conf., Nice, 1995, p. 1272-1275

/36/ R. Hezel, T. Meisel, W. Streb, J. Appl. Phys. **56**, 1756, (1984)

/37/ T. Lauinger, J. Moschner, A.G. Aberle and R. Hezel, Conf. Record 25th IEEE Photovoltaic Specialists Conf., Washington DC, 1996

/38/ R. Hezel, 1st World Conference on Photovoltaic Energy Conversion (24 IEEE PVSC Conf.), Hawaii, 1994, p. 1466

/39/ R. Hezel, Proc. 13th European Photovoltaic Solar Energy Conf., Nice, 1995, p. 115

/40/ R.A. Sinton and R.M. Swanson, Conf. Record 19th IEEE Photovoltaic Specialists Conf., New Orleans, 1987, p. 1201

/41/ M. Grauvogl, A.G. Aberle and R. Hezel, accepted for publication in Appl. Phys. Lett.

/42/ S. Shibuya, K. Okamoto, T. Namoriad, H. Itoh, Conf. Record 21st IEEE Photovoltaic Specialists Conf., Kissimimee USA, 1990, p. 664

/43/ G. Willeke, H. Nussbaumer, H. Bender and E. Bucher, Solar Energy Materials and Solar Cells, **26**, 345, (1992)

/44/ R. Hezel and R. Ziegler, Conf. Record 21st IEEE Photovoltaic Specialists Conf., Louisville, 1993, p. 260

/45/ M. Grauvogl, S. Friedrich and R. Hezel, Proc. 12th European Photovoltaic Solar Energy Conf., Amsterdam, 1994, p. 1807

/46/ R. Hezel, FORSCHUNGSVERBUND SONNENENERGIE, „Themen 95/96" Photovoltaic 3, p. 18 (1996), c/o DLR, D-51140 Köln, Germany

/47/ K. Jaeger-Hezel, W. Schmidt, W. Heit and K.D. Rasch, Proc. 13th European Photovoltaic Solar Energy Conf., Nice, 1995, p. 1515

/48/ M.A. Green, A.W. Blakers, J. Shi, E.M. Keler and S.R. Wenham, IEEE Trans. on Electr. Dev., **ED-31**, no. 5, p. 679 (1984)

/49/ M. Verbeek, A. Metz, A.G. Aberle and R. Hezel, Conf. Record 25th IEEE Photovoltaic Specialists Conf., Washington DC, 1996

Fine-line Screen Printing for Silicon Solar Cells

H.H.C. de Moor A.W. Weeber J. Hoornstra W.C. Sinke
Netherlands Energy Research Foundation ECN
PO Box 1 1755 ZG Petten The Netherlands
Tel: +31 224 564781 Fax: +31 224 563214 E-mail: demoor@ecn.nl

Abstract

The screen printing process is discussed, as it is applied for the front grid of a crystalline silicon solar cell. On the basis of modelling, it is shown that the challenge is to print fine lines of 50 µm width and 20 µm high. A review of the printing process, involving screen, paste and firing, shows where difficulties arise and how printing and firing parameters can be adjusted.
A variant of the screen printing technique, stencil printing, is presented. The use of a metal foil instead of a mesh screen can give the required lines. The technique, however, is not mature yet for solar cell applications.

Introduction

Metallization is one of the major cost determining and efficiency limiting steps in solar cell processing [1,2]. Industrial processing of crystalline silicon [3,4] is mainly based on two metallization techniques: screen printing [5,6,7,8,9,10] and plating [11,12,13,14]. Evaporation can be considered if the added value is substantial. In this paper the status of screen printing is reviewed, with emphasis on formation of the front grid.

-- Comparison of metallization techniques

Screen printing is a well established technology used for many applications, including printing soldering pads on PCB's (printed circuit boards). It has the advantage of a self-aligned, dry process: the front grid pattern is defined in only one process step, the metal paste is efficiently used and the environmental impact is small. A drawback is the cost of metal paste, as micrometer-sized silver particles of high purity are required, with a well controlled size distribution, and a paste composition designed for solar cell processing.
Plating on the other hand, involves general chemical baths, with only minor modifications, in use for a variety of low-cost processes. However, making the front grid of a solar cell involves an additional step in which the pattern has to be defined. This step is for example laser scribing [15], or lithography. The latter is considered expensive, as it consists of several operations. Laser scribing or mechanical grooving is an elegant method to define the front grid as it combines a selective emitter and buried contacts. Plating itself is a well-established production technology. In the case of solar cell manufacturing it involves many chemical baths, including electroless copper deposition, with a slow growth rate of only 3 µm/h.
Evaporation is a technique used for high-efficiency (laboratory) cells. In production it could be taken into consideration, if a full coverage is needed, as for the rear of the cell, if the efficiency improvement gives sufficient added value, or if a simple mask can be applied [16]. An elegant approach is evaporation of a grooved surface under a shallow angle. The grooves act as a mask, making it a self-aligned technique with hardly any reflection loss after encapsulation [17].
When choosing a metallization technique one should consider the total process sequence, the temperature requirements and the cell efficiency which is pursued. Screen printed contacts are fired at high temperatures, typically 700°C; plated or evaporated metallization is sintered at only 400°C. Not in all process sequences is a high temperature allowed.

-- Screen printing

In screen printing the reflection loss due to the front grid is important. Therefore it is necessary to reduce the metal surface coverage, while retaining good series resistance. Modelling shows that it pays off to develop very fine lines: 50 µm width and 20 µm height. However, this only applies if the contact resistance is low. Choosing a proper paste composition and emitter profile usually prevents a high contact resistance. Therefore a small line width combined with sufficient height is the first concern in screen printing.
In industrial screen printing the line width of the grid fingers has been reduced from 300 µm to 100 µm in recent years [8,18]. In the laboratory 50 µm has been achieved. However, yield and series resistance are still a problem. In this review, the background of this development will be evaluated as well as the items which are still under investigation.

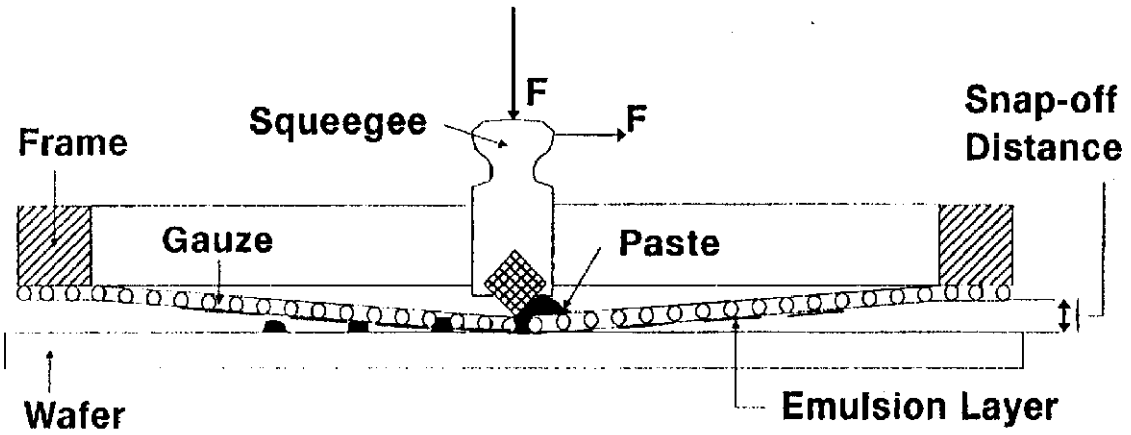


Fig. 1 Principle of screen printing

Figure 1 shows schematically the principle of screen printing. Paste is put on top of a patterned screen just before the squeegee, which forces the paste through the openings when moving from left to right. The screen is forced down by the squeegee onto the wafer. After the squeegee has passed, the screen relaxes to the original distance from the wafer: the snap-off. When the screen moves upwards, the paste releases from the screen and sticks to the solar cell.
The total process takes 5 to 10 seconds, which allows for a typical throughput of 500 wafers per hour. For a semi-automated line, in principle, one operator can control the printing process and the subsequent firing of the metallization. The high throughput and yield combined with a moderate cost of ownership and cost of the consumables makes it a low-cost technique, well suited for present production volumes.

Screen

The screen consists of a stainless steel wire gauze mounted in an aluminium frame. The stainless steel mesh is stretched over the frame with a screen tension of typically 25 N/cm. The stress, which is introduced in the screen, gives the screen the possibility to resist the force applied by the squeegee and to relax back to the original position. A higher stress in the screen gives in principle a better sticking of the paste to the substrate as it allows a higher squeegee pressure.

-- Wire gauze

In fine-line screen printing typically a 325 mesh or higher is used [8]. In fig. 2b it can be seen that the opening in the emulsion layer becomes critical when the line width is in the order of the pitch (for a 400 mesh screen 65 µm). In this case, the percentage of open area fluctuates significantly, especially if the small "triangular" openings near the emulsion edge contribute little to the paste supply onto the wafer. Non-uniformity in the open area causes fluctuations in the amount of paste lengthways of the metal lines.
The fabric is oriented 45° with respect to the frame, in order to have a uniform distribution of nodes in the open line and to have equal stress for both the perpendicular set of wires.
The use of thinner wires or increasing the wire distance, improves the uniformity of the metal paste deposited and reduces the chance of paste not releasing from the screen. The strength of the wire gauze, however, decreases, reducing the lifetime of the screen and the maximum squeegee pressure, considerably.

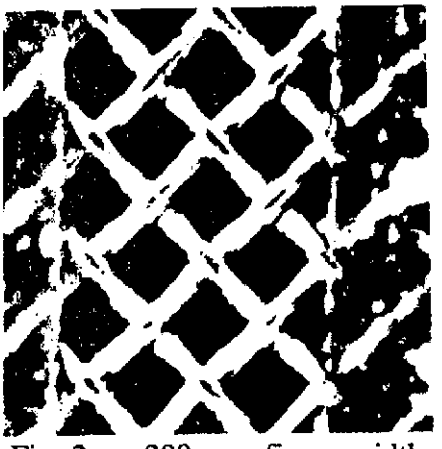


Fig. 2a 200 µm finger width

Fig. 2b 50 µm finger width

-- Emulsion layer

The pattern of the metal grid is based on the openings in a light-sensitive emulsion layer. A uniform photo resist layer is built up at the substrate side and pressed into the wire gauze. A typical emulsion thickness is 15 µm under the screen. A positive transparency (metal pattern: black) is laid on the emulsion layer and illuminated with a powerful UV lamp. The exposed areas become hard and the grid pattern can be washed out.
For fine-line screen printing it is strongly recommended to process the emulsion layer in a dust controlled area. If the width/thickness ratio is small, it is important to have a good parallel light beam. This gives a straight slope in the emulsion layer, which is preferable. It is essential to wash the non-exposed areas very carefully, since residues can obstruct the metal paste during the printing.
In fine-line printing the emulsion layer is an important factor in improving the height of the metal fingers. It increases the printing volume and levels height differences.

Fig. 3 Paste deposit as a function of the screen opening
A Screen B Emulsion C Paste D Wafer

The maximum amount of paste which can be deposited on the substrate depends on the volume between the wire gauze and the volume in the emulsion layer. For a 400 mesh screen the open area is 40%, and the thickness 50 µm; this results in a theoretical thickness of 20 µm. The thickness of the emulsion layer in principle adds to this.
Two effects reduce this maximum amount of paste

- the paste adheres to the wire mesh and the emulsion layer
- the screen is bent, reducing the distance to the wafer far from the emulsion layer

The final height of a fine-line is also affected by slump. Typically the width increases by 20 µm.

The cleaning of the screen after the printing should be done carefully. No paste should remain in the screen. If so, it is almost impossible to remove the dried paste during the next printing session, thus giving interruptions. Normally the emulsion layer dissolves in water, so a special screen wash or waterfree ethanol should be used. One should take care that the emulsion layer does not swell up, become soft or roughen due to the cleaning. As a inevitable result of wear of the emulsion layer at the substrate side, the line width typically increases 10 µm compared with the first printed lines.

Paste

The silver paste used for the front grid basically consists of microsized silver particles, glass frit, a solvent and a binder. This should take account for the basic requirements:

- high aspect ratio (height vs width)
- low contact resistance between silver and silicon
- low resistivity of the metal lines
- good mechanical adherence of the busbars to the silicon

-- Silver

Typical front side paste contains about 70% silver. As can be seen in fig. 4, silver is present as very fine spherical particles, 1 to 2 µm, and flakes (only a small fraction), which are about 5 µm. The silver particles have a great tendency to agglomerate, therefore clogging of a fine mesh screen is a serious danger. As a rule of thumb, the particle size should be less than 1/5 of the openings in the screen.
The choice of the solvent is important as to prevent too much interaction between the silver particles. The printing of fine lines would be much easier if only spherical particles are present. The flakes, however, are a necessity as they contribute in decreasing the contact resistance between silver and silicon and prevent blistering of the fired silver lines.

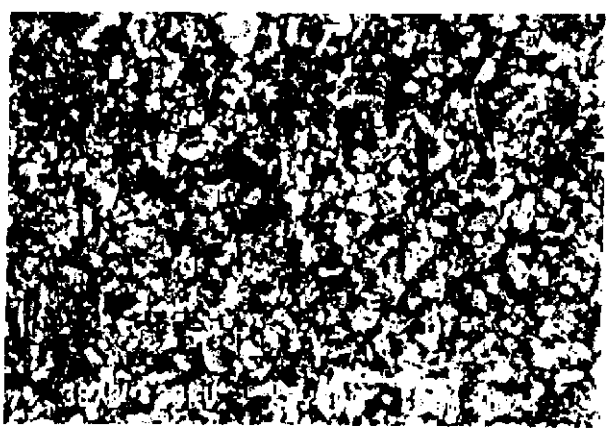


Fig. 4 SEM photo of Ag paste

-- Frit

Glass frit is added to the paste, 2-5%, to enhance the sinter activity and to establish good mechanical adhesion of the metallization to the silicon surface [19]. Frit is a mixture of metal oxides (including SiO_2), melted to a uniform glass. The glass is milled to a thin sheet and crushed.
Normally the most important ingredient of the blend is lead oxide. Other components can be oxides of boron, bismuth, aluminium, copper and titanium. Phosphorous can be added to enhance the contact with the n-type emitter.
In fig. 5 it can be seen that the larger particles in the metal paste are frit (Pb). It would be advantageous to reduce the size of the frit particles.

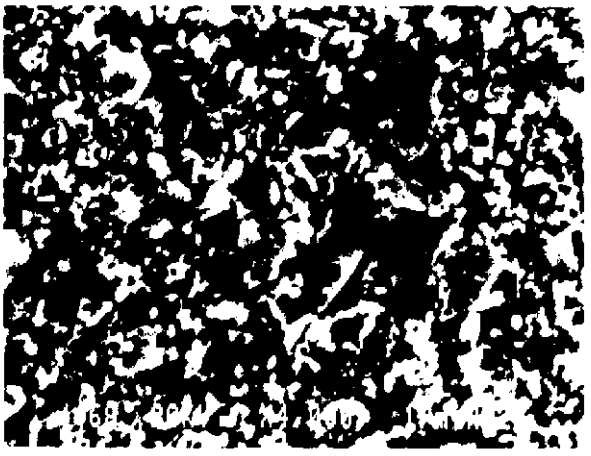


Fig. 5a SEM photo of silver paste

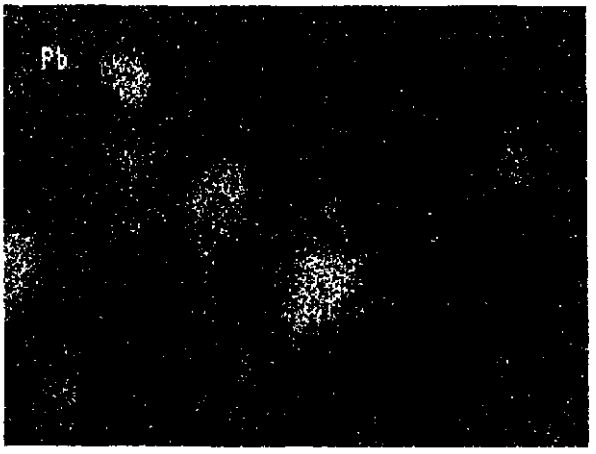


Fig. 5b Microprobe image of identical spot

-- Solvent and binder

The main purpose of binder and solvent is to give the metal paste the rheological properties needed to have good printing behaviour. Essentially viscosity of the paste should be low, when it is pressed through the openings in the emulsion layer, and it should be high, when the screen has moved upwards. The paste must be pseudoplastic, a viscosity decreasing with an increasing shear stress, and thixotropic, keeping its low viscosity for a given time.
The dynamic response to the applied shear stress is critical. When the paste is put on the screen its viscosity must decrease fast, due to squeegeeing, in order to roll on the screen and flow through the screen openings easily. It helps to put only a small amount of paste in front of the squeegee, as the motion is more intense then. As the squeegee has passed, the screen lifts. Then the paste should release easily from the stainless steel wires and adhere to the wafer. The viscosity should be low in the first instance, 10 - 20 seconds, to level off the metallization (at some parts the supply of paste is high as no wire is present, at some it is very low due to nodes). But the relaxation time of the paste should not be too long, as the paste flows in all directions, also giving line broadening.

Printer

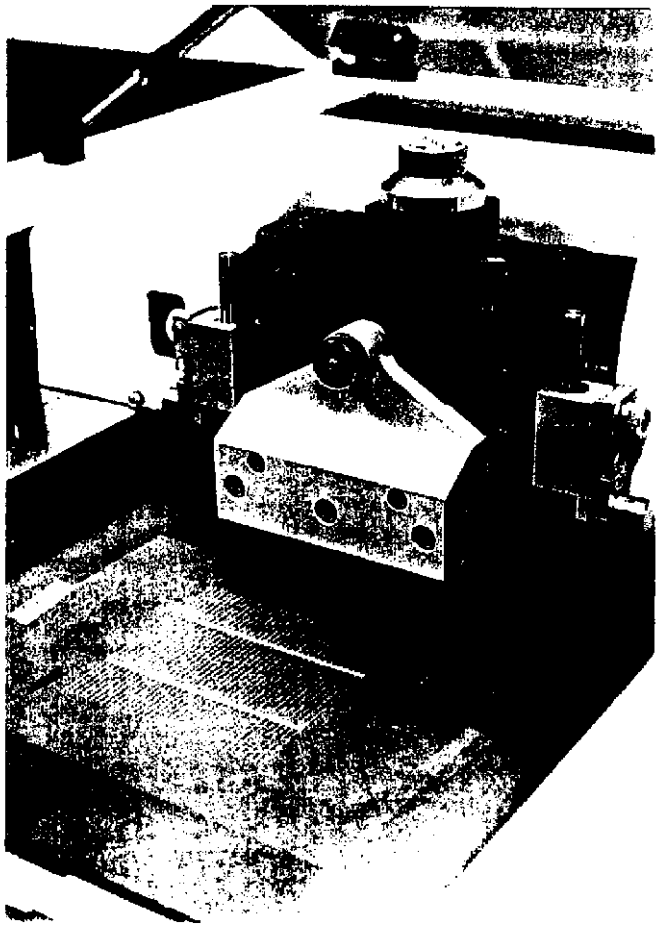


Fig. 6 Photo of a screen printer used at ECN

Due to these high demands a state of the art screen printer line is placed in a dust and temperature controlled area. Large dust particles can give blocking of the screen or interruptions of the metal fingers. Further the temperature plays an important factor in the rheological behaviour of the metal paste.
The screen printing process starts with depositing a small amount of paste, which is stirred in the jar to lower the viscosity, about 3 cm before the pattern. The squeegee is in the upward position and the screen and wafer are separated by approximately 1 mm: the snap-off distance. The exact setting is dependent upon the tension of the screen. The squeegee comes down before the paste and a pressure of 100 N/m is applied. In a few seconds the squeegee moves over the pattern, pressing the pasta through the openings. A few cm behind the pattern the squeegee is lifted and can be used to print the next wafer (in the reverse direction).
The printing direction is parallel to the fingers, as this improves the line definition. If printed perpendicularly, paste is easily pushed under the screen. The reproducibility of the positional accuracy can be better than 10 µm, which is important if a selective emitter is used.
Height differences larger than 15 µm perpendicular to the metal fingers are difficult to overcome. Without special precautions screen printing is restricted to really flat substrates [20].

The most important parameters to be set in the printing process are:
- snap-off distance
- squeegee pressure
- squeegee speed

The snap-off determines the upward movement of the screen, when the squeegee has passed. The forces accompanied with this motion lower the viscosity of the paste, which is then able to release from the wire gauze.
If the snap-off distance is too small, the paste will not release from the screen, if it is too large the squeegee pressure needed to push the screen to the wafer must be too high. This decreases the tension in the screen, reducing the life time.

-- squeegee

For screen printing a rubber (polyurethane) squeegee is commonly used. The cross-section is often of the diamond type: square and mounted under a 45° angle (see fig. 1), such that a sharp edge touches the screen. Also the trailing edge type is used, a rectangular strip of rubber mounted with the short side parallel to the wafer. Important is that screen and squeegee are mounted exactly parallel to the wafer.
For fine-line screen printing the hardness of the squeegee is typically 60-80 Shore. If the squeegee is too soft it follows the shape of the screen exactly and scoops paste out of the fingers. If the squeegee is too hard, it can not follow the roughness of the wafer and the paste is not supplied uniformly.

- speed

The squeegee speed which can be applied depends on the thixotropic behaviour of the metal paste and determines the amount of paste which is deposited. A typical speed to obtain fine and high lines is 2 cm/s. If the speed is too high the paste has too little time to fill the openings in the screen and too little time to release from the screen, which may cause interruptions. At very high velocities, 25 cm/s, the viscosity reduces so drastically that it becomes more easily to fill the openings [8].

- pressure

It is necessary to force the squeegee downwards to overcome the snap-off distance and to press the paste through the openings. If the emulsion layer is thicker, then the squeegee pressure should be increased.
If the pressure is too low the squeegee will not follow the roughness of the wafer and the paste is not supplied uniformly. This is a problem, especially if the squeegee is not parallel to the wafer. Poor release of the paste from the screen is a threat, as the paste might dry and cause clogging of the screen.
If the force is too high the squeegee scoops the paste out of the fingers, the emulsion layer might be compressed and the wear of the screen may be significant, reducing the life time.

Firing

After the cell has been printed, the metal paste has to be fired. This is done in a belt furnace, at present typically infrared heated. Essentially this is a three step process:

- Drying
- Burn-out
- Firing

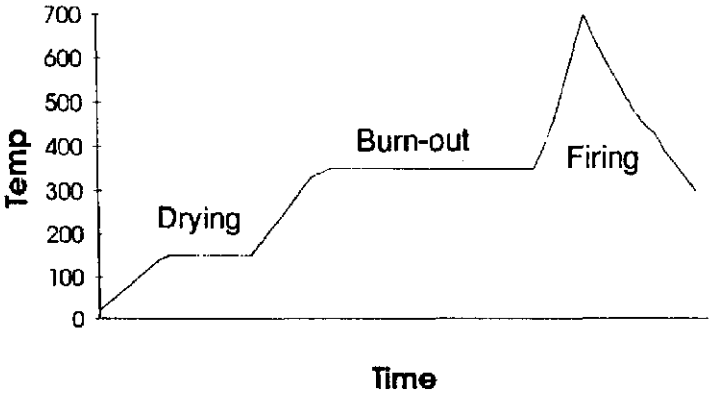


Fig. 7 Schematic temperature profile in a belt furnace

-- Drying

First the organic solvents should evaporate. Normally drying is performed using infrared heating in the first section of the belt furnace at 150°C for 1 minute. It is important to evaporate all the solvent, otherwise it causes gas bubbles at higher temperatures, resulting in cracking of the metallization. This may happen if the outside is dried too fast, forming a crust which can not be permeated by the solvent.
Typically it takes a few minutes between the printing and the wet paste entering the drying zone. In this time the paste might slump. It is important to prevent exposure of the wafers to elevated temperature prior to infrared drying, because of crust formation and slump.

-- Burn-out

At a temperature of 300 - 400°C the organic binders are burned. A sufficient air flow must be used to obtain complete oxidation of the organic components. As the resulting metal residue is quite porous this step is not critical. Excessive burning however, should be avoided as the gas bubbles could give cracks. The temperature is not critical, it could also be a gradual increase instead of a plateau.

-- Firing

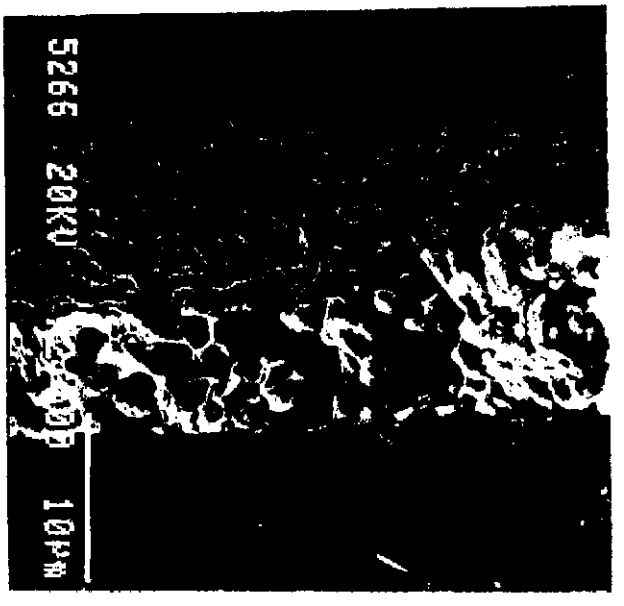


Fig. 8 SEM photo of fired metallization

The sintering or firing takes place at temperatures around 700°C. The profile is peaked here. The cell is only 30-60 seconds at a temperature less than 50°C from the peak. As a rule of thumb, it is best to fire fast and hot. The upward slope may be up to 50°C/s, the downward slope could better be set slower to prevent detachment of the silver, due to differences in expansion coefficients. A danger of firing screen printed contacts is that in cooling down from high temperatures point defects in the solar cell can be trapped.

In fig. 8 can be seen that the resulting metallization is porous, the individual metal particles cannot be distinguished anymore. The volume of the fired metallization is reduced by a factor of 2-3 compared to the volume of the wet paste.
The sinter activity of silver is increased by the frit [19]. Slightly below T_peak the frit melts; the exact temperature depending strongly on the frit composition. In the molten frit silver can dissolve and thus the silver can be "transported" very effectively: the silver particles are sintered. The frit also etches the silicon and a TiO_2 anti-reflection coating, if present. A typical etching depth is 0.1 µm. This can be seen in a SEM cross section (fig. 9). At the arrow a depression in the silicon (black) can be seen; in the upper part silver is present at the silicon surface (etching), in the middle silver is absent. The etching of the silicon accounts for the adherence of the metallization to the wafer.

Fig. 9

A cross-section of the silver-silicon interface

Right side (black) silicon
Left side (grey) metallization

A microprobe analysis of this wafer shows that the frit agglomerates at the silicon surface. In the metallization Pb is present in the percentage range. At the silicon surface it increases to 25%.
At the Ag/Si-interface (the spot was mainly on the Ag) no titanium is detected. This could be reproduced, indicating that the TiO_2 is etched away.

Table 1 Microprobe analysis of cross-section Ag on TiO_2(80 nm)/Silicon (fig. 9)

Element	Metallization	Ag/Si interface	Si surface no metallization
Si (%)	1.4	5	72
Ag (%)	98	66	2.8
Pb (%)	0.9	28	23
Ti (%)	0	0	3

The frit tends to form an isolating layer between the metallization and the silicon wafer, resulting in a high contact resistance. At higher temperatures the frit layer becomes thicker. On the other hand at low temperatures there is too little sintering, giving a low contacting area between silver and silicon. As sketched in fig. 10 there is an optimum in the fill factor, ranging between 75 and 78%.

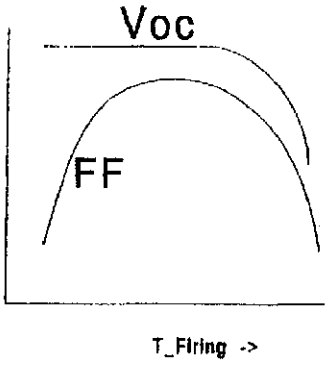


Fig. 10 Schematic influence of firing temperature on FF and Voc

As depicted in fig. 10, Voc decreases with temperature. This is due to impurities in the depletion region. The frit etches silicon, decreasing the distance to the depletion region, impurities from the frit and silver itself diffuse into silicon [21,22] and impurities are segregated into silicon when the frit recrystallizes [19].
There could be an "optical effect" [23] in this impurity incorporation and diffusion. It has been experienced that for a paste critical with respect to impurities, for a given thin emitter, firing in a resistant heated furnace gives good cells, while a significant impurity effect is observed in an infrared heated furnace.

Optimizing the firing process means finding conditions where Voc still is unaffected and the fill factor reaches its maximum value. Whether such a point gives good cells depends on the frit composition and the emitter profile. Firing fast and hot which is considered to be best, means that the impurities do not get the chance to diffuse, while the sintering is already effective. The activation energy for impurity transport obviously is in general lower than for sintering.

Emitter

It is essential that the emitter profile is taken into account when optimizing the firing process [24]. In case of screen printed metallization a heavily doped surface is necessary to obtain a reasonable contact resistance. This means that a shallow emitter must be used, whereas with plated or evaporated contacts, a rather deep, moderately doped, emitter should be applied.

In fig. 11 a typical emitter profile is given [25]. It shows a very high doped region, with a thickness of 0.1 µm, and an emitter which is in total 0.5 µm. One should realize that due to the etching of the frit the contacting surface has a lower dopant concentration than the original surface. For an etch depth of 0.05 µm it is still $3x10^{20}$ cm^{-3}, for 0.1 µm it is $2x10^{19}$ cm^{-3} and for 0.2 µm it is only $5x10^{18}$ cm^{-3}.
For this emitter it is recommended to use a mild frit which only etches 0.05 µm. It is also important to use a frit which wets the silicon well. This means that the etching is uniform. If locally more frit is present, the etching is deeper at these points and could eventually cause local shunt paths.

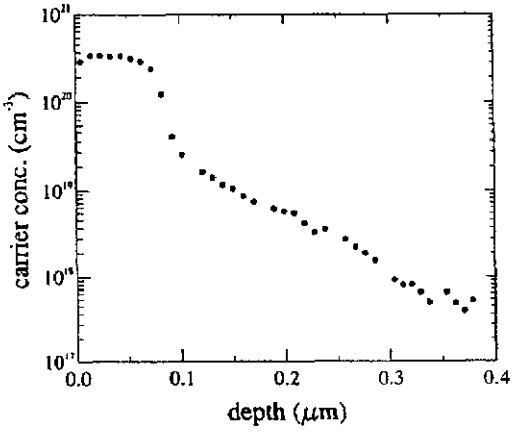


Fig.11 The active doping profile of a 43 Ω/□ emitter, $POCl_3$ diffused [25] (Stripping Hall)

A good method to evaluate the etching behaviour is to print a uniform layer of e.g. 1 cm^2, on a polished wafer. After firing, the metallization is carefully etched off. The silicon should not be etched. With a step profiler the roughness can be measured, indicating the possibility of local shunt paths. For multicrystalline material in particular, it can be expected that the frit etches faster at the grain boundaries and dislocations [26]. The etch depth can be determined by measuring the step height at the edge of the metallized and bare regions. If the emitter profile is known, then the sheet resistance of the formerly metallized region also gives an indication of the etch depth.

Modelling screen printed metallization

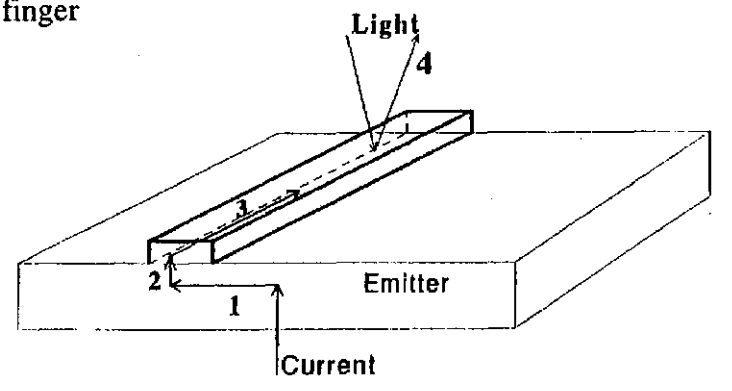
Optimizing screen printed metallization is basically finding a compromise between reflection and ohmic losses. To find the optimum and to get understanding of all the relevant factors a computer program has been developed [27,28].

Fig. 12 Current flow to and in a metal finger and reflection of light

Basic loss factors:

Resistance
1 Emitter
2 Contact Ag-Si
3 Metal (fingers and busbars)

Reflection (4)



The basis for the calculations is an assessment of the fundamental parameters:

- reflection coefficient for the metallization
- sheet resistivity of the metallization
- contact resistance
- sheet resistance (also under the metallization)

These parameters have been determined for a typical state of the art (multicrystalline) silicon cell: 15% efficiency, 100 µm finger width, 10x10 cm^2, encapsulated and tabbed (table 2).

Table 2 Parameters for the grid optimization

Cell	
Vmp	500 mV
Isc	3 A
R_emitter	40 Ω/□*

Metal		
	Fingers	Busbars+ Tabs
number	51**	2
width (µm)	100	2000
Rc (Ωcm^2)	5	
R_Ag (Ω/cm) R_tab	0.75	0.015 0.001
Reflectivity	75%	100%

* Under the fingers the sheet resistance of the emitter increases to 100 Ω/□.
** The number of fingers is optimized for this set of data.

The light reflected at the fingers is partly (25%) reflected back into the cell at the glass-air interface. This value is established by measuring the reflection before and after encapsulation.
The tab is assumed to be mirror like, giving no back reflection into the cell.
The line resistivity for a busbar is 0.015 Ω/cm, which gives a bulk resistivity of $3x10^{-8}$ Ωm for a typical height of 10 µm and width of 2 mm; to be compared with pure silver: $1.59x10^{-8}$ Ωm. The porous structure gives an increase in resistivity of a factor 2.
The bulk resistivity of the fingers is $7.5x10^{-8}$ Ωm. The, experimentally observed, increase compared with the busbars is due to a slightly smaller height and the non-uniformity of the fingers. The height and width are not constant due to the influence of the wire gauze on the deposited amount of paste.

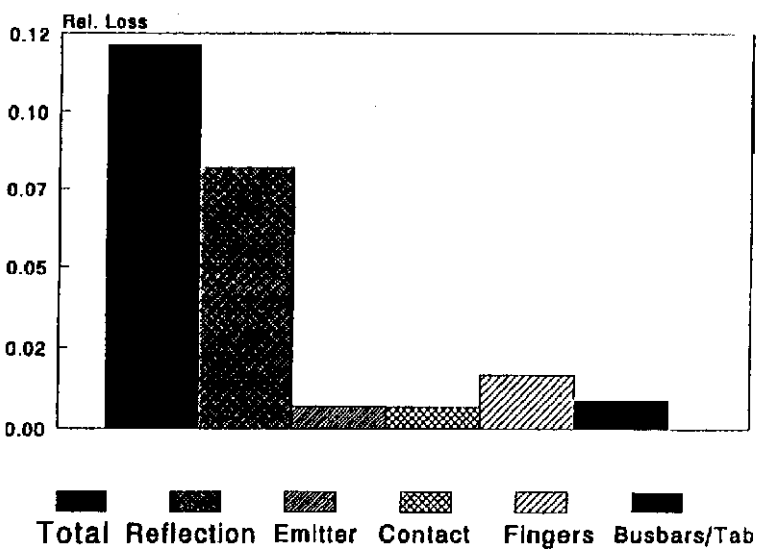


Fig. 13 Loss factors for a 15% cell 10x10 cm^2
100 µm finger width

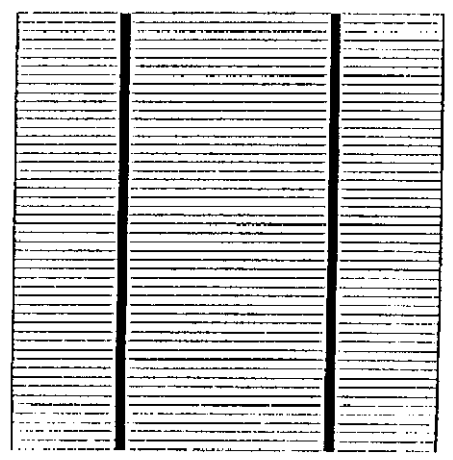


Fig. 14 Front grid pattern
used for fig. 13

In fig. 13 it can be seen that the reflection loss accounts for 2/3 of the total loss. Busbars and fingers contribute 4% each to the total power loss.
For the busbars a solution could be to give them a triangular cross section [29]; most of the light reflected at the busbars reenters the cell by internal reflection at the glass-air interface.
For the fingers it would be best to reduce the number and the width and meanwhile increase the height. An alternative approach is to use the concept of buried metallization. With screen printing it is difficult to align with the grooves and to fill them, plating is more suitable [15,20].

In fig. 15a can be seen that striving for fine lines only makes sense if the contact resistance is low. In these calculations a sheet resistance of 60 Ω/□ is assumed. For a high efficiency surface passivated cell this is a typical emitter. For this range of sheet resistances it is difficult to obtain good contact resistances at present. (The other data are in principle from table 2)

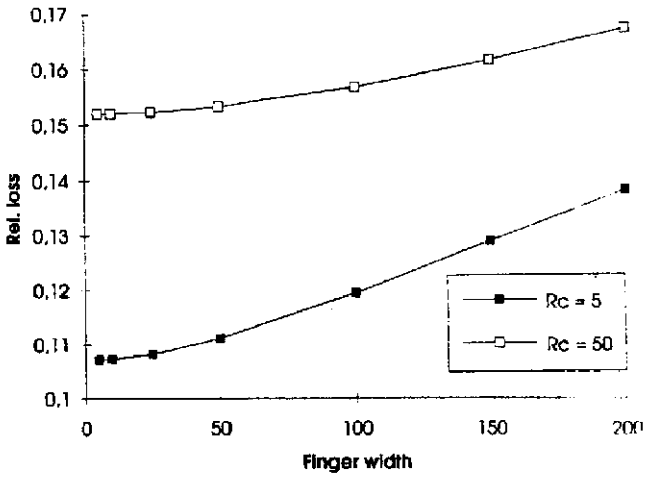


Fig. 15a Power loss as a function of line width
Contact resistance: 0 and 50 mΩcm^2
R_sheet(Ag) constant (height)

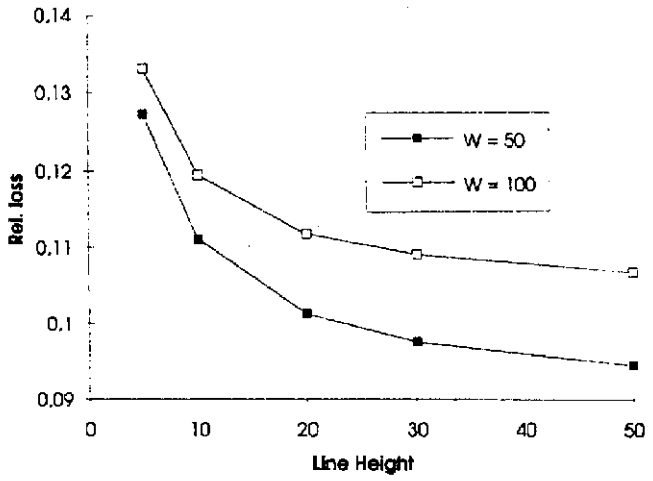


Fig. 15b Power loss as a function of line height
Finger width 50 and 100 µm
R_sheet(Ag) proportional to height

In fig. 15a can be seen that for an Rc of 50 mΩcm^2 (FF is 3% lowered) reducing the line width below 100 µm is of little use, for small contact resistances it is worthwhile down to 50 µm.
For a 50 µm fine line a height of 20 µm is required to take advantage of the small line width.

Cell processing

In the laboratory it is possible to print metal lines up to 50 µm. However, to do this routinely at a high throughput and yield is not yet feasible. A realistic target should be 100 µm.
For a standard paste the line width on the wafer is 20 µm larger than in the screen. This could be reduced by taking a more viscous paste which does not slump. However, such a paste can not be printed reliably as yet. The high viscosity of the paste prevents the levelling off which should happen directly after the screen has moved upwards. The deposit on the wafer directly reflects the presence of the wire gauze and the chance for clogging of the screen and interruptions in the finger pattern is very high.

The height should be preferably about 20 μm as fired. At this moment 10 to 15 μm is typical for a 100 μm fine line. This can be increased by choosing a thicker emulsion layer, although this is at the expense of some line broadening and more difficulties to fill the screen completely. Going to smaller line widths, retaining the height is still a challenge.
A difficulty which is observed is the decrease of the contacting area due to the surface tension of the wet paste (the line is smaller at the surface than slightly above).
A possibility to overcome the difficulties mentioned above is the use of metal stencils. This will be discussed in the next chapter.

Not only the power loss due to the metallization is a point of concern. Also the integration of the screen printed contacts in the process flow is a very interesting topic [30]. It is important that the metallization process does not influence the material quality and the surface passivation. Not only the overall cell efficiency, but also the simplicity of the process is a major topic, as cost reduction is crucial to solar cell manufacturing [31].
A simple production flow can be based primarily on screen printing [32]. It can be applied for making the emitter as well as the AR-coating. The back contact may consist of aluminium, giving a back surface field [33] and Ag/Al upon which to solder the busbars. The whole metallization, consisting of three different pastes can be fired simultaneously.

The crucial factor in all process scenarios is preservation of material quality (Voc) and, if introduced, surface passivation, while obtaining a low contact resistance. This means a simultaneous optimization of paste composition (frit) and emitter to the firing conditions, which are tolerated by the cell in the given state of processing.

Stencil printing

The policy in finding new printing techniques, which might be applied for solar cell processing, is to adapt well-known production technology to solar cell requirements. This means that techniques used to print large surface areas must be upgraded. Two techniques are considered promising nowadays: offset printing and stencil printing.
Offset printing is still in its early stage of development with respect to thick film applications, although interesting results are obtained with roller printing [34].
Stencil printing is widely used in PCB processing. The requirements with respect to width are less stringent than for solar cells, the length of the metal lines is less. On the other hand the thickness of the soldering pads is much higher, which is a major issue for the front grid of a solar cells.

In stencil printing a metal foil is used, instead of a mesh screen, with openings at places where the paste has to form the front grid. For a PCB stencil the openings are rectangular, with a length never longer than a few millimetres. For a solar cell the front grid consists of long continuous lines. As can be seen in fig. 14, where the white parts are the metal, no single-layer stencil is possible. The metal (white) parts will remain as loose strips.
One solution is the omit the busbars and give the fingers a length of only 24 mm (fig. 16a). A more elegant solution is to build the stencil up in two layers, one with the openings (emulsion layer) and one with bridges crossing the openings (the wire gauze) (fig. 16b). The advantage over a mesh screen is that only "wires" are present at the openings. The rest of the stencil is rigid. Another advantage is that openings and bridges can be aligned easily. The blocking therefore is far less than for a mesh screen, allowing more viscous pastes.

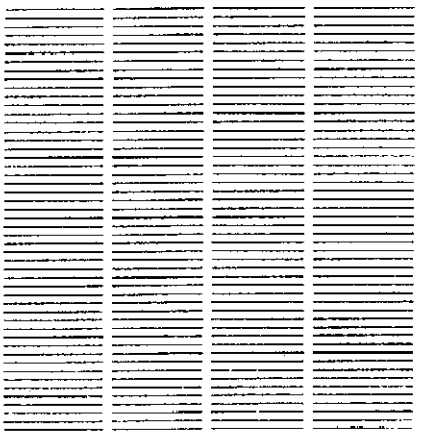


Fig. 16a Grid pattern used for a single-layer stencil

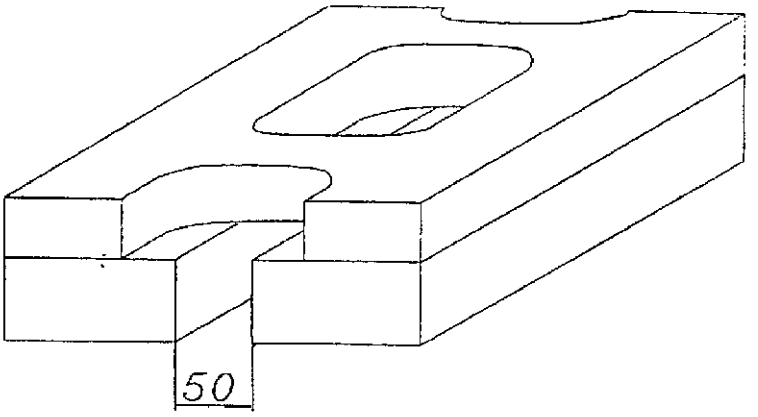


Fig. 16b Double-layer stencil
Upper layer strength (bridges)
Bottom layer line definition

The use of viscous paste is very advantageous to prevent slump. In fig. 17 the influence of the viscosity on the aspect ratio can be seen. Stencil printing is able to produce fine lines having a width of only 50 µm and a height of 20 µm as fired.
At this moment stencil printing is not a mature technology for solar cell processing. Effort is still needed in both paste and stencil development.

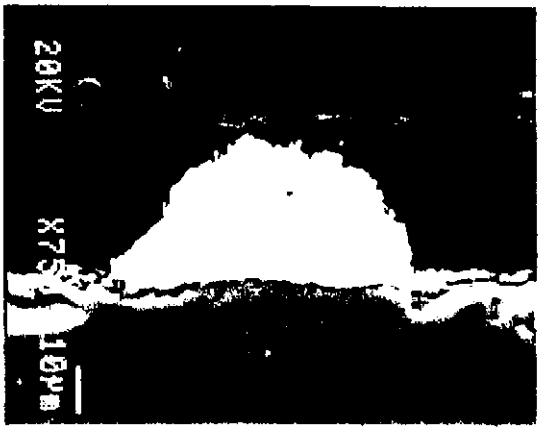


Fig. 17a High viscosity paste
Height 22 µm
Width 54 µm

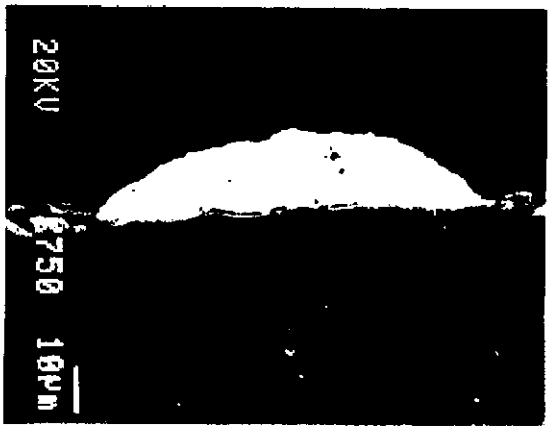


Fig. 17b Standard paste

Conclusions

There has been a lot of progress in recent years. In the laboratory a line width of 50 µm has been achieved. This is not due to a single factor but the result of a gradual improvement in screen manufacturing, accuracy of the screen printers, composition of the metal paste and last but not least the skill and experience to take advantage of the improvements.
A low-cost process scenario which includes surface passivation is still something to look for.

The knowledge gained in the laboratory has to be transferred to industry. Paste and screen development is needed to add reliability to the technology.
Screen manufacture could be improved in the field of the emulsion technology. It is important that a thick emulsion can be made with very fine lines in it, having a straight slope and no residue in the wire gauze. Also, improvement of the life time of the emulsion layer and the ability to clean the screen is worthwhile.
Paste development should include better tuning of the rheology to the printing process, decreasing the size of the largest particles and tuning the frit composition to the process requirements and emitter profile. For this, close interaction between paste manufacturers and solar cell researchers is a requirement.

Acknowledgements

The authors would like to thank for financial support ECN (Long-Term Energy Research Programme) the European Commission (Joule-project DOLMET Development of Low-cost Metallization for silicon solar cells JOR3-CT95-0040) and the Netherlands Agency for Energy and Environment (Novem)

References

1 S. Narayanan and J.H. Wohlgemuth Progr. Photovolt. 2 (1994) 121-128
2 J.H. Wohlgemuth, S. Narayanan and R. Brenneman Proc. 21th IEEE PVSC (1990) 221-226
3 J. Nijs Int. J. Solar Energy 15 (1994) 91-122
4 S.R. Wenham and M.A. Green Progr. Photovolt. 4 (1996) 3-33
5 R.J. v Overstraeten and R.P. Mertens *Physics, Technology and Use of Photovoltaics* Adam Hilger, Bristol (1986) ch 4
6 L.A. Verhoef, P-P. Michiels, R.J.C. v Zolingen, H.H.C. de Moor, A.R. Burgers, R.A. Steeman and W.C. Sinke Proc. 1th WCPEC (1994) 1547-1550
7 J. Nijs, E. Demesmaeker, J. Szlufcik, J. Poortmans, L. Frisson, K. De Clercq, M. Ghannam, R.P. Mertens and R. v Overstraeten Proc. 1th WCPEC (1994) 1242-1249
8 A. Dziedzic, J. Nijs and J. Szlufcik Hybrid Circuits 30 (1993) 18-26
9 H. Nakaya, M. Nishida, Y. Takeda, S. Moriuchi, T. Tonegawa, T. Machida and T. Nunoi Sol. Energy Mat. Sol. Cells 34 (1994) 219-225
10 S. Roberts, T.M. Bruton, D.W. Cunningham, K.C. Heasman, N.B. Mason and R. Russell Proc. 13th EPSEC (1995) 1409-1411
11 M.A. Green, S.R. Wenham, C.B. Honsberg and D. Hogg Sol. Energy Mat. Sol. Cells 34 (1994) 83-89
12 M.A. Green *Silicon Solar Cells Advanced principles & Practice* Bridge Printery, Sydney (1995)
13 K.A. Münzer, K.T. Holdermann, H.L. Mayr, R.E. Schlosser and H.J. Schmidt Proc. 12th EPSEC (1994) 753-756
14 T.M. Bruton, K.C. Heasman, J.P. Nagle, D.W. Cunningham, N.B. Mason, R. Russell and M.A. Balbuena Proc. 12th EPSEC (1994) 761-762
15 S.R. Wenham, C.B. Honsberg and M.A. Green Sol. Energy. Mater. Sol. Cells 34 (1994) 101-110
16 W.K. Schubert, D.S. Ruby, P.A. Basore, J.M. Gee, M.E. Buck and H.L. Tardy Proc. 1th WCPEC (1994) 1327-1330
17 P. Fath and G. Willeke Proc. 12th EPSEC (1994) 1037-1040

18 K. Fukui, H. Yamashita, M. Takayama, K. Okada, K. Masuri, K. Shirasawa and H. Watanabe Proc. 22th IEEE PVSC (1991) 1040-1044
19 G.C. Cheek, R.P. Mertens and R.J. v Overstraeten IEEE Trans. on Electron Devices Vol. ED-31 (1984) 602-609
20 P. Fath, E. Bucher, G. Willeke, J. Szlufcik, J. Hörzel, J. Nijs and R. Mertens Proc. 1th WCPEC (1994) 1543-1546
21 L. Frisson, G.C. Cheek, R.P. Mertens and R.J. v Overstraeten Proc. 5th EPSEC (1983) 1002-1006
22 H. El Omari, J.P. Boyeaux and A. Laugier Proc. 25th IEEE PVSC 1996 (Washington DC)
23 B.L. Sopori, C. Marshall, D. Rose, K.M. Jones, R. Reedy and S. Asher Proc. 23th IEEE PVSC (1993) 97-100
24 K. De Clercq, L. Dupas, J. Szlufcik, L. Frisson, J. Nijs and R.P. Mertens Proc. 13th EPSEC (1995) 17- 22
25 P. Lölgen, C. Leguijt, L.A. Verhoef, W.C. Sinke, J.A. Eikelboom, R.A. Steeman and H.H.C. de Moor Proc. 12th EPSEC (1994) 544-547
26 R.P. Mertens, G.C. Cheek, P. DePauw and L. Frisson Proc. 5th EPSEC (1983) 976-983
27 A.R. Burgers, H.H.C. de Moor, W.C. Sinke and R.A. Steeman Proc. 23th IEEE PVSC (1993) 340-346
28 A.R. Burgers, H.H.C. de Moor, W.C. Sinke and P-P. Michiels Proc. 12th EPSEC (1994) 1033-1036
29 J. Hörzel, K. De Clercq, O. Evrard, J. Szlufcik, L. Frisson, F. Duerinckx, J. Nijs and R. Mertens Proc. 13th EPSEC (1995) 1368-1373
30 J. Szlufcik, K. De Clercq, P. De Schepper, J. Poortmans, A. Buczkowski, J. Nijs and R. Mertens Proc. 12th EPSEC (1994) 1018-1021
31 R. Mertens Proc. 12th EPSEC (1994) 1-6
32 R. Peruzzi and M. D'Ovidio Proc. 12th EPSEC (1994) 1022-1024
33 Peter Lölgen, C. Leguijt, J.A. Eikelboom, R.A. Steeman, W.C. Sinke L.A. Verhoef, P.F.A. Alkemade and E. Algra Proc. 23th IEEE PVSC (1993) 236-242
34 P. Fath, C. Marckmann, E. Bucher, G. Willeke, J. Szlufcik, K. De Clercq, F. Duerinckx, L. Frisson, J. Nijs and R. Mertens Proc. 13th EPSEC (1995) 29-32

NOVEL PROCESS SEQUENCES FOR LOW-COST SILICON SOLAR CELL FABRICATION

James M. Gee, Douglas S. Ruby, and Walter Worobey
Sandia National Laboratories
Albuquerque, NM 87185-0752

The requirements to achieve high efficiency in crystalline-silicon (c-Si) solar cells are now well established. Efficiencies approaching 24% have been achieved with c-Si solar cells using high-lifetime processing and very sophisticated device structures to minimize recombination at surfaces and interfaces. Commercial c-Si solar cells, on the other hand, have relatively simple device structures and use high-throughput processes. Limitations introduced by the commercial fabrication sequence limit the cell performance to around 11-14% and 12-16% for commercial multicrystalline-silicon and Czochralski-silicon solar cells, respectively. High-efficiency cells have been fabricated on commercial photovoltaic-grade silicon substrates indicating that the material quality can be quite good; i.e., the bulk diffusion length L is much longer than the device thickness W. Hence, the most significant issue for raising commercial cell performance is developing a low-cost method to obtain better passivated surfaces.

This paper will outline some methods for incorporating high-efficiency features in commercial cell fabrication sequences. We will first review approaches for obtaining low-recombination front and rear surfaces. Optimized front surfaces use "selective emitter" doping profiles. Selective emitter refers to an emitter that is heavily doped beneath the grids to lower contact resistance and lightly doped between the grids to lower recombination losses on the illuminated surface. We will review several approaches for achieving a selective emitter profile and, in particular, discuss a new concept under development at Sandia that uses plasma processing to achieve a selective emitter profile without any alignments. Passivation of the rear surface can be achieved with diffused regions (back-surface fields) or with passivation layers (oxide, silicon nitride, etc.). Some methods for achieving back-surface passivation will be discussed. Finally, we will review opportunities for reducing the cost of the entire c-Si photovoltaic module through design-for-manufacturability principles.

This work was performed by Sandia National Laboratories for the United States Department of Energy under contract DE-AC04-94AL85000.

Processing Large-Area Silicon Substrates with High Defect Densities into Higher Efficiency Solar Cells

Michael Kardauskas

ASE Americas, Inc.
4 Suburban Park Drive
Billerica, MA 01821-3980

As the photovoltaics industry matures, and module prices decline, the ability to use low-cost materials is becoming critical to the economic viability of any particular PV technology. Ribbon and sheet silicon technologies, such as silicon growth by the Edge-defined Film-fed Growth (EFG) method, can offer a significant cost advantage over traditional crystalline silicon technology. These savings derive from the elimination of the cost and material loss associated with the process of slicing monocrystalline boules or cast multicrystalline blocks into wafers, providing an inherent cost advantage on the basis of cost per square meter of silicon. However, the ribbon and sheet technologies tend to produce material with high densities of crystal defects, such as grain boundaries, twins, and dislocations, and the sheet material can incorporate high levels of impurities during growth because of its high surface area. In order to translate the lower materials costs of these technologies into lower cost-per-watt, it is necessary to be able to process these defective materials into solar cells with efficiencies comparable to those of low-defect-density material made by the traditional technologies. While this presents a considerable challenge, ASE Americas has developed EFG growth and cell manufacturing processes compatible with high-volume manufacturing that accomplish this objective.[1]

Passivation of Crystal Defects

In order to compete with cast silicon technologies on the basis of growth rate, the crystallization rate of ribbon silicon must be one to two orders higher. This tends to result in material with high densities of twins and grain boundaries. In addition, the relatively high cooling rate of the crystallized silicon associated with its continuous removal from the crucible tends to cause high mechanical stresses. In current EFG production, the perimeter of the die tip is 80 cm in length, and the solidified EFG tube is grown to a length of about 5 m. Along a relatively short length of this rigid tube the temperature varies by nearly 1400°C, inducing very high levels of stress. This stress, which can be high enough to buckle the tube severely, introduces further dislocations. The dislocations and many of the twins and grain boundaries form electrically active recombination sites in the grown material.

The first level of protection from these defects is to attempt to prevent them from occurring. Since in EFG growth there is little that can be done to control grain structure, the principal technique employed to this end is the use of thermal shields, convection baffles, and carefully tuned inductive heating of a graphite afterheater to control the cooling rate and thereby minimize dislocations. However, there are limits to what can be accomplished by this technique. A

temperature profile that reduces stresses to the minimum level possible can result in a buckled tube, since buckling is a mechanism for relieving stress. Since highly buckled material cannot be processed into cells without high breakage rates, the optimum thermal profile results in a tube which contains some residual stress, and dislocation densities on the order of 10^4-10^6 cm^{-2}.

Passivation of defects is carried out by the introduction of hydrogen during cell fabrication. In processing, hydrogen is incorporated into the near-surface region of the silicon, and then distributed throughout the thickness of the wafer. EBIC studies clearly show that most dislocations (though not all) are passivated throughout the wafer thickness. Cell efficiencies typically increase by 1- 2% absolute as a result of this processing.

Minimization of Impurity Effects

Although most of the silicon charge material in Czochralski and cast multicrystalline growth is located more than 1 cm away from the crucible walls during growth, no part of an EFG ribbon is farther than 1.5×10^{-2} cm away from the die wall at the point where the melt exits the die. The purity of the graphite used in the construction of the die is therefore extremely important if the concentrations of metallic impurities in the ribbon are to be minimized. The need to control the cooling profile of the growing tube also requires a large number of graphite parts to be located in the hot zone of the furnace, including parts of the afterheater and graphite felt used as insulation, and all of these components must be highly purified in order to avoid contamination of the ribbon. This is particularly important since lifetime-killing metallic impurities such as titanium and vanadium are common in commercial grades of graphite, and can easily be transported in the vapor phase in the hot zone. All EFG hot zone parts are, therefore, purified at high temperatures to remove the metallic impurities before installation in a crystal growth furnace. Research is continuing on improvements to purification processes in order to maximize their effectiveness.

The one impurity that cannot be avoided during EFG crystal growth is carbon, since the crucible and die are made of graphite. This results in the saturation of the silicon melt with C, and a supersaturation of the silicon ribbon at C levels of about 1×10^{18} cm^{-3}. Although carbon is isoelectronic with silicon, the very high carbon level may affect the electronic quality of the material. It has been found empirically that the effect of carbon can be offset by intentional doping with oxygen, at O levels on the order of 5×10^{16} cm^{-3}. This is accomplished by the introduction of low levels of carbon monoxide (CO) into the growth ambient, which provides an oxygen source without oxidizing the graphite die components. In addition to providing interstitial oxygen, some of the CO reacts with the molten silicon to form SiO vapor, which deposits as a thin solid film on the growing ribbon at temperatures below 1100°C. There is evidence that this oxide deposit acts as an impurity sink, capturing some of the metallic impurities incorporated into the ribbon during growth. The combination of these oxygen effects results in improvements in cell voltage, current, and fill factor which together increase cell efficiency by about 5% on a relative basis.[2]

Other High-Efficiency Processing for EFG Cells

In addition to the processing, detailed above, designed to address problems unique to ribbon growth, standard EFG cell processing includes a number of steps which improve the cell performance of any silicon substrate. These include the incorporation of a graded antireflection coating, designed to optimize the performance of EFG cells when encapsulated under glass. This is an important contribution, since EFG silicon, like most multicrystalline materials, cannot be chemically textured to improve light absorption, as is commonly done with monocrystalline cells. EFG cells also use an alloyed aluminum contact on the rear (p) side to form a back surface field, which maximizes current collection from the rear side of the cell. The front surface grid, while formed from a standard silver thick film paste, is printed by a unique process which produces fingers with an unusually high aspect ratio (height/width) of nearly 50%. This grid design minimizes shadowing for a given cell series resistance, increasing cell current. These features are designed to take maximum advantage of opportunities to improve cell efficiency through cell design.

EFG Cell Efficiencies in High-Volume Production

The combination of material upgrading and state-of-the-art cell design can produce cell efficiencies which are surprisingly high for what is commonly regarded as a low-quality silicon substrate. Figure 1 shows the efficiency distribution of individual EFG tubes grown in sequence from a single graphite die; each tube represents about 300 cells, for a total of about 20,000 cells. The overall average efficiency for this long furnace run was 13.8%, with many individual tubes exceeding 14% average efficiency. Figure 2 presents the efficiency distribution for one of these tubes, showing that a significant fraction of the cells in this tube had efficiencies over 14.5%. Since EFG cells do not suffer from the degradation commonly observed in monocrystalline

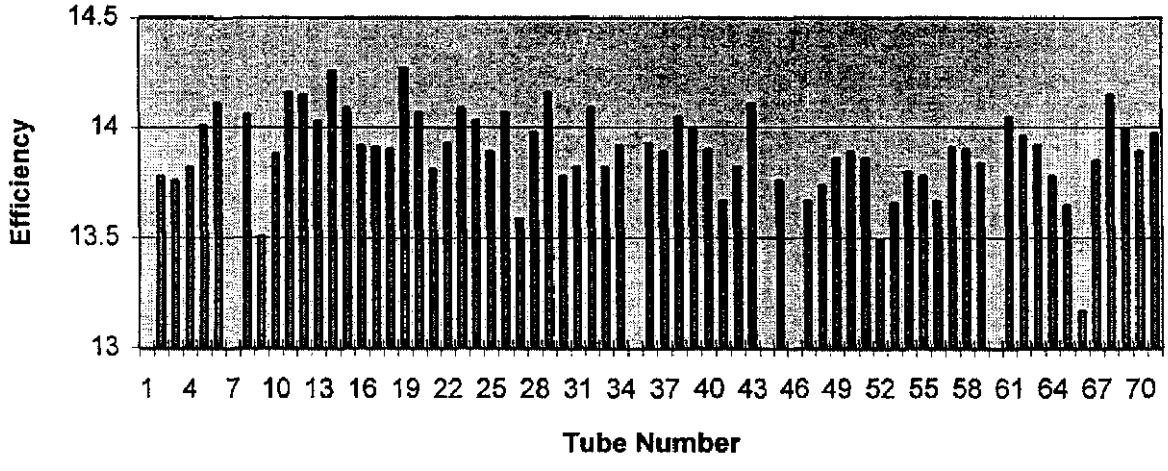


Figure 1. Plot of average efficiency of EFG solar cells in a single furnace growth run on a tube-by-tube basis. Each tube was processed into about 300 cells. Note the stability of efficiency over the length of the run, which lasted about two weeks.

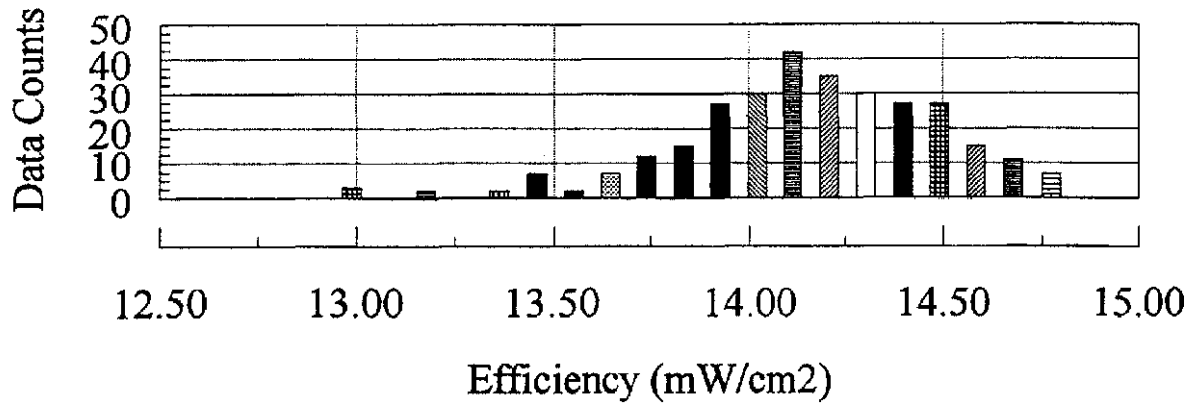


Figure 2. Distribution of cell efficiencies for Tube 11 of the furnace growth run shown in Figure 1.

silicon cells during initial exposure to sunlight,[3] these cells provide power equivalent to Czochralski cells with initial efficiencies of about 15% on an equal area basis, which is within the normal efficiency range for CZ cells in commercial production. Although only a part of the EFG distribution falls into this high efficiency range, further compensation for the higher packing density of true-square EFG cells as compared with the typical quasi-square Czochralski cells raises the average stable module efficiency to a level equivalent to that of a CZ module containing cells of 15% efficiency. Thus for all the inherent technical disadvantages of ribbon silicon, not only can EFG compete in the PV market on the basis of price, but it can do so without asking the customer to compromise on module efficiency.

Further Development Efforts

ASE Americas realizes that the EFG efficiency gains achieved during the past few years must continue to be extended in order to remain competitive in the dynamic field of modern commercial PV. A development program, partially funded by a PVMaT grant, is being carried out to continue to improve EFG technology both in areas where ribbon material has disadvantages, and in areas where it does not. Directions presently under investigation are continued improvement in graphite purity, and isolation of crystal growth furnaces from the manufacturing environment, to improve EFG silicon purity. A significant improvement in cell efficiency is also expected to result from a reduction in EFG silicon thickness, which is challenging, but which will provide an increase in the effectiveness of the back surface field effect. Changes in cell metallization are planned, which are expected to reduce both recombination at the front surface, and cell series resistance. Finally, experiments are underway to pursue a further reduction in reflection losses by the addition of a transparent textured coating, which promise to provide reflection levels comparable to those of etched monocrystalline silicon surfaces. The combined efficiency contributions of all of these improvements is expected to raise the average efficiency of EFG cells to 15.5% by the end of 1998.

Acknowledgments

The author wishes to acknowledge the contributions of many colleagues at ASE Americas, Inc. and Mobil Solar Energy Corporation in the development of the processes described in this paper.

Current development efforts are being supported by the National Renewable Energy Laboratory under PVMaT subcontract ZAF-6-14271-13.

References

1. M. J. Kardauskas, M.D. Rosenblum, B.H. Mackintosh, and J.P. Kalejs, in *Proceedings of the 25th IEEE Photovoltaic Specialists Conference,* IEEE, 1996 (in press).

2. B.R. Bathey, R.O. Bell, J.P. Kalejs, M. Prince, M.D. Rosenblum, R.W. Stormont, and F.V. Wald, in *Proceedings of the 11th E.C. Photovoltaic Solar Energy Conference* (Harwood Academic Publishers, Chur, Switzerland, 1993) pp. 462-464.

3. J.H. Reiss, R.R. King, and K.W. Mitchell, in Extended Abstracts of the Fifth Workshop on the Role of Impurities and Defects in Silicon Device Processing, 1995, pp. 120-123.

ANTIREFLECTING SILICON SOLAR CELLS WITH TEXTURED ZINC OXIDE

Haifan Liang and Roy G. Gordon
Harvard University, Cambridge, MA 02138

Abstract

We describe a method of preparing textured antireflection layers on polysilicon solar cells. Textured ZnO films were deposited by atmospheric pressure metalorganic chemical vapor deposition using diethylzinc and water as precursors. We were able to deposit textured ZnO films of high optical transmittance at a low temperature (250°C) with high growth rates (up to 4000 Å/minute), and good uniformity and reproducibility. The optical properties of textured ZnO films on soda lime glass, silicon, TiO_2/silicon, and prefabricated solar cells were studied using spectrophotometry. The improved efficiencies on polycrystalline silicon solar cells were mainly due to increases in the short circuit currents.

Introduction

Silicon has a high refractive index in the visible region. This causes above 30% reflectance at the silicon-air interface. To get high efficiency in silicon based solar cells, it is therefore crucial to have good antireflection designs. Anisotropic etching can reduce the reflectance on single crystal silicon cells to about 10%. In polycrystalline silicon cells, etching is less effective because of the random orientation of crystal directions in the grains. Antireflection coatings with high band gap dielectric coatings provide a more effective way of improving the efficiency of polycrystalline cells. Texturing of the antireflection layer can further reduce reflectance by optical confinement, trapping long wavelength, weakly absorbed light within the silicon.

ZnO is an n-type semiconductor with a band gap of about 3.3 eV. It is highly transparent in the visible region. The refractive index of pure ZnO is about 2.0. These properties make ZnO an attractive candidate as an antireflection layer on silicon solar cells. ZnO is useful in large scale commercial production because it is inexpensive and environmentally safe. ZnO films have been deposited using many thin film deposition techniques such as chemical vapor deposition (CVD), rf magnetron sputtering, and spray pyrolysis. CVD is especially useful for large scale deposition because it provides high growth rates and good uniformity. The most common precursors for CVD ZnO are dimethyzinc (DMZ) and diethyzinc (DEZ). DEZ is cheaper than DMZ and has a high volatility at room temperature. It can be used to deposit ZnO films with a high growth rate.

In this paper, we describe the preparation of textured ZnO films by metalorganic chemical vapor deposition (MOCVD). Textured ZnO films with good optical transparency were deposited at a low temperature, with very good uniformity and reproducibility. The optical properties of the films on glass and silicon substrates were studied using spectrophotometry. Films were also deposited on single crystal silicon cells and on polycrystalline silicon cells to evaluate the efficiency increase due to decreased reflectance.

Experiment

The ZnO films were prepared by atmospheric pressure MOCVD using diethyzinc (DEZ) and water as source materials. The reactant gases were stored in bubblers heated using heating tapes (Figure 1). Bubbler temperatures varied from room temperature to 80°C. The transport lines to the injector were heated to a slightly higher temperature (about 20°C higher) than the bubbler temperature to prevent precursors from condensing at cold spots. The injector had five adjacent inlet slots designed to mix the precursors close to the substrate surface. DEZ vapor in nitrogen was transported through the middle slot and water through the outer two slots (Figure 2). The two

intermediate slots carried buffer gas acting as a barrier preventing deposition on the inlet slots. Nitrogen was used as the carrier gas as well as the buffer gas. The carrier gas flow rate for the DEZ bubbler was set at 0.4 Liters/minute, with a nitrogen dilution flow of 3.6 Liters/minute. The buffer gas flow rate was 3.0 Liters/minute. The carrier gas flow rate for the water bubbler was 0.9 Liters/minute, with a dilution flow of 3.1 Liters/minute. The total flow rate into the injector was 12.0 Liters/minute. The exhaust flow was set at 15.0 Liters/minute. The DEZ bubbler temperature was set at 40 °C, and the water bubbler temperature was 80 °C.

These reactants mix under the reactor, and deposit zinc oxide film on the substrate. The distance that the gas flows over the substrate, from the nozzle slots to either exhaust slot, was about 8 cm. The growth rate of the zinc oxide was much higher under the injector slots than near the exhaust slots. In order to make films with uniform thickness, a motor driven belt drive was used to move the substrates at a uniform speed, usually one inch per minute, across the reaction zone.

DEZ and water can react to deposit ZnO films at a temperature as low as 100 °C. Since a higher substrate temperature favors larger grain sizes for better texture and a higher growth rate, which is desired for large scale production, we would like to have a high reactor temperature. This had to be compromised with the thermal stability of the solar cells. The reactor temperature was set at 250 °C. A higher temperature may cause instability in the cells, such as unwanted diffusion at the interface between the metal contacts and silicon.

Soda lime glass, single and polycrystalline silicon wafers, TiO_2 coated silicon, and prefabricated silicon solar cells were used as substrates. Except for the prefabricated cells, all other substrates were cleansed with detergent, then rinsed with deionized water and isopropanol, then blown dry with dried air. No cleansing was used for the prefabricated solar cells. Substrates were preheated in nitrogen for about 20 to 30 minutes before deposition to bring the substrates up to the desired temperature.

Thicknesses of the ZnO films were measured using a stylus profilometer. The step was etched with dilute HCl. Because of the roughness of the films, only an estimate of the average thickness could be obtained.

Results

DEZ and water reacted very fast at a substrate temperature of 250°C. Deposition on stationary substrates showed that the films were deposited right under the injector slots. The belt speed was set to 1.0 inch/minute. Film thickness was varied either by controlling the bubbler temperatures or the number of times the substrate passed under the injector. A high growth rate is essential for successful large scale commercial production. At a DEZ bubbler temperature of 70°C, deposition rate as high as 4000 Å/minute was achieved.

If the ratio of DEZ to water was too low, we found brown absorption in the deposited ZnO films, especially near the edges of the reactor zone. This is presumably due to carbon contamination from incomplete reaction of the DEZ. The minimum water to DEZ molar ratio for a clear film was 4:1. A larger excess of water had no observable effect on the films.

The deposition efficiency was calculated as the ratio of the molar quantity of zinc atoms in the film deposited over the molar quantity of zinc atoms in the precursor used. The deposition efficiency was above 50%.

Texture of the films increased with film thickness, as can be judged by light scattering and disappearance of interference colors from the specular reflection. The minimum thickness for a textured film on soda lime glass substrates that showed no specular reflectance was about 2 μm. The silicon and prefabricated solar cell substrates we used were from several different sources and had varying flatness. The thickness of ZnO required to eliminate specular reflectance varied between 2 μm and 3 μm.

The optical properties of the textured ZnO films were measured with a spectrophotometer using an integrating sphere detector which could measure both the total and diffuse components of the reflectance and transmittance. The reflectance standard was a barium sulfate plate taken to be 100%. To estimate the optical absorption within the ZnO film, optical measurements were made by covering ZnO films on glass with a thin layer of refractive index fluid and a thin cover glass. The structure of these samples was cover glass/index fluid/ZnO/glass. The absorption in the ZnO films on glass substrates was estimated by subtracting the total reflectance and transmittance from 100%, and finally subtracting the absorption of a blank measurement of a sample of cover glass/index fluid/glass without any ZnO film. Figure 3 shows the measured spectra of a 3 μm ZnO film. The absorption increased slightly with film thickness. For textured films, the effect of optical confinement increased the apparent absorption because some of the light travels in the plane of the film until it is absorbed. Light trapping within the ZnO layer is less likely to happen in an actual cell structure since silicon has a higher refractive index than ZnO, so there is no total internal reflection at the ZnO/Si boundary. Thus the absorption measurements reported in Figure 3 should represent an upper limit to the amount of light actually absorbed in the ZnO layer of a coated and encapsulated cell.

Reflectance of cover glass/index fluid/ZnO/silicon and cover glass/index fluid/ZnO/TiO_2/silicon were also measured to model the reflectance from encapsulated solar cells. The cover glass/index fluid/ZnO/silicon structure gave a solar-weighted reflectance of about 10%. The cover glass/index fluid/ZnO/TiO_2/silicon structure gave a solar-weighted reflectance of about 6% (Figure 4). We also studied the grain sizes of ZnO on silicon and TiO_2/silicon using SEM micrographs. ZnO/Si films had average grain sizes of about 0.5 μm and ZnO/TiO_2/Si films had average grain sizes of about 1μm. The larger grain size in the ZnO/TiO_2/Si films provided better texture and optical confinement. The encapsulated ZnO coated cells had 0.5% absolute improvement in efficiency . This was mainly due to a 2.3% improvement in the short circuit current.[3]

Summary

We were able to deposit textured ZnO films by atmospheric pressure MOCVD using DEZ and water, with a high growth rate, good uniformity and reproducibility. The films had high optical transparency. Absorption increased slightly with film thickness. Textured ZnO films were deposited on soda lime glass, single and polycrystalline silicon, TiO_2/silicon, and prefabricated solar cells. The reflectance on cells were reduced to as low as 6%. There was a 0.5% net increase in the efficiency mainly credited to the increase in short circuit current.

References

1) H. Takato et al, "Effects of Optical Confinement in Textured Antireflection Coating using ZnO Films for Solar Cells", Jpn. J. Appl. Phys., **31**, 1992, pp. L1665-L1667
2) J. M. Gee, R. G. Gordon, H. Liang, "Reflectance Control for Multicrystalline-Silicon Photovoltaic Modules using Textured-Dielectric Coatings", *1st World Conf. on Photovoltaic Energy Conv.*, 1994, pp. 1274-1277
3) J. M. Gee, R. G. Gordon, H. Liang, "Optimization of Textured-Dielectric Coatings for Crystalline-Silicon Solar Cells", *25th IEEE Photovoltaic Specialists Conference,* 1996, pp. 1-4.

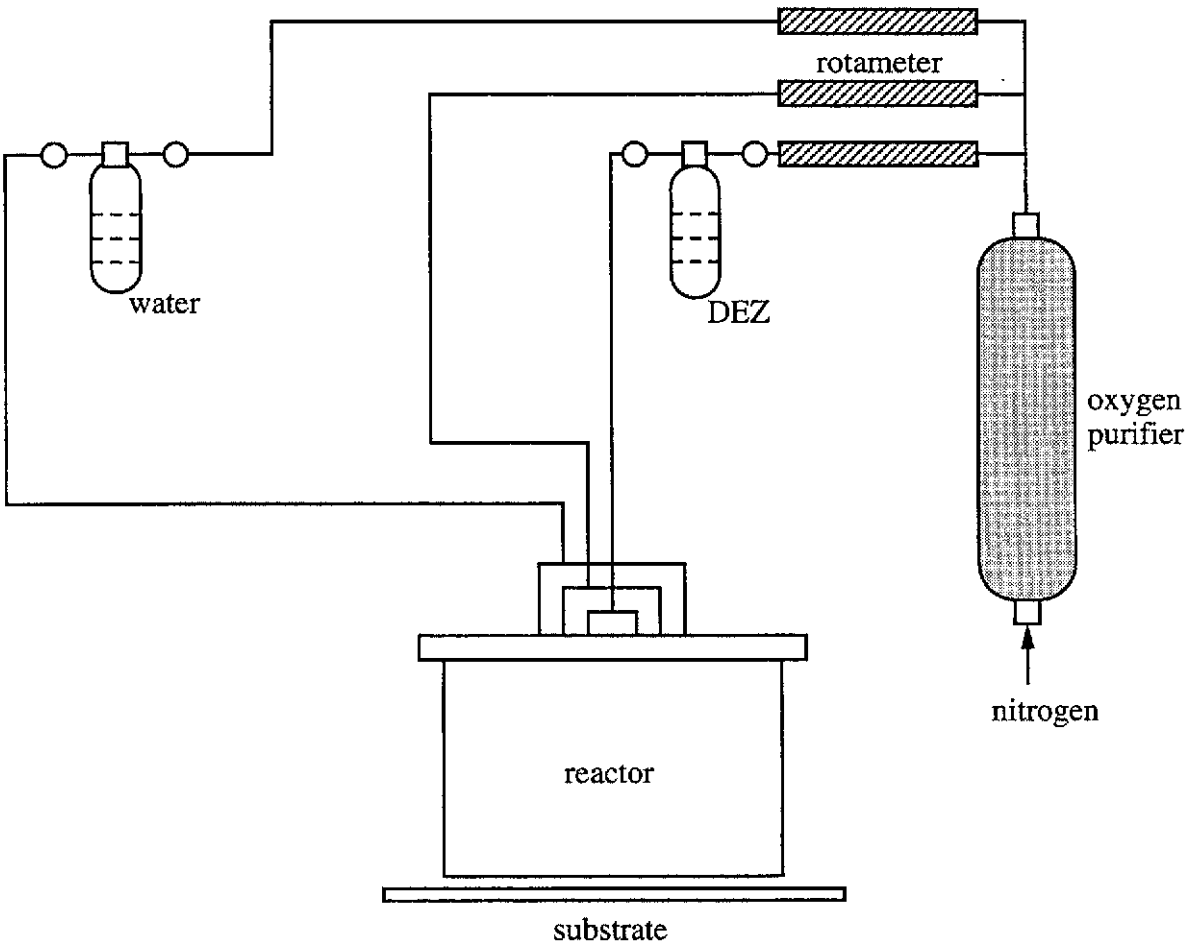


Figure 1. Schematic drawing of the CVD apparatus

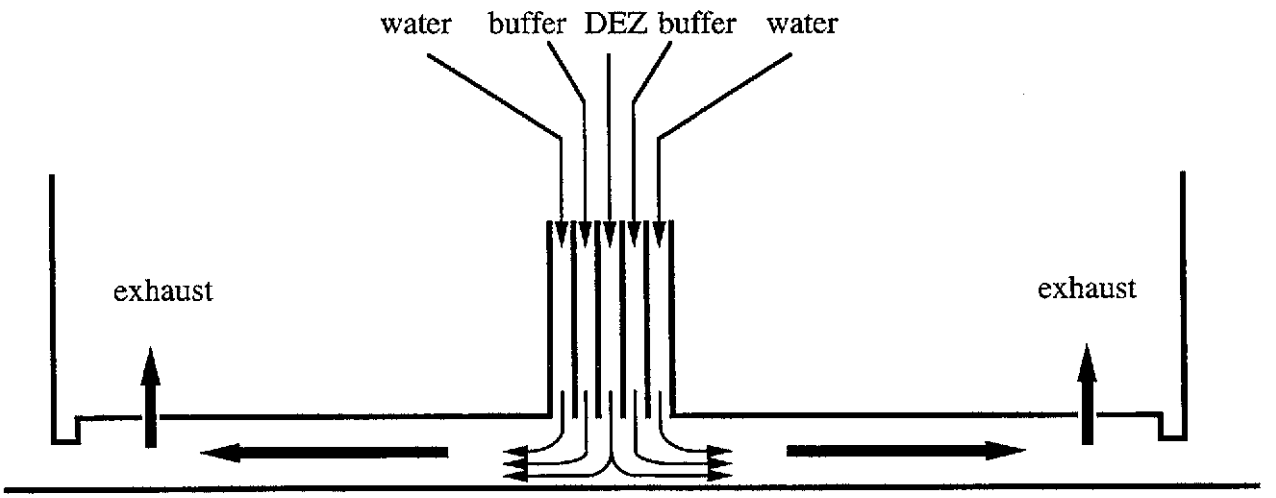


Figure 2. Cross section of the gas flow in the CVD reactor

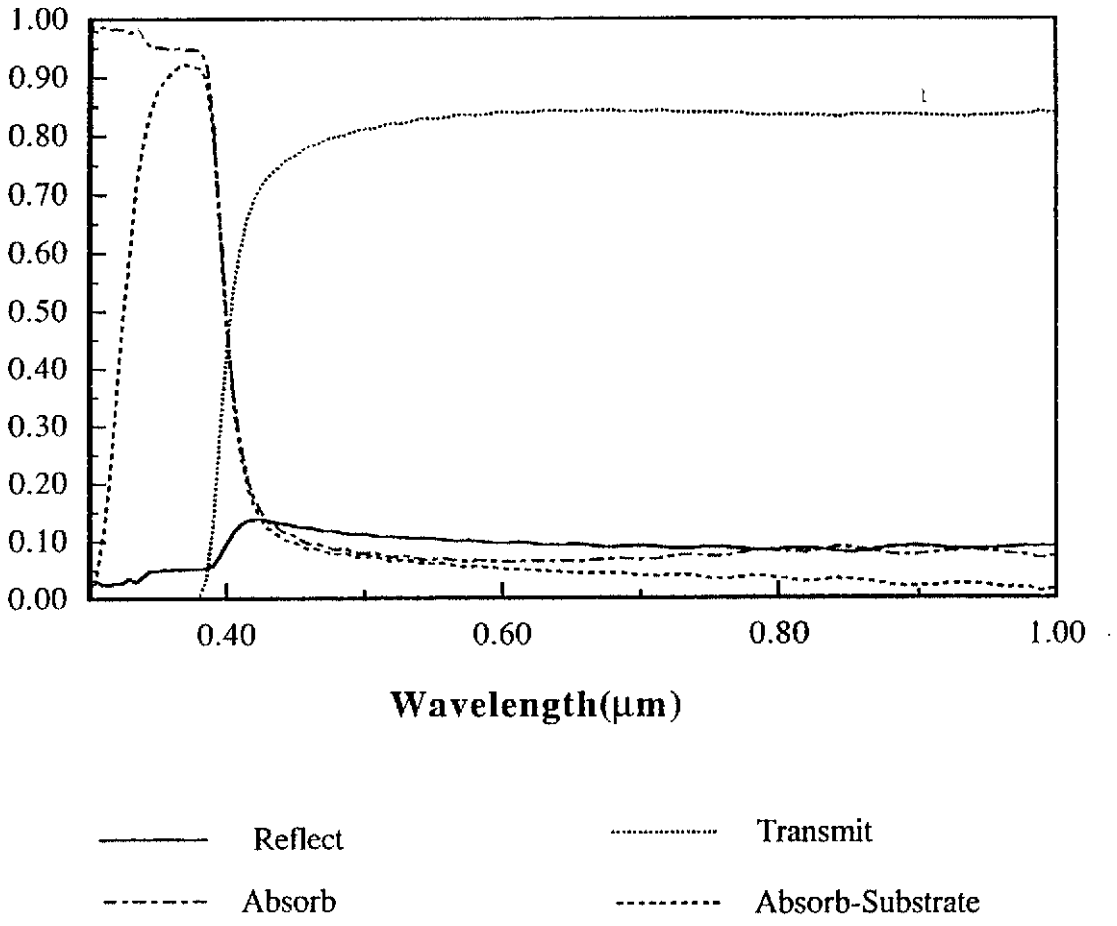


Figure 3. Cover Glass/Index Fluid(n=1.75)/Textured ZnO/Galss

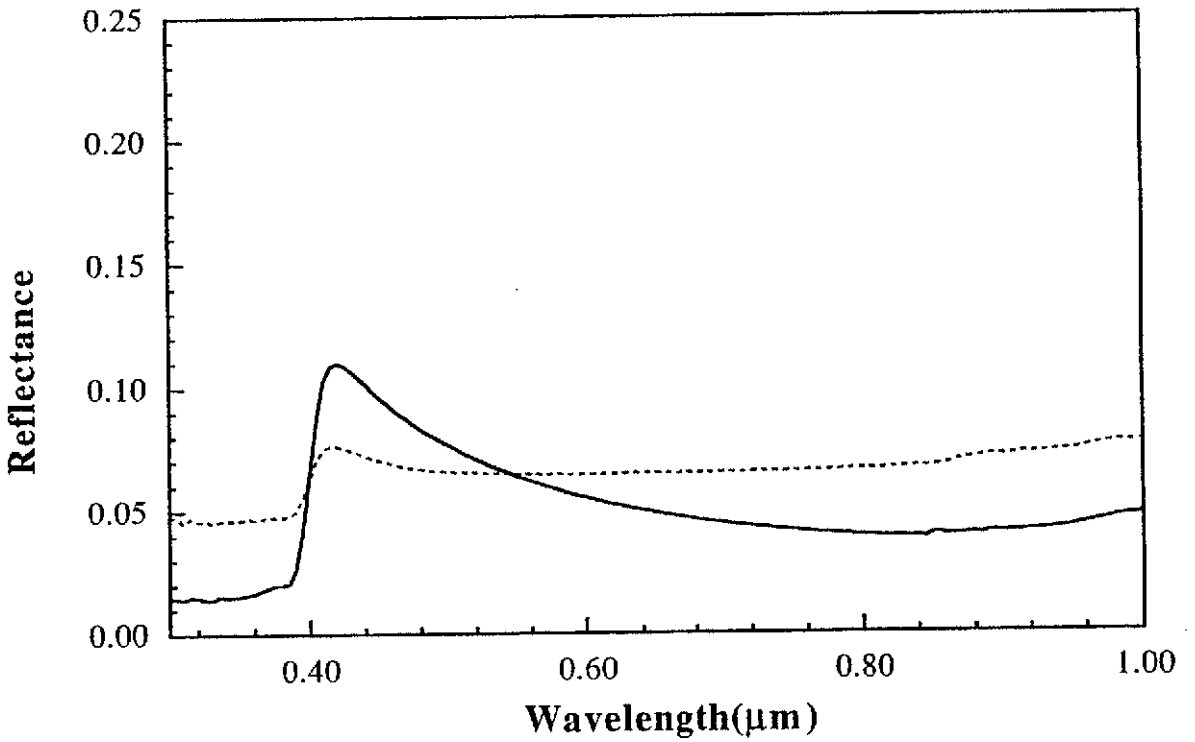


Figure 4. Textured ZnO on TiO_2/Si

COST ANALYSIS OF HIGH EFFICIENCY POLYCRYSTALLINE SILICON SOLAR CELL SEQUENCES.

S. Narayanan and J. Wohlgemuth
Solarex (A Business Unit of Amoco/Enron Solar)
Frederick, Maryland 21703

INTRODUCTION

Cast polycrystalline silicon solar cell technology, accounting for nearly 50% of the crystalline silicon solar cells manufactured world wide, is an important commercial photovoltaic (PV) technology. The vast majority of commercial silicon solar cells produced have screen printed contacts. The average cell efficiency of commercial polycrystalline cells is approximately 13%. Many efficiency enhancement techniques, incorporated in laboratory high efficiency polycrystalline silicon solar cell process sequences, reduce the deleterious effects of structural defects and impurities (1). A detailed review of high efficiency polycrystalline silicon solar cell sequences and cost-benefit analysis of some of the sequences using a model developed by Jet Propulsion Laboratory has been published by the authors of this paper (2). In recent years, many organizations are increasingly involved in adapting high efficiency enhancement techniques to commercial large area solar cell processing (3-6). While this paper analyses the sequences used for cast polycrystalline substrates, many individual steps are relevant to single crystalline cells also.

COST ANALYSIS METHODOLOGY

The Solar Array Manufacturing Industry Costing Standard (SAMICS) methodology, developed by the Jet Propulsion Laboratory (JPL), has been used to compare different cell process steps, on the same cost basis (7). SAMICS costing programs are developed from a description of a manufacturing facility that is designed for commercial PV module production. The description includes all of the factors contributing to production costs. Direct costs are divided into specific categories: equipment used in production; labor of workers assigned to the production stations; materials used in production; utilities required for manufacturing; floor space required for manufacturing; and yield losses. Remaining cost inputs are classified as indirect and are matched to the appropriate direct cost input. Use of a detailed computer program to calculate indirect expenses is not necessary because all of the indirect components produce similar overhead rates that are independent of process detail. The uncertainties in the cost inputs are usually larger than the differences in the results between the detailed program and using fixed overhead rates. Therefore, JPL developed a simpler version called Interim Price Estimation Guidelines 2 (IPEG2), which provides indirect coefficients for labor, materials, utilities, floor space and equipment. The equipment coefficients include standard depreciation, the

cost to maintain the equipment and a return on the investment. Therefore, the "cost" generated by IPEG2 is actually the "predicted selling price" of the product.

CRITERIA FOR HIGH THROUGHPUT SEQUENCE

Solar cell manufacturers utilize high throughput process steps to meet their high volume requirements. The throughput rate of any new step to be incorporated in the cell process sequence should meet this requirement. In order to maintain consistency in yield and flexibility in manufacturing the optimum process window for any new step should be broad. In addition, the operating cost of high throughput equipment should be low and it should operate with minimum down time. Process step and equipment have to be developed to meet these requirements. The requirements for large scale manufacturing of solar cells (6-10 MW/ year) are presented in Table 1.

Table 1 Requirements for large scale solar cell manufacture

Parameter	
Throughput	500-1000 wafers/hour
Wafer Size	4- 6" square or round
Material	CZ, Multicrystalline or ribbon
Thickness	150- 300 micrometers

HIGH EFFICIENCY PROCESS SEQUENCE

A typical process sequence used for the manufacture of the commercial solar cells may consist of the following steps:

- saw damage etch
- phosphorus diffusion
- junction isolation
- screen print and fire metal contacts
- deposition of anti reflective (AR) coating.

Some of the efficiency enhancement techniques used to improve screen printed polycrystalline cells are:

- selective emitter
- oxide passivation
- SiN passivation
- mechanical texturing
- aluminum back surface field
- phosphorus gettering

The process sequences and the efficiency enhancement techniques as reported by various organization are presented in Table 2.

A figure of merit to evaluate the cost effectiveness of these efficiency enhancement techniques has been developed. The cost of each technique ($/cell) and the cost per watt of each technique, calculated in 1996 US dollars using the model, are presented in Table 3. Polycrystalline PV module are available commercially for $3.5-4/watt. The cost (as calculated by the model) of the additional power generated by the efficiency enhancement technique should be less then the selling price for a technique to be commercially viable.

CONCLUSIONS

Using the established figure of merit, sequences like evaporated front contacts, selective emitter involving photolithography are not likely to be commercially viable, at least in the present form. Techniques like oxide passivation, phosphorus gettering, screen printed Al- BSF and mechanical texturing may be cost effective.

Table 2
High Efficiency Processes Reported by Various Organizations

Group	Material	Year	Size (cm^2)	Eff (%)	Cell process
UNSW	SiTiX	1989	4	17.8	Extraheavy emitter diff, emitter etch back. Al Evap and sinter, SiO2 Passivation Ti/Pd, Ag plating, DLAR MgF_2/ZnS* (8)
UNSW	Solarex	1989	10	16.7	Laser Textured, Laser grooved, Buried contact process: Emitter Diff, Wet oxidation, front contact grooving, groove diff, Al evap and sinter, Ni/Cu electroless plating (9)
GIT	SiTiX	1992	1	17.7	Extraheavy emitter diff, emitter etch back. Al evap and sinter, H_2 passivation. Oxide passivation, Ti/Pd, Ag plating, DLAR ZnS/ MgF_2 *(10)
IMEC	SiTiX (EMC)	1993	4	16	Selective emitter process: Heavy phos diff, selective etching off diffusion, Heavy phos diff, Emitter etch back, H_2 passivation on rear, Ti/Pd/Ag Evap, Al evap Forming gas sinter, DLAR Evap-ZnS/ MgF_2 *(11)
IMEC	Euro Solare	1992	4	15.8	Selective emitter process: Heavy phos diff, selective emitter etch, Heavy phos diff, emitter etch back, SiO_2 pass., Ti/Pd/Ag evap, Al evap, Tantalum oxide AR, Plasma, hydrogenation (12)
IMEC	Polix 200 mic	1993	4	16.9	Selective emitter process Phos gettering, heavy phos diffusion Emitter Etch back, Boron BSF, SiO2 passivation Ti/Pd/Ag evap, DLAR Evap- MgF_2/ ZnS* Rear Al evap, H_2 passivation by plasma Forming gas anneal (12)

CRN & FhG-	Bayer	1993	4	14.1	Phos diff by RTP Ti/Pd/Ag evap, Al evap. on rear Forming gas sinter DLAR TiO_2, MgF_2 * (13)
FhG	Bayer	1993	4	16.7	Phos diff Ti/Pd/Ag evap, Al evap. on rear Forming gas sinter DLAR TiO_2, MgF_2 *(13)
Sandia	HEM	1993	4	15.1	Phos diff, APCVD SiO_2 for masking,Ti/Pd/Ag evap DLAR TiO_2/SiO_2 * by solgel process Forming gas anneal (14)
IMEC	SiTiX (EMC)	1993	100	14.2	Heavy phos diff., Emitter etch back, H_2 passivation on both sides, Rear Al evap and forming gas sinter, Ti/Pd/Ag Evap, DLAR MgF_2 /ZnS *(11)
Sharp	SiTiX	1991	100	16.4	Mech. Texturing by dicing saw, SiO_2 passivation. DLAR - TiO_2/MgF_2*, Al BSF, Fine screen print: 4% front coverage (16)
Sharp	SiTiX	1991	100	15.9	Mech. Texturing by dicing saw ,SiO_2 passivation. TiO_2 AR, Al BSF, Screen print (15)
Sharp	SiTiX	1991	100	15.3	Chem. Texturing, SiO_2 passivation. TiO_2 AR, Al BSF, screen print (15)
Sharp	SiTiX	1992	100	17.2	Mech. Texturing by dicing saw, SiO_2 passivation. TiO_2/MgF_2 AR*, Al BSF, Fine screen print (16)
Hitachi	SiTiX	1992	100	16.8	Bi -facial cell, 160 micron thick Phos diff on both sides oxide passivation, TiO_2 AR on both sides Hydrogen Passivation (17)
Kyocera	SiTiX 270 microns	1992	225	16.4	Bifacial Silcon Nirtide cell, Selective emitter formation Surface Texture by photolith and wet etch Al BSF, SiN both sides, DLAR* Evaporation of Ti/Ag on both sides (18)
Solarex	Solarex	1993	130	15.8	Mech. Textured, Mech. grooved Buried contact cell SiO_2 AR (19)

* Double layer AR coatings optimized for air will lose 4 to 5% of their effciency when encapsulated.

Table 3
Cost Analysis of Efficiency Enhancement Techniques

Technique	Organization	Process Steps	Cost $/cell	Cost $/w	Efficieny Improvement	References
Phos. Gettering	IMEC	Pre difusion clean				20
		Phos. diffusion				
		Etch difused layer				
			0.305	3.81	5%	
Phos. etch back	UNSW	Pre-diff clean				19
	GIT	Phos. diffusion				
	IMEC	(875-925 C, 45 min-2 Hr)				
		Emitter etch				
			0.156	1.51	6%	
Selective Emitter	IMEC	Predif clean				20
	Kyocera	Phos. diff				
		oxide mask				
		Photolith				
		Oxide and Si etch				
		Phos. etch back				
			0.835	5.75	9%	
SiO_2 Pasivation	UNSW	oxidation	0.057	0.57	6%	19
	IMEC					
	Hitachi					
	Sharp					
	Solarex					
H_2 Plasma Pass.	IMEC	H_2 Plasma dep			4%	
	Hitachi	Damage etch			5%	21
Boron BSF	IMEC	Boron doped oxide dep				20
		masking oxide dep				
		Furnace Drive in	0.38	1.91	12%	
Evaporated AL BSF	UNSW	Al evap.sinter	0.383	3.27	7%	
	GIT					22
Al pste BSF	Sharp	Screen print paste				
	Kyocera	Fire				
	Solarex	Clean up	0.306	3.82	5%	23
Phtolith. contacts	UNSW					
	GIT	Photolithography				
	IMEC	Evaporation				
	Kyocera	lift off				24
	FhG	Forming gas/N_2 anneal	0.777	15.6	3%	

REFERENCES

1. H. Watanabe, 4th International Photovoltaic Science and Engineering Conference, Sydney, Australia, 1989, pp. 103-110.

2. S. Narayanan and J. Wohlgemuth, Progress In Photovoltaics, Vol. 2, 1994, pp. 121-128.

3. J. Szlufcik, P. Fath, J. Nijs, R. Mertens, G. Willeke and E. Bucher, 12th EC Photovoltaic Solar Energy Conference, Amsterdam, Netherlands, 1995, pp. 768- 772.

4. F. Duerinckx, J. Szlufcik, K. De Clercq, P. De Schepper, W. Laureys, J. Nijs, R. Mertens, 13th EC Photovoltaic Solar Energy Conference, Nice , France, 1995, pp. 1493-1496.

5. P. Doshi, J. Mejia, K. Tate, S. Kamra, A. Rohatgi, S. Narayanan, R. Singh, 25th IEEE Photovoltaic Specialists Conference, Washington, DC, 1996, in print.

6. S. Narayanan, J. Creager, M. Roy and J. Wohlgemuth, 25th IEEE Photovoltaic Specialists Conference, Washington, DC, 1996, in print.

7. B. Jackson, J. Glyman, P. Henry, H. Awaya, D. Burger and S. Herman, Advanced Photovoltaic Module Costing Manual, NREL, Golden, CO, USA, SERI/TR-214-1965, 1983.

8. J. H. Wohlgemuth, S. Narayanan and R. Brenneman, 21st IEEE Photovoltaic Specialists Conference, Las Vegas, NV, 1990, pp. 221-226.

9. S. Narayanan, S. R. Wenham and M. A. Green, 4th International Photovoltaic Science and Engineering Conference, Sydney, Australia, 1989, pp. 111-116.

10. J. C. Zolper, S. Narayanan, S. R. Wenham and M. A. Green, Appl. Phys. Lett., 55;, 27 (1989).

11. H. E. Elgamel, M. Y. Ghannam, J. Nijis and R. Mertens, 23rd IEEE Photovoltaic Specialists Conference, Louisville, KY, 1993 pp. 220-223.

12. J. Nijis, M. Y. Ghannam, J. Coppye, G. Palmers, Le Quang Nam, M. Rodot, S. Sivoththaman, D. Sarti and R. Peruzi, 11th EC Photovoltaic Solar Energy Conference, Montreux, Switzerland, 1993, pp. 164-167.

13. R. Schindler, I. Reis, B. Wagner, A. Eyer, H. Lautenschlager, C. Schetter and W. Warta, 23rd IEEE Photovoltaic Specialists Conference, Louisville, KY, 1993, pp. 162-166.

14. C. P. Khattak, F. Schmid, W. K. Schubert, M. Cudzinovic and B. L. Sopori, , 23rd IEEE Photovoltaic Specialists Conference, Louisville, KY, 1993, pp. 73-77.

15. T. Machida, K. Nakajima, Y. Takeda, S. Tanaka, N. Shibuya, K. Okamoto, T. Nammori, T. Nunoi and T Tsuji, 22nd IEEE Photovoltaic Specialists Conference, Las Vegas, NV, 1991, pp. 1033-1034.

16. T. Machida, M. Nishida, T. Nammori, T. Nunoi and H. Sawai, , Proc. of Fourth Sunshine Workshop on Crystalline Solar Cells, 1992, pp. 99-102.

17. T. Warabisako, K. Matsukuma, S. Kokunai, Y. Kida, T. Uematsu and H. Yagi, 23rd IEEE Photovoltaic Specialists Conference, Louisville, KY, 1993, pp. 248-251.

18. J. H. Wohlgemuth and S. Narayanan, Proc. of Sixth Sunshine Workshop on Crystalline Solar Cells, 1993, pp. 145-147.

19. S. Narayanan, S. R. Wenham and M. A. Green, , Appl. Phys. Lett., 48, 873-875 (1986).

20. M. Y. Ghannam S. Sivoththamam, H. E. Elgamal, J. Nijis, M. Rodot and D. Sarti, 23rd IEEE Photovoltaic Specialists Conference, Louisville, KY, 1993, pp. 106-110.

21. H. Yagi, K. Matsukuma, S. Kokunai, Y. Kida, N. Kawakami, K. Nishinoiri, T. Saitoh, R. Shimokawa and K. Morita, , 20th IEEE Photovoltaic Specialists Conference, Las Vegas, NV, 1991, pp. 1600-1603.

22. A. Rohatgi, P. Sana, M. S. Ramanachalam, J. Salami and W. B. Carter, 23rd IEEE Photovoltaic Specialists Conference, Louisville, KY, 1993, pp. 52-57.

23. M. Giuliano and J. Wohlgemuth, 15th IEEE Photovoltaic Specialists Conference, Kissimmee, FL, 1981, pp. 111-114.

24. K. Fukui, H. Yamashita, M. Takayama, K. Okada, K. Masuri, K. Shirasawa and H. Watanabe, 20th IEEE Photovoltaic Specialists Conference, Las Vegas, NV, 1991, pp. 1040-1044.

Status of RTP for Silicon Device Fabrication
A SEMATECH Perspective

Don Lindholm
SEMATECH Thermal Program Manager
Austin Texas

Visibility into the RTP Industry

SEMATECH obtains it's visibility into the RTP tool industry via projects, benchmarking, and discussions with member companies, universities, national labs, & suppliers. The projects and benchmarking efforts provide the data which guide SEMATECH in responding to the IC industry needs described in the National Technology Roadmap for Semiconductors (NTRS). It is important that the SEMATECH Thermal Program interface with the suppliers because it is the suppliers who will ultimately bring new technology to the market. The Thermal Program has had active interactions with both RTP suppliers and vertical furnace suppliers.

Establishment of RTP Project Goals

In 1993, SEMATECH reviewed the NTRS, conducted an RTP workshop and studied the IC Industry RTP tool needs. In addition, a review of existing or potential temperature measurement systems was conducted to identify high potential candidates for evaluation. From these 1993 efforts, SEMATECH established key goals for 0.25 micron RTP tool projects. The key goals were:

- ± 3 degree C three sigma temperature control
- 10 degree C across-wafer variation during ramp
- 50 degree C/sec ramp rates
- Cost of Ownership of $2.51 using 30 wafer/hour throughput, $750K tool cost.

Subsequent projects and benchmarking efforts used the above goals. Projects included stand-alone and cluster tools as well as RTP component technology.

Selected SEMATECH Projects

Four SEMATECH projects are highlighted because specific technical knowledge or RTP industry insights were obtained. The first project selected was worked with Texas Instruments and Applied Materials. The project objective was to deliver a cost effective, technically advanced RTP tool to meet the 0.25 micron technology needs. The two stage project sought first to establish the Centura™ RTP's temperature measurement and control capability. Wafers with varying backside conditions were a part of the first stage temperature control evaluation. After a successful first stage, the tool performance and reliability were investigated. Three sigma temperature control was determined to be ± 3 degree C for bare backside wafers and ± 6 degree C for widely varying backside wafers. Wafer throughput was 42.1 wafers/hour for the single chamber system.

The second selected project was initiated to address RTP component technology issues which were needed by the industry. Two major areas of focus were:

- Temperature measurement and control
- RTP reactor and control modeling.

Temperature measurement evaluations of ripple pyrometry at a member company, direct thermocouple control at a supplier and proximity sensors at a private lab have been conducted. RTP reactor and control system modeling have been worked with two suppliers. A key output of this project is that modeling has definitely been incorporated into the RTP suppliers and is part of their engineering capability.

A single wafer cluster tool project at Texas Instruments incorporated the Applied Centura™ HT tool with an FSI Excalibur™ vapor phase clean module. The single wafer cluster was used for evaluation of gate stack, poly emitter and low temperature epi deposition. The quality of the gate stack from the clustered gate stack tool was basically equivalent to that from the baseline process. A key output of this project was that the clustered tool was approximately 1.5X more costly per wafer pass when compared to the stand-alone tools. Throughput is the main driver for this cost differential.

The last project is a fast ramp furnace project and is included because of two significant outputs. The fast ramp furnace is being developed to reduce the thermal budgets in vertical furnaces and will provide competition for the single wafer, lamp heated RTP tools. The two outputs are:

- Demonstrated advantage of Model Based Process Control (MBPC)
- Increased knowledge of ramp rate vs. wafer damage.

Sandia has provided considerable modeling to describe the heating characteristics of a furnace and the relationship between across-wafer temperature variation & the possible occurrence of slip.

SEMATECH View of Capability Today

Since SEMATECH established RTP project goals in 1993, much progress has been made in the RTP industry to meet the temperature control goals. RTP tools have met the ± 3 degree C three sigma temperature control on non-varying backside wafers. The best RTP tool shows a ± 6 degree C three sigma temperature control with widely varying backside wafers. Refer to Table 1. for SEMATECH's temperature measurement/control data for various measurement systems in different RTP tools.

In various forms, pyrometry remains the main temperature measurement technology. Contact thermocouples are being introduced into commercial tools today. Improvements have been made to the ripple pyrometry technique and work will continue in 1996 with the linear lamp RTP tools being the beneficiary . Due to cost or robustness, alternative techniques at the university level in 1993 have not entered the commercial RTP tools.

The reactor modeling and control system modeling of present and future RTP tools have provided value to the suppliers. Reactor models and modeling skills have been inserted into the suppliers and they have moved forward improving their in-house modeling skills. The modeling of control systems has encouraged the RTP industry to think beyond the standard PID type of control methodology. SEMATECH's experience with model based process control on vertical furnaces certainly suggests that advanced control systems can provide performance and cost benefits.

The clustering of an RTP tool with a cleaning system can produce gate oxide stacks which are equal in quality with baseline processes. The problem at this time is that cluster throughput causes the cost of ownership to be about 1.5X greater than the equivalent stand alone tool process. The technical advantage of a cluster tool does not support such a cost disadvantage.

In an effort to compare the cost of ownership (CoO) and wafer throughput for both RTP tools and vertical furnaces, a common thermal process was first defined. Table 2. shows the resulting data from such a comparison. The projected fast ramp furnace appears to set the goal for the cost of ownership at $1.80 . The linear lamp RTP has the lower RTP CoO driven by the lower tool cost. The axisymetric RTP tool's data is for one module. Two modules are available for better throughput but, of course, two modules raises the tool cost above what is shown in table 2.

Future Issues

As we move toward the 0.18 micron technology node, SEMATECH sees the RTP project goals becoming:

- ± 2 degree C three sigma temperature control
- Across-wafer variation during ramp which keeps wafer out of slip region
- Cost of Ownership of $1.80 (unyielded) for a 10 sec S/D anneal process
- Minimum 30-35 wafers/hour to satisfy factory modeling needs
- Expandability to 300mm
- Cluster tool with competitive cost of ownership
- Improved monitor wafer to evaluate RTP performance.

When compared to the list of project goals established in 1993, the above shows a tighter temperature control to meet the NTRS needs, a better way to look at across-wafer temperature requirements, a reduced cost of ownership to compete with the fast ramp furnace projections and a minimum throughput needed to meet factory models. The above also acknowledges the new wafer size and the existing cost disadvantage of the clustered RTP tools. Finally as temperature control requirements become tighter, the monitor wafer used for such temperature evaluations needs to improve.

Table 1 Temperature Measurement/Control Data

Technique	Tool Type Heat source	Control (3σ)	All points ?	Emissivity Range
Corrected pyrometer	Multi-zone symmetric	+/- 5.9c	Yes (1)	Large
Modified Ripple	Cross linear lamps	+/- 10c +/- 12c	TC No	Large
Power Control	Cross linear lamps	+/- 10c	No	Small
Thermo-couple	Cross linear lamps	+/- 11c	No	Small
Ripple pyrometer	Test-bed Linear w/edge	+/- 15c	N/A TC	bare wafers only
Standard Pyrometer	Cross linear lamps	> +/- 20c	No	Small
Reflectance Pyrometer	Linear lamps Top & rotation	no clean data	N/A	N/A 3c in theory

(1) All Points? Yes - includes wafer uniformity component. No - relies on wafer means for 3σ calculation.

Table 2 Summary of Thermal Tool Cost of Ownership

Tool Type	Cost	through-put	CoO ♣	Comments
RTP - Linear lamps	$587k	30 w/hour	$2.01/pass	installed - best case
RTP - Axisymmetric	$1.5M	42	$2.49	member co. data
Vertical Furnace	$900k	23	$3.36	
Vertical w/MBPC	$960k	30	$2.68	beta site data
Fast ramp Furnace	$1.2M	57	$1.80	projected

Notes: Goal, CoO = $2.51/wafer ($2.29 unyielded)

♣ Defects = 0 (unyielded)

Overhead parameters: standardized, system fully loaded

System performance parameters: demonstrated

Process: Implant activation, 10s soak (no extended purge) or equivalent DT.

A REVIEW OF RTP AND ITS APPLICATION IN DISPLAY AND SOLAR DEVICE FABRICATION

CHUNGHSIN LEE
EATON-HTE
PEABODY, MA

Introduction

Tube furnaces have been used in a number of semiconductor thermal processing applications since the early 1950's. With this technology, a batch of wafers is inserted into a quartz (or silicon carbide) tube that has been previously heated to an elevated standby temperature. The tube is then slowly raised to the desired process temperature and maintained at that temperature for a predetermined time. Once the desired time is reached, the tube is slowly cooled down to the standby temperature again, and the wafers are pulled from the tube to complete the processing. The reduction in device dimensions and the trend toward larger wafer sizes in semiconductor processing in recent years have put constraints on the time-at-temperature to which a wafer can be subjected. Consequently, alternate heating means such as rapid thermal processors, have recently been used to reduce the thermal budget on the wafer. This technology encompasses a wide range of techniques that can heat a single wafer in a very short time (10ns to 100s) to the desired temperature, up to 1400°C.

Rapid thermal processing, RTP, is a technology that has slowly been gaining popularity for implementation in semiconductor device production [ref.1]. Advances in semiconductor technology make the use of RTP inevitable. The design rules for leading-edge integrated circuits dictate that line widths be considerably smaller than 1 micron and that junction depths be less than a few hundred angstroms. To manufacture these minute devices, the time/temperature cycle for processing wafers must be limited to minimize lateral and longitudinal diffusion. This constraint, known as the thermal budget, will be the overriding reason for the eventual phase-in of rapid thermal processors and the phase-out of tube furnaces.

Additional requirements such as larger wafer sizes, wafer transfer automation, ambient control, and particulate reduction also will soon be beyond the practical capabilities of traditional tube furnaces. It is a well-accepted belief that single wafer, rapid thermal processing techniques will be necessary to meet most of the demands of the next generation of device design.

Rapid Thermal Processors

RTP can be divided into two different configurations: lamp-based RTP and continuous heat source RTP. Most of the commercial lamp-based RTP systems today use either a bank of tungsten halogen lamps or a single arc lamp as the heat source(see Fig.1). The wafer to be processed is placed in a quartz or stainless steel chamber with a quartz window between the

wafer and the lamp. Wafer heating is achieved by passing current through the lamps in a controlled manner, generating radiation which is then absorbed by the wafer. After a pre-determined duration, the lamp current is then cut off or reduced so that the wafer is cooled.

In the continuous heat source type RTP, a heat source is fixed at an elevated temperature. Wafers are moved closer or further away from the heat source to achieve the temperature ramping on the wafers (Fig.2). Ramping speeds are increased by having a higher temperature heat source and moving the wafer towards the heat source faster. The key in the continuous heat source RTP type is that the source temperature is fixed, and the heat source area is relatively large.

In general, higher source temperature results in higher ramp rate. Lamp-based RTP can generate very high source temperature, much higher than the desired wafer temperature. Continuous heat source RTP, on the other hand, has source temperature only a couple hundred degrees higher than the desired wafer temperature. To compensate for the lower source temperature, continuous heat source RTP uses a large source area to increase the total radiation flux. Even then, the ramp rate achieved on a continuous heat RTP is still slower than lamp-based RTP. However, large temperature differences between the source and the wafer tend to contribute to temperature non-uniformity on the wafer. The wafer temperature distribution may be calculated by applying the energy conservation law and equation describing heat conduction, convection, and radiation. The temperature non-uniformity on a wafer is related to the source temperature in the following manner:

$$(dT_w/dx) \propto (T_s/T_w)^3(dT_s/dx) \qquad (1)$$

where (dT_w/dx) is the wafer non-uniformity, (dT_s/dx) is the source non-uniformity, T_s and T_w are temperature of source and wafer respectively [ref 2].

It is clear from equation (1) that the temperature non-uniformity is proportional to the cube of the ratio of source temperature to wafer temperature. It is easier to achieve good temperature uniformity on the wafer surface when the temperature difference between the heat source and wafer is small.

In contrast to lamp based RTP where the heat source is powered up and down in a rapid fashion, continuous heat source RTP employs a constant heat source. One design uses a heated silicon bell jar as the heat source, maintained at a temperature of approximately 150°C above the processing temperature. The large area of the heat source enables it to heat up silicon wafers rapidly. The steady state condition of the heat source and the smaller temperature difference between the source and the workpiece directly contribute to good uniform process results.

Large area substrate RTP

When heating large substrates, such as flat panel displays or large area solar cells, the uniform heating becomes even more critical. The thinness of the substrates make the RTP

a very suitable tool to use. If the substrate is too thick, RTP heating will generate a temperature gradient across the thickness within the substrate. In designing a large area substrate RTP, several factors must be considered for the success of the tool; substrate transfer and support during processing, heat source design and control, gas flow patterns, substrate temperature measurement, and system footprint. Take LCD flat panel display for example; the glass substrate size has changed from 300mm by 400mm in the first generation to 550mm by 650mm for the most advanced fab today and will increase to 1000mm by 1000mm size in the future. With such large size, even with 1mm thickness, each piece of glass will weigh more than 2 Kilograms. This puts a lot of constraints on the system design. Figure 3 shows a RTP system that can handle 550mm diagonal size substrates.

RTP applications in FPD and solar cell

In flat panel display fabrication, there are several processes where RTP is preferred. The key is to minimize the time the glass substrate is subject to elevated temperature, so low temperature glass can be used as substrate without worry of distortion. The first application for RTP is implant anneal for TFT-LCD type FPD. Implant anneal can be accomplished within a short time of less than 1 minute, so RTP is just the right tool. The second application is the metal line sintering. This process requires 550°C for 30 seconds. The third application is amorphous silicon film to poly-silicon conversion. Figure 4 shows amorphous film to poly-conversion under various RTP process conditions. Because poly-conversion take place above 550°C, it is necessary to use rapid thermal processing to avoid the deformation of the glass substrate. However, for a very thin substrate, even RTP can not guarantee the glass flatness if not processed within the window. The forth area of RTP application is phosphor activation in EL panel. In this case, the rapid heating is required because prolonged heating induces inter-diffusion among the junction area and degrades the emission efficiency. Figure 5 shows a simplified cross section of a EL panel.

In the case of solar cell fabrication, there also a few applications where RTP can be utilized. One is dopant activation to form p-n junction. Using RTP in this case can reduce the cross diffusion between the two side of the junction. The second area is oxide growth. And the third area is again amorphous silicon film to polysilicon conversion. All these applications can take advantage of the fast heating and cooling and short process time of the single substrate loading of the RTP.

Conclusion

RTP is unique in that the substrate is processed one at a time. This is especially advantageous when the substrate is large size. The fast ramp up and down of the temperature profile means that the substrate can be processed rapidly without staying at high temperature for a long time. Since most of the applications mentioned here need time at temperature less than 1 minute, RTP processing would have the highest throughput

compared with other thermal process tools [ref 3]. As substrates are getting larger, RTP will find more applications in the flat panel display and solar panel fabrications.

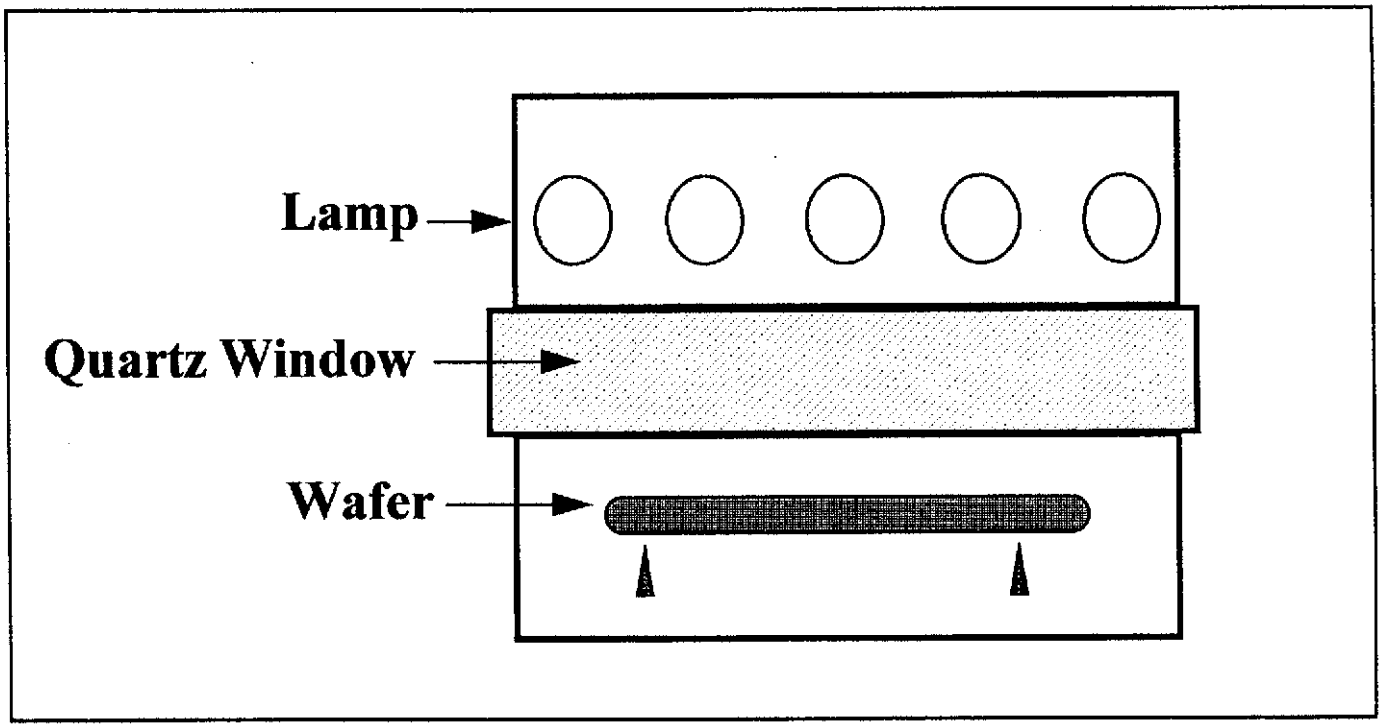
References

[1] Fred Roozeboom, editor, "Advances In Rapid Thermal and Integrated Processing", Vol. 318, Klumer Academic Publishers, 1996.

[2] C. Lee, A. Wittkower, "A Continuous Heat Source Rapid Thermal Processor", Semiconductor Fabtech, No. 1, Page 127, 1994.

[3] C. Lee, G. Noblitt, "New Generation Challenges to Thermal Processing", Semiconductor International, No. 3, 1996.

Figure One: Two Lamp Based RTP Designs



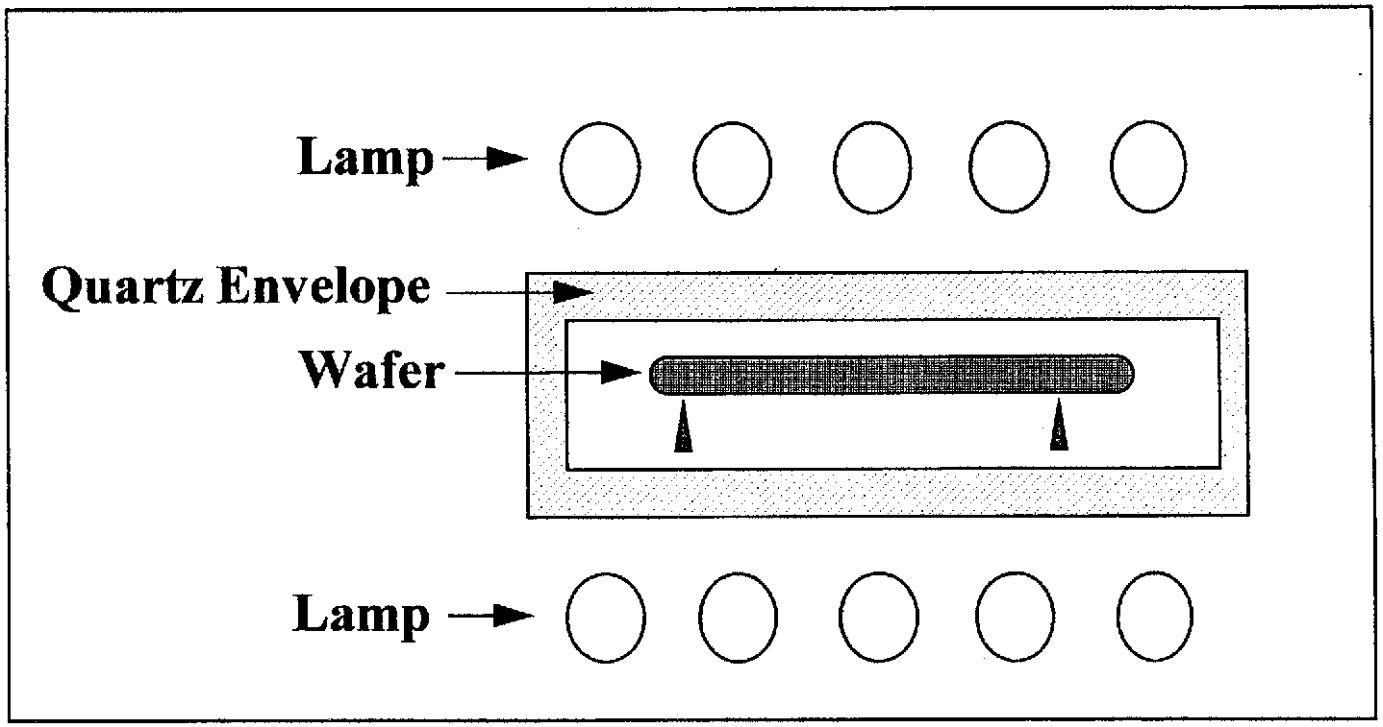
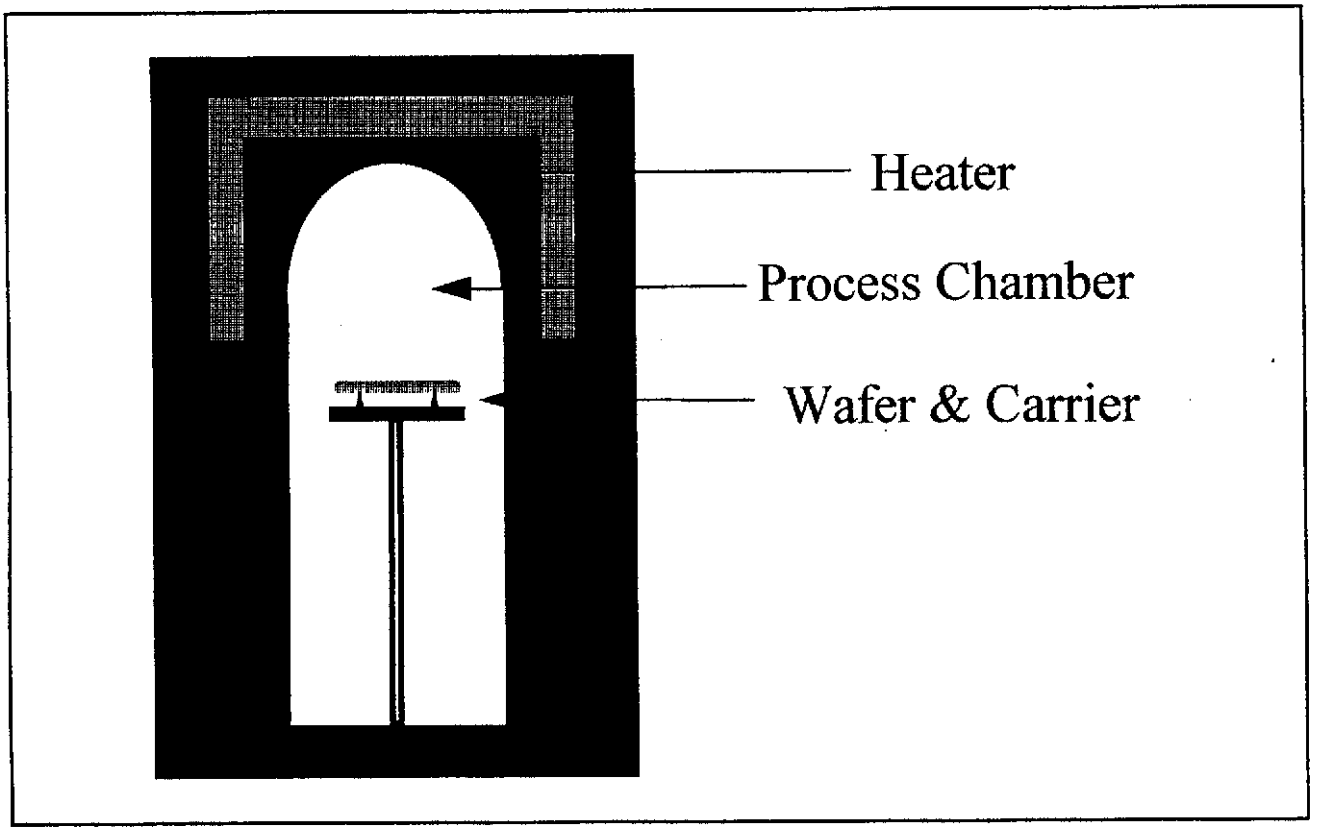


Figure Two:
Two Continuous Heat Based RTP Designs



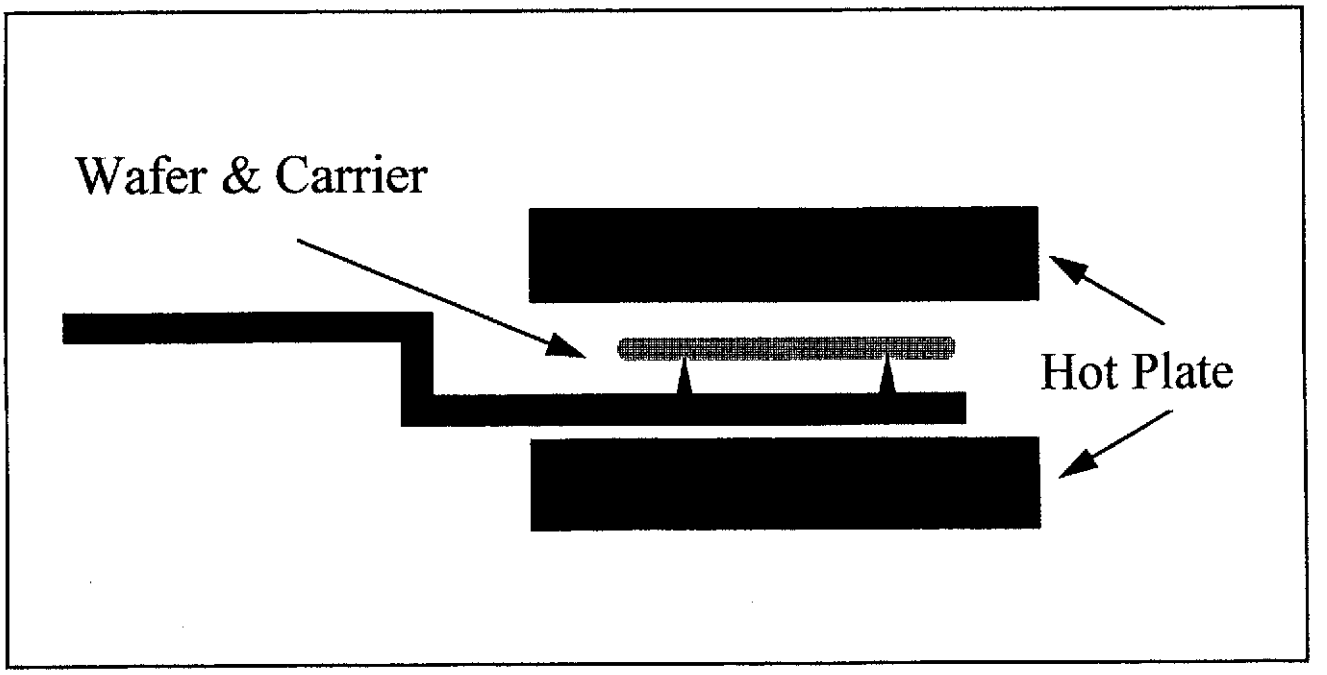


Figure Three: Large Area RTP System

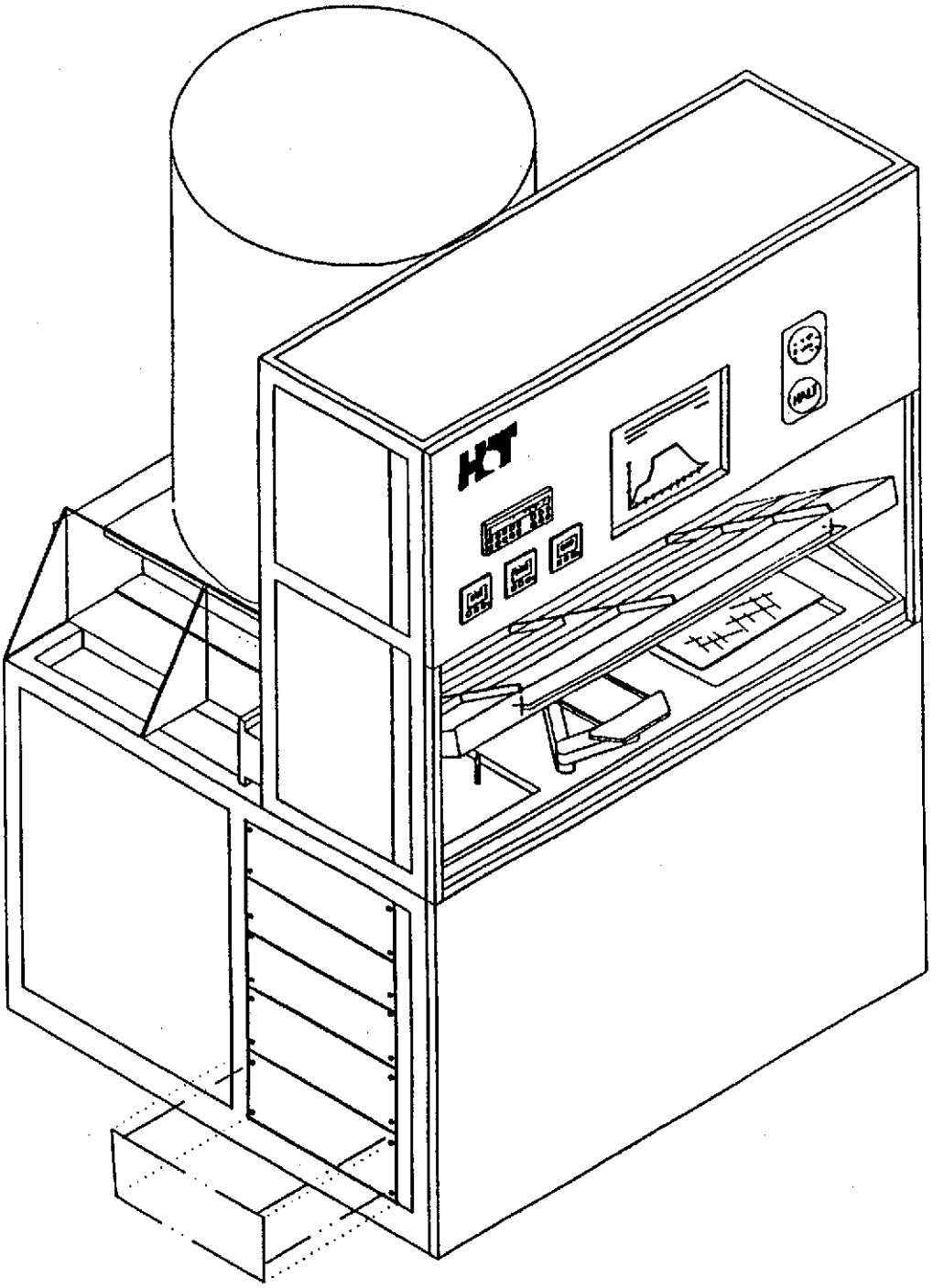


Figure Four:
Amorphous Film to Poly-Conversion Under Various RTP Conditions

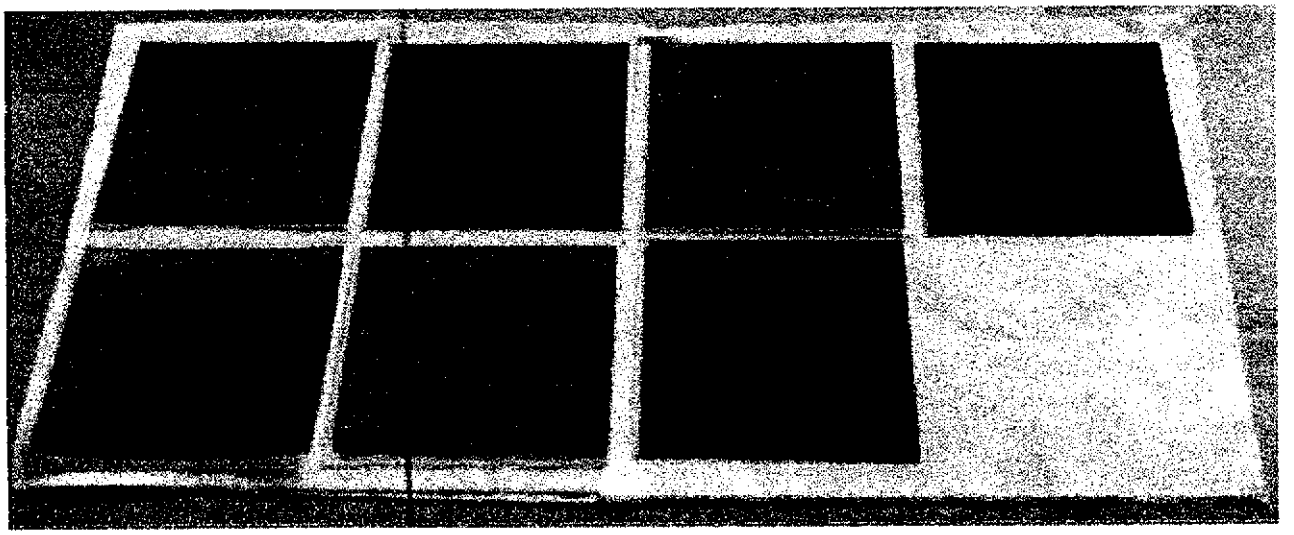
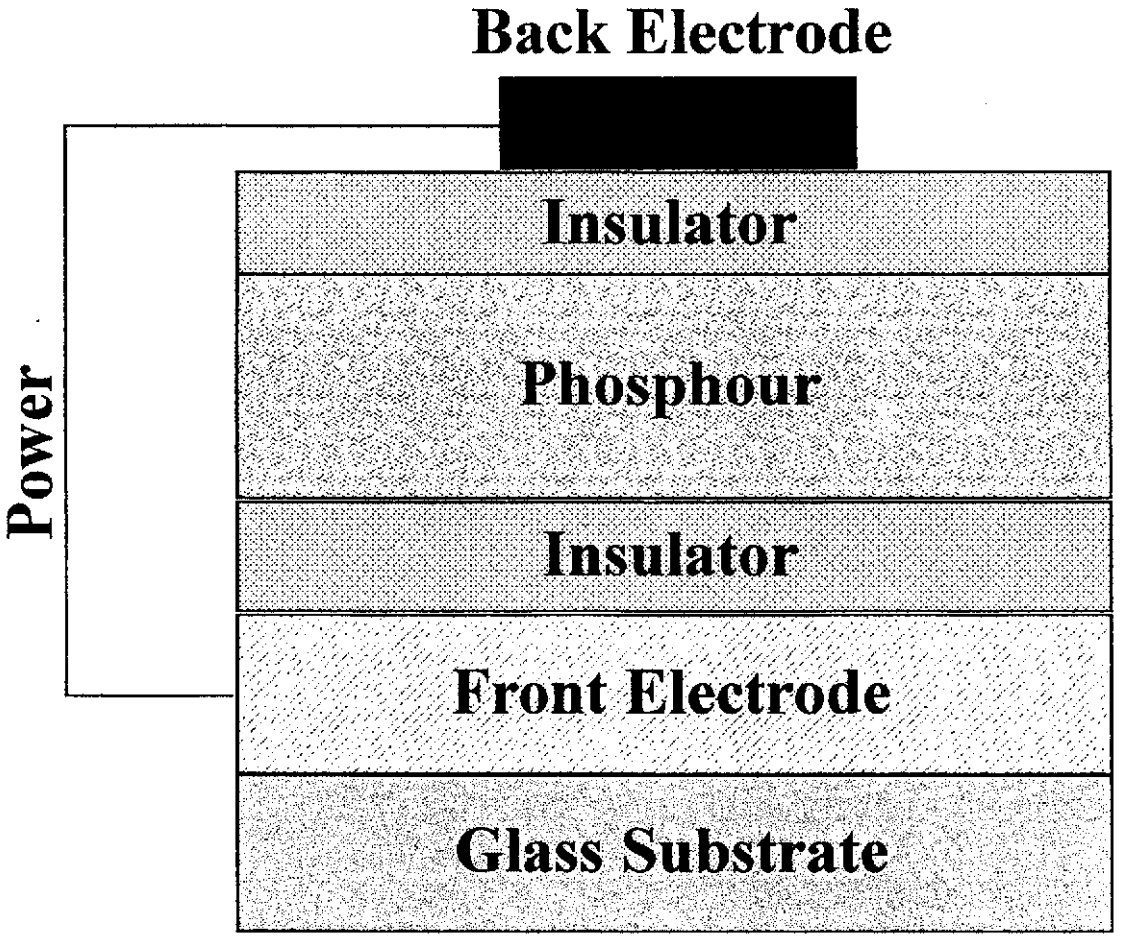


Figure Five:
Simplified Cross Section of EL Panel



100 MICRON STRING RIBBON SILICON

R. Wallace*, J. I. Hanoka*, A. Rohatgi**, and Gerald Crotty**
*--Evergreen Solar, Inc., 211 Second Ave., Waltham, MA 02154.
Tel: 617/890-7117; Fax: 617/890-7141
**--School of Electrical Engineering, Georgia Institute of Technology, Atlanta, GA 30332

Introduction

String Ribbon is a continuous sheet method of producing silicon ribbon which Evergreen Solar is commercializing. The conventional thickness of the material grown is 300 μm--similar to many other crystalline silicon solar cells now commercially available. The goal of the present work is to develop a method for growing 100 μm ribbon >5 cm wide suitable for large area solar cells to be fabricated. The advantages of such a process include: increased growth rate and machine thruput; 1/3 as much silicon needed; and the potential for high efficiency cells with thin substrates. In this report we describe the work done so far in growing flat, low stress 100 μm ribbon and some R&D solar cell results obtained with this material.

Crystal Growth

Figure 1 shows the conventional String Ribbon crystal growth method. Two strings of a high temperature material are brought up through a shallow silicon melt and a continuously grown ribbon is formed between the strings, conceptually not unlike soap bubble formation. The strings serve to stabilize the edges of the growing ribbon and then allow for virtually continuous ribbon growth in a simple and robust way. The conventional material, 300μm thick, is grown with a minimal, passive afterheater.

Last summer, at this same meeting, it was reported that very thin ribbon can be grown with the String Ribbon method. Ribbon anywhere from 100 μm down to 5 μm was grown. However, all this material was grown without any significant afterheater present and so was highly stressed and/or buckled and not suitable for solar cell making.

As is well known to anyone who has done Si ribbon growth, thermal stresses can be imposed on the ribbon by curvature in the cooling profile. If the stresses are large, the ribbon buckles. Therefore, manipulation of the cooling profile is needed to produce flat, thin ribbon.

At Evergreen, a project to design an afterheater to reduce the stress in 100 μm (>5cm wide) ribbon has been ongoing for the past year. The afterheater was designed to be "active" not passive. An active afterheater could be much more readily changed to produce a desired thermal profile. The deployment of the active afterheater was such that it was placed symmetrically on either side of the growing ribbon close to the melt and for some distance above it.

The crystal growth results obtained using this active afterheater were very promising. Figure 2 illustrates this. Three lengths of String Ribbon were grown with

differing thermal conditions imposed by the afterheater. The degree of flatness of each length of ribbon is indicated by how accurately the as-grown ribbon surface reflects the striped pattern in the rear of this picture. The sample in the rear was quite flat and represented the best conditions obtained. The contour profiles of Figure 3 also illustrate this.

Solar Cell Results

1 cm^2 and 4 cm^2 size cells were fabricated on the 100 μm String Ribbon material. The cells were made using evaporated metal contacts, surface oxide passivation, and PECVD silicon nitride. The starting material was highly doped at 0.1Ω-cm so the starting lifetime was somewhat low, about 0.8μs. The best 1 cm^2 cell made this way had a f.f. of .798, a J_{SC} of 28.8 ma/cm^2, a V_{OC} of 639 mv, and an efficiency of 14.7%

The starting lifetime of this material exhibited considerable sensitivity to processing. In one case, the as grown lifetime as measured by laser PCD was 0.82 μs. An RTP diffusion cycle of 925°C for 30 sec (without any dopant) gave a lifetime of 6.5 μs and then a PECVD SiN deposition at 350°C resulted in a lifetime of 17.3 μs. The latter value may be somewhat questionable, but the overall sensitivity and possible improvements in lifetime with processing are clearly being manifested. PCID modeling indicates that the prognosis for making 16% cells in the material seems excellent.

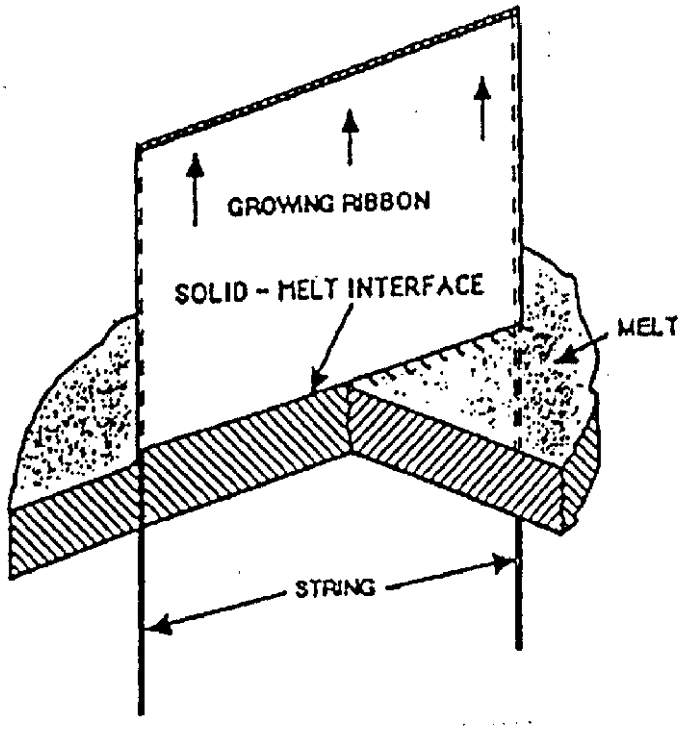


Figure 1: Schematic diagram of the String Ribbon growth process

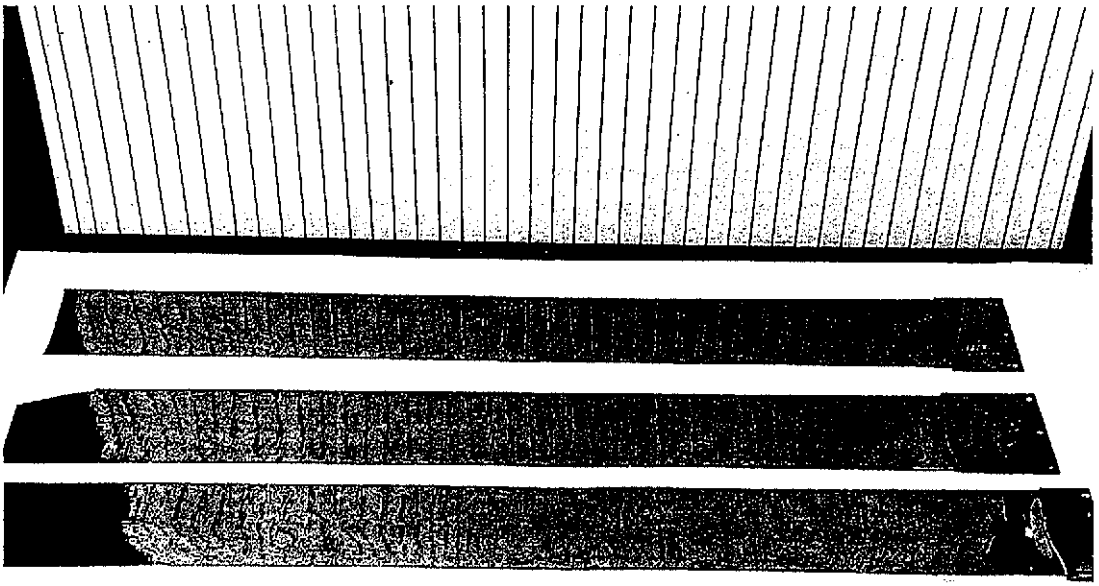


Figure 2. Flat(rear) and buckled (front) 100 μm ribbon

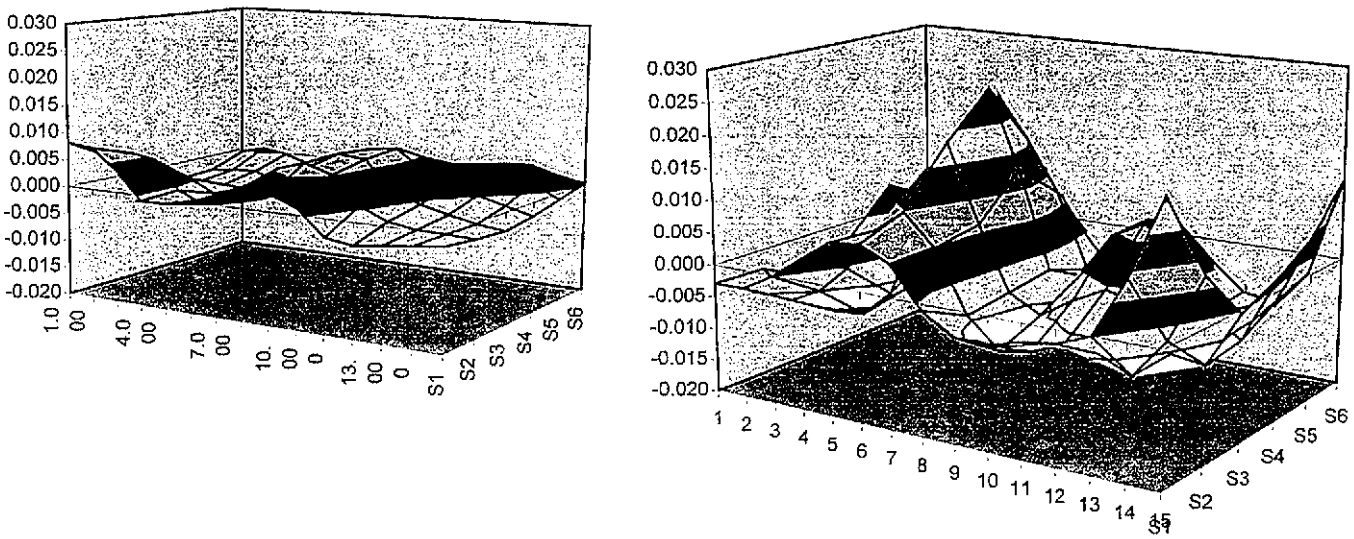


Figure 3. Contour maps of flat and buckled 100 μm ribbon

INTERACTIONS BETWEEN METALLIC IMPURITIES AND STRUCTURAL DEFECTS IN PHOTOVOLTAIC GRADE SILICON

Scott A. McHugo
Advanced Light Source, MS 2-400, Lawrence Berkeley National Laboratory, Berkeley, CA 94720

H. Hieslmair and E.R. Weber
Department of Materials Science, University of California at Berkeley, CA 94720

Abstract

The work presented here addresses structural defect-metallic impurity interactions in photovoltaic silicon and their effect on material performance. Aluminum segregation gettering was performed on photovoltaic silicon to gain an understanding of these interactions and their effect on solar cell performance. In addition, a novel rapid thermal annealing technique and Deep Level Transient Spectroscopy were utilized to determine the as-grown impurity concentration in both grades of materials. Significant differences in gettering responses and initial impurity concentrations are observed between solar and integrated circuit grade silicon. Gettering treatments greatly improve I.C. grade silicon while photovoltaic grade silicon does not respond as well and, in some regions of the material, the gettering response degrades at higher temperatures. This degradation is primarily observed in dislocated regions of multicrystalline silicon which concurrently possess the highest as-grown metallic impurity concentration of all materials studied. Dislocation-free photovoltaic silicon has a higher diffusion length relative to dislocated silicon but could not be improved by the gettering methods employed in this study. A model is presented to describe these phenomena where microdefects create an upper limit to the photovoltaic grade material's diffusion length and the high concentration of metallic impurities at dislocations produce relatively low minority carrier diffusion lengths as well as the degrading response with higher gettering temperatures.

Introduction

Solar grade silicon, in single crystal and multicrystalline form, are the most promising materials for cost-competitive terrestrial solar cells. An important property of this material is that once the material's minority carrier diffusion length (L_n) drops below the material's thickness, the cell efficiency is drastically reduced. L_n values of as-grown solar grade silicon are regularly under the cell thickness which necessitates steps for material improvement. These low L_n values have been attributed to the presence of dislocations and microdefects [1-3] whose effect on L_n is greatly exacerbated by the decoration/precipitation of metallic impurities at these defects [4-6]. Therefore, it is advantageous to remove, or getter, metallic impurities from the material and, in turn, enhance the material's L_n. Standard solar cell processing steps intrinsically possess gettering capabilities. For example, the p-n junction formation consists of a phosphorus in-diffusion which has been regularly observed to getter metallic impurities [7-11]. Additionally, aluminum backside sintering, which forms the ohmic backside contact, is also a method for metallic impurity gettering [11-14]. These processing steps should remove a significant amount of impurities and improve cell performance, however, full realization of this expectation has not occurred.

Our past work [15,16] has shown that I.C. grade silicon responds well to Al gettering treatments with a specific temperature yielding the best response as predicted in [8]. Solar grade silicon do not respond well, with either an invariant response to gettering temperature or a decrease in response with increasing temperature. The degrading response occurs in regions of multicrystalline (mc) silicon with high dislocation densities. Also, rapid thermal annealing treatments enhanced the response of only one type of solar CZ while other solar CZ, mc-silicon and I.C. silicon were not affected. The work presented here addresses metallic impurity-structural defect interactions in solar grade silicon. The objective is to understand the effect dislocations and microdefects have on gettering of metallic impurities in solar grade silicon, particularly in regions of low minority carrier diffusion length. Quantitative results of gettering efficiency in solar and I.C. grade silicon are presented as well as structural defect and metallic impurity characterization. With these results, a model is proposed to explain gettering in both solar and I.C. grade silicon which guides future studies of impurity-structural defect interactions.

Experimental Procedure

The solar grade materials used in this work were obtained from a variety of solar cell manufacturers. CZ solar grade silicon from two different manufacturers (denoted as solar CZ I and IIa&b) were included as well as ribbon grown multicrystalline (mc-) silicon (denoted as ribbon) and cast mc-silicon from three different manufacturers (denoted as cast II and III). I.C. grade CZ and FZ were used for comparison. Oxygen concentrations [cm^{-3}] were: solar CZ I $\approx 10^{18}$; solar CZ IIa&b, cast III mc and I.C. CZ $\approx 9\times10^{17}$; ribbon, cast II mc and FZ $<10^{17}$. Carbon concentrations [cm^{-3}] were: solar CZ I, IIa, I.C. CZ and FZ $<10^{16}$; solar CZ IIb $\approx 2\times10^{17}$; ribbon mc $\approx 8\times10^{17}$; cast II&III mc $<5\times10^{17}$. For mc-silicon, samples with the same grain structure, i.e. along the growth direction, were used, in order to retain the same microstructure and properties over a number of

samples. Samples from all materials were subjected to a piranha cleaning with an HF dip and slight Si etch (≈ 0.2μm) in VLSI grade sinks prior to all annealings, Surface Photovoltage (SPV) and Fourier Transform Infrared Spectroscopy (FTIR) measurements, preferential etchings and diode formation steps. All gettering anneals were performed in furnaces used for daily I.C. device fabrication, ensuring clean processes. For Al gettering, a high purity Al layer was sputtered onto the sample backside followed by sample annealing in an Al sintering furnace with a N_2 atmosphere. The Al layer was etched away with a metal etchant and 5-10μm was removed with a silicon etch to ensure all Al doped silicon was removed. Rapid Thermal Annealing (RTA) treatments were conducted in a commercially available system in a N_2 atmosphere at 1100°C for 45 seconds after which the samples were slowly cooled to 500°C within ≈ 1 min and to 300°C in 5 mins. RTA Quenching (RTAQ) treatments were carried out with a custom built system which allows for a rapid quench (≈ 1000K/sec) of the sample after anneals at 1100°C for either 45 sec or 4 min in a N_2 atmosphere.

SPV measurements of L_n were used to quantify the gettering response in this study. Deep Level Transient Spectroscopy (DLTS), with typical sensitivity limits on the order of 10^{11} impurity atoms/cm^3, was utilized to identify and quantify metallic impurities in the various silicon materials. Oxygen concentrations were measured using FTIR before and after annealing treatments (new ASTM). With these measurements and subsequent calculations using mass conservation and Ham's law [17], the oxygen precipitate density and radius were quantified. Defect densities of the various materials was determined by preferential etching and surface analysis.

Results

The influence of gettering time and Al layer thickness on the material's gettering response was studied for solar grade materials. These experiments are designed to determine whether the gettering of solar grade materials is limited kinetically or thermodynamically. The aluminum layer thickness influences the thermodynamics of the gettering process via the effective segregation coefficient, defined as: $C_{imp\text{-}Si}/C_{imp\text{-}Si_o} = t_{Si}/(t_{Si} + S\, t_{Al})$, where $C_{imp\text{-}Si}$ is the impurity concentration after gettering, $C_{imp\text{-}Sio}$ denotes the initial impurity concentration and t is thickness. S is the ratio of an impurity specie in the gettering layer to that in the silicon matrix, estimated as 10^5-10^6 by considering the maximum solubility for metallic impurities in silicon [18] and the solubility of metallic impurities in Al and Al-Si. It is apparent that a thicker aluminum layer will remove more impurities from the silicon. Aluminum gettering on as-grown solar grade materials was carried out for 1, 3 or 5 hrs at 850°C with either a 2.5μm or 0.25μm thick Al layer on the sample backside. These different thicknesses allow for an order of magnitude difference in post-gettering impurity concentrations. Figure 1 shows the time and thickness dependence for solar CZ I and II materials. The y-axis denotes the L_n value after gettering. We see the solar CZ I and the high carbon solar CZ II materials responses did not vary for any thickness or gettering anneal time. The solar CZ I material retained its initial L_n value while the high carbon solar CZ II material degraded significantly from its initial value. However, the low carbon solar CZ II L_n value shows a kinetic degradation from 1-3 hrs after which it stabilizes at a low L_n. Varying gettering times and aluminum thicknesses was also performed on regions 1-4 of ribbon mc-silicon. No significant change in gettering response is apparent for any of the regions. It must be noted that dislocation climb should be active at 850°C and should continue with increasing time. Since no change of L_n is observed with time, this data indicates dislocation motion is not responsible for L_n degradation.

With high temperature treatments, impurity precipitates should dissolve into the material and/or impurities would be rapidly released from their previous site. In turn, the aluminum gettering treatments would be more effective since the barrier for dissolution or release would have already been circumvented. Based on this premise, RTA and RTAQ heat treatments have been applied to solar grade materials [15,16] yielding beneficial results in some solar grade CZ materials but not in the mc-silicon materials studied. These results are reproduced in Figure 2 for convenience. The y-axis displays L_n values in the as-grown state, after only Al gettering, after RTA/Al gettering and after RTAQ/Al gettering treatments. The solar CZ II materials show dramatic improvement with both RTA and RTAQ processes. The treatments retain the material's as-grown L_n values while Al gettering alone degrades the material. Apparently the RTA and RTAQ treatments remove this degrading mechanism.

In the work presented here, these 1100°C/45 sec RTA or RTAQ pretreatments were applied to high and low performance regions of cast mc silicon materials prior to a 900°C/3 hr aluminum gettering treatment. The performance rating was based on solar cell parameters after full cell processing at Sandia National Laboratory. Again the hope was to see an enhanced gettering action via impurity dissolution. The results indicate the RTA or RTAQ treatments had little or no effect for any of the cast mc studied, both high and low performance regions. Figure 3 displays the results for RTA/RTAQ Al gettering treatments for cast III mc-silicon. The low performance regions of the cast III material drastically degraded from their initial L_n after all treatments. As with the ribbon material, this degradation correlated with a high dislocation density. Considering the low cell performance of these regions it seems that the solar cell processing degrades the material just as the gettering steps in this study.

In order to determine the influence of oxygen precipitation on L_n degradation in solar CZ II silicon, FTIR was used to measure interstitial oxygen (O_i) concentrations. In addition, to quantify the effect of the RTA/RTAQ pretreatments on oxygen precipitate densities (n) and radii (r), Ham's law [17] and the mass-balance equation were employed The change in O_i concentration, shown in the first column of Table 1, reveal a significant amount of oxygen has precipitated after the 900°C/3hr Al gettering anneal, especially in the high carbon material. More importantly, it is apparent that less oxygen precipitation occurs when either a RTA or RTAQ pretreatment is employed. These results and the calculations of precipitate density suggest that the pretreatments have dissolved oxygen precipitate nuclei such that during the Al gettering treatment the density of large oxygen precipitates does not increase significantly, thus the degradation mechanism has been removed. High temperature treatments have been used to dissolve oxygen precipitate nuclei sites, [19,20], supporting this model. One should also note that the density of oxygen precipitates is very high for all samples. In as-grown I.C. grade CZ silicon, precipitate densities are typically much lower. This high density could explain the solar material's poor performance.

Initial impurity concentrations of FZ, I.C. CZ, high carbon solar CZ II, cast II material (high and low performance regions) and cast III material (low performance region) were measured with a 1100°C, 4 min RTAQ treatment followed by DLTS measurements. The concept was to dissolve all impurity precipitates and then measure impurity concentrations in each material. DLTS measurements only detected Fe-B. The data, shown in Figure 4, are an average of 3-4 measurements on each sample. A typical spread in data for one material type was ±10%. We see the I.C. grade CZ possesses a very small impurity concentration, indicative of the material's and the RTAQ process' cleanliness. Surprisingly the FZ material has a significant Fe level, greater than the solar CZ II material. The detection limit for the solar CZ II material is high due to its low resistivity which limits DLTS sensitivity. Of particular interest is that high Fe concentrations correspond with low performance regions in the cast II mc. The low performance cast III material has the highest Fe concentration of all the materials, indicating that Fe is linked to the dislocations in these regions and the poor gettering response. DLTS revealed no Fe in any as-grown materials, indicating the Fe is released during the RTAQ treatment.

Discussion, Conclusions & Future Work

From past work [15,16] we've seen gettering of metallic impurities is more effective in I.C. grade silicon than solar grade silicon. Considering the invariant response of solar materials holds over a wide variance of temperatures and times, a plausible cause for the invariance is the high concentration of microdefects in the solar CZ (Table 1) and mc-silicon ($\approx 10^{11}$-10^{12} cm^{-3}) [1,6]. These microdefects create a maximum L_n and in turn limit material performance. The results also indicate that metallic impurities decorated/precipitated at the dislocations are the source for the degrading response. The high concentration of impurities at dislocations occurs during the cool from growth with the dislocations acting as preferable precipitation sites for metallic impurities. In dislocation-free regions, impurities diffuse either to these dislocated regions or to the surface where they are easily removed. The concept of a preferable precipitation site has been observed in past work on impurity precipitation with slow cooling rates [6,21]. In theory, these dislocated regions could have impurities dissolved or in precipitate form corresponding to concentrations of up to the impurity's solubility in silicon ($\approx 10^{18}$ cm^{-3} for some impurities). Of course, the question for these dislocated mc-silicon materials is why they degrade with increasing gettering temperature. This can be understood if one considers the gettering process does not run to completion for the times used in this study. With incomplete gettering, the impurities are left dispersed throughout the silicon lattice after the treatment. The temperature dependent degradation occurs because more impurities are left in the lattice at higher temperatures. This incomplete gettering can occur via stabilization of the impurity at the defect during the gettering process. Based on these conclusions, future studies should address the nature of microdefects in these materials as well as means for decreasing their concentration. Also, determination of the thermodynamics and kinetics of metallic impurity release from structural defects is crucial for material improvement.

References

1) J. Bailey and E.R. Weber, Phys. Stat. Sol. (a) **137**, 515 (1993)
2) S.A. McHugo, J. Bailey, H. Hieslmair and E.R. Weber, in 1994 IEEE First World Conference on Photovoltaic Energy Conversion, Waikoloa, Hawaii, U.S.A., 1994, p. 1607
3) B.L. Sopori, L. Jastrzebski, T. Tan and S. Narayanan, in Proceedings of the 12th European Photovoltaic Solar Energy Conference, Netherlands, 1994, p. 1003
4) V. Higgs and M. Kittler, Appl. Phys. Lett. **63**, 2085 (1993)
5) T.H. Wang, T.F. Ciszek and T. Schuyler, Solar Cells **24**, 135 (1988)
6) S.A. McHugo and W.D. Sawyer, Appl. Phys. Lett. **62 (20)**, 2519 (1993)
7) L. Baldi, G. Cerofolini and G. Ferla, J. Elec. Chem. Soc. **127**, 164 (1980)
8) J.S. Kang and D.K. Schroder, J. Appl. Phys. **65**, 2974 (1989)
9) W. Schröter and R. Kühnapfel, Appl. Phys. Lett. **56**, 2207 (1990)

10) L. Jastrzebski, W. Henley, D. Schielein and J. Lagowski, J. Elec. Chem. Soc. **142**, 3869 (1994)
11) R. Gafiteanu, U. Gösele and T.Y. Tan, in Materials Research Society Spring Meeting, Symposium B, San Francisco, CA, U.S.A., 1995, p. 297
12) P. Sana, J. Salami and A. Rohatgi, IEEE Transactions on Electron Devices **40**, 1461 (1993)
13) M. Apel, I. Hanke, R. Schindler and W. Schröter, J. Appl. Phys. **76**, 4432 (1994)
14) S.M. Joshi, U.M. Gösele and T.Y. Tan, J. Appl. Phys. **77**, 3858 (1995)
15) S.A. McHugo, H. Hieslmair and E.R. Weber, in Defects in Semiconductors 18, International Conference on Defects in Semiconductors, edited by M. Suezawa and H. Katayama-Yoshida, Sendai, Japan, 1995, p. 1979
16) S.A. McHugo, H. Hieslmair and E.R. Weber, Appl. Phys. A, in print, 1996
17) F.S. Ham, J. Phys. Chem. Solids **6**, 335 (1958)
18) E.R. Weber, Appl. Phys. A **30**, 1 (1983)
19) F. Shimura, Appl. Phys. Lett. **39**, 987 (1981)
20) S. Ishikawa, M. Matsushita and J.-I. Shimomura, in Defects in Semiconductors 18, International Conference on Defects in Semiconductors, edited by M. Suezawa and H. Katayama-Yoshida, Sendai, Japan, 1995, p. 1823
21) B. Shen, T. Sekiguchi, J. Jablonski and K. Sumino, J. Appl. Phys. **76**, 4540 (1994)

Figures

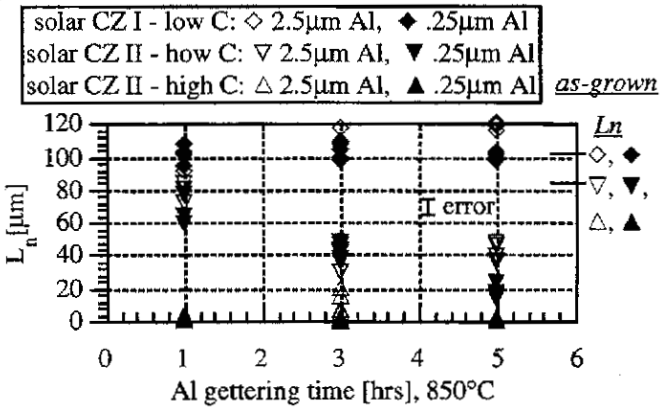


Figure 1: Solar CZ I and II gettering response dependence on gettering time and aluminum layer thickness.

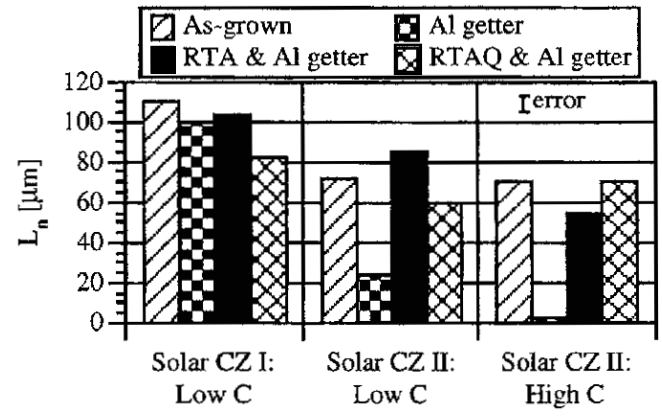


Figure 2: RTA & RTAQ with aluminum gettering results for solar grade CZ I and II.

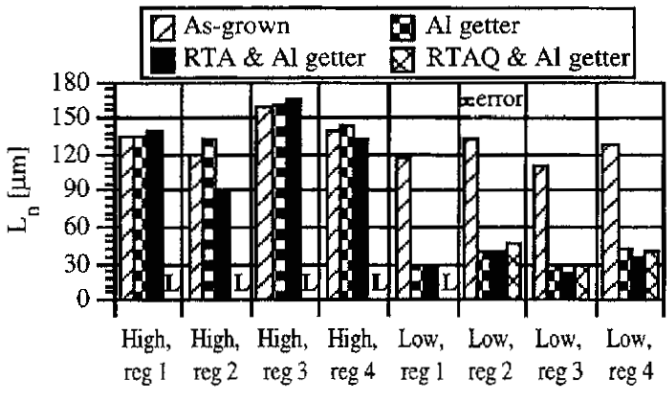


Figure 3: RTA & RTAQ with aluminum gettering results for as-grown cast III mc-silicon, high and low performance regions. L denotes sample was lost during processing.

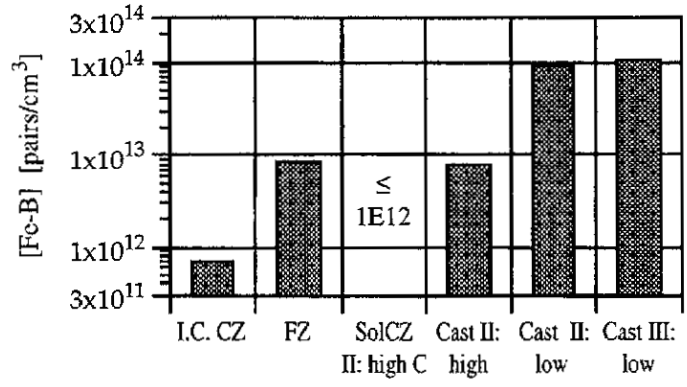


Figure 4: RTAQ/DLTS results of FZ, IC CZ, high C solar CZ II, high & low performance cast II mc and low performance cast III mc.

sample	Δ Oxygen, $[\Delta O_i]$ (cm^{-3})	Precip. density, n (cm^{-3})	Precip. radius, r (nm)
Al gett, High C	- $2x10^{17}$	$9.72x10^{11}$	9.76
RTA- Al gett, High C	- $3x10^{16}$	$1.69x10^{11}$	10.2
RTAQ- Al gett, High C	- $5x10^{16}$	$2.55x10^{11}$	10.2
Al gett, Low C	- $6x10^{16}$	$2.31x10^{11}$	10.4
RTA-Al gett, Low C	+ $1x10^{16}$	-	-
RTAQ-Al gett, Low C	- $4x10^{16}$	$1.55x10^{11}$	10.4

Table 1: Interstitial oxygen change, oxygen precipitate and radii values in high & low carbon solar CZ II silicon.

Iron Precipitation Kinetics in Silicon and the Relation to Carrier Diffusion Lengths and Aluminum Gettering

Henry Hieslmair, Scott McHugo, and Eicke Weber
Department of Materials Science and Mineral Engineering
University of California, Berkeley
Berkeley, CA 94720

Abstract

Precipitation of iron in FZ silicon was investigated. It was observed that the precipitation site density and radius product (nr_o), obtained from Ham's law, increased as the iron supersaturation increased. This nr_o product ranged from $1x10^3/cm^2$ to $4x10^5/cm^2$ as the annealing temperature dropped from 600°C to 235°C. The minority carrier diffusion length does not significantly change on precipitation from the dissolved state. This indicates that at small supersaturations, as during a slow cool from melt, iron would only precipitate at highly favorable precipitation sites leading to minority carrier diffusion length inhomogeneities and weak Al gettering responses.

Introduction

This work was motivated and is a continuation of a previous paper[1]. In that study, various effects of processing, including precipitation during a slow cool, were studied so that the effects of aluminum backside gettering on minority carrier diffusion lengths could be isolated. Thus precipitation of iron in silicon was studied as possibly improving Ln.

Aluminum Gettering

Our past work[2,3,4,5] has shown various responses to backside aluminum gettering for different materials. For some of the silicon materials, particularly the polycrystalline materials, we observed a small or invariant response to aluminum gettering and questions arose as to the actual segregation coefficient and effectiveness of aluminum gettering. Thus, a study was performed on FZ silicon where the gettering temperature was the same as the initial iron contamination temperature. This prevents any significant effects of precipitation on the gettering.

The results of the gettering are shown in Figure 1. Two types of samples were simultaneously annealed. The first group of five samples (left five samples in Figure 1) had intentional iron contamination and approximately 0.65 μm of aluminum evaporated onto the back of the samples. The second group (right five samples in Figure 1) has no aluminum but has been intentionally iron contaminated. The gettering times and temperatures were the same as the intentional iron contamination

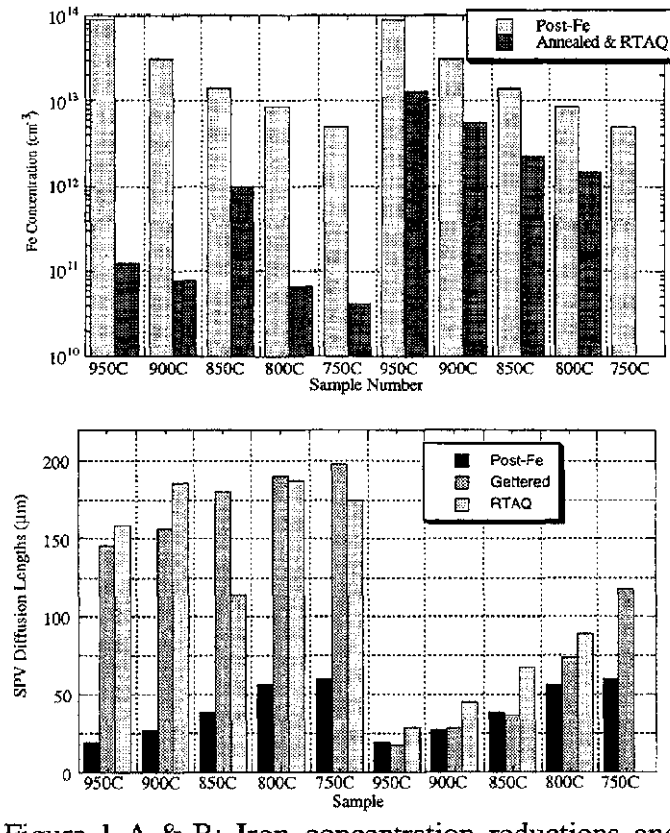


Figure 1 A & B: Iron concentration reductions and minority carrier diffusion length improvements after aluminum backside gettering

times and temperatures, and are shown in Table 1.

Segregation Coefficients were obtained for these gettering runs and ranged from 10^5 to 10^6 and might be up to 10^7 based on finite differences modeling. Thus aluminum gettering is indeed very effective.

Sample	1	2	3	4	5
Temp C	950	900	850	800	750
Time min	40	60	85	110	150

Table 1: Iron diffusion and aluminum gettering temperatures and times

Iron Precipitation and Ln

The difficulty of evaluating gettering efficiency by minority carrier lifetimes or diffusion lengths, as has been done in the past, is that the backsurface field may influence these measurements. Additionally, precipitation, during the slow cool after the gettering or during further processing, could alter the diffusion lengths. Thus, precipitation studies were performed to rule out possible Ln improvements due to precipitation. Two precipitation anneals were performed, one at 600°C and the other at 235°C The results of these precipitation studies are shown in Figure 2 and Figure 3. The temperatures shown next to the sample numbers refer to the temperature at which the intentional iron contamination was performed at. The 950°C samples thus had approximately 1×10^{14} Fe/cm^3 and so on.

One can see that for high starting concentrations of Fe, there is a slight improvement in diffusion length whereas for lower initial Fe concentrations, the diffusion length remains approximately constant or degrades. Thus, the iron remains highly recombination active, independent of whether it is dissolved or precipitated. Additionally, the precipitation rates are different at 600°C for different supersaturations of iron where as at 235°C the precipitation rates are very similar. This is what motivated further investigation into the precipitation of iron in silicon.

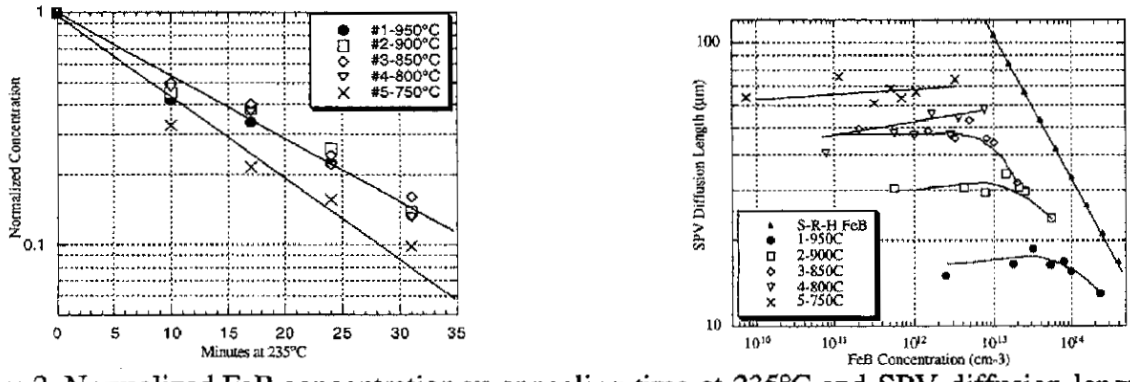


Figure 2: Normalized FeB concentration vs annealing time at 235°C and SPV diffusion lengths vs FeB concentration annealed at 235°C.

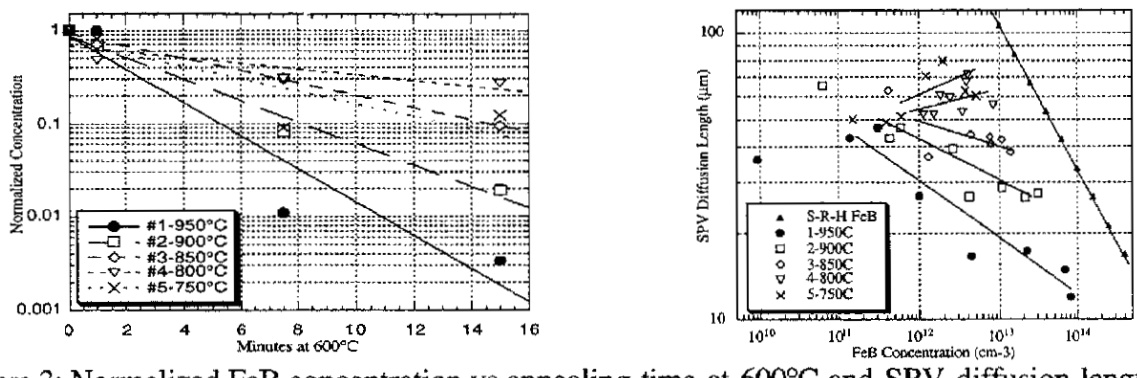


Figure 3: Normalized FeB concentration vs annealing time at 600°C and SPV diffusion lengths vs FeB concentration annealed at 600°C.

Results and Discussion

Two groups of FZ silicon samples were intentionally contaminated with iron. The 'high' group had an initial concentration of 1×10^{14} Fe/cm^3 and the 'low' group had a concentration of 4.2×10^{12} Fe/cm^3. These samples were then annealed for various times at 600°C, 475°C, or 350°C. The data for annealing at 235°C was taken from the previous study discussed above. The precipitation results are shown in Figure 4. From these slopes nr_o products were obtained using Ham's equation for spherical precipitates[6]:

$$nr_o = 4D\pi\tau$$

Here nr_o refers to the precipitation site density and radius, D is the diffusivity and $1/\tau$ is the precipitation rate. These products are shown in Figure 5 and demonstrate a clear dependence on supersaturation. At 600°C, the iron solubility is 2×10^9 Fe/cm^3 and the difference in iron concentration of the 'high' and 'low' samples are significant in comparison. The result is a slower precipitation rate in the 'low' sample which is not as supersaturated as the 'high' sample. As the annealing temperature drops, the supersaturation becomes so large in both samples that the difference in the 'high' and 'low' samples become negligible and both have the same nr_o products. This is similar to observations by Shen[7] and McHugo[8] who observed copper decoration at certain sites only during a fast cool. This also implies that at *low* supersaturations, such as during a slow cool from melt or other high temperature processing, nr_o will be small and iron will only precipitate at the <u>most</u> favorable sites. We can speculate that these are probably sites on dislocations, at SiO_2 particles or in grain boundaries. Additionally, since at high temperatures iron diffuses quickly, it is likely that much of the iron will diffuse to these few favorable sites which become highly recombination active. The probable result of this is inhomogeneities in Ln. Additionally, these few precipitates could also continuously emit the impurity when gettering at a lower temperature. This can significantly slow the gettering process and would qualitatively explain our results.

The measurements of minority carrier diffusion length as a function of iron precipitation in this study have slightly different results as the previous study. The anneal at 600°C improved the Ln from 16 to ≈40 μm in the previous study [1] while in this study the diffusion length improved from approximately 18 to 21 μm. However, both studies still dramatically show that precipitated iron is still very recombination active. Once it is in the silicon it must be removed from the device areas which, for photovoltaics, is the entire wafer.

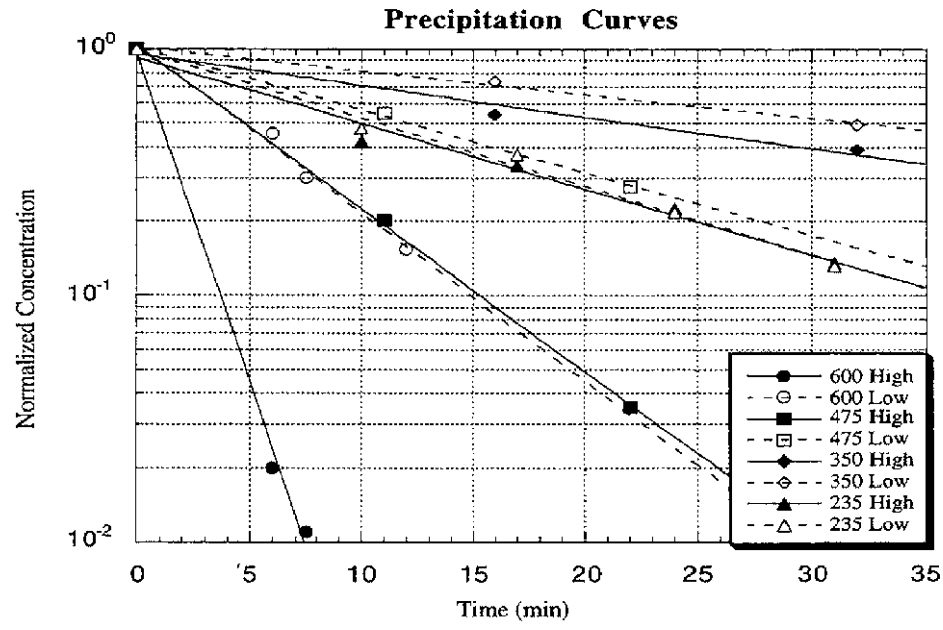


Figure 4: Precipitation rates for iron in silicon at various annealing temperatures.

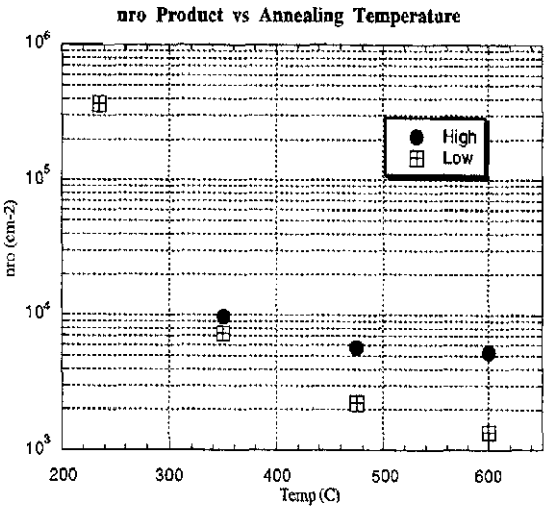


Figure 5: nr_o products vs anneal temperatures

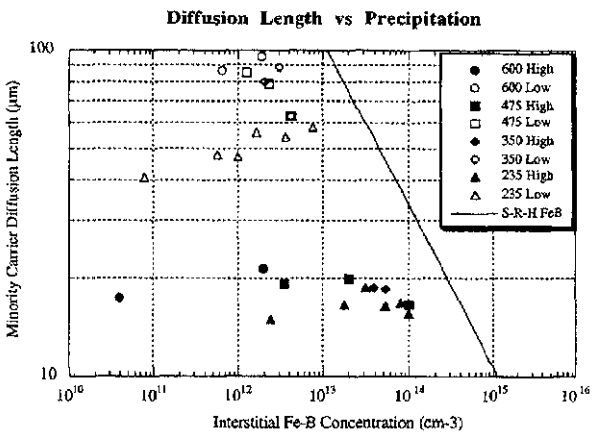


Figure 6: Ln Vs FeB concentrations

Conclusions

We have observed that the precipitation rate and nr_o depend on the amount of supersaturation of the iron. At low supersaturations, iron will precipitate at only few, highly favorable precipitation sites. This implies that during a slow cool from melt, any iron impurity will precipitate in certain favorable areas which become the highly recombination active zones, resulting in Ln inhomogeneities. At higher supersaturations, iron will precipitate out readily at numerous sites. The iron remains highly recombination active in either the dissolved or the precipitated form.

---

1 H. Hieslmair, S. McHugo and E. R. Weber,"Aluminum Backside Segregation Gettering", In: IEEE 25th Photovoltaics Specialists Conference, Washington D.C., May 13-17, 1996, To be published,

2 S. A. McHugo, H. Hieslmair and E. R. Weber, "Gettering of Metallic Impurities in Photovoltaic Silicon", Appl Phys A, in print, (1996)

3 S. A. McHugo, H. Hieslmair and E. R. Weber,"Aluminum Gettering in Single and Multicrystalline Silicon", In: 5th NREL Workshop on Role of Point Defects, Copper Mountain Co, (1995)

4 H. Hieslmair, S. McHugo and E. Weber,"External Gettering Comparison and Structural Characterization of Single and Polycrystalline Silicon", In: Defect and Impurity Engineered Semiconductors and Devices, MRS Symposium, San Francisco, MRS, 327 (1995)

5 S. A. McHugo, H. Hieslmair and E. R. Weber, "Gettering of Transition Metals in Multicrystalline Silicon", in Defects in Semiconductors 18, ed. M. Suezawa and H. Katayama, Materials Science Forum, vol 196-201, 1979 (1995)

6 F. S. Ham, "Theory of Diffusion-Limited Precipitation", *J. Phys. Chem. Solids*, **6**, 335 (1958)

7 B. Shen, T. Sekiguchi, J. Jablonski and K. Sumino, "Gettering of copper by bulk stacking faults and punched-out dislocations in Czochralski-grown silicon", *J. Appl. Phys.*, **76**, 4540 (1994)

8 S. A. McHugo and W. D. Sawyer, "Impurity Decoration of Defects in Float Zone and Polycrystalline Silicon via Chemo-Mechanical Polishing", Appl. Phys. Lett., 62 (20), 2519-2521, (1993)

Thermal and Microstructural Modelling for Cast Silicon

D. Franke, I. Steinbach
ACCESS e.V., Intzestr. 5, 52072 Aachen, Germany

W. Krumbe, J. Liebermann, W. Koch
Bayer AG, Rheinuferstr. 7-9, 47825 Krefeld, Germany

H.J. Möller
TU Bergakademie Freiberg, Silbermannstr. 1, 09596 Freiberg, Germany

Abstract

The SOPLIN (SOlidification by PLanar INterface) casting process of silicon ingots for photovoltaic applications at the Bayer AG, Germany, is supported by numerical modelling. Thermal modelling with the "Virtual Casting Furnace" (VCF) is used to optimize the process control of the casting furnace in view of the solidification velocity, the planarity of the solid-liquid interface and a low stress cooling stage. Microscopic modelling is used to gain further insight into material quality cryteria and their dependence on process parameters. Microscopic models cover aspects of dislocation generation, segregation of foreign elements and the grain structure of the multicrystalline material.

Introduction

To optimize the process control and the material quality of directional solidified multicrystalline silicon, numerical modelling is applied. Examples are given for a strategy to find a low dislocation cooling program in silicon casting. Furthermore a calculated segregation profile of boron on its dependence to the solidification velocity is shown. As third example for the use of numerical modelling in process optimisation, calculated grain selection in facetted grown silicon is presented.

Thermal modelling

Basic software for the thermal simulations is the finite element package CASTS [1], that is designed for the simulation of technical casting processes in radiative heated furnaces. The VCF-computer model [2] additionally consists of a special user interface for the ingot casting process and post processing tools to visualize the temperature distribution, temperature gradients and the solidification velocity. Calculations for the SOPLIN casting process were made with a mesh of 40.000 finite elements, including 20 different materials. The figure 1 shows a temperature distribution on a cross section of the casting furnace. The dark line indicates the position of the solidification front. Light colours show high - and dark colours low temperature.

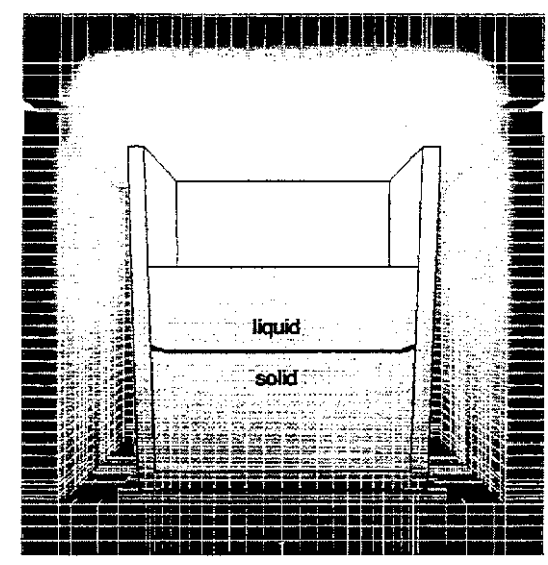


Fig. 1: Calculated temperature field in a cross section of the casting furnace

Low dislocation cooling

Dislocations in the bulk material of solar silicon may limit the carrier lifetime and reduce the solar cell efficiency. Therefor the control of dislocation multiplication, during the cooling stage, is one of the major tasks of silicon ingot casting for photovoltaic applications.
The principles of dislocation motion and - multiplication in semiconductors are well described by the Haasen model [3]. Inhomogenious temperatures during the cooling stage of silicon casting causes thermal stress in the material. In interaction with inhomogeneities in the material, this stress is acting as driving force for dislocation multiplication. On the other hand, dislocations relax stress by plastic deformation [4]. Both effects are taken into account in a numerical model to describe the dislocation generation rate and its dependence on the temperature, the applied stress and the time. Output of a calculation run is a "dislocation map",as shown in figure 2 in principle. These dislocation maps show the predicted dislocation density, beeing generated for a limited time and under constant temperature and stress conditions. At a given location in the silicon block, series of dislocation maps, at different time limit, show the time dependence of the dislocation multiplication. An evalution of the dislocation maps allows to find process conditions that lead to dislocation densities lower than empirical achievable values.

Calculation of segregation

Segregation of dopands and impurities in silicon occures at the solid-liquid interface, depending on the solidification velocity. The difference in solubility of the foreign atoms in solid and liquid silicon leads to a pile up of impurity concentration in the melt, - for boron, phosphorus and metallic impurities, with a segregation coefficient lower than one -, or to a depletion of foreign atoms in the melt - for oxygen and carbon, with a segregation coefficient larger than one. This pile up or depletion respectively is in balance with chemical diffusion and the convective transport in the melt.
The segregation problem is treated in 1-D approximation for the diffusional boundary layer in front of the solid-liquid interface, using the model of I.J. Favier [5]. The solidification velocity, deduced from the FE-Simulation of the process, is taken as input for the calculation of segregation. Figure 3 shows a sample of the solidification velocity versus position of solidification front. Figure 4 shows the corresponding calculted segregation profile of boron for the SOPLIN process. After the sharp initial transient at the bottom of the ingot, the boron concentration varies slightly around the mean boron concentration c_0, resulting in an almost constant value in the silicon material over the ingot hight.

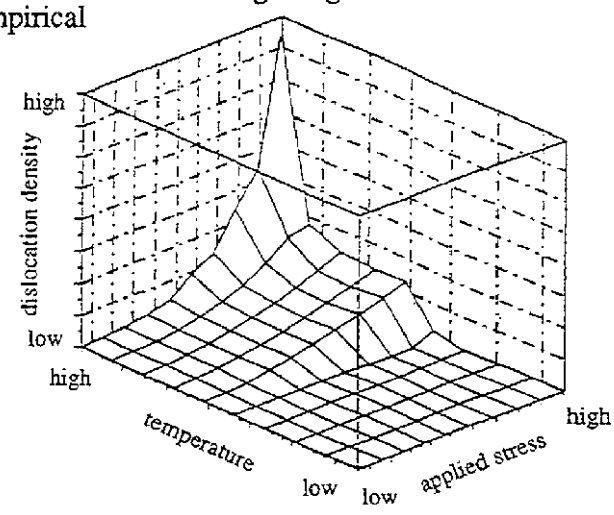


Fig. 2: Scheme of a dislocation map. In a dislocation map the value of generated dislocations are shown on its dependence on the temperature and applied stress for a fixed time limit.

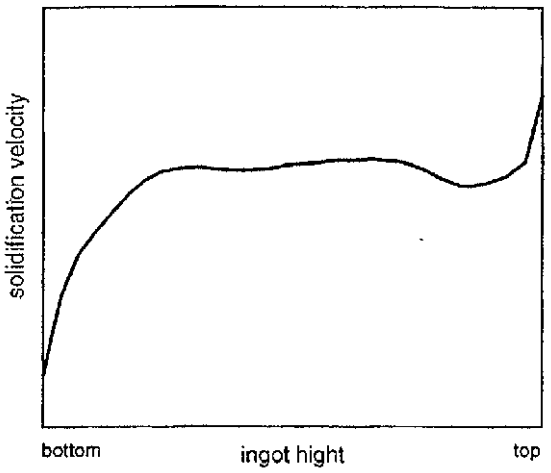


Fig. 3: Sample of a calculated solidification velocity versus the ingot hight

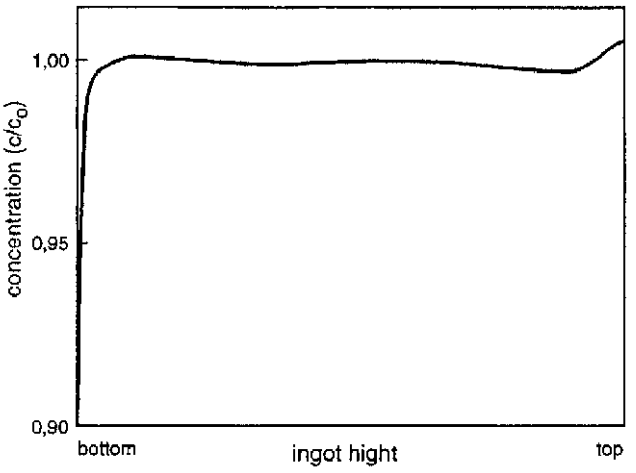


Fig. 4: Corresponding to fig. 3 calculated segregation profile of boron.

Calculation of grain structure

One of the quality criteria for high efficient solar cells, made from multicrystalline silicon wafers, is the grain shape. Numerical modelling is applied in order to study the selection behaviour of silicon crystals and to predict the size of the grains on their dependence from the process conditions. For the numerical simulation a phase field model is used [6] to describe the cristallographic orientation and their influence on the growth velocity. The model distinguishes between the [111] and [001] low index planes of the silicon crystal. The individual grains are nucleated at the bottom of the mould with a prescribed nucleation density and a random orientation. The figure 5 shows a 3-D calculation of an array of silicon crystals at three time steps. A two dimensional calculation of grain selection, starting from 100 grains, is shown in figure 6.

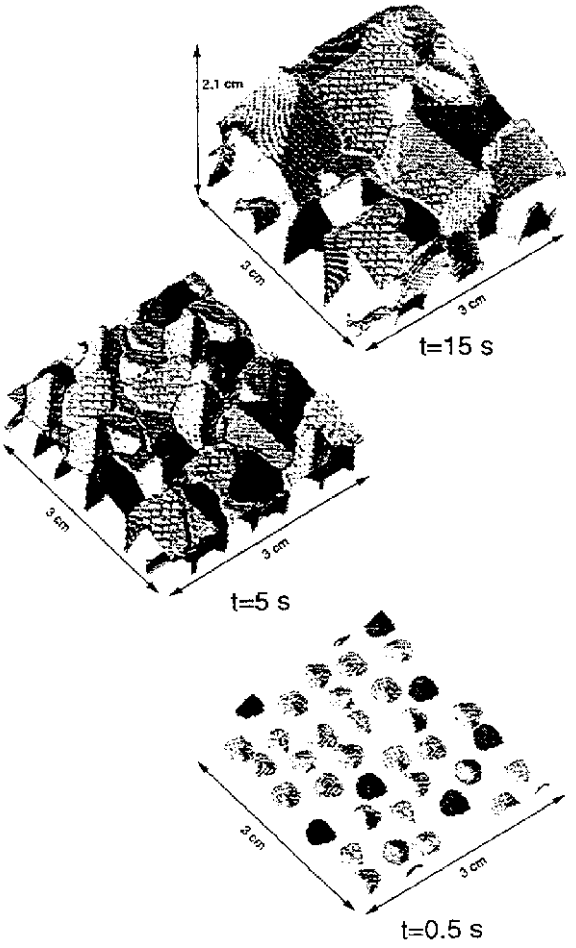


Fig. 5: 3-D calculation of the grain selection in multicrystalline silicon casting.

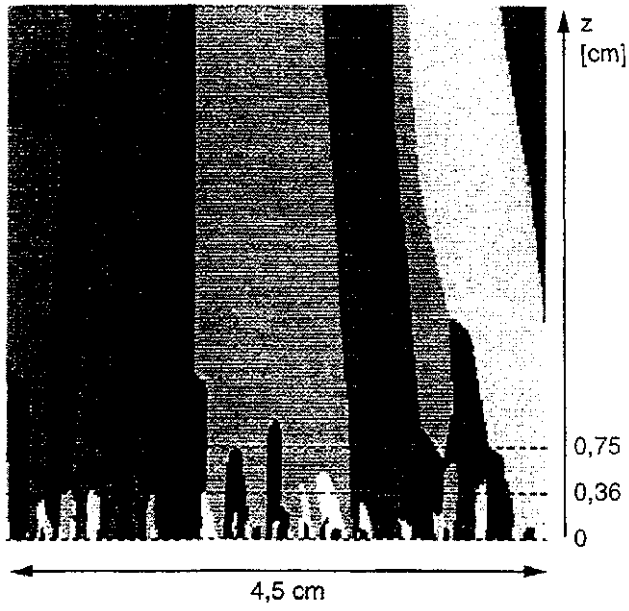


Fig. 6: 2-D grain selection in facetted grown silicon

Conclusion

Numerical modelling has proven to be a powerful optimization tool for the SOPLIN casting process. Thermal modelling with the VCF shows the influence of the process control on the casting conditions. Dislocation maps are calculated to find process conditons for a low dislocation cooling. Microscopic modelling of segregation profiles and grain structures allows to optimize the material quality by computer calculations.

Acknowledgment

This work was carried out with financial support of the Federal Ministry of Education, Science, Research and Technology (BMBF) under the Grant Number 0329305D.

References

[1] F. Hediger, N. Hofmann
Process Simulation for Directional Solidified Turbine Blades of Complex Shape. Proc. 5th International Conference on Modelling and Casting 1990, Davos, Switzerland, P. 611-619

[2] I. Steinbach, et.al.
A Virtual Crystallization Furnace for Solar Silicon. Proc. 1th World Conference on Photovoltaic Energy Conversion 1994, Wailoloa, Hawaii, P. 1270 - 1273

[3] H. Alexander, P. Haasen
Dislocation and plastic flow in the diamond structure. Solid state physics, 1968, 22, P. 27 - 157

[4] J. Völkl, G. Müller
A New Model for the Calculation of Dislocation Formation in Semiconductor Melt Growth by Taking into Account the Dynamics of Plastic Deformation. Journal of Crystal Growth, 1987, 97, P. 136 - 145

[5] I.J. Favier
Macrosegregation I & II, Acta Met, 1981, 29, P. 197

[6] I. Steinbach, et.al.
Grain Selection in Faceted Crystal Growth using the Phase Field Theroy. Proc. Modelling of Casting, Welding and Advanced Solidification Processes VII 1995, London, England, P. 695 - 703

Long-time stability of quenched-in self-interstitials available for impurity-defect kinetics in $5d^n$ - doped silicon crystals

M. Höhne , U. Juda , and O. Scheerer

Institut für Kristallzüchtung
im Forschungsverbund Berlin
Rudower Chaussee 6 , D-12489 Berlin , Germany

Abstract

Results of electron paramagnetic resonance (EPR) measurements in mostly platinum doped silicon crystals are presented. Although self-interstitials are not detected directly in our experiments, three phenomena strongly suggest the stable existence of quenched-in self-interstitials. All these phenomena are observed in samples prepared in such a way that one expects a high supersaturation with self-interstitials trapped anywhere in the lattice. First, the hyperfine structure of shallow donors indicates the existence of neighbouring defects. Second, several paramagnetic complex defects are formed by annealing the samples subsequently between 450 and 540° C. Third a Fermi-level shift, monitored by the EPR of Pt^- and a shallow oxygen-related Pt defect, proves the formation of more than 10^{16} cm^{-3} acceptor-like mid-gap defects.

1. Introduction

Level positions and capture cross sections of complex defects containing an impurity metal may differ essentially from those of the isolated metal defect. Doping of silicon with platinum effectively shortens the lifetime of free carriers. For decades the isolated substitutional Pt defect (Pt_s) was believed to be the dominant lifetime limiter. Its level positions [(-/0) with E_c - 0.243 eV, (0/+) with E_v + 0.330 eV, (+/++) with E_v + 0.067 eV] [1,2] and electronic structure [3-5] are well known.

Since 1986 a midgap level with E_c - 0.051 eV in Si:Pt was investigated and shown to exhibit a recombination activity stronger than that of Pt_s [6-9]. The structure of the corresponding defect is unknown up to now. Several complex platinum defects were detected and investigated by electron paramagnetic resonance (EPR) [10-18]. Although the samples were rapidly quenched after doping with Pt in order to achieve defect concentrations sufficient for an EPR detection, low concentrations of those defects are expected to arise at cooling rates in usual processing procedures.

Some of the defects are related to oxygen, present in Czochralski (Cz) Si, one contains hydrogen, introduced by different procedures. We will give reasons in this contribution for the assumption that some of the paramagnetic defects are formed with participation of quenched-in self-interstitials. Another self-interstial related defect (SIRD) causes a near-midgap (-/0) level.

Silicon self-interstitials are highly mobile even at 4K, at least in electron-irradiated

p-type Si. They are trapped at several defects, like aluminum or boron [19]. Surface reactions with oxygen or with metals [20-22] introduce an excess of self-interstitials. This excess can be quenched in to a large extent, which was shown in Si:Au by the detection of stacking faults after annealing subsequently near 800 to 900° C [22].

2. Sample preparation with or without a strong supersaturation of self-interstitials

Self-interstitials are created in the silicon-lattice if the formation of oxide or silicides requires an excess of volume. Such a process is expected also in samples (3x3x8 mm^3) during the doping with Pt at 1200° C from a metallic layer covering the surface. Platinum diffuses into the bulk by a kick-out mechanism [20] and finally occupies substitutional lattice sites. Thus, at least $1x10^{17}$ cm^{-3} self-interstitials are created, corresponding to the solubility of platinum. Samples treated in this way are expected to contain a concentration of self-interstitials strongly exceeding the concentration of thermal equilibrium.

In a second treatment the surface of such samples was cleaned. The reaction layer was mechanically removed; and furthermore a 50 μm thick layer was removed by etching. The samples where then heated once more to 1200° C and annealed for one or two hours. Samples treated in this way are assumed to contain intrinsic defects only corresponding to thermal equilibrium.

As will be shown in Sec. 3 , the two types of samples behave essentially different after quenching. This difference exists homogeneously in the bulk and it is stable for at least more than a year. Obviously, it is possible to quench in defects, which are assumed to be self-interstitials following the arguments mentioned above. There is a supersaturation with self-interstitials in both types of quenched samples; but that in the samples doped from a covered surface is remarkably higher.

3. Self-interstitial related phenomena

3.1 Local stress at shallow donors

The EPR spectrum of dilute phosphorus donors consists of two symmetrical hyperfine lines in a distance of 4.2mT [23]. In samples strongly supersaturated with self-interstitials these hyperfine components are asymmetrical. By choosing suitable saturation conditions the asymmetry is resolved into a substructure as demonstrated in Fig.1. The phenomenon can be explained by reminding to two previous results. Uniaxial stress applied to the sample diminishes the hyperfine splitting and shortens the spin-lattice relaxation time [23]. In SiGe alloy crystals with a low content of Ge a similar phenomenon was detected. It was interpreted by the admixture of excited states into the shallow donor

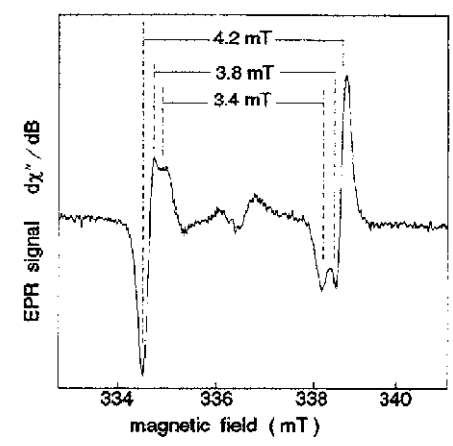


Fig. 1: EPR spectrum of P in samples supersaturated with selfinterstitials

ground state caused by the stress due to Ge atoms in the vicinity of the P donors [24]. The existence of point defects near to a part of the P donors is strongly suggested in samples assumed being supersaturated with self-interstitials. This exlanation is supported by the preliminary results that the same phenomenen is produced in samples doped with gold instead of platinum and that a similar anisotropy is observed also in the line shapes of arsenic donors instead of phosphorus.

3.2 Formation of complex defects

Three types of very stable trigonal 6-Pt clusters were detected by EPR [12,15-17]. They are formed within several hours or days between 450°C and 540°C up to concentrations of 1/3 of the isolated Pt content. It turned out that even two years after quenching from 1200°C to room temperature the formation rate and the final concentrations of these clusters strongly differ in the two types of samples characterized in Sec.2. The same is true for one of the complex 2-Pt defects [17]. Therefore, we conclude that self-interstitials, stored anywhere in the lattice, are available for defect kinetics.

3.3 Formation of acceptor-like defects

Another defect is also formed in silicion strongly supersaturated with self-interstitials. The annealing near 540°C can be done also in this case after long storage at room temperature. These self-interstitial related defects (SIRD) are not directly detected by EPR, but their existence in a concentration of more than 10^{16} cm^{-3} is unavoidably concluded from a Fermi-level shift. Fig. 2 shows some levels involved in the processes discussed here. In n-type Si with $1x10^{16}$ P/cm^3 saturated with Pt the Fermi level is locked to the Pt(-/0) level (FL 1 in Fig.2). Consequently about $1x10^{16}$ cm^{-3} of Pt_s is in its negative charge state, which is detected by EPR. After the formation of the SIRDs the EPR signal of the Pt_s defects is detected only under illumination. That means, these defects lost their electrons to a lower acceptor-like defect. The position of this acceptor-like level was recently determined from photo-EPR experiments [18] . The EPR signal of a thoroughly analyzed oxygen-related 1-Pt defect (Or-1-Pt) is detected when empty. The Or-1-Pt level was shown to be above the B(-/0) level, but near to the valence band (VB). In p-type starting material doped with Pt the Fermi-level is locked at the Pt(0/+) level (FL 2 in Fig.2). Illumination with suitable infrared light causes the capture of holes at the Or-1-Pt defects and thus their EPR activity, if the photon energy is sufficient for exciting electrons to a level in the gap. In this way, the position of the SIRD level was determined to be in the range E_v+(0.4 ... 0.5) eV .

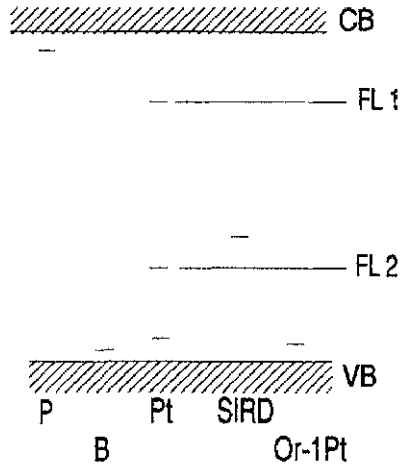


Fig. 2: Levels of defects involved in the processes of the Fermi-level shift caused by formation of SIRDs.

4. Conclusions

Quenched-in self-interstitials in silicon crystals are stable at room temperature for a time of more than a year. In view of the high mobility of isolated self-interstitials demonstrated by previous EPR investigations of silicon irradiated with high-energy electrons, one must conclude that the self-interstitials in $5d^n$ doped silicon are trapped anywhere in the lattice. Shallow donors are such traps, which might explain the lower mobility of self-interstitials in irradiated n-type Si compared with p-type Si [19]. The activity of different traps might be responsible for the widespread range of diffusivity data above 500°C for self-interstitials [20], partly compatible with an extrapolated long-time stability at room temperature.

The concentration of self-interstitials is strongly enlarged by doping with $5d^n$ impurities from a metallic layer covering the surface.

The quenched-in self-interstitials are available for defect kinetics at temperatures up to 540°C. Several complex defects are formed in concentrations comparable with the total content of isolated Pt atoms. These complex defects may change device properties. Especially a near-midgap defect is formed, which converts Si:P,Pt samples from n-type to p-type.

References

[1] H. Lemke, Phys. Status Solidi **A 101**, 193 (1987).
[2] H. Zimmermann and H. Ryssel, Appl. Phys.Lett. **58**, 499 (1990).
[3] C.A.J. Ammerlaan and A.B. van Oosten, Physica Scripta **T25**, 342 (1989).
[4] F.G.Anderson, R.F.Milligan, G.D.Watkins, Phys.Rev. **B 45**, 3279 (1992).
[5] F.G. Anderson, F.S. Ham, and G.D. Watkins, Phys. Rev. **B 45**, 3287 (1992)
[6] W. Stoffler and J. Weber, Phys. Rev. **B 33**, 8892 (1986).
[7] Y.K. Kwon, T. Ishikawa T., and H. Kuwano, J.Appl.Phys. **61**, 1055 (1987).
[8] H.Lemke, Phys. Status Solidi **A 101**,193 (1987).
[9] A.A. Gill, N. Baber, and M.Z. Iqbal, J.Appl.Phys. **67**, 1130 (1990).
[10] H.J.v.Bardeleben, D.Stiévenard, M.Brousseau, J.Barrau, Phys.Rev.**B 38**,6308 (1988).
[11] M. Höhne, Phys.Rev. **B 45**, 5883, (1992).
[12] M. Höhne and U. Juda , J. Appl. Phys. **72**, 3095 (1992).
[13] P.M.Williams, G.D.Watkins, S.Uftring, M.Stavola, Phys.Rev.Letters **70**, 3816 (1993).
[14] M.Höhne, U.Juda, Yu.V.Martynov, T.Gregorkiewicz, C.A.J.Ammerlaan, L.S. Vlasenko, Materials Science Forum **143-147**, 1659 (1993).
[15] M. Höhne and U. Juda, Solid State Phenomena **32-33**, 207 (1993).
[16] M. Höhne and U. Juda, Materials Science and Technology **11**, 680-683 (1995) .
[17] U. Juda and M. Höhne, Solid State Phenomena **47-48**, 293 (1996).
[18] U. Juda and M. Höhne, to be published in J.Appl.Phys. **80**, No.5 (1996).
[19] G.D.Watkins in *Materials Science and Technology*, ed. by R.W.Cahn, P.Haasen, E.J. Kramer (VCH,Weinheim,1991), Vol. 4 ,vol.editor W. Schröter, p.105.
[20] U.M. Gösele und T.Y. Tan , ibid. p.197.
[21] S.M. Hu, Materials Science and Engineering **R 13**, 105 (1994).
[22] F.H. Baumann and W. Schröter, Phys. Rev. **B 43**, 6510 (1991).
[23] D.K. Wilson and G. Feher, Phys. Rev. **124**, 1068 (1961).
[24] A.A. Bugai, V.M. Maksimenko, E.I. Neimark, B.D. Shanina, V.G. Graczev, V.I. Shachovzov, Fizika Tverdogo Tela **26**, 3338 (1984).

Selective Solid Phase Crystallization with Controlled Grain Size and Location in Ge Thin Films on Silicon Dioxide

C.M. Yang and H.A. Atwater
Thomas J. Watson Laboratory of Applied Physics, California Institute of Technology
Pasadena, CA 91125.

Selective solid phase crystallization is an approach for fabrication of thin polycrystalline Ge and Si films on amorphous substrates with potentially very large grain sizes and controlled grain boundary locations. Achievement of very large grain sizes in thin Ge and Si films on amorphous insulating substrates is of interest to future low-cost thin-film electronic device technologies such as displays and thin-film polycrystalline solar cells. Particularly important for low-cost thin-film solar cell applications is the use of low-cost substrates, such as glass. Since grain size enhancement and film growth must be accomplished at temperatures below the softening point of the glass substrate, solid phase crystallization methods are of particular interest. While approaches that employ film melting and solidification can lead to large grain size [1], the high temperatures required are most likely incompatible with low-cost substrates. In this paper, we describe results of selective solid phase crystallization for producing large grained (20 μm) polycrystalline Ge films at low temperatures ($<$ 500 °C), which is the first step in a process for fabrication of low-cost polycrystalline GaAs solar cell on glass substrates. For GaAs thin-film cells, achievement of large grain sizes is a concern as grain boundaries act as traps for minority carriers that lower cell efficiency [2]. Since GaAs is lattice matched to Ge, a Ge film with large grain size could be used to seed epitaxial growth of a GaAs overlayer to fabricate solar cells with large GaAs grain size [3].

The approach to selective solid phase crystallization taken here is based on a thin-film reaction between a deposited metal layer and an amorphous semiconductor film. This reaction causes selective nucleation to occur at a much earlier time than random homogeneous nucleation. Thus crystals which are selectively nucleated can grow to very large sizes via lateral solid phase epitaxy before their growth is impeded by impingement with randomly nucleated crystal grains.

It has been shown that cerain metals which form low-temperature eutectic phases or binary ordered compounds with crystalline Si or Ge can induce crystal nucleation in amorphous Si or Ge at temperatures much lower than those required for homogeneous nucleation. For Si, reductions in the crystallization temperature have been observed for reactions with Al, Ag, Au, Ni, and Sn [4]–[7]. Similarly, many metals (most notably Al, Ag, Au, Cu, and Sn) have been shown to induce Ge crystal nucleation at substantially reduced temperatures [6, 8, 9]. The temperature for crystallization of amorphous Ge is lowered substantially (by up to 200 °C) as a result of reaction between amorphous Ge and various metals such as Cu, Au, Al, and Sn [6]. A change of apparent activation energy for nucleation and growth was reported from 2.0 eV for pure amorphous Ge to 0.9 eV for amorphous Ge in contact with Al or Cu [9]. Co-deposited Au-Ge alloys also crystallize at temperature below that for pure amorphous Ge, and the Au-Ge coordination in the alloys suggest that enhanced crys-

tallization is associated with first formation of a maximum number of Au-Ge bonds and that nucleation is followed by Au segregation at the amorphous-crystal interface, leaving a low concentration of Au behind in the crystal Ge, and fcc Au particles in the fully crystallized Ge film.

In the present work, amorphous Ge films either 20 or 50 nm thick were deposited by ultrahigh vacuum electron beam evaporation (base pressure 7×10^{-11} Torr; pressure during deposition typically 4–8 $\times 10^{-9}$ Torr) at 100 °C onto cleaned, thermally grown SiO_2 films on Si substrates. A patterned metal film was deposited in another high vacuum evaporator by mechanically masked lithography on top of the amorphous Ge film, with 5-μm-diameter metal islands spaced in periodic arrays of periods 20–100 μm. The metals used included Au, Cu, In, Co, and Ni with thicknesses ranging from 10 to 20 nm. These films as well as films of pure amorphous Ge were annealed in a high vacuum furnace at temperatures ranging from 225 to 475 °C.

For 50-nm-thick pure amorphous Ge films, an incubation time before crystallization was observed, with crystal fraction $\chi = 0$ at $T = 475$ °C after 5 min, $\chi = 0.05$ after 20 min, and $\chi = 1$ after 40 min, where crystal fractions were measured from bright-field and dark-field transmission electron micrographs. Isochronal anneals for 60 min yielded crystal fractions of $\chi = 0$ at $T = 425$ °C, $\chi = 0.05$ at $T = 450$ °C, and $\chi = 1$ at $T = 475$ °C. These data are broadly consistent with previous studies of Ge crystallization (e.g., Ref. 9; we note that the films here were deposited under ultrahigh vacuum conditions, while the films described in Ref. 9 were deposited under ordinary high vacuum conditions, and no measureable differences in the Ge crystallization kinetics were found in these different experiments, suggesting that either significant levels of impurities are not incorporated into amorphous Ge or that their presence does not significantly affect crystallization.)

Selective nucleation was found to occure for reactions between amorphous Ge and In, Cu, Au, Co, and Ni at 225 °C after 20 min, which is approximately 250 °C below the temperature at which crystallization of pure amorphous Ge occurs on a similar time scale. For reasons of convenience in subsequent film growth and device processing, In was selected as the metal of choice for all further studies. It was found that selective nucleation resulted in not one but many grains per 5-μm-diameter metal island. The grain density was found to be highest near the edges of metal islands where metal island thickness was smaller, possibly due to penumbral shadowing during mechanically masked deposition. Since crystal grains at the edge of the metal islands act as seeds for lateral solid phase epitaxial growth, the microstructure after lateral solid phase epitaxy consists of many large elongated grains rather than a single large grain growing radially from under each metal island. This microstructure is illustrated in Fig. 1, which is a brigh-field transmission electron micrograph of selective nucleation and growth of Ge grains in a 50-nm-thick amorphous Ge film on SiO_2 following a two-step vacuum anneal of $T = 350$ °C for 20 min to induce selective nucleation, and a $T = 425$ °C anneal for 2 hr to induce lateral solid phase epitaxy. It was found that anneals at higher temperatures for shorter times that produced the same overall crystallized fraction as the 425 °C anneals (e.g., 450 °C for 50 min or 475 °C for 10 min) resulted in a greater extent of random nucleation relative to selective nucleation.

Some amorphous Ge films were doped by ion implanation with electronically active dopants, such as B and P prior to seletive solid phase crystallization. Doping with B and P up to concentration of 0.6 at. % had no observable effect on the rate of random nucleation, as

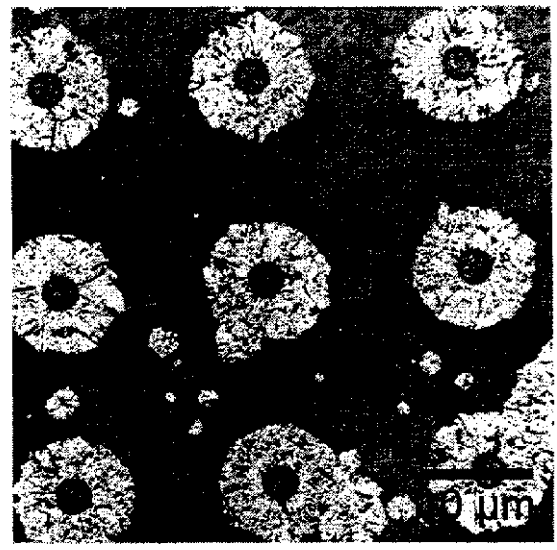
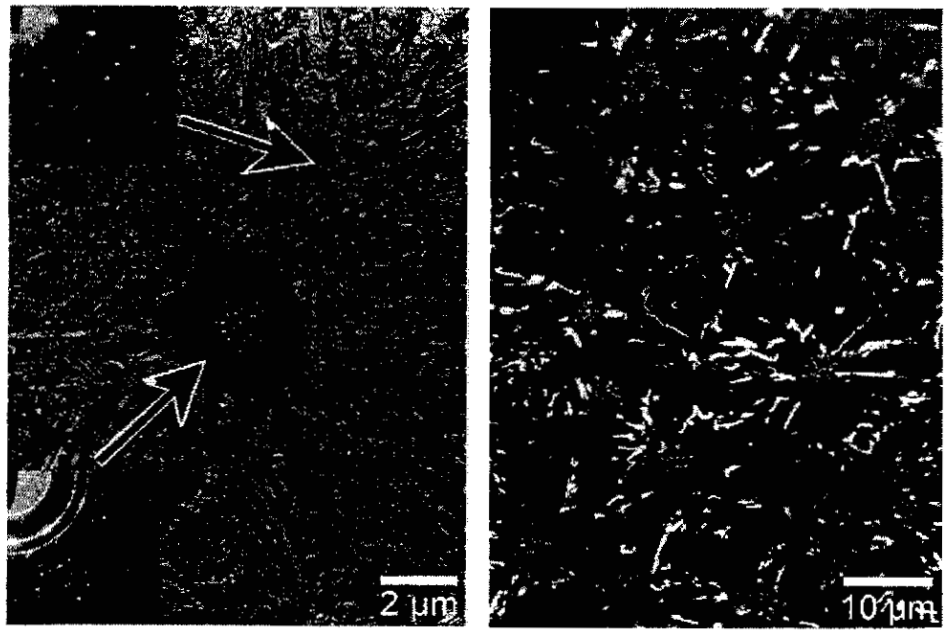


Figure 1: Bright-field transmission electron micrograph illustrating selective nucleation and growth of Ge grains in a 50-nm-thick amorphous Ge film on SiO_2, during a two-step vacuum anneal of $T = 350$ °C for 20 min to induce selective nucleation, followed by a $T = 425$ °C anneal for 2 hr to induce lateral solid phase epitaxy.

compared with undoped films. However B and P doping resulted in significant lateral solid phase epitaxial growth rate enhancements: a factor of 2 times for 50 nm Ge films doped with 0.6 at. % B and 5 times for 50 nm Ge films doped with 0.6 at. % P in the temperature range from 400 to 475 °C. Figure 2 illustrates the microstructure of crystallized Ge films doped with 0.6 at. % P. Figure 2(a) is a bright-field transmission electron micrograph near an In nucleation site for selective nucleation and growth in a 50-nm-thick P-doped amorphous Ge film on SiO_2 after a two-step vacuum anneal of $T = 350$ °C for 20 min followed by $T = 450$ °C for 50 min. The selected-area diffraction patterns indicate very small grain sizes in the nucleation site region and large grains outside of the nucleation site region. In Fig. 2(b), a lower magnification transmission electron micrograph of the fully crystallized film indicates Ge grain sizes as large as 20–30 μm, which were limited in size by the spacing between nucleation sites.

In summary, selective solid phase crystallization has been shown to lead to grain sizes as large as 20–30 μm in 50-nm-thick Ge films at temperatures less than 475 °C, for a grain-size-to-film-thickness aspect ratio of 600:1. Selective nucleation by metal alloy reaction does not at present lead to growth of a single grain per nucleation site, and achievement of this goal will be a subject of future investigation, as will be heteroepitaxial growth of GaAs films on polycrystalline Ge films. Nonetheless, the results indicate that selective solid phase crystallization is a simple process for achievement of large grain sizes that is compatible with the use of low-cost substrates.

This work was supported by the National Renewable Energy Laboratory.



(a) (b)

Figure 2: In (a) bright-field transmission electron micrograph of nucleation site for selective nucleation and growth in a 50-nm-thick P-doped amorphous Ge film on SiO_2 after a two-step vacuum anneal of $T = 350$ °C for 20 min followed by $T = 450$ °C for 50 min. Selected area diffraction patterns indicate very small grain size in the nucleation site region and large grains outside of the nucleation site region. In (b), a lower magnification transmission electron micrograph of the fully crystallized film with grain sizes as large as 20 μm.

References

[1] Y. Ohmachi, T. Nishioka and Y. Shinoda, Appl. Phys. Lett. **43** 971 (1983).

[2] M. Yamaguchi and Y. Itoh, J. Appl. Phys. **60**, 413 (1986).

[3] S. Choi, K. Bachmann, M. Timmons, T. Colpitts, and J. Posthill, J. Electrochem. Soc. **139** 312 (1992); J. Chen, M. Ristow, J. Cubbage, and J. Werthen, J. Electronic Mater. **21** 347 (1992).

[4] J. Bosnell and U. Voisey, Thin Solid Films **6** 161 (1969).

[5] C. Hayzelden, J. Batsone, and R. Cammarta, Appl. Phys. Lett. **60** 255 (1992).

[6] D. Smith, C. Grovenor, P. Batson, and C. Wong, Ultramicroscopy **14**, 131 (1984).

[7] Z. Tan, S. Heald, M. Rapposch, E. Bouldin, and J. Woicik, Phys. Rev.B **46**, 9505 (1992).

[8] F. Oki, Y. Ogawa, and Y. Fujiki, Jpn. J. Appl. Phys. **8**, 1056 (1969).

[9] F. Edelman, Y. Komem, M. Bendayan, and R. Beserman, J. Appl. Phys. **72**, 5153 (1992).

Selective Nucleation and Solid Phase Epitaxy Process For Si Thin Film Photovoltaics

Claudine M. Chen and Harry A. Atwater
Thomas J. Watson Laboratories of Applied Physics
California Institute of Technology
Pasadena, CA 91125

INTRODUCTION

For Si photovoltaics to be broadly competitive with presently available commercial sources of energy, the cost per watt must be reduced. The most promising strategy is to use a lower quality but low-cost device material, like polycrystalline silicon (poly-Si) thin film, as well as an inexpensive substrate. In order to take advantage of present low cost glass substrates, processing temperatures are limited to 600 °C or lower. This requirement is likely to exclude crystallization techniques based on melting and solidification such as zone-melting recrystallization. Solidification processes have achieved grain sizes of mm to cm lengths, but such grain sizes have not been demonstrated with solid phase crystallization. In this paper we assess the potential for a new process, selective nucleation and solid phase epitaxy (SNSPE) to produce large-grained polycrystalline silicon thin films from amorphous silicon (a-Si) at low process temperatures. This approach has recently been demonstrated as a means to generate large (20 - 50 um) grain size in Ge/SiO_2 thin films[1]. Use of a similar selective nucleation and solid phase epitaxy for Si may enable grain sizes greatly exceeding those which result from conventional solid phase crystallization by taking advantage of the transient incubation time, t_{inc}, which is the time period between the start of an anneal and the onset of observable nucleation.

SELECTIVE NUCLEATION

The overall process for selective nucleation and solid phase epitaxy of Si is shown in Fig. 1. A thin film of a-Si is first crystallized by SNSPE. The crystallized film then forms a template upon which a thicker Si layer is grown, either via a vapor phase epitaxy process by CVD or sputtering, or by vertical solid phase epitaxy of deposited a-Si layer grown on the template. To maximize the extent of grain growth during the transient incubation time, crystals are nucleated at specified locations in a periodic array of the beginning of the anneal. Metal induced crystallization enable crystal nucleation at these specified sites without a transient incubation period [2].

Metal induced crystallization of a-Si has been shown to occur with an assortment of metals: Au, Ag, Al [3], In, Cu, Ni and Pd [4], all of which crystallize Si below 600 °C, which is the temperature at which random nucleation occurs in a-Si in a few hours. These metals can be grouped into two categories: (i) those that form simple eutectic phase diagrams with Si, with low eutectic temperatures (Au, Ag, Al, In), and (ii) those that form silicides (Cu, Ni, Pd). While complete understanding of the interface reactions that occur is not yet possible, plausible mechanisms have been advanced for growth (rather than nucleation) in which an alloy [4] or silicide [5] front can move through the c-Si, leaving c-Si in its path. For both eutectic and silicide forming metals, heterogeneous nucleation of c-Si can occur without an incubation period, so the mechanisms for nucleation and growth may be related. Another potential concern is the rate of heterogeneous nucleation at the a-Si film surface and the film/substrate interface, since the barrier

to crystal growth is usually smaller for heterogeneous nucleation. However, there is no apparent heterogeneous nucleation at either the Si/SiO_2 substrate interface or the Si surface covered by a native SiO_2 layer, which is fortuitous, since a-Si easily forms a native oxide [6] thus passivating the film with respect to heterogeneous nucleation.

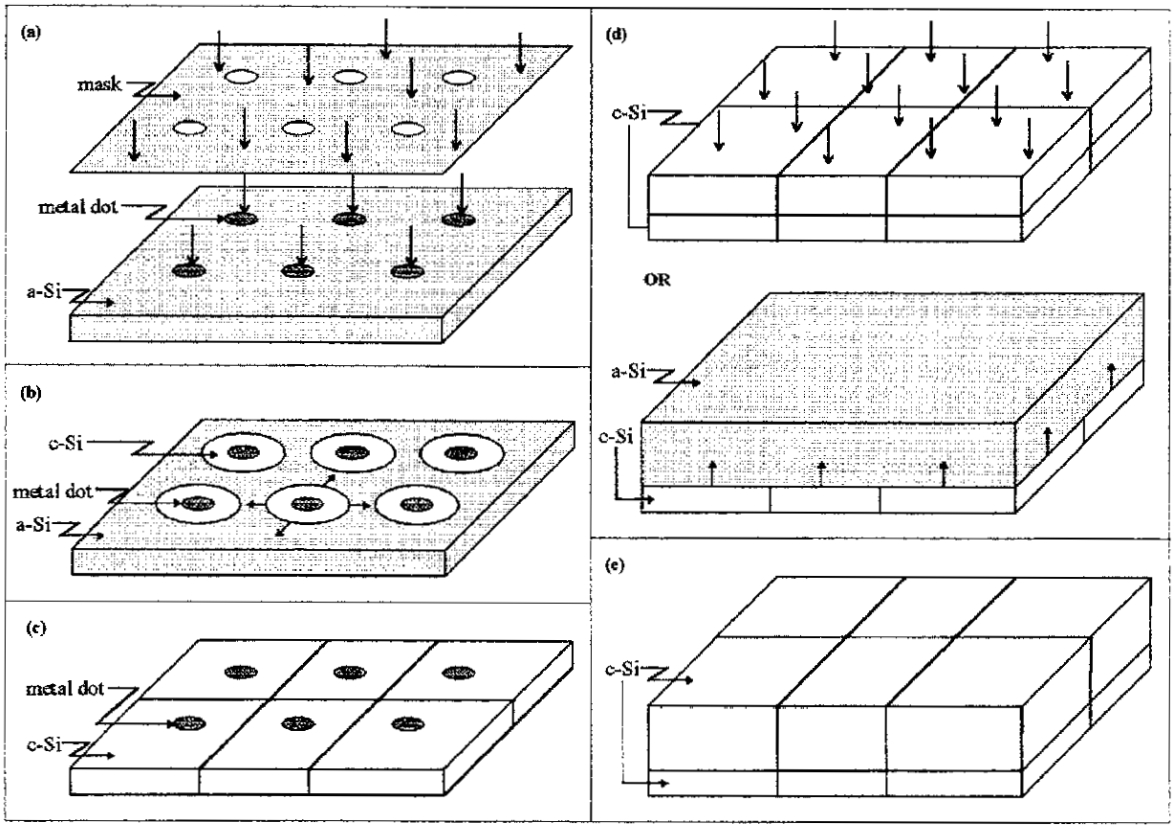


Figure 1: Procedure for fabricating large grain poly-Si: (a) metal is deposited through a mask to form patterned film on a-Si layer, (b) sample is annealed to nucleate and grow c-Si, (c) seeded grains impinge on each other, film is completely crystallized, (d) additional layer of a-Si is grown on the thin film seeded layer, either epitaxially by vapor deposition (CVD or sputtering), or by vertical SPE of an a-Si layer deposited on the template, and (e) sample is annealed to crystallize device layer.

GRAIN SIZE CONSIDERATIONS

An important criterion for an SNSPE process for growth of large-grained polycrystalline silicon is whether the maximum grain size that can be achieved is large enough to avoid a significant penalty in photocurrent loss in a thin film Si solar cell due to carrier recombination associated with grain boundaries. For conventional p^+n single junction cell designs with film thickness in the 10-100 μm range, grain sizes of 200 μm or greater are needed for efficiency greater than 10% [7]. Simulations of a single junction single crystal PERL cell [8] as a function of material quality indicate a decrease in efficiency from 24% to 7% as the minority carrier lifetime is reduced from 1 ms to 10 ns. However, a multilayer cell design [8], which greatly improves the performance of a poorer quality material, is calculated to have 15-18% efficiency for grain sizes 20-200 μm. It is noteworthy that solid phase crystallization can be performed after deposition of doped multilayers without degradation of the doping profile, thus implying compatibility of the SNSPE process with multilayer cell designs.

For our proposed procedure, the expected grain size can be very roughly estimated as the product of the transient incubation time, t_{inc}, and the solid phase epitaxial growth rate, v_{SPE}. Once random nucleation starts, further growth of the seeded crystals will be inhibited by impingement of randomly nucleated grains, thus limiting the grain size to that which is achievable before random nucleation occurs. The SPE rate of Si as an Arrhenius function of temperature (T) [6] is given by,

$$v_{SPE} = v_0 e^{-E_A/kT}, \text{ where } v_0 = 2.3 \times 10^8 \text{ cm/s and } E_A = 2.7 \text{ eV},$$

and the transient incubation time as an exponential function of T is given by [9],

$$t_{inc} = t_0 e^{E_A/kT}, \text{ where } t_0 = 1.12 \times 10^{-11} \text{ s and } E_A = 2.7 \text{ eV}.$$

The product of the exponential functions is approximately one, so the estimated maximum grain size of intrinsic (i.e., undoped) Si is 25 μm. For doped Si, the SPE rate is enhanced by 8 times for P to 66 times for Al [10], resulting in grain sizes of 200 μm (see Table 1).

Dopant	SPE Rate Enhancement	Grain size = $t_{inc} \times v_{SPE}$ (μm)
Undoped	1	25 μm
P (0.8 at. %)	8	200 μm
B (0.6 at. %)	40	1000 μm
Al (1.0 at. %)	66	1650 μm

Table 1: Estimated grain size for intrinsic and doped Si.

The ultimate grain size may be smaller, since different crystal orientations have different SPE rates, ranging from (111) which is the slowest, to (100) which is 25 times faster than (111) [10]. Also, the increase in solid phase epitaxy rate with doping is dependent on the dopant concentration, and the maximum dopant concentration is likely to be limited by its solid solubility in Si. If the concentration exceeds the solubility limit, then it is possible that the dopant may precipitate and form a heterogeneous nucleation site, which is undesirable.

EXPERIMENTAL RESULTS

Preliminary experiments have been performed to assess the use of selective nucleation for Si crystallization. For our experiments, deposited In was used to create seed regions that enable selective heterogeneous nucleation. In films 20 nm thick were deposited by thermal evaporation in a high vacuum evaporation chamber on 100 nm a-Si films, which were deposited by electron beam evaporation at low temperatures onto SiO_2 in ultrahigh vacuum. The In was evaporated through a mechanical mask in a grid pattern of 5 μm diameter circles with a periodic spacing of either 20 μm or 25 μm. The samples were then annealed at 450 °C for 20 minutes to induce selective nucleation of a-Si, and then at 575 °C for 16 hours, or 600 °C for 3.5 hours to enable lateral solid phase epitaxy. The sample that was annealed for 575 °C for 16 hours is shown below. The seeded grains are about 3 μm in diameter, which is much larger than the submicron sized crystals obtained from random nucleation. The discontinuous In film seeded several Si crystals per In circle, each with different orientation.

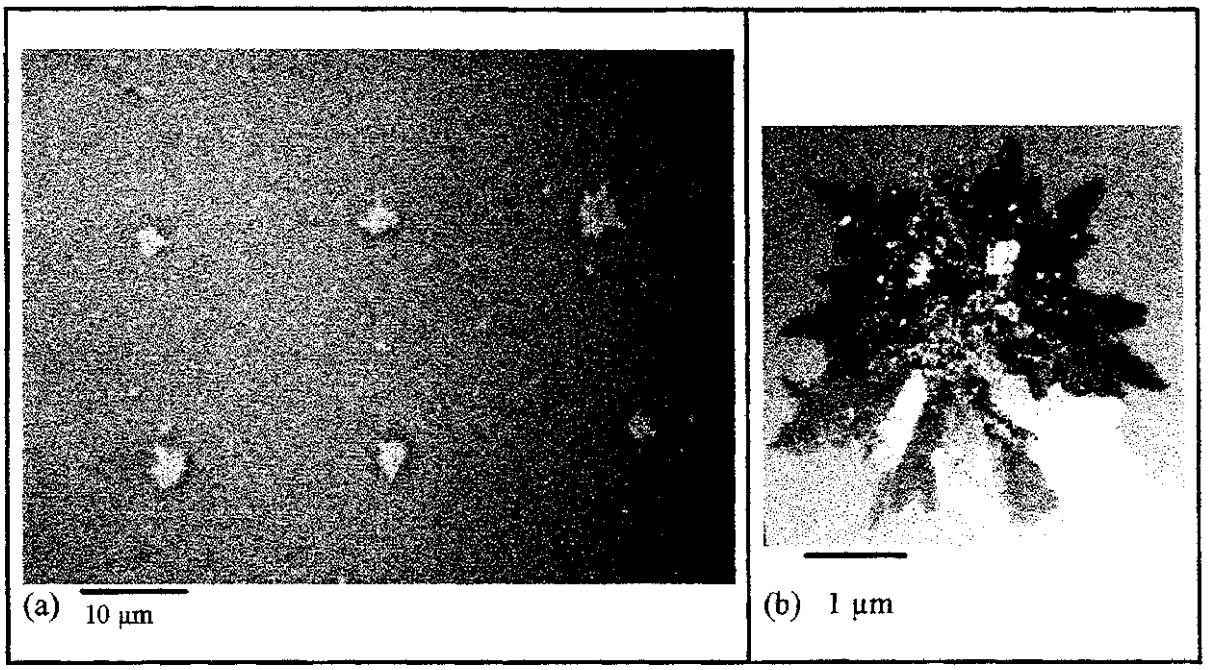


Figure 2: Images of a-Si/In samples after 450 °C/20 minutes, 575 °C/16 hours anneals: (a) Optical image of the controlled growth. Brighter areas correspond to c-Si. The six grains in the three-by-two grid formation, separated by 20 μm, were nucleated by In. The smaller specks are from random nucleation of the a-Si. (b) TEM plane-view DF image of an In seeded grain.

CONCLUSIONS

A process for low temperature solid phase growth of large-grained polycrystalline Si films on SiO_2 by selective nucleation and solid phase epitaxy has been outlined. A first experiment demonstration of selective nucleation of Si using In was described, and limited to the achievable grain size following lateral solid phase epitaxy in doped Si films have been estimated, and suggest that grain sizes of 25-2000 μm may be achieved through careful control of crystal nucleation.

REFERENCES

[1] C. M. Yang and H. A. Atwater, *Appl. Phys. Lett.* **68** (24) 1996, pp. 3392-3394.
[2] G. Radnoczi, A. Robertsson, H. T. G. Hentzell, S. F. Gong, and M.-A. Hasan, *J. Appl. Phys.* **69** (9) 1991, pp 6394-6399.
[3] T. J. Konno and R. Sinclair, *Mat. Sci. Eng.* A179/A180, 1994, pp. 426 432.
[4] S. W. Lee, Y. C. Jeon, and S. K. Joo, *Appl. Phys. Lett.* **66** (13) 1995, pp. 1671-1673, (and reference contained therein).
[5] C. Hayzelden, J. L. Batstone, and R. C. Cammarata, *Appl. Phys. Lett.* **60** (2) 1992, pp. 225-227.
[6] G. L. Olson and J. A. Roth, *Material Science Reports 3*, 1988.
[7] A. K. Ghosh, C. Fishman, and T. Feng, *J. Appl. Phys.* **51** (1) 1980, pp. 446-454.
[8] S. R. Wenham, M. A. Green, S. Edmiston, P. Campbell, L. Koschier, C. B. Honsberg, A. B. Sproul, D. Thorpe, Z. Shi, and G. Heiser, "Limits to the Efficiency of Silicon Multilayer Thin Film Solar Cells," Presented at the First World Conference on Photovoltaic Energy Conversion, 1994.
[9] R. B. Iverson and R. Reif, *J. Appl. Phys.* **62** (5) 1987, pp. 1675-1681.
[10] G. L. Olson and J. A. Roth, *Handbook of Crystal Growth 3*, edited by D. T. J. Hurle (Elsevier, Amsterdam, 1994), pp. 257-312.

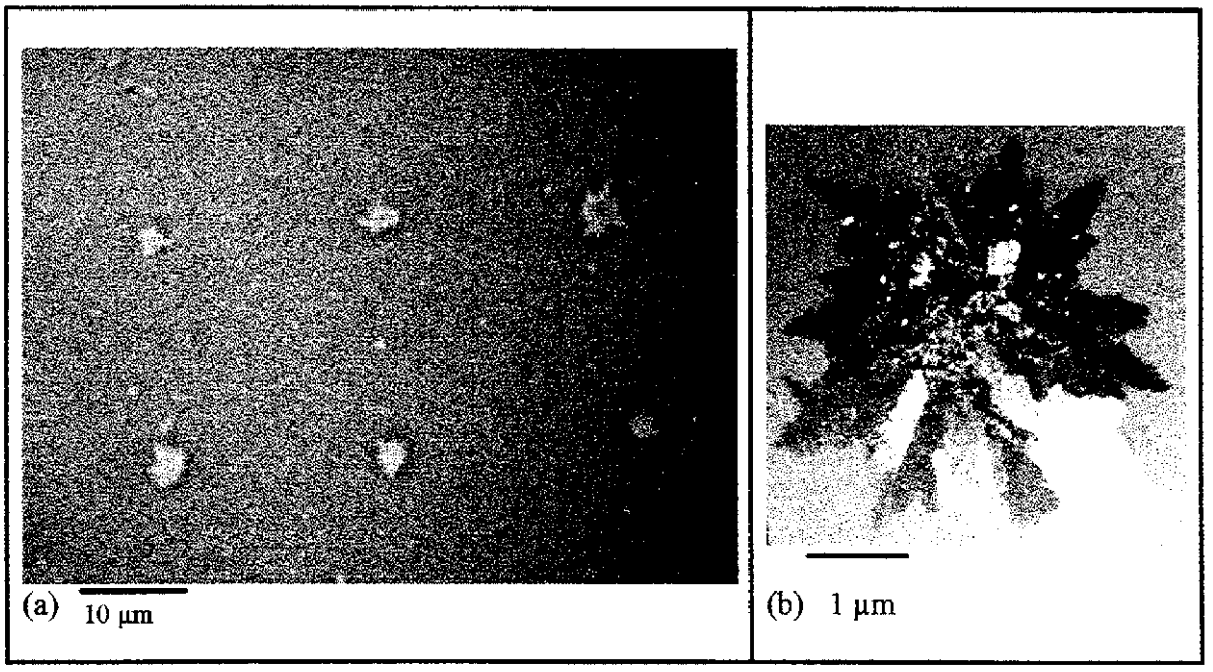


Figure 2: Images of a-Si/In samples after 450 °C/20 minutes, 575 °C/16 hours anneals: (a) Optical image of the controlled growth. Brighter areas correspond to c-Si. The six grains in the three-by-two grid formation, separated by 20 μm, were nucleated by In. The smaller specks are from random nucleation of the a-Si. (b) TEM plane-view DF image of an In seeded grain.

CONCLUSIONS

A process for low temperature solid phase growth of large-grained polycrystalline Si films on SiO_2 by selective nucleation and solid phase epitaxy has been outlined. A first experiment demonstration of selective nucleation of Si using In was described, and limited to the achievable grain size following lateral solid phase epitaxy in doped Si films have been estimated, and suggest that grain sizes of 25-2000 μm may be achieved through careful control of crystal nucleation.

REFERENCES

[1] C. M. Yang and H. A. Atwater, *Appl. Phys. Lett.* **68** (24) 1996, pp. 3392-3394.
[2] G. Radnoczi, A. Robertsson, H. T. G. Hentzell, S. F. Gong, and M.-A. Hasan, *J. Appl. Phys.* **69** (9) 1991, pp 6394-6399.
[3] T. J. Konno and R. Sinclair, *Mat. Sci. Eng.* A179/A180, 1994, pp. 426 432.
[4] S. W. Lee, Y. C. Jeon, and S. K. Joo, *Appl. Phys. Lett.* **66** (13) 1995, pp. 1671-1673, (and reference contained therein).
[5] C. Hayzelden, J. L. Batstone, and R. C. Cammarata, *Appl. Phys. Lett.* **60** (2) 1992, pp. 225-227.
[6] G. L. Olson and J. A. Roth, *Material Science Reports 3*, 1988.
[7] A. K. Ghosh, C. Fishman, and T. Feng, *J. Appl. Phys.* **51** (1) 1980, pp. 446-454.
[8] S. R. Wenham, M. A. Green, S. Edmiston, P. Campbell, L. Koschier, C. B. Honsberg, A. B. Sproul, D. Thorpe, Z. Shi, and G. Heiser, "Limits to the Efficiency of Silicon Multilayer Thin Film Solar Cells," Presented at the First World Conference on Photovoltaic Energy Conversion, 1994.
[9] R. B. Iverson and R. Reif, *J. Appl. Phys.* **62** (5) 1987, pp. 1675-1681.
[10] G. L. Olson and J. A. Roth, *Handbook of Crystal Growth 3*, edited by D. T. J. Hurle (Elsevier, Amsterdam, 1994), pp. 257-312.

Contactless Frequency Resolved Microwave Spectroscopy of the p-Si in the Presence of CarrierTrapping.

A. Romanowski, A. Karoui*, and G. Rozgonyi

North Carolina State University, Dep of Materials Sci.&Eng, Box 7916, Raleigh, NC 27695
*Institut National de Recherche Scientifique et Technique, Tunisa.

The contactless frequency resolved microwave technique has been used to evaluate p-type Si. It has been shown that in the case of a single recombination model (SRH model) both carrier lifetime and surface recombination velocity can be determined from the Lorentz peak (resonance frequency) position and from the spectrum width [1,2]. The more complex case which includes traps and recombination centers has also been considered. In this case, the Lorentzian profile is distorted [1], and we have used a two level recombination/trapping model to describe the spectra. To simplify the analysis the following assumptions have been used: (i) homogeneous distribution of the recombination and trapping centers, (ii) constant quasi-Fermi levels, (iii) constant surface recombination velocity. A linear approximation of the rate equation and the diffusion equation in the frequency domain yields a minority carrier lifetime described by the formula:

$$\tau_n^* = \tau_n \Theta, \quad \Theta = 1 + \frac{1}{\tau_T(\delta + i\omega)}$$

where $\delta = v_T \sigma_T (n_o + n_2)$, with $n_2 = N_V \exp[-(E_C - E_T)]$, n_o is the equilibrium minority carrier concentration, v_T the free carrier thermal velocity, σ_T the capture cross section of trapping electrons, τ_T the trapping relaxation time, E_T energy of the trapping centers, ω angular frequency, and τ_n the electron lifetime. We have used above formulas to simulate frequency spectra. It has been found that a two level recombination/trapping model accurately describes the measured data for long time thermally processed wafers. For example, the following parameters of a p-type CZ phosphorous diffusion gettering (PDG) wafer have been found with a recombination center: [FeB] = $9 \times 10^{11} cm^{-3}$, trapping center: E_T = 0.6eV, σ_T/σ_n = 0.005, $N_T = 5 \times 10^{11}$ cm^{-3}, and v_s = 1488 cm/s. The recombination level has been estimated from the relationship between resonance frequency and DC excitation level, the surface recombination velocity from the Lorentzian width, and traps have been fitted corresponding to the above formulas.

1. M. A. Lourenco and K. P. Homewood, Semicond. Sci. Technol. **8**, 1277(1993).
2. A. Romanowski, A. Buczkowski, N. Sukidi, and G.A. Rozgonyi, AIP Conference Proceedings **353**, 545(1995) Woodbury, New York.

IMPURITY SEGREGATION DURING EFG OF SILICON OCTAGONS

J. Cao, M. Prince and J. P. Kalejs
ASE Americas, Inc., 4 Suburban Park Drive, Billerica, MA 01821, USA

We report on a study of impurity segregation during Edge-defined Film-fed Growth (EFG) of polycrystalline silicon sheet material used for manufacture of solar cells. The data we report here involves growth runs which last up to several weeks in duration and produce between 100 and 300 m total length of crystals from a single graphite crucible. Melt replenishment takes place continuously during growth by a technique described elsewhere [1]. An individual crystal is in the form of hollow octagon tube, with eight 10-cm wide faces; the tube wall thickness averages 300 μm. A full-length tube is 4.6 m long. The quality of the material is monitored through study of impurities in crystal at ppb levels with Deep Level Transient Spectroscopy (DLTS), and through solar cell performance.

Figure 1 shows a plot of solar cell efficiency evolution during the growth of 36 tubes from a single crucible, where there is accidental contamination of the melt during the melt replenishment process. We see a declining trend in cell efficiency in the successive crystals grown. This decline persists throughout all 36 tubes, or over 165 m of crystal, in the run. A DLTS plot on the wafer from this run is shown in Fig. 2 which reveals the presence of CrB in the crystal with a concentration in excess of $1x10^{13}$ /cm^3. Cr is normally found bonded to boron near room temperature in its equilibrium state [2]. The DLTS analysis thus identifies CrB as the impurity complex contributing to quality limitations and the changes in its concentration are assumed responsible for the bulk diffusion length decline over the length of the growth run.

From published data [3], we estimate concentrations of transition metals that need to be present in order to produce the observed bulk material diffusion length decrease responsible for the solar cell efficiency decline seen in Fig. 1. Typically, concentrations of all transition metals must drop to below $2\text{-}4x10^{11}$/cm^3 if 14% efficiencies are to be achieved in hydrogen passivated material. Hydrogen does not effectively passivate transition metals. The high efficiency cells have maximum diffusion lengths which peak in the range of 300-500 μm. At the other end of the cell efficiency range in Fig. 1, typical bulk diffusion lengths have dropped to below 100 μm in material produced from the later tubes. This is demonstrated with the Infrared Photoconductivity (IRPC) maps and diffusion length histograms in Fig. 3 (a) and (b) for typical low and high efficiency solar cells, respectively. The dark dots in the IRPC map in Fig. 3 (b) result from the silver pads on the back surface of the cell which are not revealed on Fig. 3 (a) due to the low diffusion length. The decrease in diffusion length requires a concentration of about 10^{13}/cm^3 in the case of CrB pairs. Thus, we establish that the impurity increase that accounts for the decline in cell efficiency in Fig. 1 spans about two orders of magnitude.

Neither the effective segregation coefficient, k_e, nor the extent of stirring or back mixing of segregated interface impurities into the bulk melt are known for the current EFG growth configuration. Initial models [4] argued that the confining nature of the graphite die, capillary channel and the high EFG growth speeds promote $k_e = 1$ conditions. The EFG die design has

changed considerably since these early system configurations [5]. The EFG octagon die and capillary channel are much shorter and the meniscus volume has increased by a factor of more than ten with respect to the geometry represented in early analyses. This enhances the opportunity for mixing and reduction of k_e. We have not observed a variation in cell efficiency over the length of an octagon tube, which suggests that the normal segregated impurity interface transient is much greater than the time needed to grow a single octagon tube. In addition, in order to account for the cell efficiency decline in Fig.1, impurity concentrations in the crystal C_s must range from 10^{11} /cm^3 to 10^{13} /cm^3. The interface concentration C_I would then range from 10^{16} /cm^3 to 10^{18} /cm^3 if there were no mixing. At such high interface concentration, second phase formations would be expected [6].

Impurity transients with different degrees of mixing were analyzed with the help of a model. The impurity concentration in crystal at growth length x can be expressed as [7]

$$\frac{C_s(x)}{C_o} = 1 - (1 - k_e)\, e^{-k_e \frac{Ax}{V}}$$

Here C_o is the impurity concentration in the silicon feedstock being replenished into the melt, A ($A \approx 2.4$ cm^2) is the octagon cross section, and V is the effective mixing volume. Figure 4 shows the dependence of $C_s(x)$ on the tube length for the total length of about one tube with several effective mixing volumes V and effective segregation coefficients k_e. The values of V span the range from the meniscus volume to the crucible volume. Values at V = 10 cm^3, which are close to the case of no mixing, do not produce the experimental variation of impurity levels deduced on the basis of the observed solar cell efficiency variation. The curves predicted for V = 300 cm^3 and k_e between 10^{-3} and k_o appear to represent most closely the segregation observed in EFG octagon growth.

In conclusion, we have studied impurity segregation during EFG of polycrystalline silicon octagon tubes with continuous melt replenishment. We observed effects of impurity accumulation on crystal quality as the run progressed, and the accumulation was attributed to interface segregation. This impurity accumulation will require that only very pure starting materials are used if it is desired to maximize the growth length of high quality crystals. The purity of the starting feedstock and graphite crucible, and the crucible volume all are parameters influencing the growth length of high quality crystals

Growth takes place with k_e between 10^{-3} and k_o for transition metal impurities with k_o on the order of 10^{-5}. This is different from EFG systems which were analyzed previously, for which $k_e \sim 1$. This change is attributed to use of a new EFG die design which allows more convection to take place in the interface region during growth.

[1] D.S. Harvey, J. Crystal Growth 104 (1989) 88.
[2] S.H. Park, D.K. Schroder and J. P. Kalejs, Twenty-second IEEE PVSC (1991) 964.
[3] J. Kalejs, L. Jastrzebski, L. Lagowski, W. Henley, D. Schielein, S. G. Balster and D.K. Shroder, Twelfth EC PVSEC&E (1994) 52.
[4] J.P. Kalejs, J. Crystal Growth 44 (1978) 329.
[5] U. S. Patent Nos. 5,037,622 and 5,102,494.
[6] J.P. Kalejs, B. Bathey and C. Dube, J. Crystal Growth 109 (1991) 174.
[7] J. Cao, M. Prince, and J.P. Kalejs, to be published in J. Crystal Growth.

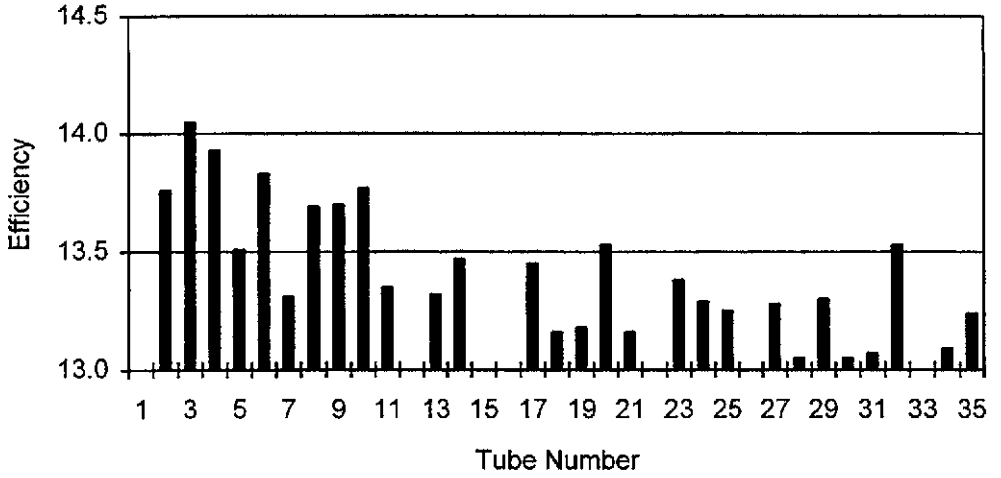


Figure 1. Plot of solar cell efficiency vs. octagon tube number for crucible impurity change during a growth run where Cr was introduced during melt replenishment.

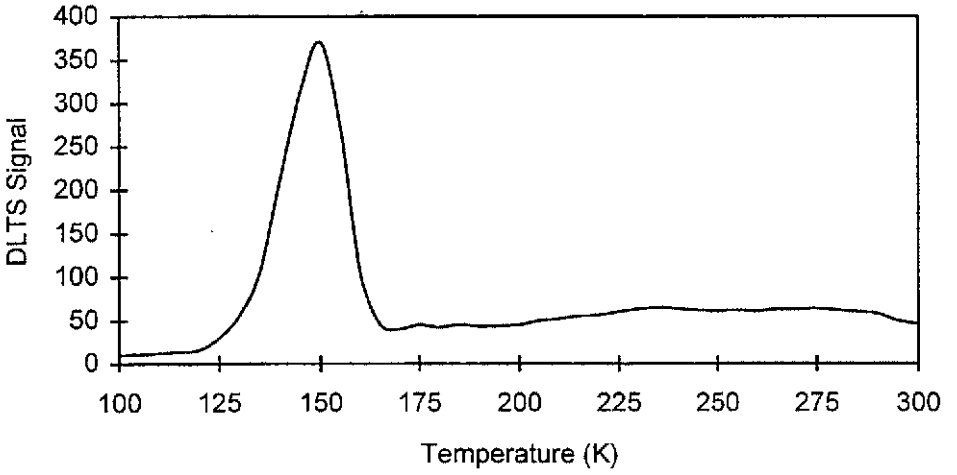
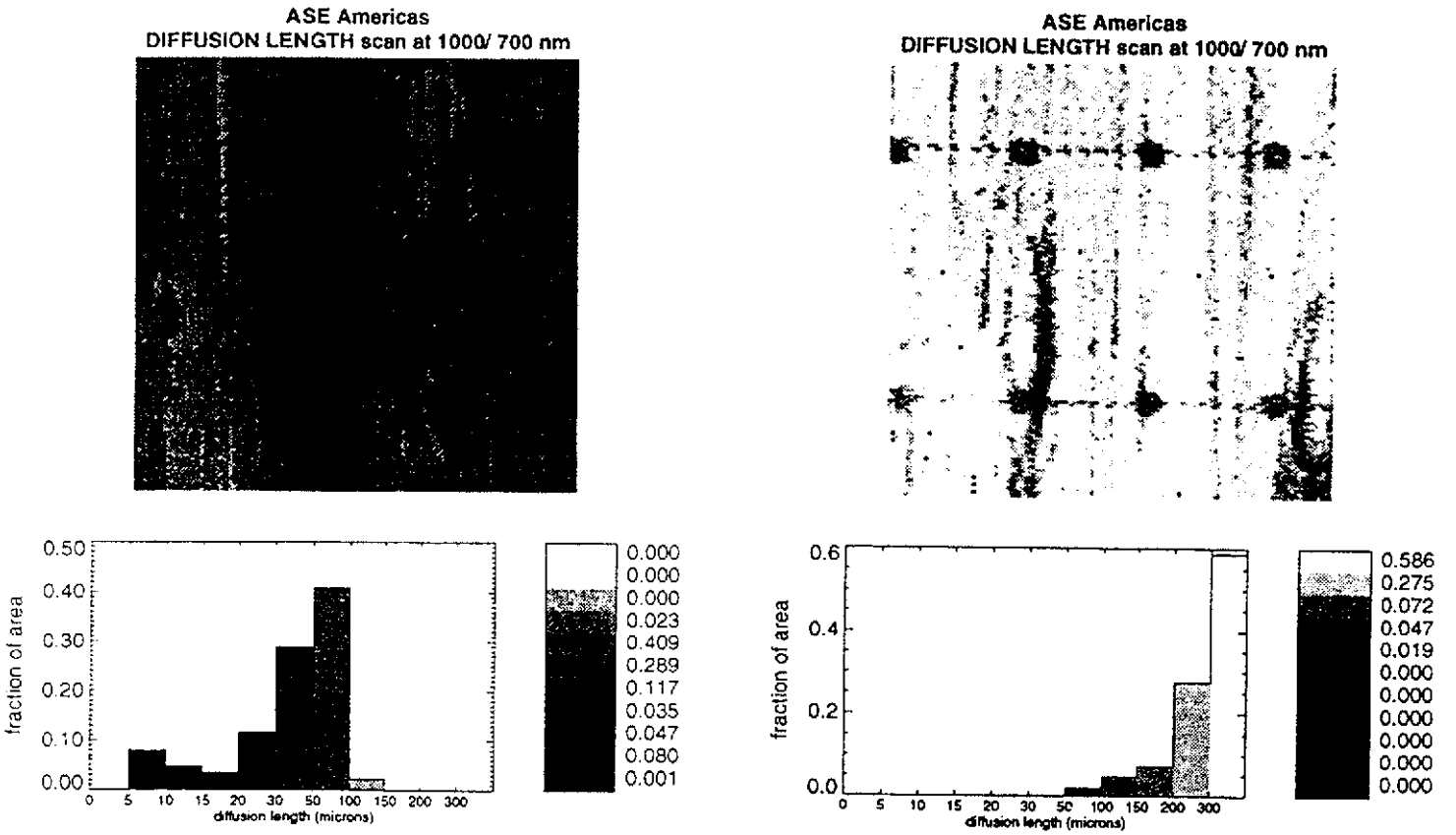


Figure 2. DLTS spectrum in arbitrary units showing peak for CrB pair in EFG wafers.



(a) (b)

Figure 3. IRPC map of minority carrier diffusion length for (a). low efficiency cell, and (b). high efficiency cell.

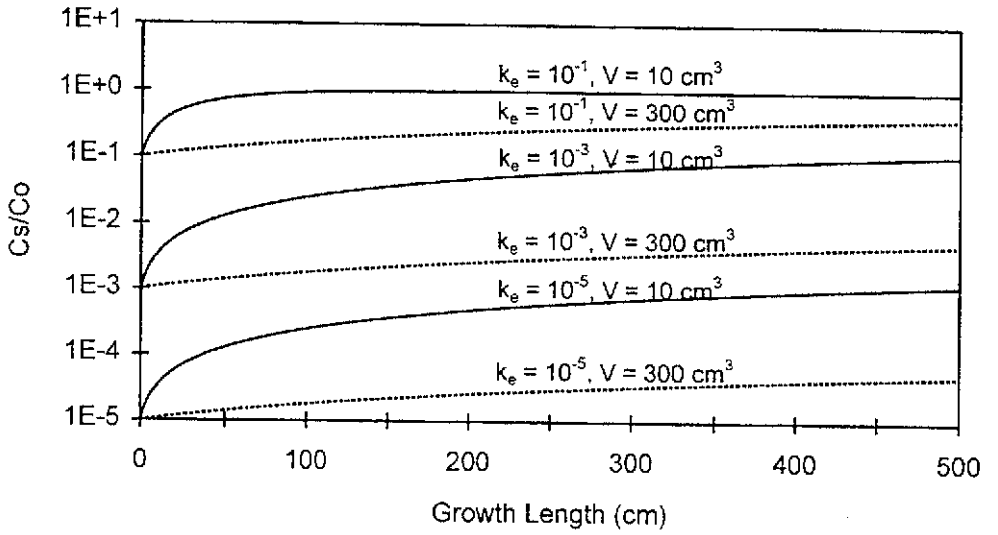


Figure 4. Plot of C_s/C_o in a single tube for three different effective segregation coefficients k_e and two extreme values of mixing volume: V=10 cm^3 and V=300 cm^3.

EMISSIVITY MEASUREMENTS OF SILICON RELATED MATERIALS AND STRUCTURES - APPLICATIONS TO RAPID THERMAL PROCESSING

N.M. Ravindra, F.M. Tong, W. Chen, S. Abedrabbo and W. Schmidt
New Jersey Institute of Technology, Newark, NJ 07102
A. Nanda, T. Speranza and A. M. Tello
SEMATECH, Austin, TX 78741
S. Narayanan
Solarex (A Business Unit of Amoco/Enron Solar), Frederick, MD 21703

Abstract -- Experimental results of the high temperature optical properties of (a) single crystal Czochralski -, (b) polycrystalline -, and (c) ion - implanted - silicon are reported in this study. The measurements have been performed using a spectral emissometer, operating in the wavelength range of 1-20μm and temperature range of 300 to 2000K. These measurements lead to evaluation of sample emittance and temperature. Diffusion in poly-Si is seen to exhibit increased emissivities. The results of the emissivity of arsenic implanted silicon samples show increase in emissivity with temperature.

I. INTRODUCTION

Rapid Thermal Processing (RTP) is currently used in silicon device manufacturing for processes such as post-implant anneal for dopant activation, junction formation and silicidation[1]. Its applications to processes such as Rapid Thermal Oxidation (RTO) have been hampered by limitations of wafer-to-wafer and across the wafer temperature uniformity and control. With the current trend in increasing silicon wafer diameters and shrinking device size, the ability to measure, monitor and control temperature uniformity, spatially and temporally, has become a challenging issue. For RTP, pyrometers are the standard sensors for non-contact temperature measurement and control. These sensors are designed to operate at one or more wavelengths. A fundamental knowledge of emissivity and its variation with wavelength and temperature is critical to the reliable operation of the pyrometer.

II. EMISSIVITY FUNDAMENTALS

Emissivity is an important parameter in radiation thermometry. It is defined as the ratio of the radiance of a given object to that of a blackbody at the same temperature and for the same spectral and directional conditions. It is a function of wavelength and temperature. It is a property which must be known for accurate temperature determination of an object by measurement of its emitted electromagnetic radiation with a radiation thermometer. For normal incidence, the emissivity $\varepsilon(\lambda)$ of a plane parallel specimen is given by:

$$\varepsilon(\lambda) = [1-R(\lambda)]\,[1-T(\lambda)] \,/\, [1-R(\lambda)T(\lambda)] \qquad (1)$$

where, λ is the wavelength, $R(\lambda)$is the true reflectivity and $T(\lambda)$ is the true transmissivity. $R(\lambda)$and $T(\lambda)$ are related to the fundamental optical parameters -- $n(\lambda)$, the refractive index and $k(\lambda)$, the extinction coefficient by the following relations:

$$R(\lambda) = [\{n(\lambda)-1\}^2 + k(\lambda)^2] / [\{n(\lambda)+1\}^2 + k(\lambda)^2] \quad (2)$$

$$T(\lambda) = \exp[-\alpha(\lambda)t] = \exp[-4\pi k(\lambda)t / \lambda] \quad (3)$$

α is the absorption coefficient and t is the thickness of the material. Thus, from equation (1), for a perfect opaque body, since $T(\lambda) = 0$, Kirchoff's law follows as:

$$\varepsilon(\lambda) = [1-R(\lambda)] \quad (4)$$

The experimentally measured values of transmittance and reflectance include effects such as light trapping and multiple internal reflections depending on the angle of incidence, surface roughness, presence of grains, grain-boundaries, interface roughness, etc. These apparent transmittance $T(\lambda)^*$ and apparent reflectance $R(\lambda)^*$ are related to real or true transmittance $T(\lambda)$ and true reflectance $R(\lambda)$, respectively, by the following well known equations[2] :

$$T(\lambda)^* = T(\lambda) \frac{(1 - R(\lambda))^2}{(1 - R(\lambda)^2 T(\lambda)^2)} \quad (5)$$

$$R(\lambda)^* = R(\lambda)\left\{1 + \frac{T(\lambda)^2 (1 - R(\lambda))^2}{1 - R(\lambda)^2 T(\lambda)^2}\right\} \quad (6)$$

The above equations (5) and (6) are the result of considering multiple internal reflections. A simultaneous measurement of reflectance and transmittance can yield true values of reflectance and transmittance and therefore, the refractive index, $n(\lambda)$ and the extinction coefficient, $k(\lambda)$ of single substrate materials. With choice of appropriate models, $n(\lambda)$ and $k(\lambda)$ of multi-layers can also be resolved from experimentally measured spectral properties. Our calculations of true reflectance and true transmittance for single crystal doped silicon have shown minimal disagreement with measured values[3]. Such calculations on Cz- and poly- Si have shown large differences between the corresponding sets of values.

III. EXPERIMENTAL DETAILS

The details of the spectral emissometer, acquired from On-Line Technologies, have been described in recent publications [3, 4] . It consists of a hemi-ellipsoidal mirror providing two foci, one for the exciting source in the form of a diffuse radiating near-blackbody source and the other for the sample under investigation. A microprocessor controlled motorized chopper facilitates in simultaneous measurement of sample spectral properties such as radiance, reflectance and transmittance. A high resolution Bomem FTIR, consisting of Ge and HgCdTe detectors, interfaced with a Pentium PC, permits data acquisition

of the measured optical properties.

IV. RESULTS AND DISCUSSION

The results of the measurements of the wavelength dependent optical properties of Cz- and poly- Si are presented in Fig.1(a) - 1(c). As can be seen in Fig. 1(a), the Cz-Si is characterized by a high T and R that is typical of intrinsic Si. Its low ε is comparable to that of intrinsic Si as reported by Sato[3]. Similar measurements have been performed on mechanically textured poly-Si, before and after diffusion. These results have been shown in Fig. 1(b) and 1(c). Comparisons of results in Fig. 1(b) and 1(c) show enhanced ε in poly-Si upon diffusion with decreases in R and T. The poly-Si exhibits ε similar to that of Cz-Si before diffusion as seen in Fig. 1(a) and 1(b). It is very likely that, indeed, the spectral emissometry technique can be utilized to estimate diffusion/doping activation in poly-Si.

In Figs. 2 and 3, the results of the emissivity spectra as function of temperature are presented for arsenic implanted samples. The silicon wafers considered in this study are -- p- type, of orientation <100>, thickness t = 650- 700 microns, resistivity ρ = 8-24 Ω·cm. The observed sharp features in the infrared spectra in the wavelength range of 1 μm (10000 cm^{-1}) to 20 μm (500 cm^{-1}) are due to the presence of the following infrared sensitive molecules: (a) C in Si -- 607 cm^{-1} (b) SiO_2 -- 1110 cm^{-1} (c) interstitial oxygen in Si -- 1130 cm^{-1}, (d) water -- 1600, 3500 cm^{-1}, (e) CO_2 -- 2400 cm^{-1}. The narrow-band features below 1000 cm^{-1} (10 μm) are due to lattice vibrations in silicon[5].

In Fig.2(a), $\varepsilon(\lambda)$ of arsenic implanted p-Si wafers are compared under three particular conditions -- #12 - As^+ implanted, furnace annealed and oxide etched; #16 - As^+ implanted and furnace annealed and #20 - 10nm SiO_2 and As^+ implanted. As can be seen in Fig.2(a), the emissivity of arsenic implanted samples are close to each other regardless of the presence of the cap. The as-implanted sample exhibits slightly lower emissivity than the annealed samples. However, the difference in emissivities is not significant enough. This is also the case for the presence or the absence of the SiO_2 cap. In order to illustrate the effects of implant on emissivity, for a given dose and energy (in this case, 10^{16} /cm^2, 25 KeV As^+), a comparison between the front-side and back-side emissivity of implanted Si wafer are plotted as function of wavelength for both sides of the wafer at almost similar temperatures. Again, no significant difference is observed.

In Figs. 3(a) and 3(b), temperature dependent emissivity spectra are plotted for sample #12. As can be seen in the figure, as temperature increases, emissivity increases. However, at 956 °C, the sample surface exhibits physical changes in color. A repeat measurement on this sample at T = 488°C showed irreversible changes in emissivity indicating a possible change in the chemical composition. Such chemical changes are anticipated at high temperatures. However, the pattern in emissivity-wavelength behavior remains similar to the spectra evaluated at 479°C.

CONCLUSIONS

Results of the reflectance and transmittance of Cz- Si, poly-Si and ion-implanted Si, measured using a spectral emissometer, have been presented in the above study. The experimentally measured optical

properties have led to evaluations of emissivity. These studies have been performed in the wavelength range of 1 to 20 microns. The emissivity results of Cz-Si and poly-Si are seen to be comparable to those of intrinsic silicon. These samples exhibited high reflectance and transmittance. Diffusion in poly-Si leads to decreased reflectance and transmittance and a significant increase in emittance. Ion-implanted silicon does not show any considerable change in emissivity. The effect of the SiO_2 cap on changes in emissivity is seen to be minimal. Emissivity increases with temperature for As^+ implanted samples.

ACKNOWLEDGMENTS

This work was supported partially by grants from SEMATECH contract No. 360220900, the U.S. Air Force Wright Laboratory and the ARPA Microelectronics Technology Office under contract F33615-92-C-5817, ARPA (TRP) contract DAAH04-94-C-0041, and ARPA contract DAAH04-95-1-0056 awarded through the U.S. Army Research Office, Research Triangle Park, N.C.

REFERENCES

[1] R. P. Kramer, in Proc. 3rd International Rapid Thermal Processing Conference, Edited by R.B.Fair, B. Lojek, Amsterdarm, Netherlands, RTP'95, 3 (1995).

[2] K. Sato, Japanese Journal of Applied Physics, 6, 339, (1967).

[3] N. M. Ravindra, F. M. Tong, S. Abedrabbo, W. Chen W. Schmidt, A. Nanda, T. Speranza and A. M. Tello, in Proc. 4th International Rapid Thermal Processing Conference, Edited by R.B.Fair and B. Lojek, Boise, Idaho, RTP'96 (1996).

[4] N.M.Ravindra, W. Chen, F.M.Tong and Arun Nanda, in Transient Thermal Processing Techniques in Electronic Materials, edited by N.M. Ravindra and R.K. Singh, TMS - The Minerals, Metals, Materials Society, Warrendale, PA, 159 - 164 (1996).

[5] J.R. Ferraro and K. Krishnan, Editors, Practical Fourier Transform Infrared Spectroscopy, Academic Press, Orlando, (1990).

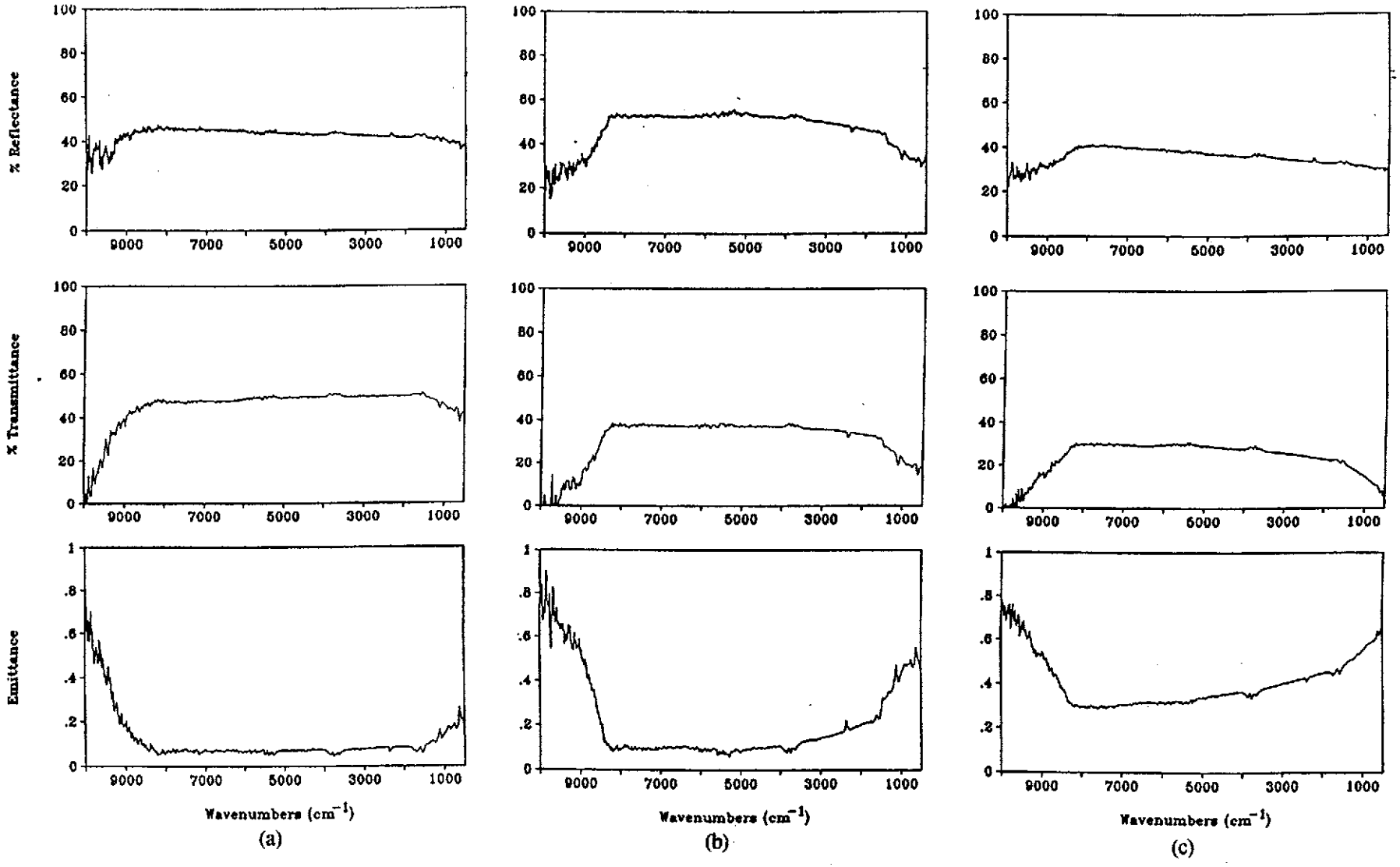


Fig. 1. Measured reflectance, transmittance and emittance of (a) Czochralski single crystal silicon, backside at (132°C), (b) mechanically textured polysilicon at (96°C), and (c) diffused polysilicon at (96°C).

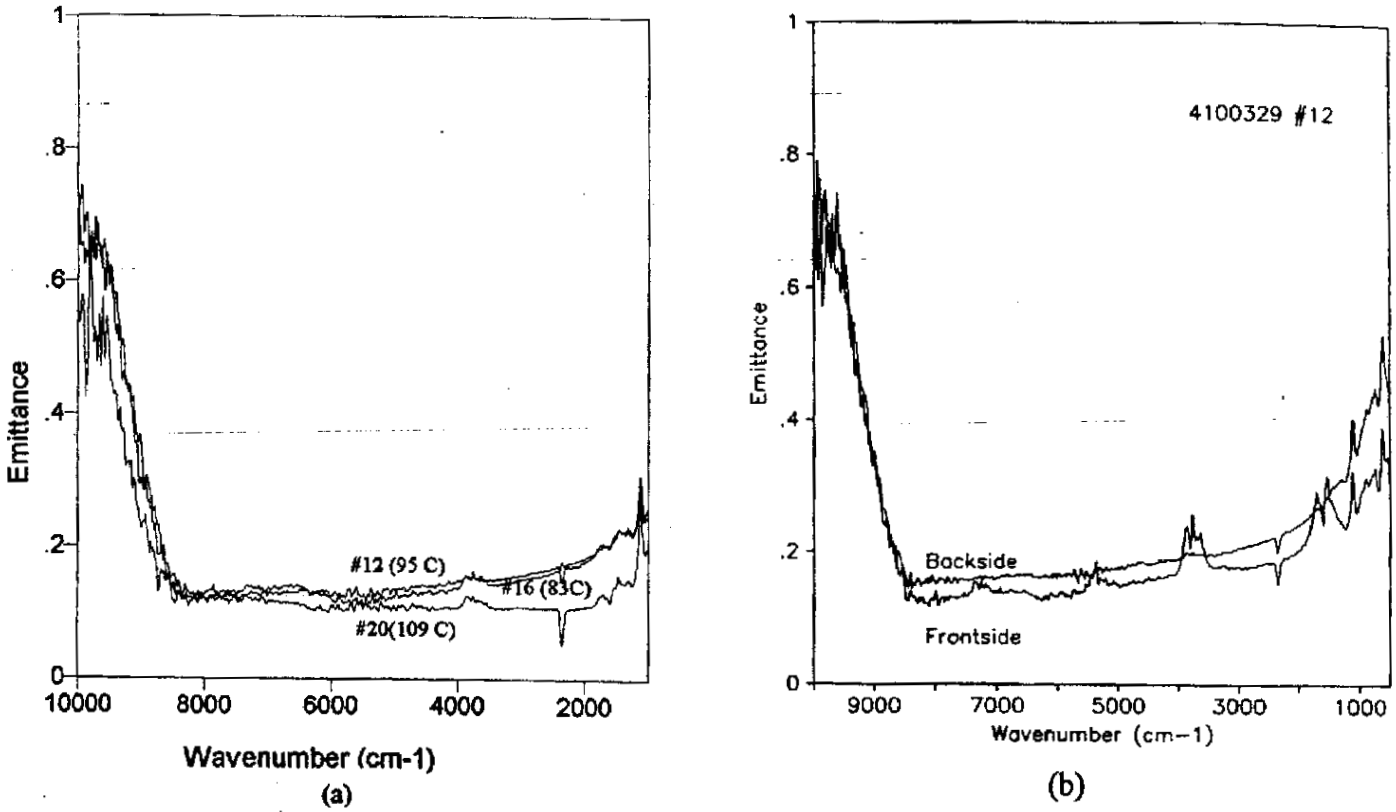


Fig.2. (a)Comparison of emissivity of As^+ implanted furnace annealed samples (with SiO_2 #16 and without SiO_2 #12 on top) and As^+ implanted unannealed sample #20. (b) Emissivity of frontside (95°C) versus backside (69°C) of As^+ implanted annealed samples.

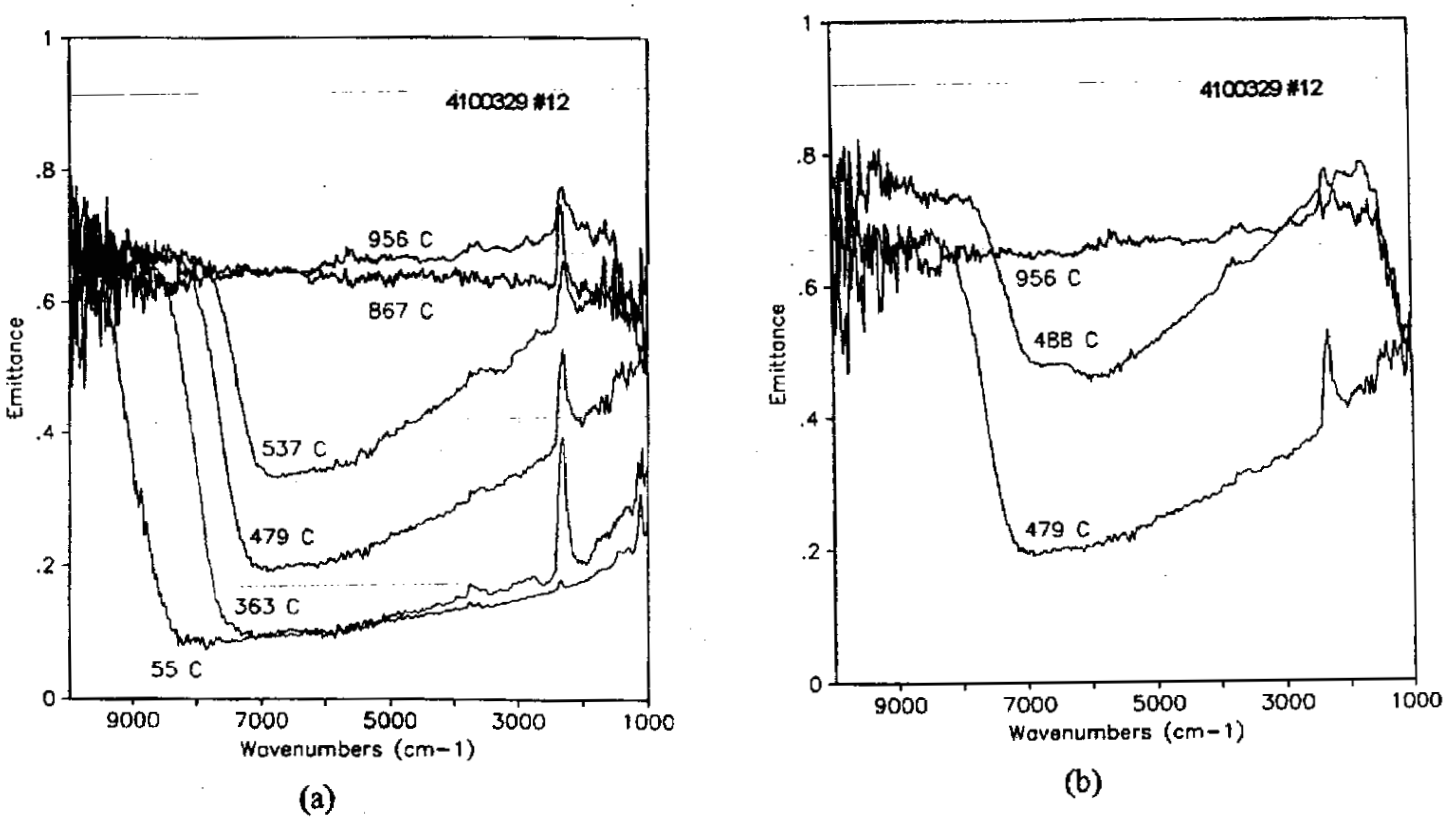


Fig.3. Emissivity as function of temperature of As^+ implanted furnace annealed sample (a) from 55 to 956°C, (b) from 956 to 488°C. The spectra at 479°C has been shown in order to demonstrate irreversible changes in the sample.

Solar Cell Materials and Device Characterization by PVSCAN

Bhushan Sopori, Jamal Madjdpour, and Marta Symko

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, CO 80401

As the commercial use of PV energy increases, a need for instruments using high speed techniques for characterization of material and cell quality is imminent. In fact, this need already exists for low-cost, single- and multi-crystalline silicon solar cells since they constitute more than 70% of the current PV energy sales. A meaningful characterization of low-cost materials and devices requires determination of the degree of spatial nonuniformities, as well as identification of the sources of these nonuniformities. In commercial PV silicon, the material nonuniformities arise from crystal defects, impurity segregation, and residual stresses. These nonuniformities can be altered by the cell-fabrication processes, which in turn can also introduce additional nonuniformities associated with nonideal processing. Some examples of the latter type of nonuniformities are reflectance variations in the surface texture and antireflection coatings, and spatial variation in the junction characteristics. It is imperative that instruments suitable for such detailed characterization be developed and be available to the PV industry and the research laboratories.

We have previously (23rd IEEE PVSC) described a technique for characterizing crystal defects in silicon using optical scattering from these defects. Here we describe implementation of these concepts into a novel instrument, PVSCAN5000, with extended capabilities for light-beam-induced current (LBIC) and reflectance mapping. This instrument can perform a host of analyses related to both the material quality of the substrate as well as spatial variations in a number of cell parameters. PVSCAN5000 is now commercially available from Labsphere Inc.

Figure 1 is a simplified schematic illustrating various components of PVSCAN5000. The system uses two lasers (λ_1= 0.63μm , and λ_2=0.905 μm) that can illuminate the solar cell or a wafer at normal incidence. Lens and aperture combinations (LL_1, A1) and (LL_2, A2) are used to control the sizes of the light beams in the sample plane. The reflected light is separated into specular and diffuse components; the specular component is collected by detector GBD. The diffuse component is collected by an integrating sphere and detected by detectors DD1 and DD2 corresponding to the illumination by lasers 1 and 2, respectively. In addition, the system has detectors (LPD_1 and LPD_2) that measure the intensity of light incident on the sample .

The integrating sphere can be moved out of the optical path to make LBIC measurements on the solar cells. The functions of other components are self explanatory. The various modes of the system operation are briefly described below:

Dislocation and grain boundary (GB) mode: This system can simultaneously produce maps of the dislocation density and the GB distribution. The sample is first etched in Sopori etch to delineate defects. This etch consists of $HF:CH_3COOH:HNO_3$ in the ratio 36:15:2. The defect-etched wafer is then scanned by an X-Y scanning stage under a light beam from the laser 1. When the light beam is incident on a region with dislocations, the light is scattered. This scattered light is collected by the integrating sphere and is detected by the dislocation detector, DD1. The total integrated light, scattered by the dislocations, is used to statistically count dislocations. When the light beam hits a GB, a part of the beam is reflected within a small angle around the specular beam, and escapes from the front aperture of the integrating sphere. The reflected light is directed by the beam

splitter BS_1 through an annular aperture (AA) and the lens L_{GBD}, toward the grain boundary detector (GBD). The annular aperture has a central stop to block the specular component of the reflected beam, thus allowing only the GB signal (consisting of a near-specular component that rides on the specularly reflected beam) to reach the GBD. When the light beam is incident on a defect-free region, the reflected light consists of only a specular component that is reflected along the GB path and gets blocked by AA, producing no signal at the GBD or at the DD1. In this manner, the GB signals and the dislocation signals are isolated and simultaneously measured.

The signals from various detectors are digitized and fed into a computer along with the position signals from the X-Y table to produce maps of dislocation density and the GB distribution. It should be noted that a dislocation map does not show grain boundaries and vice versa. The time required to produce both maps is about one hour for a 4-in x 4-in wafer.

Light beam induced current mapping: Figure 2 shows an LBIC map of a polycrystalline silicon solar cell taken with λ_1= 0.63μm. This figure clearly demonstrates the high resolution features of the system to obtain information on the spatial variations in the photoresponse.

Reflectance of the cell (or wafer): The PVSCAN5000 can provide the diffuse, specular, and total reflectances of a solar cell or a wafer. These parameters allow (i) mapping spatial variations in the AR coating, and (ii) generation of the internal LBIC response maps that are free from the effects of the changes in the reflectance due to different texture or variations in the antireflection coating thickness. This capability of making separate (and simultaneous) maps of the specular and diffuse reflectance allows this instrument to be used for both polished as well as textured or rough cells.

Figure 1.A schematic of thePVSCAN5000

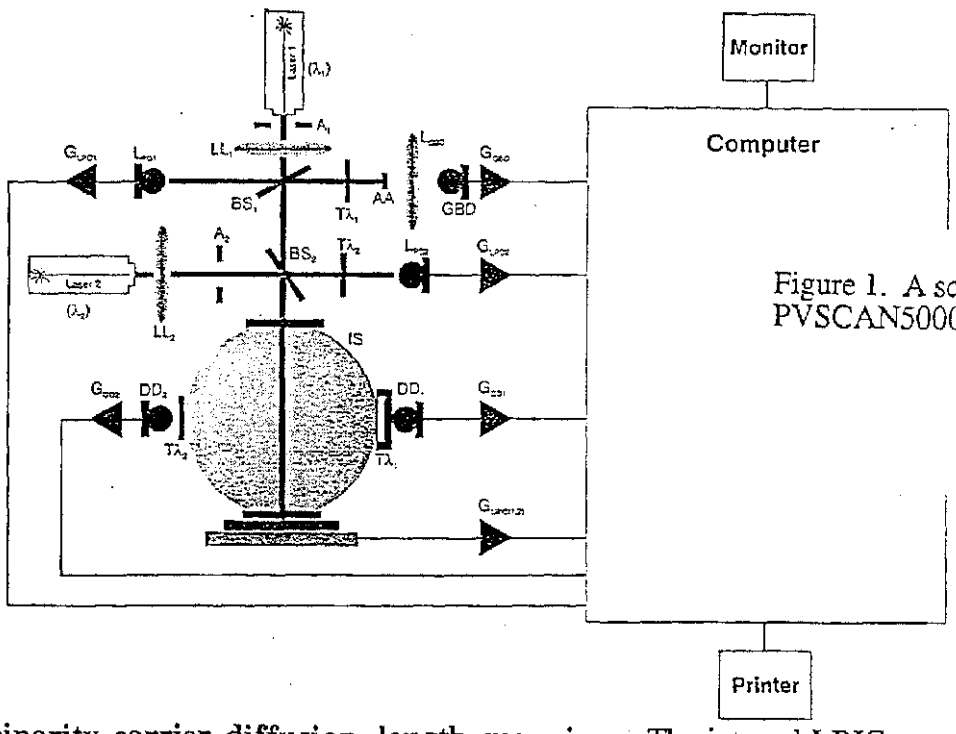


Figure 1. A schematic of the PVSCAN5000

The minority carrier diffusion length mapping: The internal LBIC response of a solar cell, for λ_2=0.905 μm excitation, is used to make minority carrier diffusion length maps. Thus, by mapping with short and long wavelength light beams separate maps of the recombination in the near-surface region and the bulk are obtained.

The capabilities of PVSCAN5000 can be seen in Figures 2, 3, and 4. In the LBIC map of Figure 2, one can see three major regions of low response; these are labeled as A, B, and C. Figure 3 is the reflectance map of the same cell and shows that there are significant changes in the reflectance of various grains. However, the cell response map in Fig. 2 and reflectance map in Fig. 3 are not well correlated. Figure 4 shows a dislocation density map of the cell whose map is shown in Fig. 2. This figure shows that the three regions A, B, and C correspond to high dislocation densities, as identified in Figure 4. It is thus clear that by combining the defect mapping, LBIC, and the reflectance capabilities of the instrument, one can unambiguously determine the source of nonuniformities. Such mapping capabilities are also essential for comparing effects of various processes such as gettering and passivation, for optimizing these process steps, and for understanding how these processes are influenced by defects and impurities.

Another example of the application of PVSCAN5000 is seen in Figure 5. Figure 5a is an external LBIC map (Fig. 5a) of a cell that has grain-to-grain variations in the photoresponse. However, this map alone cannot identify the source of these variations. By making a separate map of the total reflectance of the cell, the effect of changes can be separated. Figure 5b is the resultant internal LBIC map of the cell; the regions of low internal-LBIC response can be identified (because of high bulk recombination) and correlated with the dislocation maps.

Thus, PVSCAN5000 is a valuable tool for characterization and analysis of material growth and cell processing. Its applications include: determining the thermal stresses that result in dislocations during the crystal growth, controling the quality of material by measuring dislocation and grain size distributions from wafer to wafer (or ingot to ingot), monitoring reflectance of wafers and cells, and identifying sources of nonuniformities.

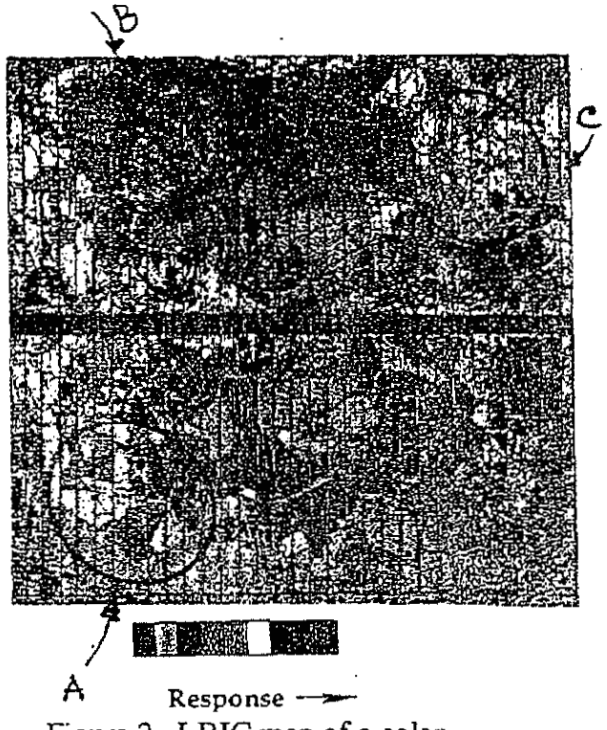


Figure 2. LBIC map of a solar cell (λ_1= 0.63μm)

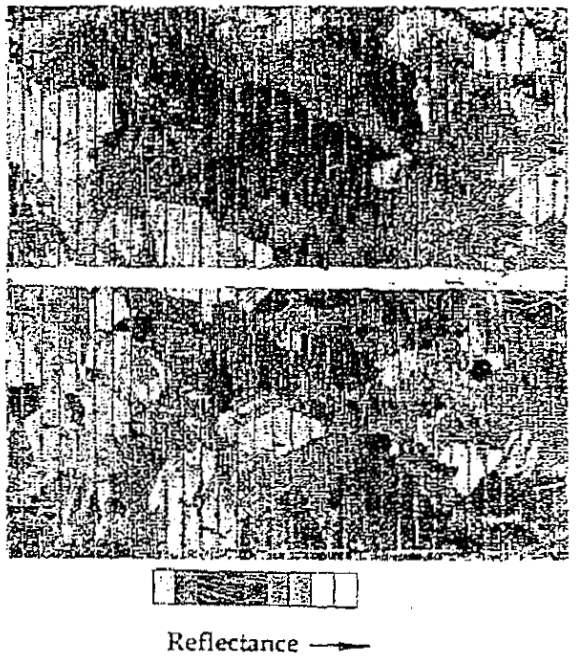


Figure 3. Reflectance map of the cell in Fig 1

Figure 4.
Disclocation map of the cell (photoresponse and reflectance maps are shown in Fig 2 and 3 respectively) The low response regions, A. B and C are identified in figure 2 and 4

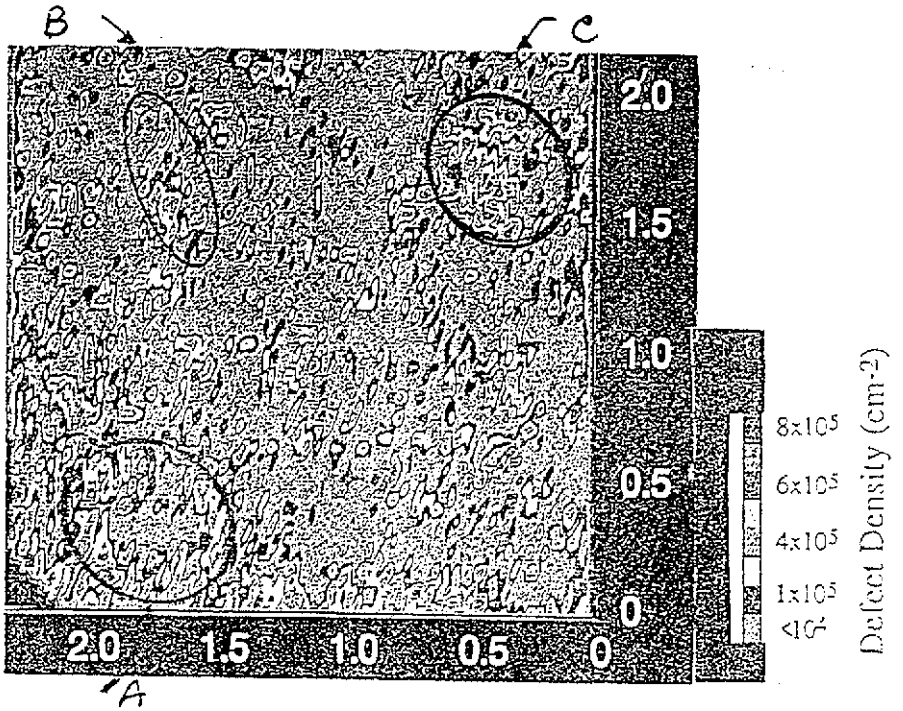


Figure 5a. External LBIC response of a cell taken at $\lambda = 0.6328\mu m$

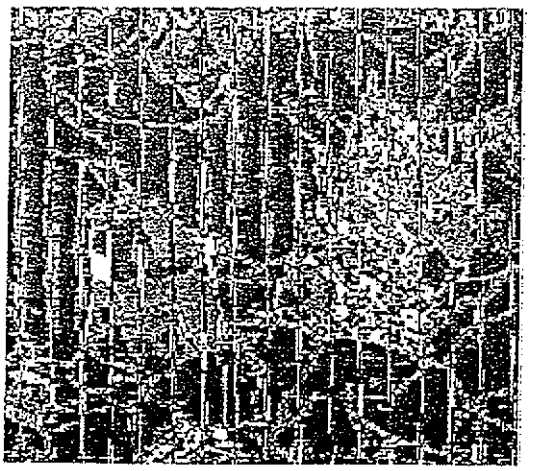
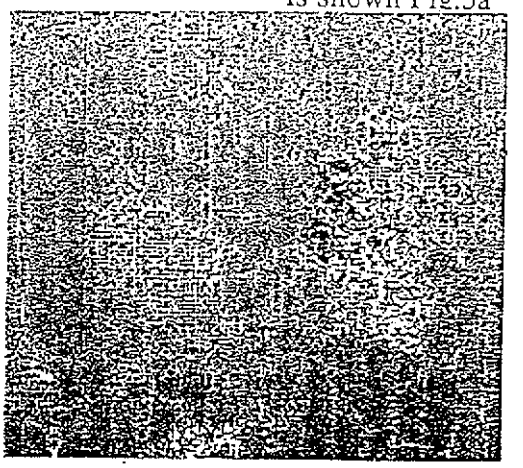


Figure 5b. Internal Respons of the cell whose external response is shown Fig.5a



ENHANCED HYDROGENATION IN POLYCRYSTALLINE SILICON THIN FILMS USING ULTRASOUND TREATMENT

J.Koshka, S. Ostapenko, L. Jastrzebski and J.Lagowski

Center for Microelectronics Research, University of South Florida, Tampa, FL 33620

Ultrasound treatment (UST) was applied to improve electronic properties of polycrystalline silicon films on glass. A strong decrease of sheet resistance was observed in plasma hydrogenated films at UST temperatures lower than 100°C (Fig.1). This is accompanied by improvement of hydrogenation homogeneity as confirmed by spatially resolved photoluminescence study. An enhanced passivation of grain boundary defects after UST is directly measured by nano-scale contact potential difference with atomic force microscope. We also observed a dramatic increase of infra-red photoluminescence (PL) intensity by a factor of two orders of magnitude after a few minutes of UST at 250°C. In films obtained by solid-phase crystallization of α-Si, UST activates a new PL maximum at about 0.9eV related to the amorphous fraction of poly-Si films (Fig.2). This hydrogen mediated UST effect has the activation energy of 0.33eV.

A new mechanism of ultrasound stimulated hydrogenation of dangling bonds in polycrystalline and amorphous Si films is proposed: UST promotes a liberation of trapped atomic hydrogen due to a selective absorption of ultrasound at grain boundaries, dislocations, and other extended defects. This is following by a fast hydrogen diffusion and capturing at dangling bonds.

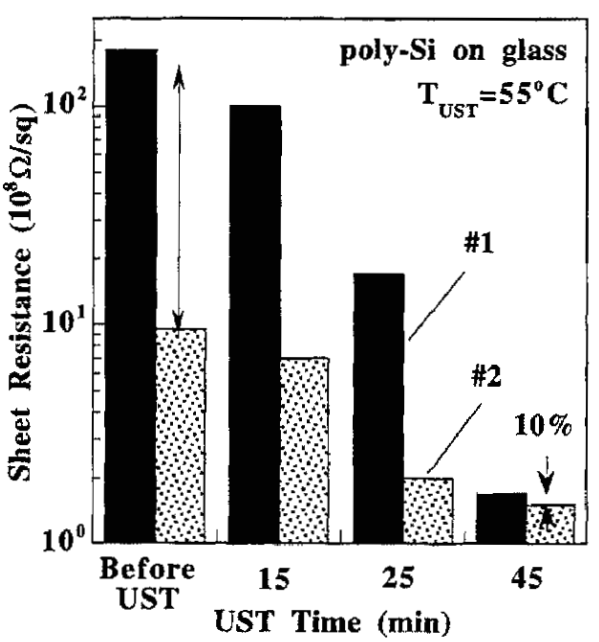


Fig.1 UST effect on sheet resistance.

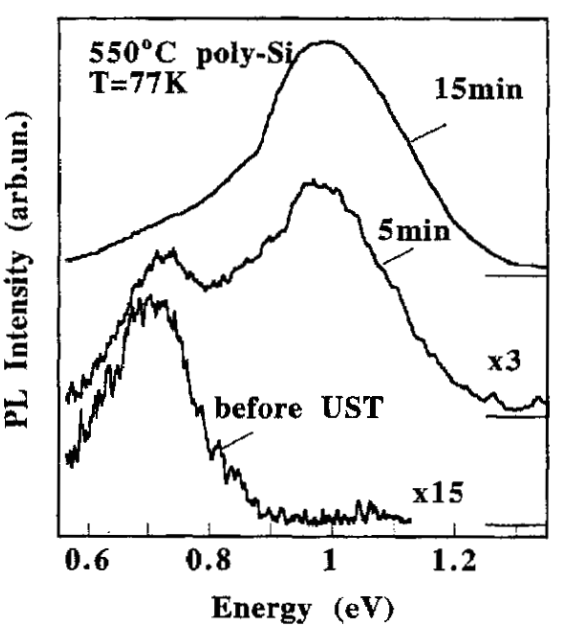


Fig.2 UST activation of luminescence (T_{UST}=250°C)

ENHANCED HYDROGENATION IN POLYCRYSTALLINE SILICON THIN FILMS USING ULTRASOUND TREATMENT

J.Koshka, S. Ostapenko, L. Jastrzebski and J.Lagowski

Center for Microelectronics Research, University of South Florida, Tampa, FL 33620

Abstract Ultrasound treatment (UST) was applied to improve electronic properties of polycrystalline silicon films on glass. A strong decrease of sheet resistance was observed in plasma hydrogenated films at UST temperatures lower than 100°C. An enhanced passivation of grain boundary defects after UST is directly measured by nano-scale contact potential difference with atomic force microscope. This is accompanied by improvement of hydrogenation homogeneity as confirmed by spatially resolved photoluminescence study. We also observed a dramatic increase of infra-red photoluminescence (PL) intensity by a factor of two orders of magnitude after a few minutes of UST at 250°C. In films obtained by solid-phase crystallization of α-Si, UST activates a new PL maximum at about 0.9eV related to the amorphous fraction of poly-Si films. A new mechanism of ultrasound stimulated hydrogenation of dangling bonds in polycrystalline and amorphous Si films is proposed.

Introduction. Hydrogenated amorphous (α-Si) and fine grain polycrystalline silicon (poly-Si) films on glass are materials for thin-film-transistors and solar cells. Operational parameters of both α-Si and poly-Si devices are affected by a high density of localized states (predominantly Si dangling bonds) at the interface and in the bulk. A conventional approach to reduce a density of these states is the passivation of thin films with atomic hydrogen. The hydrogen diffusivity in poly-Si and α-Si is described by an activation energy of 1.3 to 1.5eV and is recognized as a trap-limited process. As a consequence of hydrogen trapping in poly-Si, a conventional plasma hydrogenation requires several hours at 350°C. It was recently observed that low-temperature (T<100°C) ultrasound treatment (UST) applied to plasma hydrogenated poly-Si thin films causes an enhancement of the hydrogenation process [1]. A new mechanism of UST enhanced liberation of atomic hydrogen from an electrically non-active trapped state and following passivation of dangling bonds has been suggested [2]. We report basic experiments supporting this model.

Semi-insulating LPCVD silicon films with thicknesses about 0.5μm were deposited at 550°C or 625°C Corning 7059 glass or fused silica substrates. The 625°C films had a crystallite structure. As-deposited 550°C films were amorphous, and their annealing under nitrogen flow for 8 to 75hr at 550°C caused a gradual crystallization. The poly-Si films were selectively plasma hydrogenated using a pattern defined by an opening in an Al mask. This enabled us to study UST effects by comparing hydrogenated with non-hydrogenated areas on the same film. The hydrogenation was performed at 300°C in a parallel plate RF plasma system operating at a 100ccm H_2 flow with 0.3Torr pressure and 200W radio frequency power or using a low pressure ECR plasma system. For UST experiments, ultrasound vibrations were generated in poly-Si or α-Si films through a glass substrate using a circular 75mm diameter piezoelectric transducer. The UST transducer was operated at 25kHz resonance of radial vibrations. The amplitude of sample vibrations in acoustic contact with the transducer was monitored "in-situ" by a calibrated non-contact acoustic probe. The maximum acoustic strain amplitude on a film surface was of the order of 10^{-4}.

We used the PL mapping technique with a resolution of 100μm to monitor UST changes in distribution of recombination centers. The results are presented in Figure 2 in as two histograms of exactly the same hydrogenated film area prior to and after UST. The average 0.72eV PL intensity after UST exhibits an additional 25-30% increase and also narrowing by a factor of two of the half-width of the PL histogram in the mapped region. This result is consistent with the UST-induced improvement of resistance homogeneity shown in Fig. 1.

Contact potential difference (CPD) mapping using the atomic force microscope was performed in 30min ECR hydrogenated films. CPD contrast originates from the charge trapped at grain boundary defects in poly-Si. We performed the UST on hydrogenated films and observed a noticeable reduction of the CPD contrast after UST [1]. The UST effect on CPD mapping contrast provides a direct proof of ultrasound enhanced hydrogenation of grain boundary defects in poly-Si.

We also applied UST processing at T_{UST}=150-280°C to as-grown and 550°C annealed films. Two changes in the PL spectrum were observed (Fig.3). The first is the increase of the 0.72eV band intensity by a factor of 2 to 4 (in different samples). The second effect is a strong UST activation of a "new" broad PL band with a maximum at about 0.9eV. We notice that a dramatic enhancement of 0.9eV band exceeding *two orders* of magnitude compared to untreated sample requires only a few minutes of UST processing performed at 250-280°C. By using 550C films with controlled by Raman spectroscopy amorphous fraction, we proved that UST activated 0.9eV band corresponds to "defect" luminescence in α-Si:H. UST processing was performed at temperatures between 150 and 280°C. The UST kinetic is characterized by a time constant of 3min at 280°C which increases to 25min at 150°C. From the Arrhenius plot of UST time constant we found the UST activation energy: E_{UST}=0.33 +/- 0.05eV.

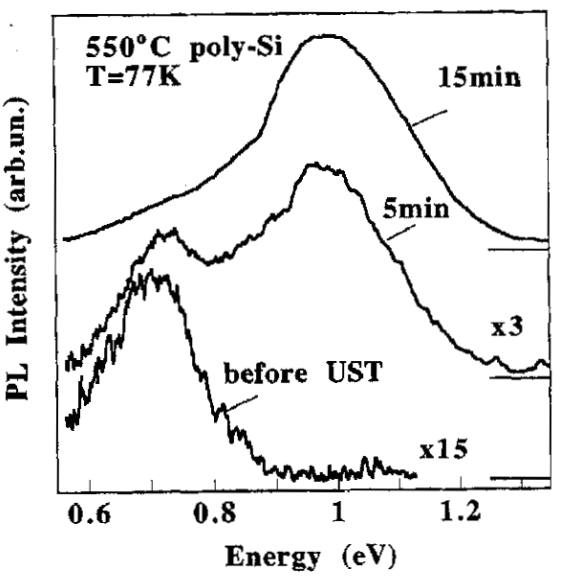


Fig.3 UST activation of luminescence (T_{UST}=250°C)

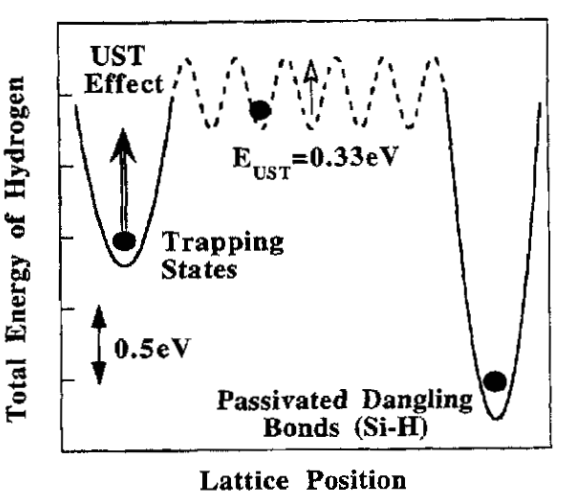


Fig.4 Model of UST enhanced hydrogenation in poly-Si and α-Si films.

Model. The following mechanism of UST activated hydrogenation of dangling bonds is illustrated in Fig.4. After film deposition and 550°C anneal and plasma hydrogenation, the atomic hydrogen is partially trapped at grain boundary defects, while there is a substantial number of non-saturated dangling bonds. UST processing promotes the hydrogen liberation from trapped states.

We used the PL mapping technique with a resolution of 100μm to monitor UST changes in distribution of recombination centers. The results are presented in Figure 2 in as two histograms of exactly the same hydrogenated film area prior to and after UST. The average 0.72eV PL intensity after UST exhibits an additional 25-30% increase and also narrowing by a factor of two of the half-width of the PL histogram in the mapped region. This result is consistent with the UST-induced improvement of resistance homogeneity shown in Fig. 1.

Contact potential difference (CPD) mapping using the atomic force microscope was performed in 30min ECR hydrogenated films. CPD contrast originates from the charge trapped at grain boundary defects in poly-Si. We performed the UST on hydrogenated films and observed a noticeable reduction of the CPD contrast after UST [1]. The UST effect on CPD mapping contrast provides a direct proof of ultrasound enhanced hydrogenation of grain boundary defects in poly-Si.

We also applied UST processing at T_{UST}=150-280°C to as-grown and 550°C annealed films. Two changes in the PL spectrum were observed (Fig.3). The first is the increase of the 0.72eV band intensity by a factor of 2 to 4 (in different samples). The second effect is a strong UST activation of a "new" broad PL band with a maximum at about 0.9eV. We notice that a dramatic enhancement of 0.9eV band exceeding *two orders* of magnitude compared to untreated sample requires only a few minutes of UST processing performed at 250-280°C. By using 550C films with controlled by Raman spectroscopy amorphous fraction, we proved that UST activated 0.9eV band corresponds to "defect" luminescence in α-Si:H. UST processing was performed at temperatures between 150 and 280°C. The UST kinetic is characterized by a time constant of 3min at 280°C which increases to 25min at 150°C. From the Arrhenius plot of UST time constant we found the UST activation energy: E_{UST}=0.33 +/- 0.05eV.

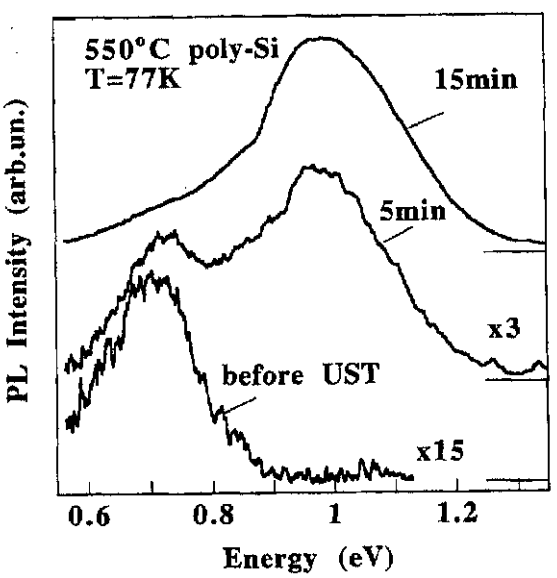


Fig.3 UST activation of luminescence (T_{UST}=250°C)

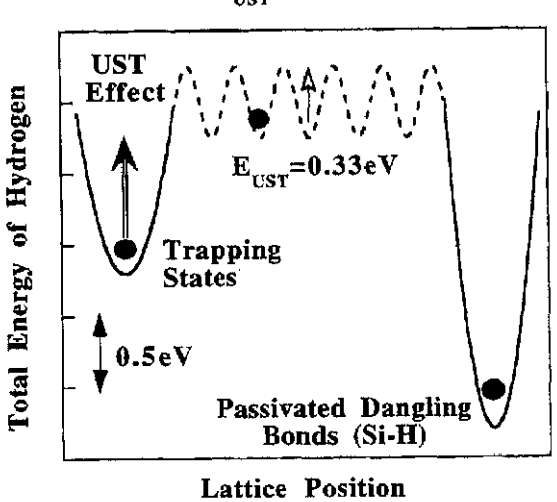


Fig.4 Model of UST enhanced hydrogenation in poly-Si and α-Si films.

Model. The following mechanism of UST activated hydrogenation of dangling bonds is illustrated in Fig.4. After film deposition and 550°C anneal and plasma hydrogenation, the atomic hydrogen is partially trapped at grain boundary defects, while there is a substantial number of non-saturated dangling bonds. UST processing promotes the hydrogen liberation from trapped states.

A physical reason of such UST induced hydrogen detrapping is a selective absorption of ultrasound by grain boundaries, dislocations, voids, and other extended crystal defects where hydrogen can reside. Being liberated from traps, hydrogen will diffuse with the diffusion coefficient of crystalline silicon: $D_H=9.4\cdot10^{-3}*\exp(-0.48eV/kT)$ [cm^2/sec], until it is captured at dangling bonds (Fig.4).

The UST activation energy (E_{ust} = 0.33eV) has a value close to the activation of H diffusion (E_o=0.48eV). A possible UST reduction of E_o can be caused by UST stimulated diffusion of hydrogen similar to Cr_i in Cz-Si [4]. The diffusion length for H migration under UST (T_{ust}=280°C, Δt=3min) can be estimated as $L=(D_H\cdot\Delta t)^{1/2}$=76μm. This value substantially exceeds a 100nm grain-size of poly-Si films, which explains why liberated hydrogen atoms can quickly approach non-radiative centers in poly-Si and α-Si phases.

We suggest that the UST effect is beneficial to both hydrogenated poly-Si and α-Si:H films on glass, where hydrogen binding and transport can be affected by ultrasound to engineer thin films with optimal parameters.

This work was supported by NREL contract XD-2-11004-5 and ARPA under NASA cooperative agreement #NCC8-31. Matching funds were provided by the State of Florida, Inc. and Semiconductor Diagnostics, Inc.

References

1. S.Ostapenko, L.Jastrzebski, J.Lagowski, and R.K.Smeltzer, APL, **68**, 2873 (1996)
2. J.Koshka, S.Ostapenko, T.Ruf, and J.M.Chang, APL, in press
3. A.Savchouk, S.Ostapenko, G.Nowak, J.Lagowski, J.Jastrzebski, APL, **67**, 82 (1995)
4. R.Bell, S.Ostapenko, and J.Lagowski, in *Defect and Impurity Engineered Semiconductors and Devices,* (MRS, Pittsburg, PA, 1995), p.647

The Effects of External Gettering on Silicon-Film™

K.M. Dugan Cavanagh, D.H. Ford, J.A. Rand, R.B. Hall, and A.M. Barnett
AstroPower
Solar Park
Newark, DE 19716-2000

Abstract

External gettering has been employed as a means to improve the minority carrier diffusion length in Silicon-Film™ Product I material. A comparison of $POCl_3$ and combined $Al/POCl_3$ gettering treatments have been conducted on $1 cm^2$ solar cells. One of these processes has demonstrated minority carrier diffusion lengths greater than 200 μm.

Introduction

Silicon-Film™ is comprised of a thin layer of polycrystalline silicon material grown on a low-cost substrate. Large sheets of Silicon-Film™ have been developed yielding solar cells with areas of up to 700 cm^2 and a power rating of 7.87 W (AM1.5G). Recently, AstroPower has reported the development of the AP300, a Silicon-Film™ 316 cm^2 area solar cell providing 3.5 W of power [1].

Development of these devices is the result of innovations in material process development, post growth treatments, and device fabrication techniques. The post growth treatment includes a gettering procedure for improved minority carrier transport properties.

Generation and collection of carriers are hindered by recombination due to lifetime killing impurities such as Fe, Au, Cr, and Ni. Gettering, the process of removing these unwanted impurities from an active device volume, has been employed in the semiconductor industry to improve material quality. During gettering, impurities are released from their location in the semiconductor, diffuse to the gettering regions, and are captured into these gettering regions [2]. Internal gettering encourages impurities to diffuse toward precipitates in the bulk of the semiconductor. This increases the quantity of recombination centers in the bulk but decreases those on the semiconductor surface. External gettering regions are provided by damaging the surfaces of the wafers through mechanical or chemical means including $POCl_3$ and combined $Al/POCl_3$ treatments at high temperatures. Following an external procedure, the gettering regions can be removed chemically or mechanically, leaving the bulk with reduced recombination centers. In the computer industry, the critical issue is purifying the semiconductor surface, which is accomplished by both internal and external gettering. However, in photovoltaics, the surface and the bulk material purity are both critical. Therefore, only external gettering is employed to reduce impurities in the bulk.

The minority carrier diffusion length (Ln or simply diffusion length) of solar cells fabricated from as-grown Silicon-Film™ has improved from 20 to 35 μm to greater than 200 μm with a combined Al/$POCl_3$ external gettering procedure. The experimental process and results are detailed below.

Experimental Procedure

Prior to gettering, the Silicon-Film™ material was cleaned in HNO_3:HF (95:5) etch and polished in HNO_3:HF (90:10). The chemical etch was followed by a microsoap scrub and rinse in DI water. An H_2SO_4:H_2O_2 (1:1) organics etch and an HCl:H_2O_2 (1:1) heavy metals etch was utilized to ensure that the samples were thoroughly clean. A brief H_2O:HF (20:1) etch was then employed to remove any remaining oxide.

Three gettering conditions were evaluated in this study: no getter, $POCl_3$ getter and a combined Al/$POCl_3$ getter. Those samples which received the combined Al/$POCl_3$ treatment had a 4μm Al layer evaporated on the front side prior to gettering. All gettering experiments were performed in a diffusion furnace at 890 °C for 4 hours with a flow rate ratio of 60:40 O_2:$POCl_3$. The samples were cooled for 1 hour at 1.5 °C/ min and were removed from the furnace.

Following the gettering process, the samples with Al on the front side were highly discolored. This was due to an Al-Si eutectic formation during the high temperature and long duration of the gettering procedure. A post-getter cleaning procedure was developed to remove the gettering regions and establish a clean, usable surface. The cleaning procedure included etching the gettering region with HNO_3:HF (90:10) until a smooth surface resulted.

The post getter clean was followed by a microsoap clean, an organics etch, heavy metal etch, and oxide strip (similar to the pre-getter clean). The final steps in fabrication included emitter diffusion into the active area, (Rsh = 60 ohm/sq), a post-diffusion cooldown to less than 300 °C in a forming gas ambient, and an emitter etchback (Rsh = 80 ohm/sq). Thermally evaporated Ti/Pd/Ag contacts were deposited on the front (patterned) and back (planar) surfaces. The samples were alloyed at 425 °C for 1 minute in 15% H_2 forming gas ambient and were then isolated by dicing.

Results

Internal quantum efficiency (IQE) data for samples gettered with $POCl_3$, gettered with both Al/$POCl_3$, and with no gettering (control) are shown in Figure 1. The combined Al/$POCl_3$ gettering process yields the greatest increase in IQE, particularly in the bulk of the material. The same starting material was used for each sample and therefore the initial impurity concentration was approximately the same. The oxygen concentration (measured at NREL via FTIR) was $2x10^{17}$ cm^{-3} for this material. All samples were diffused and processed together.

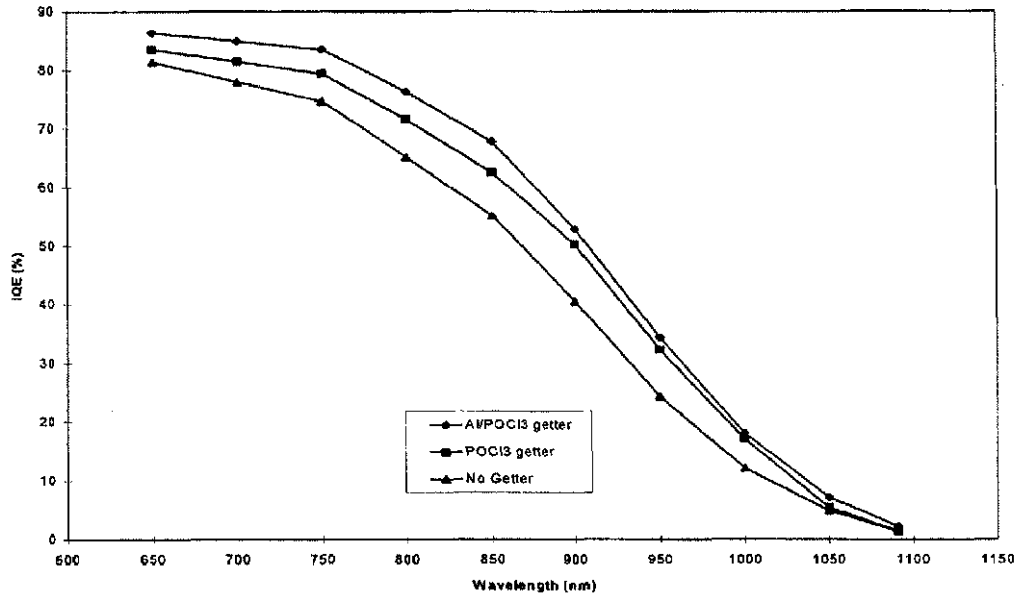


Figure 1. IQE vs. wavelength for $POCl_3$ getter, Al/$POCl_3$ getter, and a control (no getter).

The diffusion length is determined by correlating the IQE data with the absorption coefficient (α) of silicon. From the definition of IQE, and the following assumptions:

$$\frac{1}{\alpha} >> x_j + W \qquad \text{and} \qquad \frac{1}{\alpha} >> H' >> L_n$$

where Ln is the diffusion length, H' is the width of the base region, W is the width of the space charge region, x_j width of the emitter region, the relationship between IQE, Ln and α is found by:

$$\frac{1}{IQE} = \frac{1}{\alpha}\frac{1}{L_n} + 1$$

The measured diffusion length for as-grown Silicon-Film™ material varies between 20 and 35 μm depending on the growth conditions. Development of the Al/$POCl_3$ gettering sequence described in this paper enabled fabrication of solar cells with diffusion lengths between 50 and 218 μm for a single wafer as measured by the inverse slope of the 1/IQE vs 1/α curve. Figure 2 shows the IQE for a solar cell which employed a 4 hour $POCl_3$ getter combined with 4 μm of Al deposited on the front side of the wafer. This particular sample had a measured diffusion length of 218 μm. The variation in diffusion length for this wafer is reflected through both a difference in grain size and most likely a difference in impurity profiles throughout the wafer.

The differences in the quantum efficiency between samples using the same Al/$POCl_3$ gettering sequence in Figure 1 and Figure 2 may be explained in part by a difference in grain size. Figure 1 shows IQE data for samples with grain sizes less than 130 μm, while grain size in samples with the IQE shown in Figure 2 are greater than 320 μm.

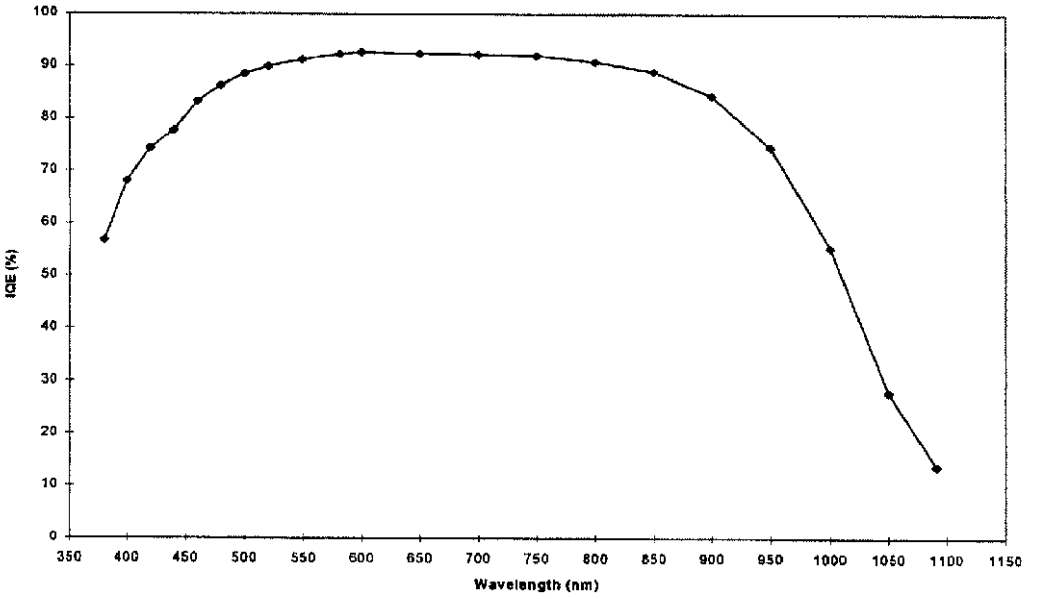


Figure 2. IQE vs. wavelength for a solar cell with combined Al/$POCl_3$ gettering treatment (Ln=218 μm).

Discussion

External gettering of Silicon-Film™ has improved the as-grown material for enhanced solar cell performance as determined by minority carrier diffusion length measurements. The combination of an Al layer on the front side of the wafer with a $POCl_3$ gettering treatment provided the greatest increase in diffusion length. Misfit dislocations generated by the high temperature $POCl_3$ diffusion damage the material surface thus providing gettering regions[2]. In addition, an Al-Si eutectic forms and provides sinks for the impurities[3]. Variations in the diffusion length for the same gettering procedure may be explained by a difference in grain size and/or the impurity concentration inherent in the starting material.

Further gettering experiments are underway with the goal of developing a gettering process for manufacturing which is capable of producing high efficiency Silicon-Film™ solar cells.

References

[1] David H. Ford, Allen M. Barnett, et. al "High Power, Commercial Silicon-Film™ Solar Cells", Proceedings of the 25th IEEE PVSC, (May, 1996).

[2] K.V. Ravi, Imperfections and Impurities in Semiconductor Silicon, John Wiley & Sons,(1981) 336-346.

[3] L.A. Verhoef, P-P. Michiels, et. al. "Gettering in Polycrystalline Silicon Solar Cells", Materials Science and Engineering, B7 (1990) 49-62.

Screen Printed Aluminum Back Surface Fields for Silicon Solar Cells

S. Narasimha, J. Mejia, and A. Rohatgi
University Center of Excellence in Photovoltaic Research and Education
Georgia Institute of Technology, Atlanta, GA. 30332-0250

Introduction

In high quality silicon solar cell materials, minority carrier recombination at the back surface plays an important role in determining the overall device efficiency. Back surface recombination velocity (S_b) begins to influence cell performance when the ratio of diffusion length to device thickness exceeds one-half. Most single crystal materials, like Czochralski (CZ) or float zone (FZ), have minority carrier diffusion lengths longer than the wafer thickness. In addition, multicrystalline silicon (mc-Si) growth techniques have improved to the point where grain sizes and intragrain diffusion lengths are relatively large. These observations emphasize the need to reduce S_b of solar cells fabricated on such materials. Furthermore, there exists a need to reduce S_b by using a cost effective process which lends itself to high-throughput production.

In the past, differing methods have been implemented to lower the S_b experienced in silicon solar cells. For example, high efficiency silicon solar cells (> 24%) have been fabricated by employing thermally grown oxides to passivate the back surface [1]. The problem with this method is that it is process-intensive, usually requiring high temperature furnace processing and photolithographic masking steps. The more commonly implemented method of reducing S_b is to incorporate a back surface field (BSF) into the solar cell structure. On p-type substrates, BSFs are realized by either boron diffused regions or by aluminum alloyed layers. Boron diffused BSFs can be effective, but they require lengthy diffusion steps at high temperatures (> 1000°C). This limits their applicability in high-throughput processes. Aluminum alloyed BSFs (Al-BSFs) are attractive from a production standpoint because they can be formed rapidly. In order to be effective, however, significant quantities of aluminum (> 5 μm) must be deposited onto silicon prior to alloying. Because of this requirement, traditional deposition methods such as evaporation or sputtering are not suited for effective Al-BSF formation. On the contrary, screen-printing provides an effective way to apply large quantities of aluminum onto a wafer in a matter of seconds. Screen-printed (SP) samples can then be alloyed in a few minutes time using rapid thermal annealing. Thus, effective Al-BSFs, resulting in low S_b values, can be achieved in a high-throughput fashion. The objective of this paper is to model and characterize SP Al-BSFs, and to report on their integration into high efficiency solar cell fabrication.

Theory and Simulation

Al-BSF formation occurs through an alloying process which is dictated by the aluminum-silicon (Al-Si) equilibrium phase diagram. The formation procedure has been discussed elsewhere [2]. The thickness of the p^+ region can be calculated according to:

$$W_{BSF} = \frac{g_{Al}}{\rho_{Si}}\left(\frac{F}{100-F} - \frac{12.2}{100-12.2}\right) \qquad (1)$$

where g_{Al} is the amount of deposited aluminum, ρ_{Si} is density of silicon, *12.2* is the silicon atomic weight percentage at the eutectic temperature, and F represents the silicon atomic weight percentage of the molten phase at the peak alloying temperature [3]. The parameter F is determined from the Al-Si phase diagram. For the short firing times typically implemented in the formation of Al-BSFs, aluminum diffusion into silicon can be neglected [2].

Using the above formulation, theoretical Al-BSF profiles can be calculated as a function of deposited aluminum and the maximum firing temperature. For these BSF profiles, the effective S_b at the p^+p interface can be calculated numerically using an elemental approach put forth by Rohatgi et. al. in [4]. The inputs to this numerical method are simply the BSF profile and recombination velocity at the true back surface of the device, S_o. In all calculations given in this paper, S_o has been set to 10^7 cm/s to simulate metal coverage. To maintain consistency with other simulators used in the photovoltaic community, mathematical models for bandgap narrowing, mobility in the silicon, and heavy doping effects were chosen to be the same as those used in the

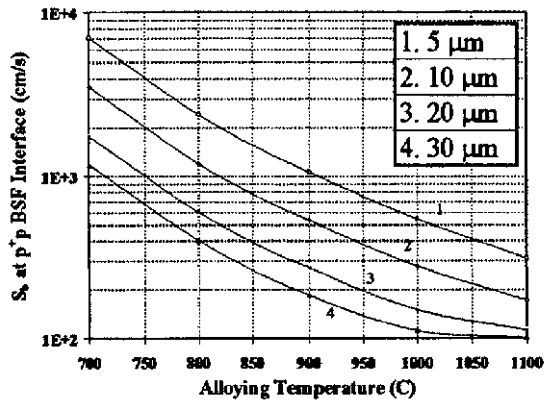


Fig. 1. Calculated S_b values for Al-BSFs on 2 Ω-cm substrates as a function of deposited aluminum thickness and peak firing temperature.

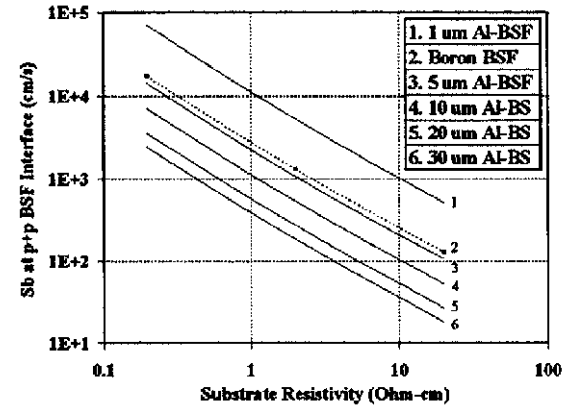


Fig. 2. Calculated S_b values for Al-BSFs alloyed at 900°C as a function of deposited aluminum thickness and substrate resistivity.

semiconductor simulator PC-1D [5]. Solubility data published by Murray and McAlister [6] was used to calculate the aluminum profiles. Fig. 1 shows the results of a number of calculations of S_b on a 2 Ω-cm substrate as a function of deposited aluminum and peak alloying temperature. It is clear that increasing either the amount of deposited aluminum or the firing temperature serves to decrease S_b.

Fig. 2 shows a plot of calculated S_b values versus substrate resistivity for different thickness' of deposited aluminum which undergo alloying at 900°C. Also included for comparison is an S_b plot of a typical boron BSF that is diffused for one hour at 1100°C resulting in a surface concentration of 1e20 cm^{-3} and a junction depth of 1µm. It is clear from this analysis that the BSF effect improves with increased substrate resistivity. Fig. 2 reveals that the boron BSF is superior to the Al-BSF when thin aluminum layers (< 5 µm) are deposited. However, the boron BSF is inferior to the Al-BSF when thick aluminum layers (> 5 µm) are used. The latter situation occurs naturally when screen-printing techniques are implemented in processing.

Experimental Procedures

Initially, simple 1 cm^2 n^+pp^+ solar cells were fabricated on high quality 2.0 Ω-cm FZ wafers which were 520 µm thick. The PCD lifetime measured in this material was quite high (i.e. the diffusion lengths are significantly longer than the wafer thickness). The n^+ emitters were formed by 30 minute $POCl_3$ diffusions which resulted in sheet resistance between 100-125 Ω/sq. The junction depth was approximately 0.3 µm and the peak doping concentration did not exceed 5e19 cm^{-3}. Next, a passivating thermal oxide (100 Å) was grown on the emitters at 850°C. Then, the BSFs were formed by screen-printing commercially available aluminum conductor paste onto the backside of the wafers. The Al-BSFs were alloyed in an RTP system in which they were exposed to the peak temperature for two minutes. In order to determine optimal process conditions, samples were fired at selected temperatures between 850°C and 1000°C. Front contacts were formed by evaporation of 600 Å of Ti, 400 Å of Pd, and 4.5 µm of Ag followed by lift-off photolithography. This method of front contact formation was selected instead of screen-printing in order to keep the J_{oe} component of the reverse saturation current density as low as possible, thereby making V_{oc} of the finished devices a strong function of J_{ob} and S_b. On each wafer, sixteen 1 cm^2 devices were defined by mesa isolation in order to gauge the variability of the process across a circular area of 46 cm^2 (3 inch diameter). Finally, a double layer antireflection (AR) coating consisting of ZnS and MgF_2 was applied on each wafer.

Once the optimal BSF alloying conditions were determined, the SP Al-BSF process was applied to three high quality substrates: FZ (0.6 Ω-cm, 1.2 Ω-cm, 2.0 Ω-cm). Devices with SP Al-BSFs were compared with solar cells which underwent a standard baseline process. The BSF of the baseline procedure was formed by evaporating 1 µm of aluminum onto the wafer prior to alloying at 850°C for thirty minutes.

Results and Discussion

Fig. 3a shows the thickness profile for an aluminum paste layer screen-printed on a silicon substrate prior to firing. Fig. 3b shows the profile after firing the sample at 900°C for 2 minutes. At this firing temperature, the

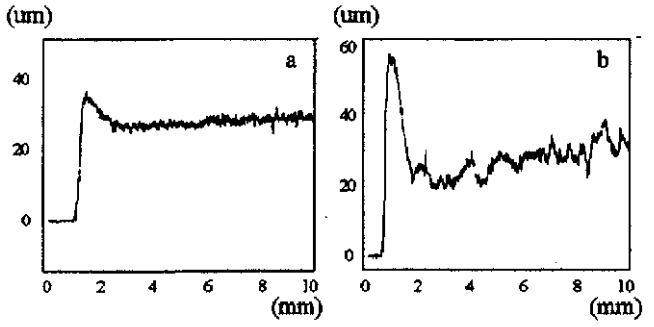


Fig. 3. Profile measurements of screen-printed aluminum layers: a) before firing b) after firing.

Fig. 4. SEM micrograph of the delineated Al-BSF region.

binding material present in the paste evaporates, and the only remaining ingredient is the aluminum which is 20-30 μm thick. After the firing, pieces from the sample were cleaved out and viewed with an SEM in order to observe the cross sectional layer formation. The samples were etched in an acid mixture to delineate the junction depth of the p^+ aluminum doped region. An SEM micrograph of the layered structure is shown in Fig. 4. Clearly, the BSF region is quite thick. However, the junction depth is noticeably nonuniform across the wafer. A number of measurements taken on this sample reveal an average junction depth of 8.4 μm, with minimum and maximum values of 3.9 μm and 14.5 μm. It is believed that the fast ramp-up and cooldown rates are the primary cause for this nonuniformity. Other reasons may be temperature variation across the wafer during the high temperature firing or insufficient mixing of the of the aluminum in the paste solution.

In order to determine the peak concentration of the BSF region at the p^+p interface, a spreading resistance profile was taken at a random spot on the sample. The result, shown in the inset of Fig. 5, indicates a peak concentration of 4e19 cm^{-3} which is roughly one order of magnitude higher than the solid solubility at 900°C reported in [6]. However, the measurement is in better agreement with the solid solubility data presented by [7]. The measured junction depth is roughly 10 μm (on 2 Ω-cm material) at the spot under test. For this BSF profile, the numerically calculated S_b as a function of substrate resistivity is shown in Fig. 5. This particular BSF profile results in an S_b between 200-300 cm/s on a 2 Ω-cm substrate wafer. The deviation bars shown in Fig. 6 indicate the swing in the S_b value that is expected for the same profile as the junction depth is scaled from the maximum to the minimum values measured by SEM analysis (3.8 μm to 14.5 μm).

Fig. 6 shows the average V_{oc} response of solar cells fabricated on 2 Ω-cm FZ material as a function of the SP Al-BSF alloying temperature. (The emitters of these devices were not oxide-passivated.) The optimum temperature of 900°C resulted in the best V_{oc}, which is a strong function of S_b in this high quality material. It was observed that increasing the firing time from 2 minutes to 5 minutes at 900°C increased the uniformity (and thus the average) of the measured V_{oc} values across a wafer. As the alloying temperature was increased beyond 900°C, the cell performance degraded. At 1000°C, the V_{oc} was lowered to levels which indicate a significant loss in bulk lifetime. Long wavelength IQE measurements showed that the bulk lifetime in these devices was lowered

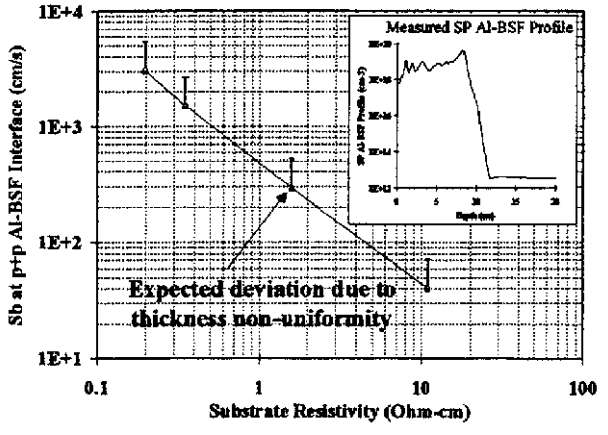


Fig. 5. Measured Al-BSF profile along with calculated S_b values as a function of substrate resistivity.

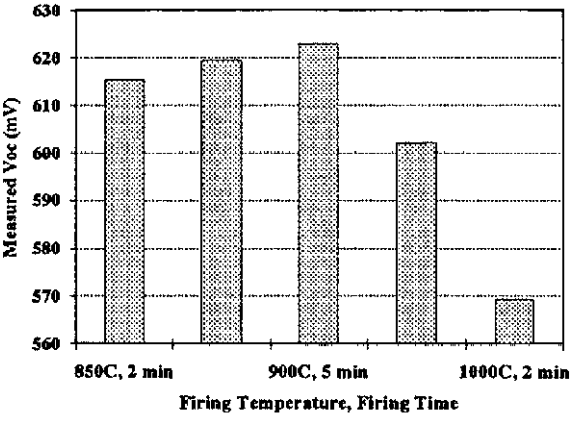


Fig. 6. Measured V_{oc} on 2 Ω-cm material as a function of SP Al-BSF alloying conditions.

below 5 μs. The source of contamination in this process was the aluminum conductor paste. The paste used in this study contained metallurgical grade aluminum (99.7%), with the major impurity (as specified by the vendor) being Fe. It is evident from Fig. 6 that this particular conductor paste can not be used at firing temperatures above 900°C because of lifetime degradation sustained by the silicon.

Fig. 7 shows the difference in the long wavelength IQE between solar cells fabricated on 2 Ω-cm FZ material with SP Al-BSFs and those with evaporated Al-BSFs. Integrating the spectral response of the two devices against the AM1.5 Global solar spectrum shows an increase of 1 mA/cm^2 in J_{sc} between 780-1100 nm for the device with the SP Al-BSF. In this wavelength range, the current response is largely a function of S_b and bulk lifetime. A curve-fitting procedure was done on the measured IQE in the long wavelength range in order to determine the S_b for the two BSF processes. An S_b of 200 cm/s (for bulk lifetimes ranging from 300-400 μs) was extracted for the SP Al-BSF, whereas a minimum S_b of 7,000 cm/s (for bulk lifetimes ranging from 200-300 μs) was extracted for the evaporated Al-BSF. The effects of the SP BSFs on the two other FZ materials are listed in Table 1. In Fig. 8, the S_b values shown in Table 1 are plotted along with the S_b values derived from the spreading resistance profile measured in Fig. 5. The data points fall reasonably well within the limits given by the deviation bars.

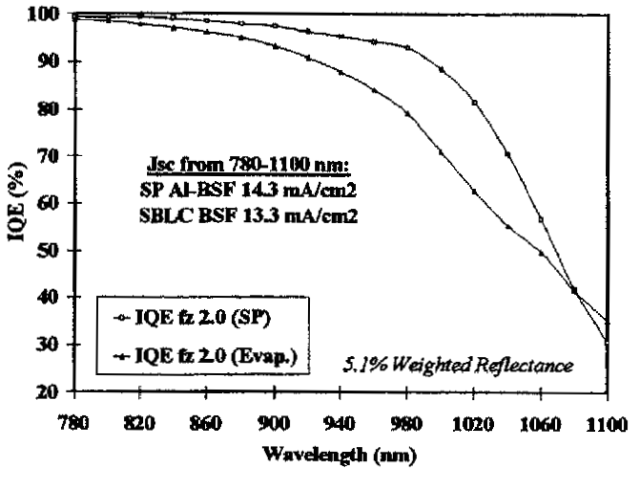


Fig. 7. Long wavelength IQE difference for solar cells fabricated on 2 Ω-cm material with SP and evaporated Al-BSFs.

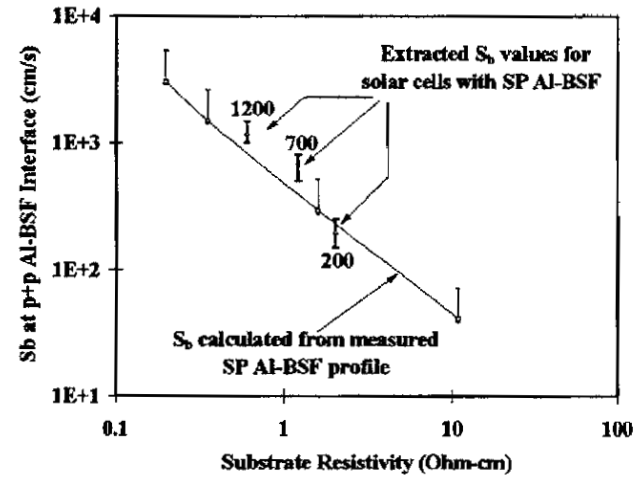


Fig. 8. Measured S_b values (with uncertainty) compared with S_b values calculated from the Al-BSF profile in Fig. 5.

Table 1. Effects of screen printed BSFs on the performance of solar cells fabricated on float zone silicon. Efficiencies were calculated using normalized fill factors of 0.79, 0.80, and 0.80 for the 0.6 Ω-cm, 1.2 Ω-cm, and 2.0 Ω-cm materials, respectively. All devices have thermal oxide passivation on the n$^+$ emitters.

Resistivity (Ω-cm)	Process	Voc (mV)	Jsc (mA/cm2)	Efficiency (%)	ΔJsc (mA/cm2) (780-1100 nm)	S_b (cm/s)
0.6	Evaporated Al	621	35.4	17.6		> 10,000
	SP Al	635	36.3	18.4	+ 0.7	1200
1.2	Evaporated Al	627	36.3	18.2		> 10,000
	SP Al	635	37.1	18.8	+ 1.2	700
2.0	Evaporated Al	622	36.7	18.0		> 7000
	SP Al	635	37.8	19.0	+ 1.0	200

Conclusions

As solar grade material quality improves, and as photovoltaic materials become thinner, the need for back surface passivation will become critical. In this study, SP Al-BSFs have been shown to effectively lower S_b in a manner which lends itself to high-throughput processing. The as-printed aluminum layers measured 20-30 μm in thickness. Physical characterization showed that the resulting BSFs were quite thick (average depth: 8.4 μm). S_b values as low as 200 cm/s were achieved with SP Al-BSFs formed during 2 minute anneal cycles at 900°C. Thin evaporated Al-BSFs alloyed for 30 minutes at 850°C were significantly poorer (S_b > 7000 cm/s). The S_b values

extracted from solar cells with SP Al-BSFs matched remarkably well with values calculated from measured profiles. The experimental work in this study was done largely on high quality silicon so that the solar cells may be strongly affected by the BSF. Future work will focus on applying the results to less expensive photovoltaic materials.

Acknowledgment

We would like to thank D.L. Meier at Ebara Solar, Inc. for his helpful suggestions regarding delineation etching. This work was supported under Sandia subcontract number AO-6162 and NREL subcontract number XD-2-11004-2.

References

[1] A. Wang, J. Zhao, and M.A. Green, "24% Efficient Silicon Solar Cells," *Appl. Phys. Lett.*, **57**, p. 602,1990.
[2] P. Lolgen, *Surface and Volume Recombination in Silicon Solar Cells*, Ph.D. Thesis, 1995.
[3] J. del Alamo, J. Eguren, and A. Luque, "Operating Limits of Al-Alloyed High-Low Junctions for BSF Solar Cells," *Solid-State Electron.*, **24**, pp. 415-420, 1981.
[4] A. Rohatgi and P. Rai-Choudary, "High-Efficiency Silicon Solar Cells: Development, Current Issues and Future Directions," *Solar Cells*, **17**, pp. 119-133, 1986.
[5] P. Basore, *PC-1D Installation Manual an User's Guide: Version 3*, 1991.
[6] J.L. Murray and A.J. McAlister, "The Al-Si (Aluminum-Silicon) System," *Bulletin of Alloy Phase Diagrams*, **5**, pp. 74-84.
[7] F.A. Trumbore, *Bell Syst. Tech. J.*, **39**, p. 205, 1960.

A Simultaneous Front and Back Diffusion Technique for the Low Cost Production of High Efficiency Silicon Solar Cells.

Thomas Krygowski, Ajeet Rohatgi
University Center of Excellence for Photovoltaic Research and Education, Georgia Institute of Technology, Atlanta, Georgia 30332-0250

I. Introduction

The fabrication of high efficiency silicon solar cells by conventional techniques requires multiple high thermal-budget processing steps, such as oxidation, separate boron or aluminum diffusions for the Back Surface Field (BSF), and a separate phosphorus diffusion for the emitter region of a solar cell. To reduce processing time, and increase yield it would be desirable to simultaneously perform the emitter and BSF diffusions in a single furnace processing step. We have developed a diffusion technique, termed Dopant Oxide Solid Source (**DOSS**) diffusion which is capable of simultaneous boron and phosphorus or aluminum and phosphorus diffusions without any detectable cross doping. This process also allows for the in-situ growth of a high quality passivating oxide on the emitter and BSF regions of a cell. Solar cell efficiencies of about 19 % have been achieved on float zone silicon by these DOSS diffusion techniques. This process is carried out using commercially available chemicals in conventional diffusion furnaces, making it completely compatible with industrial solar cell fabrication techniques.

II. Experimental

To obtain simultaneous diffusions on the front and back of a solar cell, a hybrid diffusion technique was developed using liquid and spin-on diffusion sources in a solid doping source configuration. The idea is to fabricate solid phosphorus doping sources out of silicon wafers by growing an oxide doped with P_2O_5 in a conventional diffusion furnace; a step analogous to the pre-deposition step in a $POCl_3$ liquid source diffusion. These phosphorus source wafers (P) are then interleaved with the solar cells (S) as shown in figure 1, with the front side of the solar cell facing a phosphorus source and the back side facing the (back side) of an adjacent cell. In the configuration of figure 1, the BSF diffusions are formed at the same time as the emitter diffusions by spinning a high purity boron film on the back side of the solar cells, or by evaporating a thin layer of aluminum on the back side of each cell before loading into the diffusion furnace. Recently [1] it was shown that for the configuration of figure 1, a heavily doped boron film is required on only one of the two adjacent wafers, with a nearly identical boron BSF being formed on the adjacent (uncoated) solar cell through autodoping. Thus, only 1/2 of the solar cell wafers need to be brought through the spin-on process prior to loading into the diffusion furnace. The residual phosphorus diffusion glass on the diffused cell is extremely thin, on the order of 30-40 Å. This allows for the in-situ growth of a thin thermal oxide for surface passivation, without appreciably increasing the reflectance of the device after applying the antireflection coating. It should be noted that conventional, ceramic-based phosphorus solid doping sources can be damaged by exposure to oxygen at elevated temperatures, and that conventional $POCl_3$ diffusions result in a thick layer of diffusion glass on the sample, which needs to be removed for further processing. Thus with the DOSS simultaneous diffusion technique, one can form a phosphorus emitter, boron or aluminum BSF and grow a thin (or thick) passivating thermal oxide in <u>one</u> furnace processing step, without any detectable cross doping.

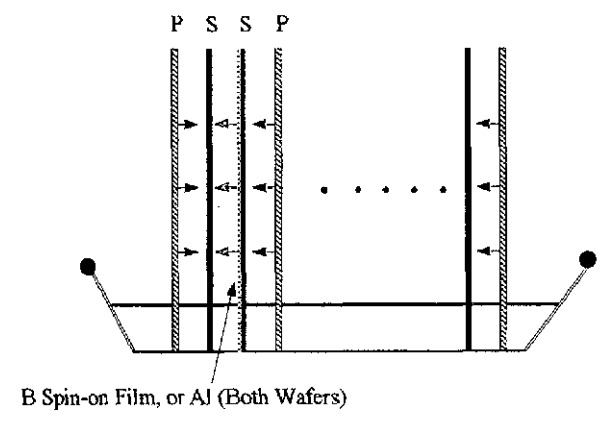


Figure 1. Schematic diagram of solar cell (S) wafer stacking arrangement in DOSS diffusion process, using phosphorus (P) sources, B spin-on film, and Al.

III. Results and Discussion

a. Process Control and Flexibility

The phosphorus solid sources fabricated for the DOSS technique are limited doping sources, which are depleted of P_2O_5 after each diffusion process. A significant advantage of using limited solid doping sources is that one can *tailor* the emitter profiles resulting from sample diffusion by adjusting the concentration of P_2O_5 in the sources. The result is that for a fixed diffusion temperature and time, one can obtain a wide range of sample sheet resistance's by controlling the concentration of P_2O_5 in the phosphorus sources during the source fabrication stage. This is shown in figure 2, in which the (phosphorus diffused) sheet resistance is given as a function of source fabrication conditions, for diffusion temperatures of 950 °C and 1050 °C. The source concentration was tailored by adjusting the flow of nitrogen carrier gas through the $POCl_3$ bubbler during the source fabrication step. The range of sheet resistance values for the 60 min 950 °C diffusion was 59.4-388.4 Ω/□, and for a 60 min 1050 °C diffusion the range of sheet resistance was 33.1-191.2 Ω/□, for a N_2 carrier gas flow range of 200 to 25 sccm. This range of sheet resistance values is quite compatible with commonly used metalization techniques, such as photolithography, screen printing or buried contacts. Work is under way to determine whether the difference in sheet resistance for the 950 °C and 1050 °C diffusions in figure 2 is due to the difference in P_2O_5 vapor pressure over the sources at the two diffusion temperatures, or due to the temperature dependence of the phosphorus diffusion constant. The carrier gas flow rates required to fabricate the phosphorus solid sources used in figure 2 are not excessive, and are in line with conventional $POCl_3$ liquid source diffusions.

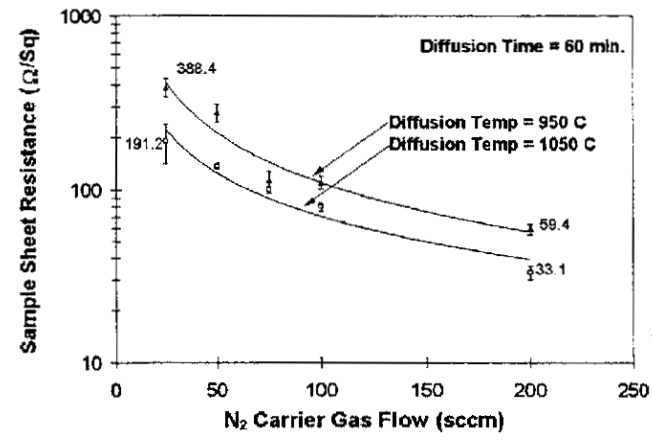


Figure 2. Phosphorus diffused sheet resistance for 950 °C and 1050 °C DOSS diffusions, as a function carrier gas flow through the $POCl_3$ bubbler, during the source fabrication stage.

The thermal cycle for the DOSS simultaneous diffusion process is designed around the need for a deep, heavily doped BSF. This requires the use of relatively high diffusion temperatures, on the order of 1000 °C and long diffusion times, particularly when a deep boron BSF is desired. A typical simultaneous diffusion cycle consists of a 1000 °C diffusion for 60 min followed by 4-5 min oxidation at the diffusion temperature to grow a thin passivating thermal oxide. Using a commercially available boron spin-on film, rated at a concentration of $1(10)^{20}$ cm^{-3}, this thermal cycle produces a boron BSF of 20-25 Ω/□, on both the coated sample and the adjacent uncoated sample (see fig 1). If an infinite-type phosphorus source was used during this thermal cycle, in which the surface concentration was set by the solid solubility (N_s=$1(10)^{21}$ cm^{-3} [2]), this high diffusion temperature would result in a very heavily doped emitter, resulting in a poor short wavelength response. Figure 3 shows the temperature dependence of sample sheet resistance, using constant P_2O_5 concentration sources, over a temperature range of 900 - 1050 °C. Together, figures 2 and 3 show the versatility of the DOSS diffusion process, in which one can use the diffusion temperatures and time necessary to form an effective boron or aluminum BSF, while tailoring the phosphorus diffusion profile over a wide range of sheet resistance by adjusting the P_2O_5 source concentration.

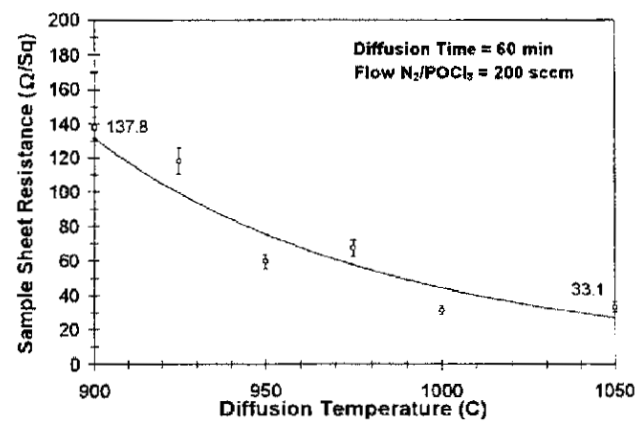


Figure 3. Phosphorus diffused sheet resistance as a function of diffusion temperature, for constant concentration sources.

b. Effectiveness of In-Situ Passivating Oxide

In contrast to conventional phosphorus diffusion sources [2] such as $POCl_3$, ceramic-based solid sources, CVD doped oxides and spin-on sources, the resulting diffusion glass in the DOSS technique is very thin, on the order of 30-40 Å. This allows for the in-situ growth of a thin thermal oxide for surface passivation, without having to remove a thick layer of diffusion glass prior to applying an AR coating. To examine the integrity of this thin in-situ oxide, measurements were made of the emitter saturation current density by the photoconductance decay technique. Figure 4 shows a plot of the inverse effective lifetime, $(1/\tau_{eff} - C_n N^2)$, as a function of injection level, N, for a n^+-i-n^+ sample at three different stages of processing. The base material is 500-1000 Ω-cm Fz silicon, with 70 Ω/□ phosphorus diffusions on each side. The bottom curve of figure 4 is for the in-situ oxide, which was grown during the DOSS diffusion cycle and was measured to be 85 Å thick. The resulting J_o from this 70 Ω/□ diffusion is quite low, giving a value equal to 33.3 fA/cm^2. The in-situ oxide was then removed in a 10% HF solution, rinsed, and left in the air for at least 5 minutes. The J_o for this oxide stripped sample rose by more than an order of magnitude to a value of 355 fA/cm^2, as shown in figure 4, demonstrating that the J_o for this sample is quite sensitive to surface passivation and that the in-situ oxide is quite effective at passivating this emitter. This sample was then cleaned thoroughly, and re-oxidized at 850 °C to grow a 100 Å thick thermal oxide. The re-grown thermal oxide gave essentially the same J_o value of 35.8 fA/cm^2 as for the in-situ oxide case, as indicated by the middle curve of figure 4. These J_o measurements demonstrate that the in-situ oxide grown during the DOSS process is as good as a high quality re-grown thermal oxide.

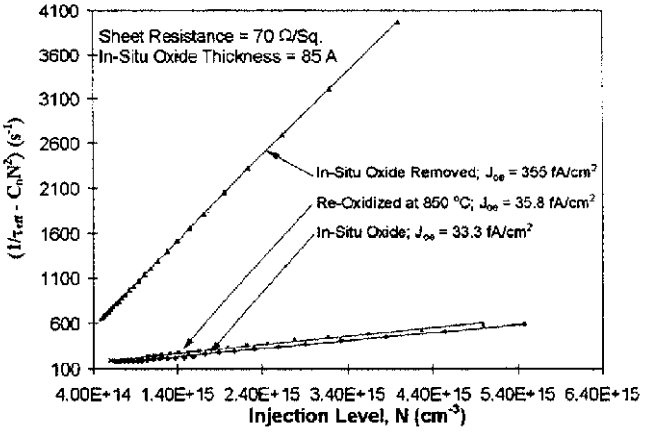


Figure 4. Measurements of Jo by the PCD technique, for the in-situ and re-grown thermal oxide case.

c. Simultaneous B and P Diffused Solar Cells Fabricated by DOSS Technique

Figure 5 shows the internal quantum efficiency, and illuminated I-V data for simultaneous boron and phosphorus diffused solar cells. The 4 cm^2 solar cells in figure 5 were fabricated on 100 mm diameter, 0.6 Ω-cm float zone silicon, with random-pyramid texturing on both sides. The in-situ oxide for the textured wafers was grown to a thickness of 1050-1100 Å for an AR coating, in addition to providing excellent surface passivation. [The measured average weighted reflectance of the in-situ oxide AR coating was less than 6% for both wafers in figure 5.] Cell A had a full aluminum back contact applied after removing the residual boron diffusion glass, while cell B had aluminum point contacts applied [through the boron glass/in-situ oxide] to the full BSF diffusion, which represented 1% of the total area of the back surface. The use of back point contacts to the full p^+ diffusion, enables a back side reflector to be formed by the $Si/SiO_2/Al$ structure. The emitter diffusions on the textured solar cells were performed using textured source wafers, which were tailored to give an emitter sheet resistance in the range of 90-100 Ω/□. The short wavelength response of 96% at 400 nm for cells A and B demonstrate that the in-situ oxide AR coating is very effective at passivating the front surface, given the additional surface area exposed as a result of texturing. The increase in red response for the point contact cell (B) is due to the light trapping provided by the back side reflector as well as oxide passivation of the back surface, leading to an increase in J_{sc} of 0.94 mA/cm^2, and a 2.9 mV increase in V_{oc} over cell A (having a full aluminum back contact). Recent experiments using textured 1.3 Ω-cm

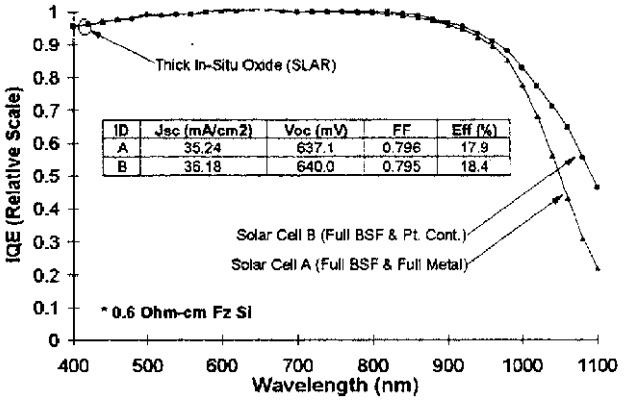


Figure 5. IQE and Light IV measurements for simultaneous B and P diffused (textured) cells incorporating a thick in-situ oxide for surface passivation and SLAR coating.

float zone silicon have produced efficiencies as high as 19.1 % for a simple n^+pp^+ structure employing a full back contact and in-situ oxide AR coating, demonstrating the potential for this new diffusion technique to produce very high efficiency solar cells in a single thermal cycle.

d. Simultaneous Al and P Diffused Solar Cells Fabricated by DOSS Technique

Figure 6 shows the results for a simultaneous aluminum and phosphorus diffused cell, fabricated from untextured 2 Ω-cm float zone silicon. The device in figure 6 had a starting aluminum thickness of 2 μm, and used a phosphorus source which was tailored to give an emitter sheet resistance of 90-110 Ω/□. A thin in-situ oxide was grown for surface passivation, and a ZnS/MgF_2 DLAR coating applied. The resulting J_{sc} of 38.5 mA/cm^2 and V_{oc} of 631 mV demonstrate that the front and back surfaces are well passivated by the thin in-situ oxide and aluminum BSF, and that minority carrier lifetime is not degraded in this 19% simultaneously diffused solar cell. A high back contact resistance problem was encountered in the development of the Al and P diffusion process, which often led to low device fill factors. The high contact resistance is believed to be due to either an insulating layer of Al_2O_3 or an aluminum silicide formed during the 1000 °C diffusion. The problem was solved by a 60 min forming gas anneal at 400 °C, which resulted in a fill factor of 0.79, as shown in figure 6. Future efforts will focus on a lower temperature simultaneous Al and P diffusion, which should prevent the formation of an Al silicide or Al_2O_3.

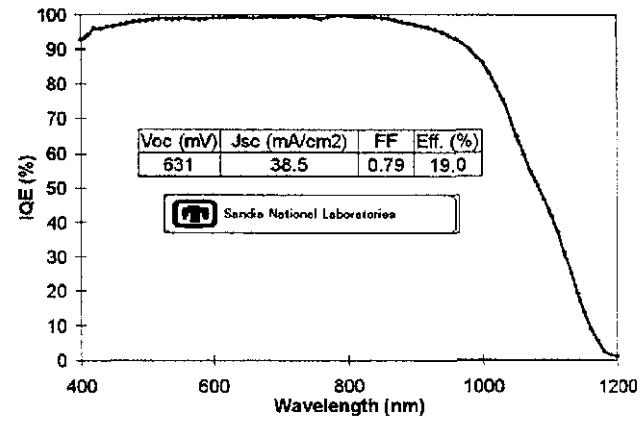


Figure 6. IQE and light IV measurements for simultaneous Al and P diffused cell, with thin in-situ oxide for surface passivation.

A major concern in carrying out simultaneous diffusions in the same furnace is cross contamination. For example, if boron were to diffuse in any part of the emitter region of a cell, it would shunt through the junction, thus destroying the device. In all the simultaneously diffused boron and phosphorus and aluminum and phosphorus cells, we have not seen any evidence of cross doping at the laboratory scale, with the devices displaying very high shunt resistance values in excess of 65,000 Ω-cm^2, and fill factors in the 0.79-0.81 range.

IV. Conclusions

A novel technique is presented to simultaneously diffuse n and p-type dopants in silicon and grow a high quality in-situ thermal oxide, all in one furnace processing step. It is important to recognize that the phosphorus solid sources used in this technique are fabricated in a separate $POCl_3$ diffusion furnace, which allows for new sources to be made in parallel with the simultaneous diffusion process. The result is that the source fabrication step in not a bottleneck to high throughput, since new sources are always available. Measurements of the emitter saturation current density show that the in-situ oxide is just as good as a high quality re-grown thermal oxide, resulting in J_o values in the low 30 fA/cm^2 range. Two approaches to forming a BSF are presented; the first, using a high purity boron spin-on film has produced cells with efficiencies in excess of 19% on textured float zone silicon, with only an in-situ oxide (1050-1100 Å) SLAR coating, the second approach uses evaporated aluminum in place of boron and has produced efficiencies as high as 19 % on untextured float zone silicon. The DOSS diffusion technique can be implemented with any type of crystalline, ribbon or cast multicrystalline silicon, and tailored to be used with any type of contact formation technique including photolithography, screen printing and buried contacts.

V. References

[1] T. Krygowski, P. Sana, G. Crotty, A. Rohatgi, " A Novel Technology for the Simultaneous Diffusion of Boron, Aluminum and Phosphorus in Silicon, Presented at the 25th IEEE PVSC, Washington DC, to be published.

[2] S. K. Ghandhi, "VLSI Fabrication Principles", 2nd Ed., John Wiley & Sons (1994).

Acknowledgments

This work was supported by Sandia National Labs, under contract AO-6162.

Effect of Oxidations on Phosphorus-Diffused Crystalline-Silicon Substrates

James M. Gee*
Sandia National Laboratories
Albuquerque, NM

Richard R. King, Joerg H. Reiss,
and Kim W. Mitchell
Siemens Solar Industries
Camarillo, CA

S. Narayanan
Solarex
Frederick, MD

INTRODUCTION

Phosphorus diffusions are used in the fabrication process for nearly all crystalline-silicon (c-Si) photovoltaic solar cells to form the emitter of the solar cell. These phosphorus diffusions are also well known to have beneficial gettering benefits – i.e., deleterious metallic impurities are gettered from the bulk of the c-Si substrate into the phosphorus doped layer.

In this study, we examined the effect of oxidations performed after the phosphorus diffusion. We were particularly interested in using the oxidation to passivate the surface of the phosphorus diffusion. Post-diffusion oxidations or moderate-temperature steps in oxidizing ambients are also commonly found in commercial fabrication sequences of c-Si solar cells. We found that the bulk lifetime was degraded in Czochralski (Cz) silicon due to the post-diffusion oxidation unless there was a gettering agent present during the oxidation. Possible explanations for these results are presented at the end of the paper.

EXPERIMENT

We performed several experiments to examine the effect of post-diffusion oxidations on bulk lifetime. The starting material included two different batches of 1-Ωcm, p-type Cz silicon. The phosphorus diffusions were performed in different locations (Solarex, Siemens, and Sandia) and with different processes (belt-furnace or tube-furnace diffusions). The oxidations were performed in the Photovoltaic Device Fabrication Laboratory (PDFL) at Sandia National Laboratories. The PDFL maintains control charts to verify high-lifetime processing, and routinely obtains photoconductance decay (PCD) lifetimes over 1 msec for oxidized intrinsic float-zone (FZ) wafers. Cell processing was completed in the PDFL, which included a photolithographically defined, evaporated TiPdAg metallization for the front grid, an evaporated aluminum back contact, and a contact sinter at 400°C in forming gas. The illuminated-IV, dark-IV, hemispherical reflectance, and absolute spectral response of the completed cells were measured. The spectral data were analyzed to determine bulk diffusion lengths and back-surface recombination velocities. Some representative results of these experiments are presented in Fig. 1-3, and in Table 1.

We also examined the susceptibility of Cz silicon solar cells to light-induced degradation (LID) with and without a post-diffusion oxidation. The wafers and cells were processed at Siemens Solar Industries (SSI) for this experiment. LID refers to degradation of bulk diffusion length L due to illumination, and is found primarily in p-type c-Si solar cells with high concentrations of oxygen [1,2]. The bulk diffusion length L was determined by internal quantum efficiency measurements both before light exposure, and after sufficient light exposure to saturate the LID effect. According to a model of LID in which an inactive or less-active recombination center is converted to a state which is more effective at causing recombination, the change in $(1/L^2)$ is proportional to the concentration of these centers that are responsible for LID [2]. Fig. 4 shows the quantity $\Delta(1/L^2)$ for SSI Cz wafers after diffusion only, after diffusion and oxidation, and for finished cells with oxide passivation. These measurements indicate that the post-diffusion oxidation increases the susceptibility of the solar cells to LID.

DISCUSSION

We consistently found a degradation in bulk lifetime due to a post-diffusion oxidation with Cz silicon substrates (Fig. 1-3 and Table 1). This degradation was found with different starting materials and with diffusions performed in different laboratories using very different processes. The presence of aluminum on the back surface during the oxidation completely prevented the bulk lifetime degradation (Fig. 2 and 3, and Table 1), while the presence of TCA during the oxidation was insufficient to prevent the lifetime

*Sandia National Laboratories was supported by the United States Department of Energy under contract DE-AC04-94AL85000.

degradation (Fig. 3 and Table 1). We also found that the susceptibility of Cz silicon solar cells to LID was increased by the post-diffusion oxidation (Fig. 4). Annealing kinetics, degradation by forward biasing, thermal degradation, and other measurements are consistent with Fe-B pair dissociation as the cause of LID [2].

The above results collectively suggest that the interstitial Fe concentration and/or other impurities are increased in the bulk of the solar cell due to the post-diffusion oxidation. These impurities degrade the bulk lifetime unless there is a gettering agent (i.e., aluminum on the back surface) present during the post-diffusion oxidation. Similarly, a higher concentration of metallic impurities due to the post-diffusion oxidation would contribute to the increased susceptibility to LID.

There are several mechanisms that could account for the increase in impurity concentration by a post-diffusion oxidation. These mechanisms include the following: (1) redistribution of the gettered Fe from the phosphorus-doped surface layer; (2) contamination of the wafer during the oxidation; or (3) dissolution of Fe precipitates already present in the bulk. We are currently examining higher concentrations of TCA during the oxidation to help prevent the lifetime degradation during the post-diffusion oxidation.

REFERENCES

1. James M. Gee, **High-Efficiency One-Sun Photovoltaic Module Demonstration Using Solar-Grade Cz Silicon**, final report, CRADA #1248, Sandia National Laboratories, Albuquerque (1996).
2. J. H. Reiss, R.R. King, and K.W. Mitchell, "Characterization of diffusion length degradation in Czochralski silicon solar cells," *Applied Physics Letters* 68, 3302-3304 (1996).

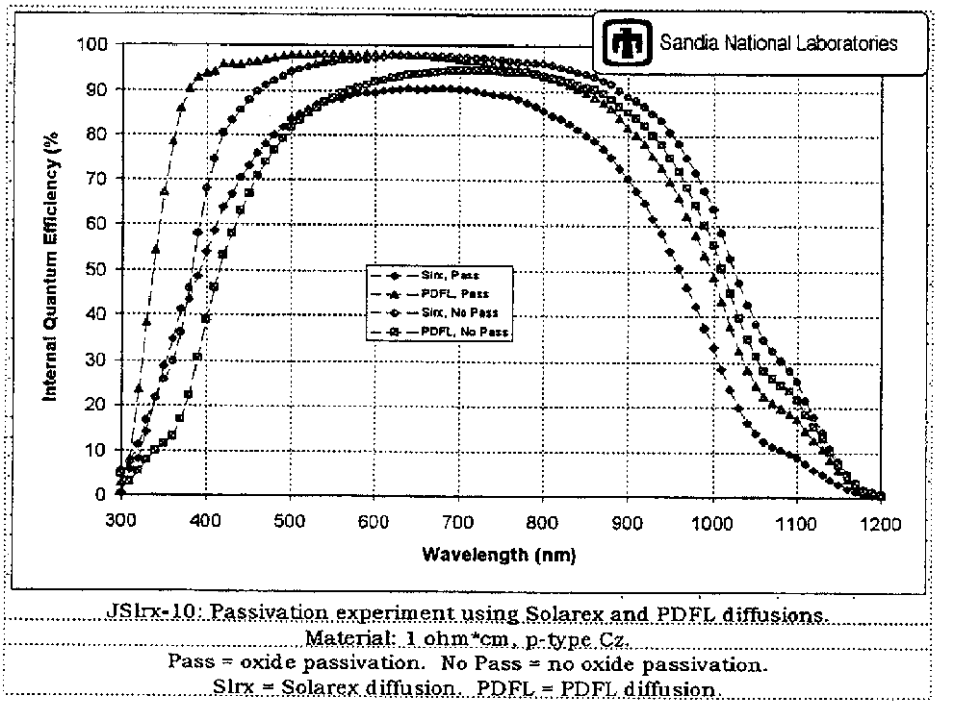
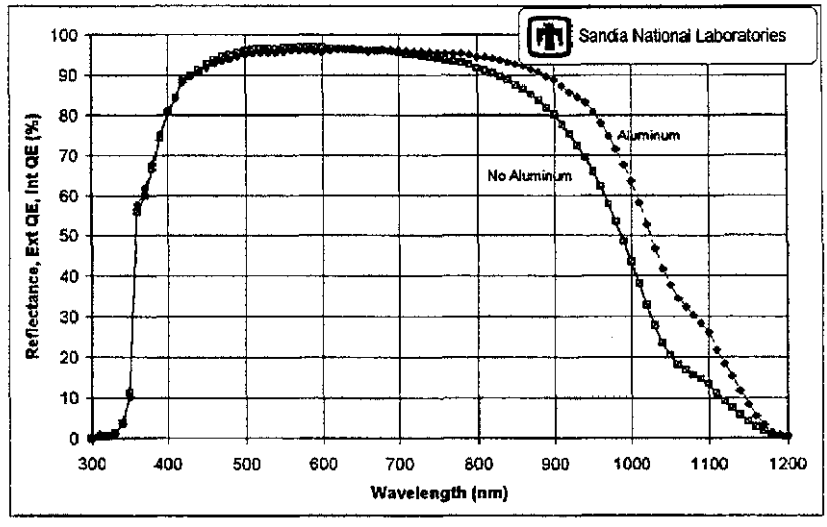
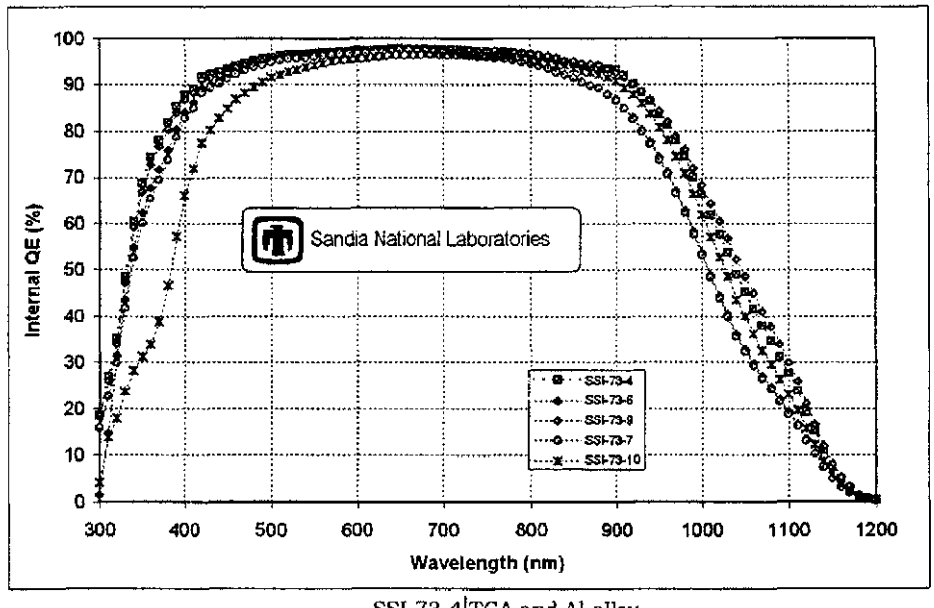


Figure 1. Representative internal quantum efficiency (IQE) spectra of an experiment that compared thermal-oxide passivation of Cz c-Si wafers diffused at Solarex and in the PDFL. The material was 1-Ωcm, p-type Cz silicon with a thickness (640 μm) much greater than the diffusion length. The large thickness means that the effective diffusion length estimated from analysis of the IQE spectra is essentially the same as the bulk diffusion length. The effective diffusion length of the Solarex-diffused wafers decreased from 280 to 80 μm due to the oxidation, while the effective diffusion length of the PDFL-diffused wafers decreased from 220 to 155 μm due to the oxidation.



Lot: JSlrx-13
Split: 15 min, 750C oxidation.

Figure 2. Results of an experiment similar to Fig. 1, except that half of the wafers had aluminum on the back surface during the post-diffusion oxidation, all the wafers were diffused at Solarex, and a variety of oxidation schedules were used (15 to 45 minutes at 750 and 850°C). The effective diffusion lengths for this particular split (15-minute 750°C oxidation) were 117 and 269 μm for the cells without and with aluminum during the oxidation, respectively. The other oxidations exhibited similar trends; i.e., degradation in lifetime unless aluminum was present.



SSI-73-4	TCA and Al-alloy.
SSI-73-6	TCA and no Al-alloy.
SSI-73-9	No TCA and Al-alloy.
SSI-73-7	No TCA and no Al-alloy.
SSI-73-10	Control.

Figure 3. Representative IQE spectra from an experiment that compared oxidations with and without aluminum, and with and without trichloroethane (TCA) during the oxidation. TCA is a source of chlorine during oxidations, which is useful for gettering and preventing contamination during the oxidation. The TCA concentration was equivalent to 2% HCl. The c-Si material was 280-μm 1-Ωcm p-type Cz from Siemens Solar Industries, and the wafers were diffused at Siemens and oxidized in the PDFL. The control cell was not oxidized, and therefore has poor front- and rear-surface passivation. Table 1 presents estimates of L and S for these cells.

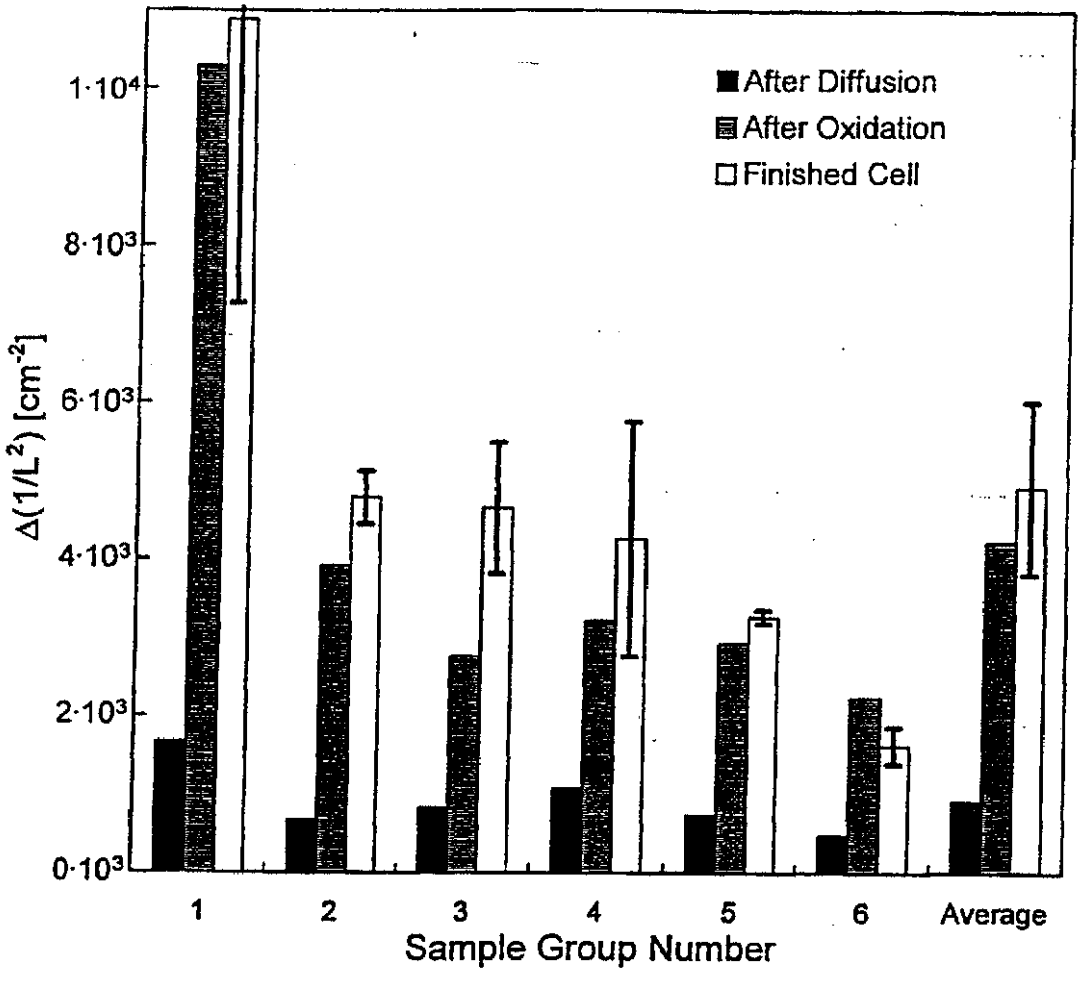


Figure 4. Change in concentration of recombination centers due to light-induced degradation of Cz silicon solar cells after a diffusion, after diffusion plus oxidation, and in complete cells that have both the diffusion and oxidation. "Sample Group" refers to a set of substrates from different portions of the ingot, and the error bars refer to the standard deviation of the group of cells.

Table 1. Summary of analysis of IQE data of Fig. 3. L_{eff} and η_c are the effective diffusion length and the internal collection efficiency for uniform photogeneration, and are derived from analysis of the IQE spectra. L and S are the bulk diffusion length and back-surface recombination velocity, and are estimated from L_{eff} and η_c. Back refers to the percentage recombination at the back surface at open circuit. Note that the analysis becomes insensitive to L or to S when L is much greater than the device width or when S if much greater than the diffusion velocity (D/W), respectively. W is the device thickness, and is equal to 280 μm.

Cell Name	TCA	Alum	L_{eff} μm	η_c %	L μm	S cm/s	Back %
SSI - 73 - 10	Cntrl		280	49	>>W	$>10^6$	89
SSI - 73 - 7	N	N	157	39	164	$3.7*10^5$	35
SSI - 73 - 9	N	Y	333	59	664	4101	83
SSI - 73 - 6	Y	N	163	40	177	$4.1*10^5$	39
SSI - 73 - 4	Y	Y	397	54	>>W	4165	85

Self-Aligned Selective Emitter Plasma-Etchback and Passivation Process for Screen-Printed Silicon Solar Cells

D. S. Ruby[1], C. B. Fleddermann[2], M. Roy[3] and S. Narayanan[3]
[1]Sandia National Laboratories, Albuquerque, NM 87185-0752
[2]University of New Mexico, Albuquerque, NM 87131
[3]Solarex (a business unit of Amoco/Enron Solar), Frederick, MD 21701

Abstract

Plasma-enhanced chemical vapor deposition (PECVD) is now widely recognized as a potentially cost-effective, performance-enhancing technique that can provide surface passivation and produce an effective antireflection coating layer at the same time. In order to gain the full benefit from improved emitter surface passivation on cell performance, it is necessary to tailor the emitter doping profile so that the emitter is lightly doped between the gridlines, but heavily doped under them. This is especially true for screen-printed gridlines, which require very heavy doping beneath them for acceptably low contact resistance. This selectively patterned emitter doping profile has historically been obtained by using expensive photolithographic or screen-printed alignment techniques and multiple high-temperature diffusion steps. We have built on a self-aligned emitter etchback technique first described by Spectrolab. In addition to the gridline-masked, plasma-etchback of the emitter they developed, we have included PECVD-nitride deposition because the low-recombination emitter produced by the etchback requires good surface passivation for improved cell performance. The nitride also provides a good antireflection coating and can be combined with plasma-hydrogenation treatments for bulk defect passivation.

We studied whether plasma-etching techniques can use standard screen-printed gridlines as etch masks to form self-aligned, patterned-emitter profiles on multicrystalline (mc-Si) cells from Solarex Corp. We conducted an investigation of plasma deposition and etching processes on full-size mc-Si cells processed in commercial production lines, so that any improvements obtained would be immediately relevant to the PV industry.

This investigation determined that reactive ion etching (RIE) is compatible with using standard, commercial, screen-printed gridlines as etch masks to form self-aligned, selectively-doped emitter profiles. This process results in reduced gridline contact resistance when followed by PECVD treatments, an undamaged emitter surface easily passivated by plasma-nitride, and a less heavily doped emitter between gridlines for reduced emitter recombination. This allows for heavier doping beneath the gridlines for even lower contact resistance, reduced contact recombination, and better bulk defect gettering. Our initial results found a statistically significant improvement of about half an absolute percentage point in cell efficiency when the self-aligned emitter etchback was combined with the PECVD-nitride surface passivation treatment. Additional improvement is expected when the successful bulk passivation treatment is also added to the process.

Introduction

The use of plasma-enhanced chemical vapor deposition (PECVD) as a low-temperature surface passivation technique for silicon solar cells is a topic of increasing

This work was supported by the U.S. Department of Energy under contract DE-AC04-94AL85000.

importance. PECVD is now widely recognized as a potentially cost-effective, performance-enhancing technique that can provide surface passivation and produce an effective antireflection coating layer at the same time [1]. For some solar-grade silicon materials, it has been observed that the PECVD process results in the improvement of bulk minority-carrier diffusion lengths as well, presumably due to bulk defect passivation [2].

In order to gain the full benefit from improved emitter surface passivation on cell performance, it is necessary to tailor the emitter doping profile so that the emitter is lightly doped between the gridlines, but heavily doped under them [3]. This is especially true for screen-printed gridlines, which require very heavy doping beneath them for acceptably low contact resistance. This selectively patterned emitter doping profile has historically been obtained by using expensive photolithographic or screen-printed alignment techniques and multiple high-temperature diffusion steps [3,4].

We have attempted to build on a self-aligned emitter etchback technique first described by Spectrolab [5]. In addition to the gridline-masked, plasma-etchback of the emitter they developed, we have included plasma-hydrogenation treatments for bulk defect passivation followed by PECVD-nitride deposition for surface passivation and antireflection coating.

Experimental Procedure

The plasma-nitride depositions were performed using a modified Pacific Western Coyote PECVD reactor. This is a commercial, RF parallel-plate reactor operating at 13.56 MHz with large batch-size and high-throughput potential. Reaction gases for nitride deposition were a 3% mixture of silane in nitrogen and pure ammonia.

These cells were made using Solarex cast multicrystalline silicon and received Solarex's standard production line processing through the printing and firing of the gridlines. Then, the cells underwent reactive ion etching (RIE) for 3 minutes to increase the sheet resistance of the emitters to 80-100 ohms/square. They were plasma-etched in a Technics PE II-A reactor using pure SF_6 at a power of 10W and a pressure of 100 mTorr. Then, the cells received either an ammonia-plasma hydrogenation (H-passivation) treatment or a silicon-nitride deposition (PECVD-nitride), both found to be effective for bulk and surface passivation in String Ribbon™ mc-Si [2]. They were then returned to the Solarex production-line for final cell processing.

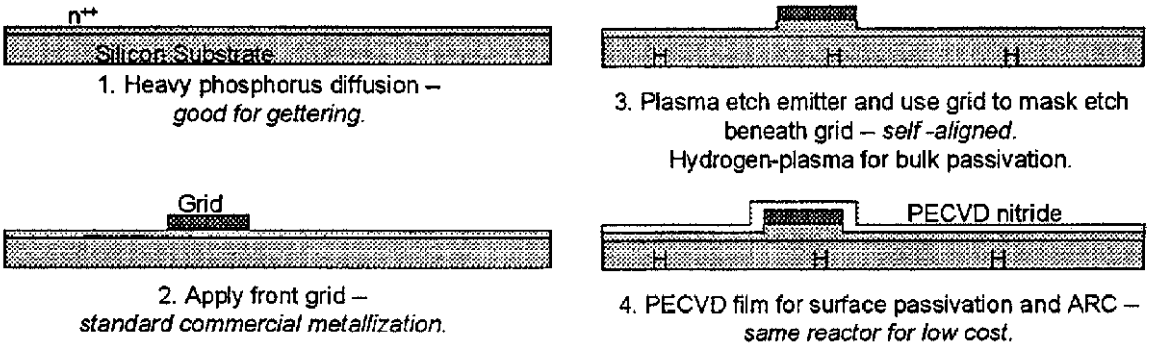


Figure 1. Process sequence for self-aligned emitter etchback. The emitter etchback can be performed after the hydrogen-plasma treatment to remove surface damage. However, in this work, the plasma-etching was done first.

Results

Table 1. Four processing sequences were applied to twelve 102.6-cm^2 Solarex mc-Si cells using matched material from the same ingot and in most cases with the same grain structure.

Eff. (%)	I_{SC} (A)	V_{OC} (mV)	FF (%)	R_S (mΩ)
Group 1. Control Cells: No emitter etchback, TiO_2 ARC				
12.6±0.1	2.91±.02	586±1	75.5±0.7	9.2±0.5
Group 2. Plasma Etchback, TiO_2 ARC				
12.2±0.1	2.93±.02	580±1	73.4±0.4	15.0±1.0
Group 3. Plasma Etchback, H-passivation, TiO_2 ARC				
12.8±0.3	2.97±.02	585±1	75.4±1.5	10.7±0.5
Group 4. Plasma Etchback, PECVD-nitride ARC, FGA				
13.0±0.1	3.00±.01	587±1	75.3±0.2	10.7±0.5

The cells from Group 2 suffered an efficiency loss due primarily to loss of V_{OC}, as expected, since the etched-back emitter is now transparent to minority carriers, which now recombine at the unpassivated front surface. An additional loss in FF is due to the increase in series resistance because of the extra sheet resistance of the etched-back emitter. In an optimized sequence, the cells would have more closely-spaced gridlines to compensate for this. In addition, an extra-heavy emitter doping could be performed, possibly resulting in additional gettering of bulk impurities, which could then be etched away. Also, heavier doping under the gridlines would better isolate them and reduce contact recombination. Finally, the heavier doping would also reduce the contact resistance that often limits screen-printed cell performance. The lack of current loss in these cells indicates that any increase in surface recombination is compensated for by reduced emitter recombination in the now lightly doped emitter.

The Group 3 cells have regained most of the V_{OC} loss, probably due to the compensating effect of reduced bulk recombination from the hydrogenation treatment. Interestingly, this is accompanied by a reduction of the series resistance, which is in agreement with observations by Wenham et al., who attributed this to a decrease in the contact resistance of the screen-printed gridlines [7]. This, in combination with the benefits of heavier emitter doping mentioned above, would address many of the shortfalls that have been ascribed to the screen-printing process.

The cells from Group 4 have totally regained their initial V_{OC} values and show a significant 3% gain in I_{SC} now that the surface of the transparent emitter is passivated by the nitride film. The effect of the plasma-nitride deposition on reducing the gridline contact resistance is still apparent, resulting in an overall average increase in efficiency of almost half an absolute efficiency point. Even better results are expected when the nitride passivation is combined with bulk hydrogenation and the benefits of heavy emitter doping.

Internal quantum efficiency curves of typical cells from Groups 1, 3, and 4 are shown in Figure 2. LBIC scans showed that the cells from Group 2 did not have the same grain structure as the others, and so it was not possible to find the same "median" grain from cells of Group 2 on which to measure the IQE.

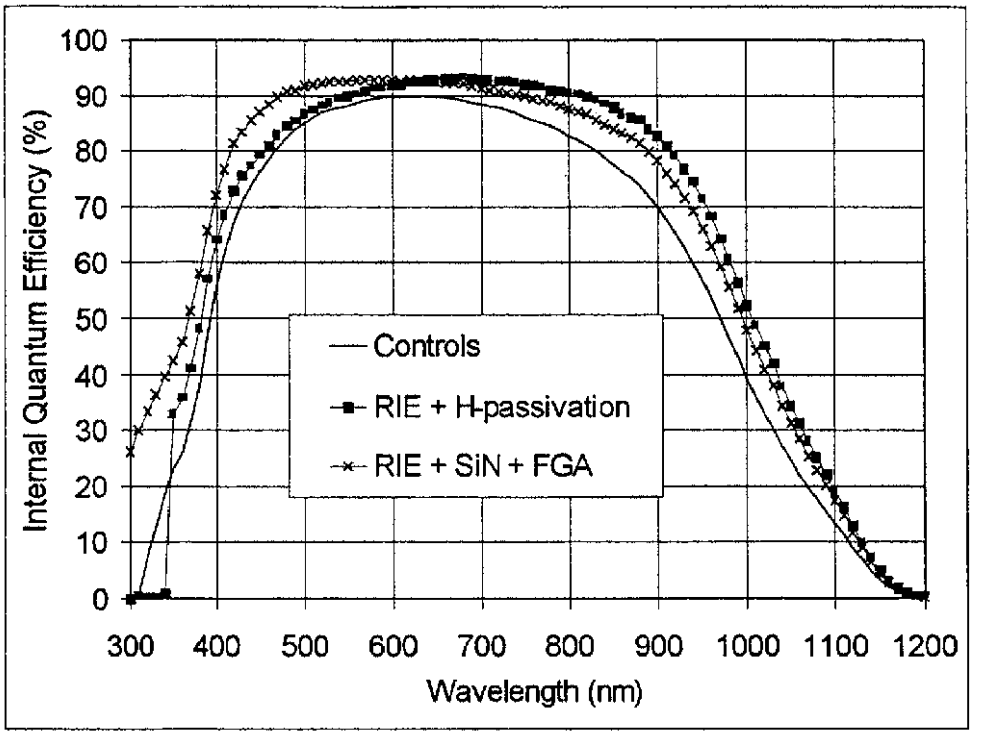


Figure 2. IQE curves of three Solarex cells representative of Groups 1, 3, and 4 described in Table 1.

The IQE curves show that while both plasma treatments increased the red-response relative to the control cell, the NH_3-hydrogenation treatment had the biggest effect. It is also clear that the nitride-ARC resulted in the best blue response due to its better passivation of the emitter surface. In fact, the IQE(400-nm) value (73%) is almost as high as that obtained previously on this material (78%) using a nitride coating optimized for low surface recombination [6]. This shows that the RIE process may not have damaged the emitter surface significantly, if at all.

Conclusions

This investigation determined that RIE is compatible with using standard, commercial, screen-printed gridlines as etch masks to form self-aligned, selectively-doped emitter profiles. This process results in reduced gridline contact resistance, an undamaged emitter surface easily passivated by plasma-nitride, and a less heavily doped emitter between gridlines for reduced emitter recombination. It allows for heavier doping beneath the gridlines for even lower contact resistance, reduced contact recombination, and better bulk defect gettering. Future work in this area will incorporate the heavier emitter doping as well as performing the bulk hydrogenation before the RIE step so that surface damage from the bulk passivation step can be removed or reduced. This will be compared with the use of a protective nitride film before hydrogenation. Finally, all three plasma processes, the bulk passivation, emitter etchback, and nitride surface passivation, will be combined for the synergistic additive effect of their benefits.

Acknowledgements

The authors would like to thank J. M. Gee for initially suggesting the self-aligned emitter etchback concept, and W. K. Schubert for his help in this area. We are also grateful to the processing staff at Sandia's PDFL and the Solarex production line for the cell processing. Many thanks also go to L. Irwin for the cell measurements.

References

[1] Z. Chen, P. Sana, J. Salami, and A. Rohatgi, "A Novel and Effective PECVD SiO2/SiN Antireflection Coating for Si Solar Cells," *IEEE Trans. Elect. Dev.*, **40**, June 1993, pp. 1161-1165.

[2] D.S. Ruby, W.L. Wilbanks, C.B. Fleddermann, and J.I. Hanoka, "The Effect of Hydrogen-Plasma and PECVD-Nitride Deposition on Bulk and Surface Passivation in String-Ribbon Silicon Solar Cells," *Proc. 13th EPSEC*, October 1995, pp. 1412-1414.

[3] A. Blakers et al., "22.8%-Efficient Silicon Solar Cell," *Appl. Phys. Lett.* **55**, 1989, pp. 1363-1395.

[4] J. Coppye et al., "Non-Conventional Emitters for Polycrystalline Silicon Solar Cells," *Proc. 10th EPSEC*, April 1991, pp. 657-660.

[5] N. Mardesich, "Solar Cell Efficiency Enhancement by Junction Etching and Conductive AR Coating Processes," *Proc. 15th PVSC*, May 1981, pp. 446-449.

[6] D.S. Ruby, W.L. Wilbanks, and C.B. Fleddermann, "A Statistical Analysis of the Effect of PECVD Deposition Parameters on Surface and Bulk Recombination in Silicon Solar Cells," *Proc. 1st WCPEC*, Dec. 1994, pp. 1335-1338.

[7] S.R. Wenham, M.R. Willison, S. Narayanan, and M.A. Green, "Efficiency Improvement in Screen-Printed Polycrystalline Silicon Solar Cells by Plasma Treatments," *Proc. 18th PVSC*, Oct. 1985, pp. 1008-1013.

ULTRASOUND TREATMENT (UST) DEFECT ENGINEERING IN SILICON-BASED MATERIALS

S. Ostapenko

Center for Microelectronics Research, University of South Florida, Tampa, FL 33620

UST technology is designed to benefit defect diagnostics and processing in poly-silicon wafers, thin films and devices. It is based on non-contact generation of low-amplitude ultrasonic vibrations into poly-Si as shown schematically in Fig.1. Computer-controlled UST station is designed for processing of large-scale wafers and devices by delivery a quasi-homogeneous distribution of UST amplitudes at temperatures up to 150°C. The station is suitable for treatment of 4"x4" wafers and can be easily scaled up to 14" diagonal by adding ultrasound transducers. A computer controls "in-situ" and adjusts UST parameters (amplitude, frequency, and temperature) operating in a feedback loop with non-contact UST probe and non-contact temperature sensor (Fig.1).

UST processing of poly-Si thin films on glass. The UST effect in plasma hydrogenated poly-Si thin films was manifested by a dramatic reduction (by *two orders* of magnitude) in sheet resistivity (Fig.2) and was accompanied by a substantial improvement of film electrical homogeneity. This strong UST effect is due to ultrasonic enhanced hydrogenation of grain boundary dangling bonds in poly-Si film, which is critical for high performance applications. UST increase of photoluminescence efficiency in poly-Si films confirmed the enhanced passivation of non-radiative defects. Nano-scale contact potential voltage AFM mapping in poly-Si films prior to and after UST proved that UST effect is grain boundary related [1]. A utility of UST processing in amorphous Si films is also shown. A new mechanism of ultrasound stimulated hydrogenation of dangling bonds is proposed: UST promotes a liberation of trapped atomic hydrogen due to a selective absorption of ultrasound at grain boundaries, dislocations, and other extended defects. This is following by a fast hydrogen diffusion and capturing at dangling bonds. It is suggested that UST can benefit hydrogenation of dangling bonds in poly-Si and hydrogenated amorphous Si solar cells.

UST defect diagnostics. Polycrystalline PV silicon contains a high density of point defects and extended defects exhibiting a complex interaction with each other. We reported previously a strong UST improvement by a factor of 3 to 10 of minority carrier diffusion length (L) in low-L regions [2]. It was suggested that heavy metal contaminations (Fe and Cr) can be affected with UST. To gain a fundamental understanding of relevant mechanisms, UST was applied to Cz-Si intentionally doped with Fe or Cr. UST vibrations activate a dissociation-association defect reactions of Fe-B and Cr-B pairs in p-type Si. These findings offer a new mean of heavy metal characterization in Si-based materials using UST defect engineering.

This work is partially supported by NREL contract #XD-2-11004-5.

References

1. Ostapenko S., L.Jastrzebski, J.Lagowski and R.Smeltzer, "Enhanced Hydrogenation by Ultrasound Treatment in Polycrystalline Silicon Thin Films", APL (1996), **68,** 2873.
2. Ostapenko S., L.Jastrzebski, and B.Sopori, "Change of Minority Carrier Diffusion Length in Poly-Si by UST", Semicond. Sci.Technol (1995), **v.10**, 1494.

Fig.1 Schematic of UST Unit

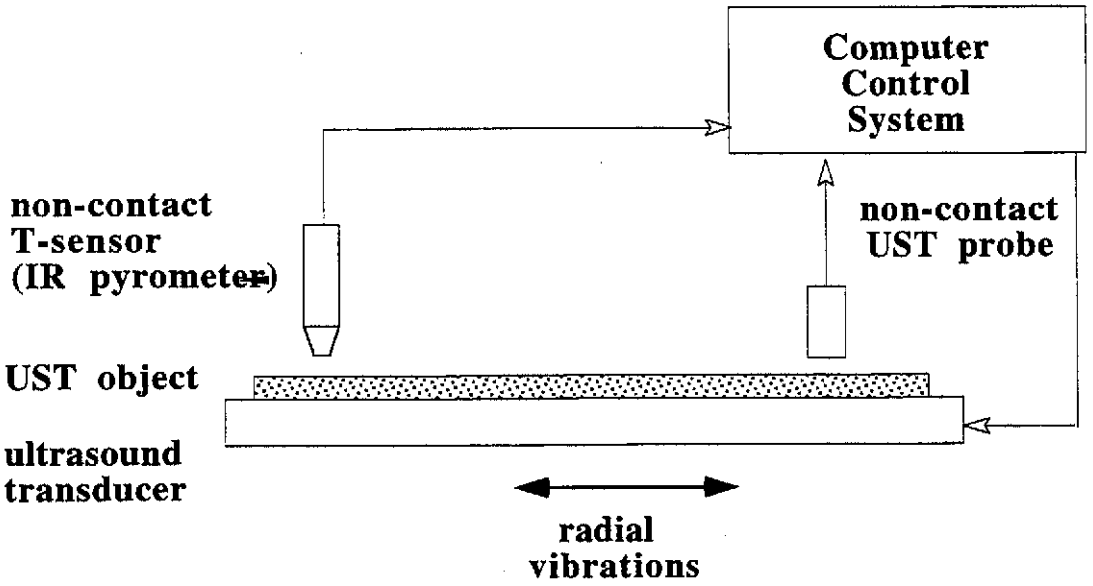
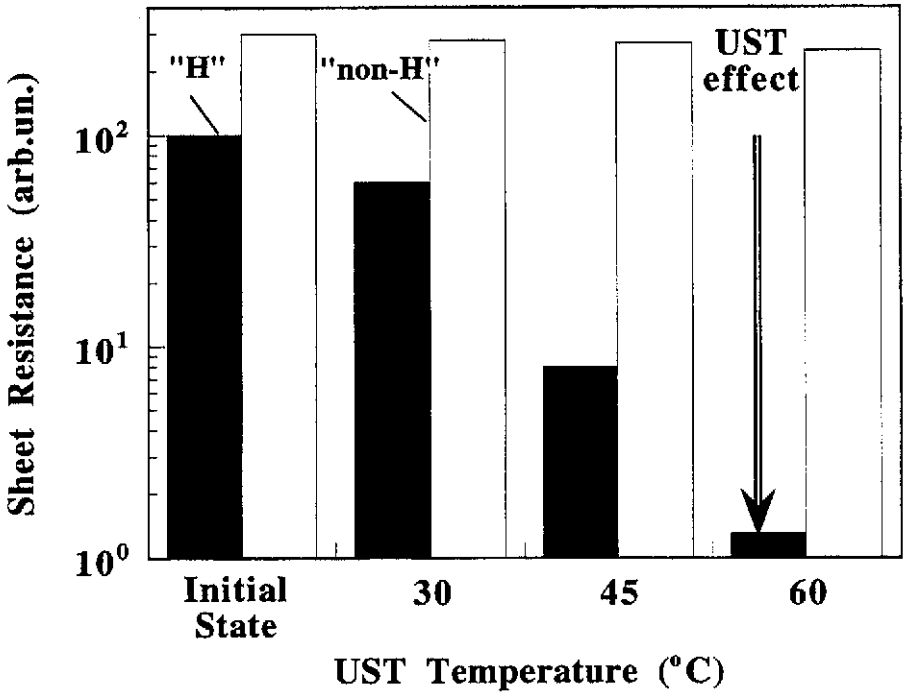


Fig.2 UST Enhanced Hydrogenation in Polysilicon Thin Films on Glass



Copper gettering in silicon studied by transient drift analyses.

T.Heiser and E.R.Weber
Department of Material Science and Mineral Engineering
University of California at Berkeley, Lawrence Berkeley National Laboratory
1, cyclotron road
Berkeley, Ca 94720

ABSTRACT

Copper is known to be the fastest diffusing impurity in silicon. The correspondingly high diffusion coefficient, together with its large solubility at high temperature, makes copper one of the major contaminants introduced during device processing. However, relatively few gettering studies have been performed on copper, compared to the large number of publications on iron gettering in silicon. This is mainly due to the high diffusivity of interstitial copper at room temperature and to the absence of analytical tools to measure low concentrations of copper in silicon. The highly sensitive deep level transient spectroscopy is well suited to detect traces of iron in silicon, as this impurity introduces well defined deep levels in the silicon band gap.[1] Several deep levels have also been attributed to copper in silicon.[2,3,4] However, the microscopic states which give rise to those levels are still unclear, and no simple relationship exists between the concentration of these levels and the total amount of Cu atoms present in the crystal.

Recently, a drift technique, called transient ion drift (TID), was developped by one of the authors to study the diffusion behaviour of interstitial copper around room temperature.[5,6] It is shown in this work that this technique gives us the opportunity to detect low concentrations of copper in silicon. The method is applied to internal gettering studies, and compared to a previous study on iron gettering.

The method is based on the capacitance change of a Schottky barrier induced by a charge redistribution in the depletion layer. In this case, the redistribution is due to drift of positively charged interstitial copper ions (or Cu_i^+) in the strong electric field of the reverse biased Schottky barrier. If a pulsed bias is applied to the barrier, the ion distribution is changed periodically, each drift process in the newly depleted region (during high reverse bias) being followed by a thermal diffusion process (low reverse bias).[5,6] The drift process gives rise to a capacitance transient which can be analysed in a similar way as are deep level carrier emission induced capacitance transients. A relatively low concentration of interstitial copper can so be detected.

In order to detect low amounts of copper impurities in silicon with this technique, the ratio of interstitial copper over total copper concentration has to be maximised. We started measuring the amount of Cu_i , after copper indiffusion at different temperatures. A sputtered copper layer was used as a source of Cu atoms. Each sample was first annealed at 800C,for 1/2 hour, a temperature high enough to avoid the in-diffusion barrier of native oxyde, followed by a second anneal at a lower temperature. The samples were finally quenched into ethylen glycole in order to avoid precipitation of copper atoms during cool down. Al-doped silicon was used, as previous measurements have shown that Cu_i are more stable in this material compared to B-doped silicon.[5,6] This behaviour has been attributed to a stronger binding energy of the Al-Cu_i pairs compared to the B- Cu_i pairs. Enhanced stability avoids room temperature precipitation of Cu_i during Schottky barrier preparation.

As expected, the Cu_i concentration measured by TID after annealing and quenching, is strongly dependent on the second anneal temperature. As shown on Fig.1, for temperatures lower than 600C, the data matches closely the solubilility limit of copper in silicon, having a pure Cu metal layer as boundary condition.[1] Hence, the quenching step is fast enough to avoid significant Cu_i precipitation for temperatures lower than 600C. Moreover, as precipitation is triggered by a supersaturation, negligible precipitation should occur after an anneal at even higher temperatures if the total amount of Cu does not

occur after an anneal at even higher temperatures if the total amount of Cu does not exceed the solubility at 600C.

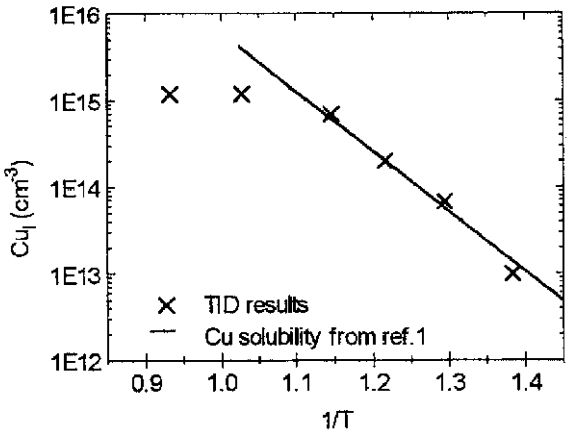


Fig.1: Cu_i concentration measured by TID after 2 step annealing. Samples were Al-doped Si, with N_{al}=1.5 $10^{15}cm^{-3}$.

Next, we applied the technique to internal gettering studies of Cu in silicon. We used a similar approach as has been used by D.Gilles et.al. on iron gettering studies.[7] The samples were submitted to a nuleation step of O-precipitates at 700C for various duration, followed by a second anneal at 1050C for O-precipitate growth. Finally, Cu was indiffused at 800C for 30 minutes and followed with quenching to room temperature.
The as-quenched Cu_i concentration is plotted in fig.2, compared to the results obtained by D.Gilles et al[7] on iron gettering.

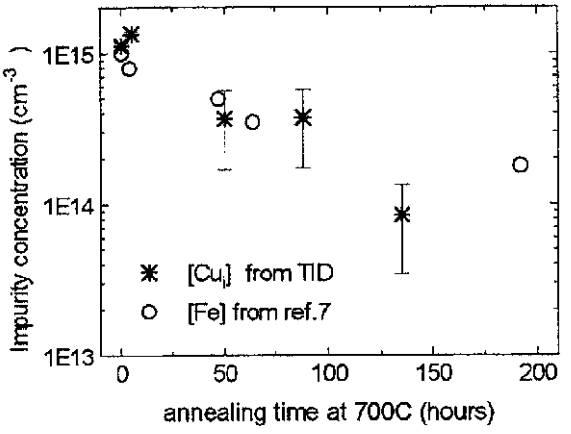


Fig.2: Dependence of the as quenched Cu and Fe concentration on the preannealing time at 700C

A decrease of the Cu as quenched concentration with increasing preannealing time is found , which is similar to what has been observed for Fe in ref.7. The gettering efficiency seems to behave similarly with increasing annealing time for both impurities. However, while the as-quenched concentration of Fe could be correlated to room temperature precipitation kinetics, no such correlation was found for Cu. This may signify that different precipitation sites are responsible for both impurities. However, in the case of Cu, the as-quenched concentration without preannealing, is already lower than the solubility at the annealing temperature. A significant amount of Cu has precipitated 'homogeneously' (i.e. not on the intentionaly introduced gettering sites) during the quenching , forming nucleation sites for further room temperature precipitation. These sites might dominate the room temperature precipitation kinetics, leading to the absent correlation discussed above.

Futur work will be based on controlled contamination of internally gettered Si avoiding the high supersaturation that occured in the present measurements. Characterization of different gettering techniques with the TID method are currently investigated.

references:

[1]E.R.Weber, Appl. Phys. **A 30**, 1 (1983)

[2]S.J.Pearton and A.J.Tavendale, J.Appl. Phys. **54** ,1375 (1983)

[3]H.Lemke, Phys.Stat.Sol.(a) **95**, 665 (1986)

[4]S.D.Brotherton, J.R.Ayres and A.Gill, J.Appl. Phys. **62**, 1826 (1987)

[5]T.Heiser and A.Mesli, Appl. Phys. **A 57**, 325 (1993)

[6]A.Zamouche, T.Heiser, and A.Mesli. Appl. Phys. Lett. **66**, 631 (1995)

[7]D.Gilles and E.R.Weber, Phys. Rev. Lett. **64**, 196 (1990)

Double Gettering Solar Grade Silicon Materials using Aluminum and Titanium.

A. Karoui*, A. Romanowski, Q. Zhang.

North Carolina State University-Department of Materials Sciences & Engineering , Raleigh, NC 27 695 - 7916
*: Fulbright grant recipient, Permanent address: Institut National de Recherche Scientifique et Technique, PoBox 95 Hammam Lif 2050 - TUNISIA Fax: 216 (1) 430 934.

Polycrystalline silicon is one of the materials featuring the highest efficiency-cost ratio. However, the diffusion length and the minority carrier lifetime are compromised by the grain boundaries and other defect activity. We are designing a central part of a new solar cell fabrication process that will use a double gettering procedure. It provides, indeed, a frontal gettering surface and an antireflective coating ARC [1], as well as a rear gettering surface, an electrical pre-contact and a BSF. The two gettering sources do not interact, since they are on opposite sides of the wafer and then act complementarily on different impurities. The gettering surfaces are deposited by sputtering a titanium layer on the front side, and an aluminum layer on the back side of the sample.

To monitor the gettering process we are measuring the lifetime by LMPCD. Since the getters are intended to act on each surface independently, we have investigate them separately. Different base materials are used for these investigations: solar grade polycrystalline p-Si - ρ = 0.5-5 Ωcm from Wacker Heliotronics (a) solar grade tri-crystal p-Si ρ = 9 Ωcm of Helios Tech.(b) and reference samples with known oxygen concentration [O_i= 10^{12}] and doping concentration 10^{15} cm^{-3} (c). For the frontal gettering we are using low resistivity n type silicon and shallow P-N junction on solar grade p-type silicon. The metal layers are sputtered and then annealed in forming gas atmosphere.

Recombination lifetime has been improved by each of these treatments. For aluminum treated samples, the carrier lifetime of tri crystal samples (b) increases from 7 µs to 23 µs (resp. 11 µs) when annealed at 400 °C during 300 min (resp. 600 °C during 80 min) whereas the samples (c) change their lifetime from 1.5 µs to 8.5 µs (respectively to7.5 µs) when annealed at 400 C (respectively 600 °C). Also an increase of lifetime has been observed when samples of type (c) are treated by titanium. They change indeed from 1.5 µs to 10 µs (resp. to 9 µs) when these samples are annealed in 400 C (resp. 600 °C) in forming gas atmosphere during the same time as previously.

The gettering has improved the lifetime and the 400 °C annealing temperature seems to gives the best results for either frontal and the rear getter. Also the tri-crystal has shown a higher aluminum gettering ability for samples cut in regions having a mosaic structure as revealed by X-ray topography.

References:

[1] G.Crotty, T. Daud, and R. Kachare, Front surface passivation of silicon solar cells with antireflection coating, J. Appl. Phys. 61 (8), p.3077 15April1987.

[2] W. K. Schubert, Multicrystalline silicon solar cells: gettering optimization and characterization. 23rd IEEE photovoltaic specialist conference, Louisville, KY May 10,1993.

[3] K. Leo, R. Schindler, J. Knobloch, and B. Voss, Titanium gettering in silicon: Investigation by deep level transient spectroscopy and secondary ion mass spectroscopy., J. Appl. Phys. 62 (8), p.3472 15 October 1987.

POROUS SILICON GETTERING

P. Menna,* Y.S. Tsuo, J.R. Pitts, K.R. Jantzen, S.E. Asher, M.M. Al-Jassim, and T.F. Ciszek
National Renewable Energy Laboratory, 1617 Cole Blvd., Golden, Colorado 80401, USA
* ENEA-Centro Ricerche Portici, Localite Granatello 80055, Portici, Italy

The objective of this study is to develop a low-cost, high-temperature, epitaxial substrate for polycrystalline silicon thin-film growth. Our approach is to make such a substrate by using a novel porous-silicon gettering method to create low-impurity layers on both surfaces of a metallurgical-grade silicon (MG-Si) wafer. The novel porous-silicon gettering method involves a simple stain etching for generating a porous silicon layer on both surfaces of the MG-Si wafer and a high-temperature (1000°C) annealing step using a high-flux solar furnace (HFSF). The porous silicon layers are removed, along with the gettered impurities, after gettering. If the subsequent epitaxial thin-film silicon growth is done on this substrate at a temperature lower than the annealing temperature, then the low-impurity layers can serve as diffusion barriers to prevent impurities in the bulk of the MG-Si substrate from contaminating the film.

Using electrochemically etched porous silicon to getter impurities and other defects in electronic-grade silicon has been studied previously using conventional furnaces [1-4]. The significant increase of the surface area achieved with the porous silicon (nearly 600 m^2/cm^3), as well as the larger lattice parameter of porous silicon compared with that of bulk Si, greatly enhance the probability of tying up the contaminants during the annealing step. Recent studies of enhanced impurity gettering by nanometer-scaled cavities in silicon also indirectly confirmed that porous silicon should provide effective gettering sites [5,6]. These studies showed that metallic contaminants react with Si dangling bonds present on the internal surface of the nanometer-scale voids created within Si crystals. The resulting cavity-trapped impurity states of the metal are more stable than the silicide phase. For instance, the binding energy of Cu within the cavity traps is 0.5 eV larger than in the Cu_3Si phase.

The intense incoherent light irradiation in a HFSF may also enhance the diffusion of metallic impurities. In a study using an artificial light source, Borisenko and Dorofeev [7] showed that intense photoelectronic excitations caused by light absorption generate excess impurity interstitials in the surface layer. This enhances the diffusivity of impurities, because the diffusion of interstitial metallic atoms is an order of magnitude faster than that of substitutional atoms [8].

The MG-Si used for this study was prepared by directional solidification casting. Wafer-sawing damage was chemically removed using an HF and HNO_3 solution before porous-silicon etching. A simple and low-cost chemical etching, using an HNO_3/HF (1:100) etching solution, is used to generate porous silicon layers on both front and back surfaces of the silicon wafers. A high-flux solar furnace available at NREL is used to provide high-temperature annealing, which typically takes 15 to 30 min. at a sample temperature of 1000°C. The porous-silicon gettering sites, along with the gettered impurities, can be easily removed by oxidation followed by a HF dip or a silicon chemical etch. Each porous-silicon gettering process removes up to about 10 μm of wafer thickness. This gettering process can be repeated so that the desired purity level is obtained.

SIMS depth-profiling measurements done from the front (illuminated) and back surfaces of the MG-Si wafers showed that the HFSF annealing treatments caused impurities in the bulk of the wafers to diffuse and segregate at the porous-silicon-etched surfaces. The effectiveness of this impurity gettering process increases with the HFSF treatment time. Strong gettering effects were observed for Al, B, Fe, Cu, and Cr impurities.

To heat a Si wafer in a HFSF to 1000°C, we need concentrated sunlight of about 40 W/cm^2. Such intense illumination can increase the ratio of interstitial impurities over substitutional impurities [7]. The diffusion of interstitial impurities is faster than substitutional impurities, because substitutional diffusion requires additional intrinsic defects such as vacancies or silicon self-interstitials. Furthermore, the diffusion of interstitials into the silicon is promoted along the direction of heat flow, from the irradiated front surface to the back of the wafer. We observed higher levels of gettered impurities in the front surface than in the back surface, especially in the grain-boundary regions. However, there is a significant temperature difference between the front and back surfaces during HFSF annealing: 78°C at the front-surface temperature of 801°C.

To more positively identify the photon-induced effects, we compared the phosphorus diffusion properties of HFSF-processed, single-crystal silicon wafers against conventional furnace-processed wafers in the temperature range of 775°C to 950°C. The two groups of samples used the same 300-μm-thick, 0.2-Ω-cm-resistivity, float-zone growth, boron-doped, single-crystal silicon wafers, same spin-on phosphorus dopants from Emulsitone Co., and same diffusion temperatures and diffusion time (20 min.). The long diffusion time of 20 min. is chosen to reduce the effects of minor variations in heating and cooling rates. The junction profile measurements after diffusion show that HFSF-diffused samples have considerably deeper junctions than conventional-furnace-diffused samples [Fig. 1]. The difference in the junction depths is equivalent to a temperature difference of 25°C on the low-temperature side and 75°C on the high-temperature side. These temperature differences are larger than the maximum possible error (20°C) in our estimation of the front-sample surface temperature during HFSF annealing. Comparisons of the peak surface phosphorus concentrations for the two groups of samples show that HFSF-annealed samples have higher peak surface phosphorus concentrations at temperatures below 875°C [Fig. 2]. At temperatures above 875°C, the peak phosphorus doping concentrations for the two groups of samples are about the same. We believe the enhanced phosphorus diffusion in HFSF-annealed samples is due to photon-related effects.

Hartiti et al. [9] obtained similar effects of photon-enhanced diffusion of phosphorus when comparing rapid thermal processing (RTP) and conventional thermal processing (CTP) methods between temperatures of 800 C and 1000 C. However, the difference between RTP and CTP decreases with temperature and disappears above 900 C, whereas the difference in the junction depths between HFSF- and CTP-processed samples observed by us increases with temperature. Hartiti et al. attributed the enhancement they observed to photon-enhanced Si-Si bond-breaking, which reduced the surface barrier for phosphorus diffusion.

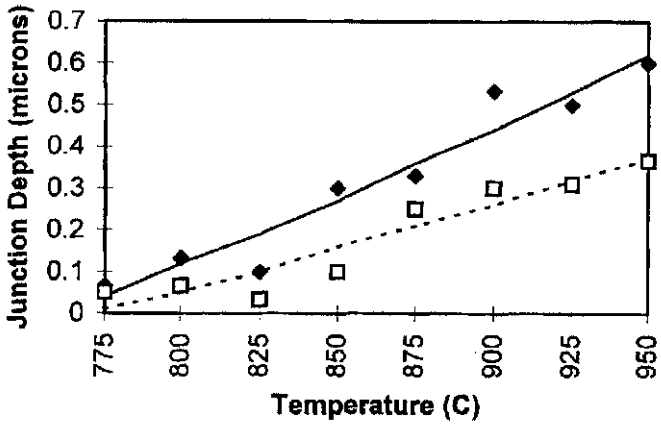


Fig. 1 Junction depth vs. diffusion temperature for solar-furnace-diffused samples (solid line) and conventional-furnace-diffused samples (dotted line).

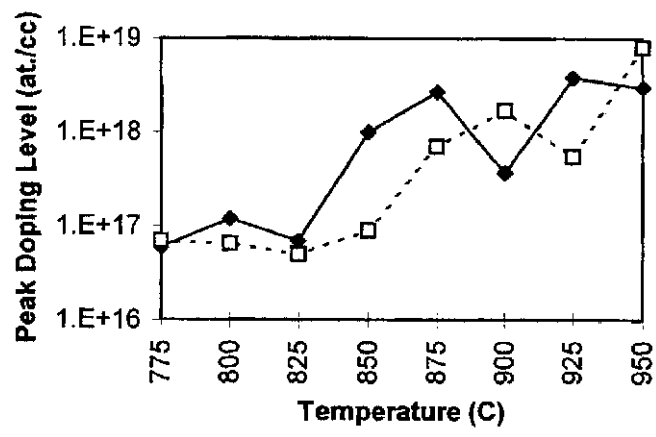


Fig. 2 Peak phosphorus doping concentration vs. diffusion temperature for solar furnace-diffused samples (solid line) and conventional-furnace-diffused samples (dotted line).

In summary, we have proposed here a new type of low-cost substrate that can be used for epitaxial growth of thin-film polycrystalline silicon without impurity contamination. We have demonstrated how such a substrate can be made from metallurgical-grade silicon wafers by showing that the large surface area created by a porous-silicon etch provides effective gettering sites and that the presence of photons during HFSF annealing enhances gettering efficiency. A porous-silicon-gettered MG-Si substrate has several advantages: (1) It is suitable for epitaxial polycrystalline silicon growth because the substrate itself is also polycrystalline silicon; (2) The film contamination from the substrate can be avoided if the film growth temperature is less than the gettering temperature of 1000°C because the gettered surface layers can serve as diffusion barriers; (3) It is a highly conductive substrate; (4) The substrate can be textured before film deposition; and (5) The porous-silicon etching and HFSF annealing can be done in large areas at low cost.

We have also demonstrated that porous-silicon gettering is a very effective extrinsic gettering technique for Al, B, Fe, Cu, and Cr impurities. The special features of porous-silicon gettering include: (1) A simple and low-cost chemical etching is used to generate the porous layers on both sides of the Si wafer to provide a large number of efficient gettering sites; (2) Porous-silicon etching causes no permanent damage to the substrate; (3) A high-flux solar furnace is used to provide low-cost, low-contamination, high-temperature annealing; (4) Impurity diffusion is enhanced by incident photon flux during annealing; (5) The gettering sites, along with the gettered impurities, can be easily removed at the end the process; and (6) The gettering process can be repeated to obtain the desired purity level, with a loss of only 10 μm of wafer thickness for each gettering cycle.

We thank Dr. T. Wang of NREL for helpful discussions. This work was supported by the U.S. Department of Energy under contract No. DE-AC36-83CH10093 through an NREL Director's Development Fund.

REFERENCES

1. Y.S. Tsuo, Y. Xiao, and C.A. Moore, "Device Applications of Porous and Nanostructured Silicon," in *Porous Silicon*, edited by Z.C. Feng and R. Tsu, World Scientific Publishing: NY, 1994.

2. M.R. Poponiak, "Method of Gettering Contaminants in Monocrystalline Silicon," U.S. Patent 3,929,529, (1975).

3. V.E. Borisenko and A.M. Dorofeev, *MRS Symp. Proc.* 13, p. 375, 1983.

4. S.Y. Shieh and J.W. Evans, "Some Observations of the Effect of Porous Silicon on oxidation-Induced Stacking Faults," *J. Electrochem. Soc.*, 140, pp. 1094-1096, 1993.

5. S.M. Meyers, D.M. Follstaedt, D.M. Bishop, and J.W. Medernach, in *Proceedings of Semiconductor Silicon*/1994, Eds. H.R. Huff, W. Bergholz, K. Sumino, The Electrochemical Society Inc., (1994), p. 808.

6. J. Wong-Leung, C.E. Ascheron, M. Petravic, R.G. Elliman, and J.S. Williams, "Gettering of Copper to Hydrogen-Induced Cavities in Silicon," *Appl. Phys. Lett.*, 66, pp. 1231-1233, 1995.

7. V.E. Borisenko and A.M. Dorofeev, *MRS Symp. Proc.* 13, p. 375, 1983.

8. M.R. Poponiak, "Method of Gettering Contaminants in Monocrystalline Silicon," U.S. Patent 3,929,529, (1975).

9. B. Hartiti, R. Schindler, A. Slaoui, B. Wagner, J.C. Muller, I. Reis, A. Eyer, and P. Siffert, "Towards High-Efficiency Silicon Solar Cells by Rapid Thermal Processing," *Prog. in PV: Res. & Appl.*, 2, pp.129-142, 1994.

Process Optimization of Alloyed Aluminum Backside Contacts for Silicon Solar Cells

Lynn L. Chalfoun, Aimee L. Smith, Song Zhao, and Lionel C. Kimerling

Department of Materials Science and Engineering
Materials Processing Center
Massachusetts Institute of Technology
Cambridge, MA 02139

abstract

Alloyed aluminum backside contacts are known to improve silicon solar cell performance. This enhancement is accomplished by gettering and by the repulsion of minority carriers from the rear contact of the cell by a highly doped $p+$ layer causing a reduction in effective surface recombination velocity. By examining how the $p+$ layer is influenced by processing and by modeling gettering mechanisms, we are able to suggest ways in which the design of processes for back contacts can be optimized.

Even in the best case, interfaces are roughened during the alloying step. Furnace anneals result in standard deviation of junction depth roughly equal to the depth. The smoothest surfaces are obtained by rapid thermal anneal. Short times are adequate to produce a thick recrystallized $p+$ region at the back of the cell. Stress caused by the difference in thermal expansion between Al and Si are high (130 MPa for 2 μm Al), and remain high after significant passage of time. Thicker films result in high stresses. Stress relief is correlated with cracking and delamination of the Al film. It is recommended that higher processing temperatures be used because they result in a thicker $p+$ region for a given amount of aluminum.

Gettering in solar cells during alloyed backside contact formation can occur in three ways: by liquid phase gettering, by segregation gettering, and by outdiffusion of impurities to the surface. Segregation coefficient, k, are calculated for iron in boron-doped silicon as a function of temperature and dopant concentration of the $p+$ region. For iron in Si with an Al-doped $p+$ layer, $k \leq 30$. Segregation coefficient increases as temperature decreases and as $p+$ doping increases. Gettering by outdiffusion occurs by similar processes as haze formation. A pair formation model is used to rank precipitation tendencies based on thermodynamic quantities. Lifetime measurements confirm that gettering is improved as alloying temperature or process time is increased.

IMPURITY GETTERING : INFLUENCE OF OXYGEN AND CRYSTALLOGRAPHIC DEFECTS

By I. PERICHAUD and S. MARTINUZZI
Lab. de Photoélectricité - DSO - Université de Marseille - France

It is schown that external gettering efficiency of bulk impurities in crystalline silicon wafers is limited by oxygen concentration when it exceeds the solubility limit. This efficiency is also depending on the presence of a too large density of bulk defects like dislocations, dislocation tangles and subgrain boundaries.

Oxygen related precipitates, their associated defects like the extended crystallographic defects contained in mc-Si wafers can induce a marked internal gettering which reduces the increase of minority carrier diffusion length during the external gettering treatment. In addition when oxygen concentration is too large the material is degraded even after a long phosphorus diffusion from a POCl3 source indicating that the internal gettering by the precipitates is more efficient . This could be explained by the presence of a large density of gettering sites homogeneoulsy distributed in all the bulk which impede the extraction of metallic impurities. The trapped metal atoms can in turn increase the recombination strength of the precipitates and the lifetime of minority carriers is drastically reduced.

Surface Passivation of Silicon by a Solution-Grown Film from Sopori Etch

Marta Symko, Bhushan Sopori, Dick Ahrenkiel, and Rick Matson
National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, CO 80401

Control of the surface/interface recombination velocity is crucial — not only in device fabrication but also for measuring a variety of material/device parameters. For example, the measured minority-carrier lifetime in the bulk of a wafer is very strongly influenced by the degree of surface passivation. Consequently, such measurements are typically performed following the growth of an oxide film or the formation of a p-n junction that produce low surface recombination (s). Because each of the high temperature process steps required for oxidation or junction formation can alter the as-grown lifetime, measurements are often made while the sample is immersed in dil. HF or in a methanol-iodine solution. Although immersion in such solutions results in very low s values with concomitant reliable bulk lifetimes, these procedures can be very annoying and raise some safety concerns. We are investigating another approach for obtaining surface/interface passivation, which consists of growing a film from an etching solution [1]. The passivating characterisitics of this solution were applied earlier to fabrication of edge-passivated diode arrays [2]. However, the mechanism of passivation was not well understood. In this work, we are attempting to study the passivation mechanisms and apply this technique to produce a low-recombination surface suitable for lifetime measurements. We will describe some preliminary results which suggest that this film lowers the s value. We find that a low-temperature anneal can further lower the s-value.

Films were grown from a solution consisting of a mixture of $HF:CH_3COOH:HNO_3$ in the ratio 36:15:1 (known as Sopori diode etch). This solution etches silicon at a rate of about 2 μm/min, while a bluish film grows on the silicon surface. Infrared spectroscopy and SIMS analysis have shown that the as-grown film contains copious amounts of H and F, which are presumed to be responsible for surface passivation. An interesting feature of the film is that it is a temporary film; it disappears in about a day, leaving a clean surface. However, the surface layer can be made permanent by annealing it in a forming gas ambient. A forming gas anneal at 250°C brings about a change in the hydrogen association resulting in a splitting of 2100 cm^{-1} band in the IR spectrum. Surface charge analysis showed that a positive charge resides within the film.

We have attempted to determine the changes in the s value of high-resistivity silicon wafers due to as-grown films and after annealing steps. Several techniques were used to estimate s value. These include RF-PCD, Laser Microwave PCD, and the surface photovoltage. From these preliminary data, the value of s with the film was estimated to be < 100 cm/s. A further reduction in the s value produced by this film is expected by improving our processing procedures.

References:

1. B. L. Sopori, " A New Defect Etch for Polycrystalline Silicon," *J. Electrochem. Soc.* **131**, 2601 (1984).
2. B. L. Sopori, " Fabrication of Diode Arrays for Solar Cell Material Characterization," *Appl. Phys. Lett.* **52**, 1718(1988).

REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE August 1996	3. REPORT TYPE AND DATES COVERED Technical Report

4. TITLE AND SUBTITLE
Sixth Workshop on the Role of Impurities and Defects in Silicon Device Processing: Extended Abstracts and Papers

5. FUNDING NUMBERS
TA: PV622101

6. AUTHOR(S)
B.L. Sopori, workshop chairman

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

SP-413-21551

DE96007959

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT

12b. DISTRIBUTION CODE

UC-1250

13. ABSTRACT *(Maximum 200 words)*

The theme of this workshop is "Technology Transition for Fabricating High-Efficiency, Low-Cost, Commercial Silicon Solar Cells." This workshop provides a forum for an informal exchange of information between researchers in the photovoltaic and non-photovoltaic fields on various aspects of impurities and defects in silicon, their dynamics during device processing, and their application in defect engineering. This interaction helps establish a knowledge base that can be used for improving device fabrication processes to enhance solar-cell performance and reduce cell costs. It also provides an excellent opportunity for researchers from industry and universities to recognize mutual needs for future joint research. The workshop format features invited review presentations, panel discussions, and two poster sessions. The poster sessions create an opportunity for both university and industrial researchers to present their latest results and provide a natural forum for extended discussions and technical exchanges.

14. SUBJECT TERMS

15. NUMBER OF PAGES
293

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. Z39-18
298-102