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Market-Driven EFG Modules

Annual Subcontract Report
14 December 1996 - 13 February 1998

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1617 Cole Boulevard
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A national laboratory of the U.S. Department of Energy
Managed by Midwest Research Institute
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PREFACE

This Annual Technical Progress Report covers the work performed by ASE Americas, Inc. for the period December 14, 1996 to February 13, 1998 under DOE/NREL Subcontract Number ZAF-6-14271-13 for the project entitled, "Market-Driven EFG Modules". This is the second Annual Technical Report for this subcontract. The subcontract is scheduled to run to February 13, 1999 (extended from the originally scheduled completion date of December 13, 1998).

The following personnel at ASE Americas have contributed to the technical efforts covered in this report.

Jeff Cao	Michael Kardauskas
Steven Ebers	Bernhard Piwcyzk
Ronald Gonsiorawski	Mert Prince
Juris Kalejs	Eric Tornstrom

In addition, ASE Americas has subcontracted a significant portion of the work on several tasks to consultants and outside organizations. Consultants include:

Dr. R.O. Bell	Prof. T. Gross
Prof. S. Danyluk	Prof. S. Mil'shtein
Georgia Institute of Technology	Prof. D. Watt

Outside organizations acting as lower-tier subcontractors include:

Automated Process Technology, Inc.	CQB Associates
Bright Technology, Inc.	GT Equipment, Inc.

SUMMARY

This report summarizes the progress made at ASE Americas Inc. during the second year (Phase II) of the planned 3 year program in Phase 4A2 on the development of Edge-Defined Film-Fed Growth (EFG) silicon wafer. This program focuses on advancing manufacturing technology to:

a) reduce EFG wafer thickness from 300 to 250 microns;
b) raise EFG solar cell efficiency to an average of 15.0% on 10 cm x 10 cm areas;
c) simplify processes and reduce costs in module manufacturing.

Good progress has been achieved in all three of these areas. Progress in Phase II includes module cost reductions of approximately 8%. With total savings of 15% achieved in the first two years, the program is on track to achieve its overall goal of reducing EFG module manufacturing costs by 25% by the end of Phase III.

Specific progress in the key tasks are summarized below.

Task 4: Wafer Manufacturing

The effort in EFG wafer manufacturing continued the work started in Phase I to reduce wafer thickness in order to reduce consumption of silicon feedstock material and to improve cell efficiency. This initiative resulted in a thickness reduction from 300 microns to 275 microns of one-half of ASE Americas' total silicon sheet production by the end of Phase II. New equipment was installed to automate the sorting silicon feedstock. New EFG crystal growth furnace components were implemented in production to reduce stresses in EFG tubes and increase by 50% the average lifetime of graphite dies. The laser systems used to cut EFG tubes into wafers were redesigned to accommodate thinner wafers and to preserve beam alignment so as to reduce edge damage and increase cutting speed. Overall wafer manufacturing improvements accomplished through Phase II reduced wafer manufacturing cost by about 6%.

Task 5: Cell Manufacturing

The major thrust in cell manufacturing is to reduce module cost by improving average cell efficiency. Initially it was anticipated that this would be accomplished mostly by improvements in cell design, in particular by optimizing the emitter grid to reduce series resistance and by adding a textured anti-reflection layer to the cell surface to reduce reflectance losses. The emitter optimization work has progressed well, and a new grid design is nearing introduction into the manufacturing line at ASE Americas. The textured anti-reflection layer did not to deliver the expected improvement and was replaced with a new module design concept that improves light collection.

Analyses of cell efficiency improvement opportunities revealed that improvements in the distribution of production cell efficiencies would likely yield greater gains than would cell design upgrades. As a consequence, Statistical Process Control (SPC) techniques were instituted

throughout wafer and cell production, including the installation of equipment to automate data collection.

A new technique for removing phosphorus glass from the cell surface after diffusion was demonstrated in prototype equipment that continuously operated during a pilot demonstration in production. Thousands of wafers were successfully processed. The result was a reduction in fluoride effluent by more than 98%.

Overall cell manufacturing improvements accomplished through Phase II reduced cell manufacturing cost by about 4%.

Task 6: Module Manufacturing

The goals for module manufacturing improvements included a simplified cell interconnection process, a reduction in the time required for module lamination, a reduction in cell breakage during lamination, reduction in the cost of diode housings and junction boxes, and reduction in both the cost of module frames and labor required for attachment. Significant progress was made during Phase II. The improvements in module yield and the new diode housing resulted in a 5% reduction in the cost of EFG modules.

Summary of Phase II Accomplishments

Accomplishments during the reporting period include:

Task 4: Wafers

- Optimization of EFG crystal growth variables, leading to reduced crystal stresses and improved wafer flatness
- Increased die run length due to improvements in the design of furnace components
- Construction and testing of EFG growth furnace enclosure
- Reduction of EFG wafer thickness from 300 µm to 275 µm for 50% of all standard production material
- Implementation of new equipment to reduce costs of silicon feedstock sorting prior to EFG crystal growth with a 3% increase in silicon feedstock utilization
- Development work demonstrating the laser cutting of EFG wafers at higher speeds and with reduced silicon damage

Task 5: Cells

- Characterization of cells after diffusion as preliminary work toward improving diffusion conditions and improving cell efficiency
- Demonstration of a continuous process to remove phosphorus glass from diffused wafers, reducing chemical consumption and hazardous waste by 98%
- Development of Statistical Process Control (SPC) methods to improve cell production process control

- The use of Design of Experiments (DoE) to study interactions between processing at various steps in cell manufacturing, and to develop strategies for productivity improvements
- Improvements in EFG cell efficiency due to the reduction in average wafer thickness
- Design and construction of equipment for producing cells with an improved grid design
- Demonstration of average efficiencies over 14.1% on production lots of EFG cells

Task 6: Modules

- Production and successful testing of prototypes of a lower-cost module diode housing
- Successful demonstration of a module design which greatly improves collection of light from space between cells in modules
- Testing of new encapsulants and lamination processes to demonstrate reduced lamination time, improved yield and enhanced durability
- Completion of options study for lower-cost module frames, and development of a frameless module design using mounting clamps

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1.0 INTRODUCTION

The goal of the PVMaT program at ASE Americas is to reduce the manufacturing cost of photovoltaic (PV) modules based on silicon wafers produced by the Edge-defined Film-fed Growth (EFG) method.

Under the PVMaT program, ASE is investigating reductions in wafer thickness, not only to reduce silicon materials costs, ergo wafer costs, but also to increase average cell efficiency. Thinner wafers require thinner EFG tube walls which can lower the yield of laser cutting of tubes into wafers. The development of improved lasers is necessary to the success of the thin wafer program. Wafer electronic quality can be improved by optimizing the tube growth process and by preventing contamination of EFG tubes during growth.

The PVMaT program is also aimed at reducing cost per watt by increasing average cell efficiency. Although the average efficiency of the EFG cells manufactured at ASE Americas is high relative to the efficiencies of mass-produced cells made on multicrystalline silicon by other manufacturers, further increases in efficiency are possible. For example, the front metal grid is being redesigned to improve cell efficiency by reducing both shadowing and series resistance by reducing finger width and increasing the number of fingers. Because of the proprietary method used at ASE to metallize cells, this change requires reengineering of the equipment and pastes used in the metallization process.

Another cell efficiency improvement opportunity is the use of Statistical Process Control techniques to determine the optimum parameters for every process step and to ensure that each is performed consistently from lot-to-lot and day-to-day. The goal is to raise average cell efficiency to 14% in the near-term and to 15% by the end of Phase III. Cell costs can be further reduced by departing from conventional processes for removing phosphorus glass after emitter diffusion.

Module assembly is the most expensive part of the manufacturing process, accounting for almost one-half of the cost of the finished module. A number of factors contribute to this; two key factors are materials cost and assembly costs. Two significant materials costs in module assembly are the aluminum frame and the diode housing. The standard frame is very robust, but it is expensive since it is assembled from four sections and mounted over a special tape, and its attachment requires a considerable amount of labor. The housing containing the protective diodes is expensive in large part due its use of a finned aluminum heat radiator. The most costly step in module assembly is interconnecting cells into ‘strings’ with soldered copper ‘tabs’. Another major cost in module assembly is the vacuum lamination process, which is relatively slow for the high reliability encapsulant used at ASE Americas.

The goal of the current PVMaT subcontract is to reduce module cost by 25% by the end of the third and final phase. This report presents the status of the program at the end of the second of the three phases, at which point technology advances resulting in 15% module cost reductions have been achieved.

2.0 ASE TECHNOLOGY PRIOR TO THIS PROGRAM

In this Section, ASE's standard manufacturing process is described; recent improvements are described in Section 3. An outline of the overall process is presented in Table 1; boldface steps are being re-engineered under the PVMaT program.

The technology used for manufacturing modules at ASE Americas is based on the EFG method for growing silicon in a closed hollow shape, which is currently in the form of an octagonal tube from which eight ribbons are cut. An 'octagon' EFG tube has a wall thickness of 300 μm and is grown to a length of approximately five meters. When the desired length is reached, the tube is detached from the die and removed from the furnace. A new seed is then lowered onto the die tip, and growth is resumed. This procedure is repeated until the die deteriorates and must be replaced. A multi-tube run between die replacements is called a 'growth run'. After a run is ended, the furnace is cooled, and the section of the furnace containing consumable parts is removed and replaced. The consumable parts are disassembled and rebuilt for re-use.

The growth furnaces are highly automated, so that several furnaces can be operated simultaneously by one operator. One of the features of the equipment that makes this possible is an automatic feedstock replenishment system which monitors the weight of the growing tube and replenishes the melt. In order for this equipment to operate properly all feedstock must be within a certain particle size range. At present silicon feedstock is manually sorted through a series of sieves.

The EFG growth furnace itself is largely constructed of graphite. Commercial grades of graphite available for furnace construction can contain harmful impurities, and these must be removed by careful processing of all furnace parts before assembly into a growth furnace. The levels of impurities in EFG wafers are very dependent on the effectiveness of the graphite purification process.

During growth of the EFG tube, the hot portions of the tube are surrounded by an atmosphere of argon to prevent oxidation of both the silicon and the graphite furnace parts. A small amount of carbon monoxide (CO) is added to improve the electronic quality of EFG wafers. The mechanism by which CO improves the wafers is not fully understood at present; it may be related to the interaction between oxygen and carbon defects in the silicon, the pinning of dislocations, and/or the gettering of metallic impurities. The use of CO can also have detrimental consequences in high-volume manufacturing. For example, the reaction of CO with silicon can form volatile silicon monoxide (SiO) which condenses to form fibrous deposits on the cooler zones of the furnace.

After an octagon tube is removed from a growth furnace, it is transported to another work station where a Neodymium-doped Yttrium Aluminum Garnet (Nd-YAG) laser cuts each face into square wafers, 100 mm in length and width. The rapid heating of the silicon with each laser pulse can generate microcracks along the wafer edges, and these cracks can propagate and cause the wafer to break during later processing.

Table 1
ASE PV Module Manufacturing Process
(Boldface indicates steps being improved as part of this subcontract)

Sorting of silicon feedstock

Growth of EFG octagon tubes

Laser cutting of tubes into wafers

Silicon wafer etch

Phosphorus diffusion

Phosphorus glass removal

Hydrogen passivation

Anti-reflection coating

Metal printing (rear and front) and firing

Cell testing

Cell interconnection into strings

Module lay-up

Lamination

Module testing

Framing

Attachment of junction box and external wiring

Safety testing

Cut wafers are etched in a mixture of nitric and hydrofluoric acids. The etching process is followed by phosphorus diffusion to create an emitter layer. The diffusion process is a continuous operation, as opposed to the batch operations used by other PV companies. After diffusion the phosphorus glass is removed with a second wet chemical process. The existing glass etch batch process is poorly matched to the continuous diffusion and consumes a significant quantity of chemicals that must undergo costly treatment before discharge.

After glass etch, cells undergo hydrogen passivation and anti-reflection (AR) coating using proprietary technologies. After the anti-reflection coating is deposited, silver contact pads and an aluminum back surface field coating are applied to the rear of the cell, and the silver grid pattern is printed on the front. The grid consists of 32 100 μm wide fingers and two bus bars which are bonded to cell interconnect tabs. Computer modeling suggests that the existing grid design is a source of significant shadow and series resistance losses.

After printing front and back contacts are co-fired, and each cell is individually tested and binned according to photocurrent at peak power.

Cells are interconnected by attaching solder-coated copper tabs by soldering them simultaneously to the front and back of one cell, followed by the feeding out of another length of tabbing and repetition of the process. The sequential nature of the process and the time required to properly heat and cool the solder bonds limit the production rate. Strings of interconnected cells are manually laid-up on a sheet of glass with layers of encapsulant and power bus strips. This lay-up is placed in a vacuum laminator, air is removed, and the encapsulant is melted and reflowed to fill all internal spaces. After removal from the laminator, the 'laminate' is tested to ensure that its output power is within specifications.

The module is completed by attaching an extruded aluminum frame, a junction box or diode housing, and electrical cables for connection to other modules. Framing is labor intensive and not readily amenable to automation. The diode housing used on most ASE modules is manually attached to the laminate using an adhesive. The diode housing is a custom-formed part which encloses the protective diodes and dissipates heat generated during their operation. The final step in module assembly is the electrical connection of the laminate to the diode or junction box circuitry, and the attachment of the cables used to connect the modules to one another. The final steps are a power rating test and a high voltage current leakage test.

3.0 PVMaT PROGRAM ACTIVITIES DURING PHASE II

This Section details the efforts to reduce the cost of ASE modules. The following paragraphs provide an overview of the work being carried out on the process steps identified in Table 1.

Sorting of silicon feedstock

The sorting operation has been converted from a manual operation to an automated process, providing significant savings in labor, an improved level of safety, and a reduction of the potential for contaminating the feedstock.

Growth of EFG octagon tubes

Improvements in the graphite purification process have resulted in an improvement in the electronic quality of EFG wafers. An enclosure to prevent air leaks into EFG growth furnaces was evaluated. Process variable optimization studies identified the optimal growth speed that balances material quality and production rate. Impurity analyses were developed to provide rapid determination of sources of wafer contamination. Additions of carbon monoxide during crystal growth were terminated after tests showed little improvement in wafer quality. Run length increased furnace component modifications prevented the accumulation of unmelted silicon pellets and reduced of oxidation of the graphite dies. The thickness of typical EFG wafers was reduced from 300 μm to 275 μm, while maintaining similar yield in cell and module fabrication.

Laser cutting of tubes into wafers

Initial tests with a low-cost, low-maintenance carbon dioxide laser showed promise, but cutting conditions were not optimal. Laboratory testing of a copper vapor laser indicated that that laser technology is not yet practical for production use. Current testing is concentrated on improvements in cutting using Nd:YAG lasers, which have proven themselves to be very reliable in a production environment. Changes in the optics of the cutting station have been demonstrated which have doubled the current cutting rate on an experimental basis, and further experimentation has shown that cutting can be accomplished with much lower levels of edge damage than that produced by the current generation of lasers. Tests have also been conducted on a modified design of the argon jet nozzle that results in much lower stresses on the EFG tube during cutting.

Phosphorus glass removal

A new approach to the removal of the phosphorus glass layer remaining after diffusion has been demonstrated both in the laboratory and on the production floor. The new process reduces chemical, waste treatment, deionized water, and labor costs, and streamlines material handling. A prototype unit processed wafers continuously, an improvement over the batch process used

currently at ASE Americas. A full-scale unit hardened for continuous service in the manufacturing environment is expected to be put into service in late 1998.

Anti-reflection coating

Development work was carried out on a textured anti-reflection (AR) coating. Unlike standard AR coatings used in the PV industry, this coating would be relatively thick and textured to produce a matte surface on multicrystalline silicon surfaces similar to that produced by alkali etching of single crystal silicon surfaces. The coating did not provide any improvement over the standard doubled-layer EFG AR coating.

Metal printing and firing

Firing conditions for the current metallization pattern have been optimized, resulting in a gain in cell efficiency to over 14% on many production lots. Equipment for increasing the number of fingers in the emitter grid has been designed and shown to provide a benefit in cell efficiency, and that equipment is being readied for use in full production. Work is continuing on reducing finger width through work with vendors to develop modified silver pastes for the front metallization.

Cell interconnection into strings

Work is being carried out to increase the cooling rate of solder bonds during interconnection, to increase the number of cells that can be bonded in a given time. Throughput improvements of as much as 50% are projected.

Module Design

A new module design has been developed and demonstrated in which most of the light which falls in between cells in the module is redirected onto the cells. Increases in module power of as much as 20% have been demonstrated for a given cell area. A patent application has been filed covering the new design, and it is being readied for introduction into manufacturing.

Lamination

Efforts are being made to reduce lamination time by changing process conditions and/or encapsulant materials. A reduction of lamination time by more than 30% has already been demonstrated using current vacuum lamination equipment and is being tested for production use. Non-vacuum processes are also being investigated to replace this step with a very different process, using much less expensive equipment. New encapsulant materials are under development for both types of lamination.

Framing

A mounting system using module clamps is under development which would eliminate the need for frames on ASE modules, providing a significant cost saving.

Attachment of junction box and external wiring

A new diode housing has been developed which reduces the cost of this component by a factor of two. Prototypes of the housing have been produced and have passed all required tests, including those for UL certification. Minor modifications are being made to the design and final environmental testing is being conducted before introduction of the diode housing into production later in 1998.

3.1 TASK 4 - IMPROVEMENTS IN EFG WAFER PRODUCTION

3.1.1 Reduction of Wafer Thickness to 275 Microns

Silicon is one of the most costly materials in an ASE module. Reduction in wafer thickness reduces silicon materials content and can also increase cell efficiency by increasing the collection of photogenerated current.

It is difficult to decrease EFG tube thickness. Although tube thickness can be changed by varying the temperature of the tip of the die during tube growth, small changes in temperature can introduce stresses in the growing tube that cause it to buckle. In addition, the thickness of the wall of the octagon tube is not perfectly uniform around the perimeter of the tube because of temperature non-uniformities caused by variations in the density of the graphite from which the die is made (which affects the transfer of energy from the induction heating coil) and other factors. As a result, some faces of an octagon tube are always thinner than others, and reducing the average thickness even by a small amount can reduce the thickness of the thinnest face to a point where it is very fragile, resulting in high breakage losses when the tube is cut into wafers. At the beginning of this program, EFG octagon tube thickness was nominally 300 microns, and the goal was to reduce thickness to 250 microns. In order to achieve that goal with a minimum negative impact on production yields, it was decided to set an intermediate goal of 275 microns, and stabilize production at that thickness level before attempting to reach the ultimate goal of 250 microns. During Phase I, it was demonstrated that it was possible to grow 275 micron tubes with relatively high yields. During Phase II, the task was to make 275 microns the standard tube thickness on the EFG manufacturing line.

This goal was achieved in several steps. In the first step, one of the nine production EFG furnaces was converted to growth of the thinner tubes. An immediate improvement in cell efficiency was observed for material cut from those tubes, with apparent improvements up to 0.5% in absolute efficiency. Production yields appeared to be only 1-2% lower throughout wafer and cell manufacturing, but higher breakage rates were observed during cell interconnection.

These results were considered very encouraging, and the experiment was continued for three months. During those months, a fuller understanding of the effects of thin material growth was obtained. With the larger quantity of data, it was found that 275 micron material did have an efficiency advantage of about 0.2% absolute over 300 micron material. Wafer yield losses during crystal growth and laser cutting of wafers due to breakage were no higher for the 275 micron material, but the thinner material was not as flat, leading to a 2-3% higher rejection rate than for 300 micron material. Growth of 250 micron tubes was also investigated, but yields for that material were often inconsistent due to fracture of thin tube faces during laser cutting. On tubes with no thin faces, cutting yields were normal, but again there was an increase in the rejection rate for non-flatness.

Based on this data, all of the nine production EFG furnaces were converted to 275 micron growth

for one month. The production experience gained during that month confirmed all of the observations made during the previous trials, along with one additional observation: yields of 275 micron cells were noticeably lower on one of the two cell interconnect machines. Because of that observation, one-half of the production line was switched back to 300 micron wafer thickness, until such time as the second interconnect machine could be upgraded to reduce breakage of thin cells. The line continued to produce a 50/50 mix of 275 and 300 micron material for the remainder of Phase II.

During the same period, efforts were made in the crystal growth area to reduce the losses due to the non-flatness of thinner wafers, resulting in a modification to the afterheater section of the growth furnaces that reduced the reject rate for non-flatness by 50%. This raised the production yields for 275 micron material to essentially the same level as for 300 micron material. It was hoped that the improved flatness would also lead to higher downstream yields, since it was assumed that some of the breakage occurring in cell processing is due to high stresses applied to non-flat material during processing, but that improvement has not yet materialized. In fact, experiments showed that the flatter wafers have slightly lower downstream yield, apparently because of higher internal stresses. All of the improvements expected at the beginning of the program, however, were fulfilled: a reduction in silicon usage combined with an increase in cell efficiency, accomplished without a negative impact on production yield.

3.1.2 Improvements in the Growth of EFG Octagon Tubes

Improvements in graphite purity

Extensive testing of several grades of graphite from several vendors, and several graphite purification processes, were conducted during Phase I of this program. This testing consisted of both spectroscopic measurement of impurity levels in the various grades, and the fabrication of the purest of these grades into furnace components for correlation of cell efficiency with material type. As a result of these studies, several graphite grades and two purification methods were qualified for production use.

One of these experiments was carried over into Phase II: further testing of the purification process used by one purification vendor. In initial tests, it appeared that this second vendor was more able to provide consistently pure graphite than was the case for ASE America's primary purification vendor. The follow-up study was made to determine if the secondary vendor should be made the primary source for purified graphite furnace components. The additional testing showed that the second vendor was fully capable of providing high quality purification, but no significant difference in efficiency was observed when wafers from furnaces purified by the two different vendors were made into cells. Since the cost of purification from the second vendor was higher than that for the primary vendor, the decision was made not to change primary vendors. However, the second vendor has been qualified as a source for purified graphite, and some fraction of the graphite used in normal production is routinely sent to them for purification, as a check on the quality provided by the primary vendor.

Solar grade silicon

An attempt was made to reduce the cost of EFG wafers by relaxing the specification for the feedstock silicon material from higher grades to the least expensive solar grade. After an initial evaluation that did not show any clear difference in cell efficiency as a result of the use of the less costly grade, a large fraction of production was converted to the use of solar grade material. While this resulted in a cost savings on raw materials, the larger body of data accumulated by the use of solar grade material in full production showed an efficiency shortfall of several tenths of one percent absolute in cell efficiency, which negated the savings on materials cost. As a result, the feedstock was changed back to the higher grades. The information obtained in the experiment will continue to be useful, however, as prices and availability of the various grades of silicon change in the future. Particularly during periods of silicon shortages, the difference in price between the different grades might justify the use of the lower grade material.

Furnace component improvements

A particularly difficult problem which has affected EFG crystal growth over the past few years has been the problem of unmelted silicon feedstock in the central portion of the EFG die/crucible, called 'mushrooms' from their appearance after solidification. The presence of mushrooms in the crucible disturbs the thermal uniformity of the melt, causing some faces of the octagon tube to grow thinner than others, and can eventually cause 'voiding' of the die, where one of the faces separates from the die tip and stops growing. The growth of mushrooms eventually leads to the termination of a growth run, and the need to replace the die.

A number of modifications of the EFG furnace aimed at reducing the mushroom problem were tested as part of Phase II of this PVMaT subcontract. A substitution was made for the material of one of the furnace components in contact with the silicon melt, in order to reduce the tendency of semi-molten feedstock material to stick to it. In addition, the mechanism that disperses feedstock into the melt during replenishment was changed to reduce the tendency of feedstock to accumulate on one of its components. As a result of these changes, the length of growth runs increased by 50%, leading to significantly improved productivity in the crystal growth area. There was also some hope that contact of molten silicon with the new material would contribute oxygen to the melt, which might improve the electronic quality of the wafers, but analysis of production data failed to show such an improvement. That finding is in agreement with the observation made in Phase I that oxygen additions to the melt during EFG growth as practiced today no longer makes the contribution to electronic quality that was seen in EFG material ten years ago.

Development of a Particle Separator for Silicon Feedstock

The silicon feedstock used to replenish EFG furnaces during octagon growth is sorted both to remove silicon particles that are too large to flow smoothly into the die during the replenishment operation and also to remove very fine particles, or dust, which has a tendency to float on the

surface of the molten silicon and contributes to the formation of 'mushrooms'. Prior to the beginning of this PVMaT subcontract, the sorting operation was performed manually, using a series of sieves. Over time, the quantity of silicon used for EFG growth had increased greatly, to the point where a considerable amount of labor was required for this operation. In addition, the relatively small fraction of material that had to be removed was accumulating at an ever increasing rate, representing a significant cost for material that could not be used for EFG growth. During Phase I, experiments were carried out to determine whether particles in the ranges considered to be out of specification could be tolerated in the growth system if their concentrations were low. This was found to be true, which led to the development of a procedure for blending rejected material back into the feedstock destined for crystal growth, while keeping tight control over the concentrations of particles in the various size ranges. This procedure greatly reduced the amount of material which was not usable in crystal growth, but it required an amount of sieving that could no longer be performed manually. Therefore, a task was begun to design and build a mechanical particle sorting machine that would permit the new procedure to be carried out in production.

A consulting engineering firm studied the problem and recommended the purchase of a commercial sieving machine. A sorting machine was first rented and outfitted with appropriate sieves, and the sorted feedstock material was used to grow octagon tubes on one of the nine production EFG furnaces. The machine operated well, and wafers produced from the feedstock material used in the test were processed into cells with efficiencies equivalent to those of cells produced from feedstock which was manually sorted. The sorting machine has now been purchased and permanently modified for use in the EFG wafer manufacturing line where it has performed well. The more effective sorting performed by the new machine has permitted the use of a higher percentage of silicon feedstock material than was possible using the manual sorting method, while reducing the labor costs associated with sorting.

Engineering of an Enclosure for EFG Furnaces

Wafer quality is affected not only by the purity of materials intentionally placed inside the furnace, but also by impurities that infiltrate into the furnace from the ambient air. Exposure of EFG tubes to the environment can cause other problems as well, e.g. tube buckling and contamination of the growth furnace atmosphere with air. Protection of the furnace and growing tube from the environment would improve the quality and consistency of EFG wafers.

During Phase I an enclosure for EFG growth furnaces was designed. During Phase II a prototype enclosure was constructed and tested. There were initial problems with tracking of the bellows enclosure and with completely purging the air from the system. After these problems were fixed, air was still found to leak into the system from several points. The air leaks resulted in oxidation of the octagon tube and the graphite components of the hot zone of the furnace.

Octagon tubes grown in the enclosure were not of higher quality than tubes grown without the enclosure. Testing was terminated pending major redesign of the enclosure.

3.1.3 Research into Improved Laser Cutting of Tubes into Wafers

One of the major causes of breakage of EFG wafers thinner than 250 microns is the presence of cracks caused by the laser cutting process by which the octagon tubes are converted into wafers. There are two aspects of the cutting process that cause these cracks. The first is the mechanical force exerted on the tubes during the cutting operation by the argon jet which is directed at the cut to eject the material melted by the laser. The second is the thermal stress induced in the vicinity of the cut by laser heating and by the resolidification of silicon in the region of the cut. While both of these problems affect the yield of EFG wafers of any thickness, they cause much greater difficulties with thin wafer growth, causing wafer yield to drop to as low as 50% in some cases. Therefore, these problems need to be addressed in order to be able to produce thin wafers at a reasonable cost. During Phase II, a program was begun to work on these problems.

The first part of this work was focussed on reducing the mechanical stresses on the wafers cause by the argon jets. A study was commissioned at Old Dominion University to determine the volume of gas required to eject the molten silicon material so that the jet could be redesigned to minimize stresses on the tube. The modeling performed in the study showed that, because of the design of the argon nozzle, the current generation of EFG cutting equipment directed three times as much argon at the cut as would theoretically be necessary to eject all of the molten material. Part of the reason that the gas flows were set to such high levels, however, was that the laser beam used to cut the tube passes down the axis of the nozzle, and, because the beam wanders slightly, reducing the diameter of the nozzle would cause the laser beam to strike the interior of the nozzle. This understanding led to a program to both reduce the amount of wander of the laser beam and to modify the nozzle so as to reduce the force exerted on the tube.

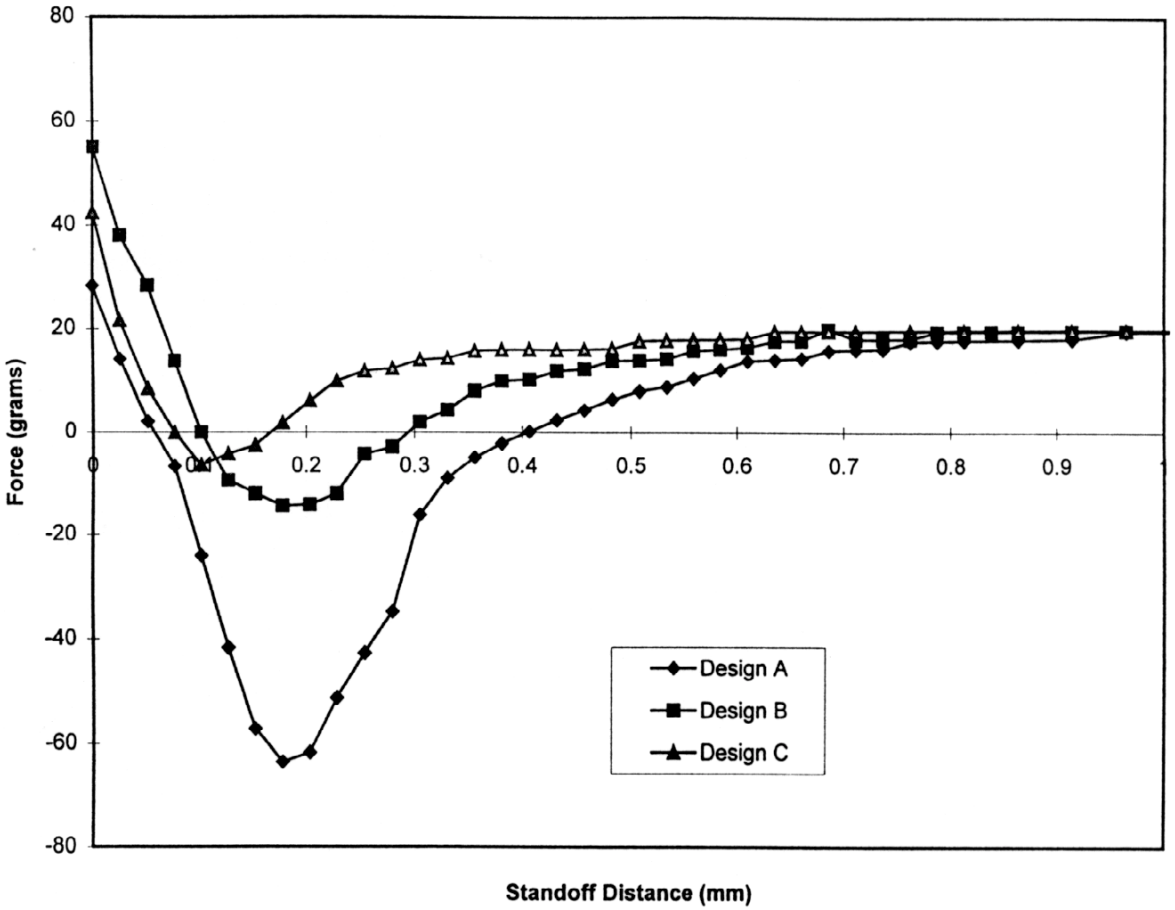
An investigation into the cause of the beam wander revealed that it was due to relatively small errors in the pointing of the laser beam by the mechanical positioning system used to direct the optics. Although the motion system was designed to be sufficiently accurate to avoid this problem, the laser cutting operation generates abrasive silicon dust which can cause wear in the bearings of the motion table. Over time, this results in inaccuracies in the beam position that are great enough to cause the beam to strike the interior of the argon nozzle, which both interferes with the cutting operation and causes damage to the nozzle. Although alternate motion table designs which might not be as sensitive to dust were studied, the cost of installing those systems throughout the manufacturing line would be prohibitive. Therefore, a method was sought to reduce the force exerted on the octagon tube during cutting without increasing the diameter of the nozzle orifice, which would allow the current generation of motion tables to continue in service.

During experimentation on modifications to the nozzle design in an attempt to reduce the gas flow necessary to remove the molten slag from the region of the cut, it was observed that certain combinations of nozzle design and positioning caused the octagon tube to be attracted toward the nozzle, instead of being moved away from it. This was recognized to be due to the Bernoulli effect, by which gas flow at high velocities causes a decrease in local pressure. Since at larger nozzle standoff distances the pressure is positive, it was realized that, at least in theory, the pressure exerted on the tube by the gas flow could be reduced to near zero by a proper combination of nozzle design and positioning. Experiments were conducted to identify a nozzle

design which would be able to produce near-zero net force over a practical range of nozzle spacings. This goal was achieved, resulting in a design which exerts less than one-half the force of a conventional nozzle over standoff distance variations of about 0.3 mm, which can be achieved in practical production equipment. A plot of the variation of force exerted by the gas jet versus standoff distance for three experimental nozzle designs is shown in Figure 1. A few nozzles of the new design were manufactured for testing in the production laser cutting equipment and were undergoing testing at the end of Phase II.

Another goal of the laser study was to increase cutting speed. Speed can be increased by using more powerful lasers, but such lasers are more expensive than the lasers currently in use, and the increased power can lead to an increase in the extent of microcrack formation in the region of the cut. Another approach is to try to focus the beam more tightly so that the beam energy is concentrated along the line which is being cut. Testing was performed on this approach, by introducing a new lens system to modify the shape of the laser beam. In tests conducted at a laser vendor's facility, this new lens led to a doubling in cutting speed with no degradation in cut

Figure 1. Force exerted on an EFG tube by gas assist nozzles of different designs, as a function of nozzle stand-off distance from the tube, at a constant gas pressure.



quality. This increase in cutting speed would result in a throughput increase of 25-30% after accounting for time to position the tube and remove cut wafers. A custom-designed lens could theoretically increase cutting speed by a factor of four. At the end of Phase II, a vendor was being sought for a lens of this type which could be installed in ASE's production lasers.

Work was also conducted on the task of locating a robust laser which could produce a higher quality cut, with a minimum of microcrack formation in the edge of the cut wafer. This is an important goal, because currently ASE Americas chemically etches all wafers to blunt the cracks caused by laser cutting, and the elimination of this step would result not only in a large cost savings, but also a large reduction in consumption of etch chemicals. A number of experiments were performed with a laser which was expected to produce higher quality cuts than the Nd:YAG lasers in current production. The new laser, which uses shorter pulses at higher power densities, was shown to produce cuts with much less edge damage. Although micro-cracks were still formed, they were much shorter, and could be blunted with much less chemical etching. At the completion of testing of the new laser, it was concluded that it was not yet practical for use in a manufacturing environment, but the testing had identified pulse parameters which were necessary to achieve the desired results. This information will be used during Phase III in a continued search for an improved laser.

3.1.4 Strengthening of EFG Wafers Without Chemical Etching

In lieu of reductions in chemical etching that might be possible with improved laser cutting, wafer strengthening was attempted using mechanical lapping of the wafer edges using an abrasive slurry of the type used to commercially polish silicon wafers.

The lapping was performed by two methods, one using commercial lapping equipment, and the other lapping manually. The automatic equipment was found to be capable of lapping the edges of stacks of about fifty wafers without weakening the wafers, provided that the wafers had already been strengthened by chemical etching. Wafers that had not previously been etched, however, suffered large yield losses in the automated lapping operation. The manual lapping tests were carried out to determine why the automated lapping was unsuccessful. It was found that small pieces of debris produced by the laser cutting operation were loosened by the lapping operation and became wedged between wafers, producing high local stresses. The manual operation could be carried out in such a way that caused the loose particles to be swept away from the wafer stack, minimizing this problem. Several stacks of wafers were processed this way with 100% yield, and then tested for fracture strength, as an indication of the effectiveness of the method as a means to remove the microcracked region of the wafers. Those wafers were found to be significantly stronger than wafers that had not been chemically etched, but they were still weaker than etched wafers. At the end of Phase II, this information was being assessed in order to determine whether the motions used in the manual lapping operation could be replicated by automated equipment, and whether the quality of the edge produced by lapping could be improved to provide the level of wafer strength achieved by chemical etching.

3.2 TASK 5 - IMPROVEMENTS IN EFG CELL PRODUCTION

3.2.1 Evaluation of Textured Anti-reflection Coatings

One of the disadvantages that multicrystalline silicon materials such as EFG face when compared with monocrystalline silicon as a substrate for photovoltaic cells is the inability to texture the surface by chemical means. Work was performed during Phase I to attempt to produce the benefits of a textured surface on multicrystalline EFG wafers by applying a textured coating to the surface of the wafers. An attempt was made to reproduce the results achieved in a study at Sandia National Laboratories, in which cells coated with textured layers of zinc oxide (ZnO). For the ASE Americas study, a number of cells were coated with the same material at the laboratory of Professor Roy Gordon at Harvard University. The cells in the ASE study were not improved significantly by the addition of the coating, although improvements of as much as 0.5% absolute were reported under similar conditions in the Sandia study. At the end of the Phase I study, work was ongoing to determine the cause of the this discrepancy and to determine whether further effort on this approach was warranted.

As part of the effort to explain the lack of improvement in the ASE cells, a number of cells produced in the study were sent to Harvard and Sandia for analysis, where the reflectance and transmittance of the ZnO films were measured, the texture of the ZnO film texture was observed by scanning electron microscopy, and modeling was carried out to determine the reflectance levels which would be expected for the observed texture. The conclusion from the tests was that the textured film was performing as expected, but its performance was not appreciably better than that of the standard ASE AR coating, because ASE's standard coating was unusually effective. ASE uses a graded AR coating, which results in a total reflection from an encapsulated cell of 7%. Since a 4% reflective loss occurs at the glass/air interface, a textured coating on the cell itself would have to produce a reflectivity lower than 3% at the cell surface in order to improve the performance of the cell over that obtained from ASE's standard process. Measurements of the reflectivity of the ZnO-coated cells showed that the reflectivity from that surface was about 2%, only slightly lower than the reflectivity of the uncoated cell. The 1% improvement that might be expected was apparently lost due to the absorption of a small amount of light in the relatively thick ZnO coating, resulting in a negligible improvement in cell performance as a result of adding the coating. Thus, it was concluded that further work in this direction would not be productive, and the study was ended. It was further concluded that the difference between the ASE results and those obtained in the earlier work at Sandia was due to the poorer performance of the titanium dioxide AR coating used as a control in the Sandia work as compared to that of the ASE AR coating.

The project on development of the textured coating had been a major part of the planned effort on this subcontract to increase cell efficiency. In order to be able to meet projected cost decrease goals for the program without it, it was necessary to redirect resources budgeted for this work toward the development of an alternate technology which promised increases in cell power. We therefore initiated modeling work on a new module technology. The modeling indicated that a flat-plate concentrator module design which had been under consideration would provide

enhancements in module power. The resources originally allocated to the coating project were therefore redirected toward this new effort. Work on that project is described in Section 3.3.6 of this report.

3.2.2 Optimization of Cell Processing

As part of an ongoing program of product improvement at ASE Americas, cell samples were sent to laboratories at Georgia Institute of Technology (GIT) and University of California at Berkeley (UCB) for analysis of the levels of impurities in EFG wafers at various steps in the production process. Initial tests indicated a measurable increase in the level of impurities after processing, suggesting that wafers were being contaminated. Further tests revealed that the impurities accumulating in the wafers were primarily iron and nickel. This result was readily understandable, because the high-throughput equipment at ASE Americas contains both of these metals in various components.

The problem was addressed by a two-pronged approach: an effort to develop new processes and equipment that would not require wafers to contact metal components, and an attempt to find substitute materials for the components suspected of causing the contamination in the standard production equipment. One candidate for a new process was the use of Rapid Thermal Processing (RTP), based on encouraging results obtained in an ongoing development program at GIT, including the production of 1 cm^2 EFG cells with efficiencies of 16%. Accordingly, tests were arranged with a manufacturer of RTP equipment for testing of a large number of cells at the manufacturer's facility. Significant problems were encountered with this approach because of the lack of facilities to apply ASE's standard dopant coating at the manufacturer's plant, and the tendency of coatings applied at ASE to degrade due to reaction with air during shipment. Eventually, a number of cells were produced by this method with efficiencies between 13.5 and 14.0%, but it was unclear whether this represented an improvement over the results that would have been obtained in the standard diffusion furnace for the same material.

Meanwhile, a search had been initiated for new materials for the standard process equipment. Samples of several candidate materials were obtained and exposed to temperatures typical of the highest temperature processes to evaluate any tendencies for the materials to change from this exposure. A few of the materials changed significantly, and were dropped from consideration. Two of the new materials, however, looked promising. Samples of these materials were placed on Czochralski wafers and subjected to ASE Americas processing, and these wafer samples were then sent, along with control samples, to UCB for impurity analysis. Both of the materials were found to cause less contamination than the metal components in the standard equipment, and one of these materials was clearly better than the other. As of the end of Phase II, an analysis is being performed to determine whether the material producing the lowest contamination would have the mechanical properties at high temperatures required in order to use it as a direct replacement for the metal components in the standard equipment. If the results are positive, the new material will be used in ASE production.

3.2.3 The Development of a New Process for Phosphorus Glass Removal

As is typical for any diffusion process on silicon wafers, the diffusion process at ASE Americas leaves the wafer surface coated with a silicate/phosphate glass, which must be removed prior to any further processing. At ASE, this is accomplished by wet chemical etching of the wafers, which are held in carriers in an acid bath. The need for the use of carriers presents a handling difficulty, since neither preceding nor following process steps require the use of carriers. In addition, although little acid is consumed by chemical reaction during the process, the bath must be replaced periodically. The disposal of the spent acid is costly, since it requires treatment before it can be discharged, and removal of the fluoride that it contains is expensive.

ASE developed a concept of an alternative process based on the use of acid vapor, which could be carried out on wafers as they are transported by belt from one processing area to another, eliminating the need for carriers and a great deal of manual handling. The task of studying the feasibility of designing such a process and developing equipment to carry it out was subcontracted to Bright Technology, Inc. During Phase I, that firm demonstrated the effectiveness of the method by successfully processing a number of EFG wafers coated with phosphorus glass, using bench-top apparatus which demonstrated the principles that could be used in a machine capable of continuos processing. The trials demonstrated that a reduction in chemical consumption at this step by 95-98% was achievable with this approach. As a result, the decision was made to build a prototype unit capable of continuous processing at the rate required to match the throughput of the cell line at ASE Americas.

The design of the prototype unit was completed early in Phase II, and construction was started immediately thereafter. After construction was finished, the unit was tested at Bright Technology for two months to develop the etching process and make necessary modifications to the machine. Test results indicated that the vapor etch process was working as expected, but that major improvements would be needed in the rinsing process to remove all of the etch residue. While a new rinsing module was being designed and constructed, the etch module was shipped to ASE Americas and installed there in a laboratory, where larger test runs could be carried out. Those early tests indicated that cells processed in the new unit had slightly lower efficiencies than those processed in the standard equipment on the ASE Americas production line, a problem which was attributed to inadequate rinsing. However, chemical consumption was found to be reduced by even more than the 98% which had been projected for the unit, indicating an extremely high efficiency in the utilization of the hydrofluoric acid etchant.

When the improved rinsing station was installed on the machine, it was expected that the efficiencies of cells processed through it would immediately rise to the level of those processed through the standard equipment. However, that did not occur, despite a near total elimination of staining visible on the wafer surface after AR coating. A major effort was undertaken to find even more effective rinsing methods, but the methods tested provided only slight improvements. Eventually, a chemical rinsing aid was tested which provided not only a visually clean surface, but also full parity in cell efficiency between the new process and the standard one. At this point the prototype equipment was moved from the laboratory to the cell manufacturing area, where it

was successfully used to etch over 10,000 wafers which were later processed into standard ASE solar cells.

After the demonstration was completed, the prototype unit was returned to Bright Technology, and negotiations were started with vendors for the construction of a unit capable of long-term reliable operation in the ASE Americas manufacturing line. As of the end of Phase II, two vendors are developing designs for such equipment. A vendor was selected, and work is proceeding on construction of the etch unit, which is planned to be installed in production before the end of Phase III.

3.2.4 Optimization of Metal Printing and Firing

Optimization of the Front Grid

The width of the silver fingers used in the front grid pattern on the cells currently manufactured at ASE Americas is approximately 100 μm; the narrowest fingers achieved in developmental engineering work at ASE is approximately 60 μm. If those narrower fingers could be produced consistently on the manufacturing line, the resultant reduction in shadowing would increase cell efficiency by about 0.2% absolute. A computer model developed at ASE Americas has shown that if, in addition, the number of fingers in the grid pattern were increased from 32 to 40 or more, the reduced spacing between the fingers would reduce series resistance losses in the cell emitter and raise efficiency by an additional 0.1-0.2%.

The difficulty in achieving this overall objective lies mainly in the flow properties of commercially available thick film silver pastes designed for use on PV cells. The number of commercial pastes compatible with the printing technology at ASE Americas is limited, and all of those pastes were designed for screen printing. These pastes have a tendency to spread after printing, increasing linewidth. In order to achieve narrower lines, modifications must be made in the formulation of the silver paste. During the course of Phase II, ASE Americas discussed the necessary changes with several manufacturers of silver paste. Unfortunately, while some of the sample pastes provided to ASE by commercial vendors to date have produced good results in developmental work, they not been consistent enough to use in manufacturing.

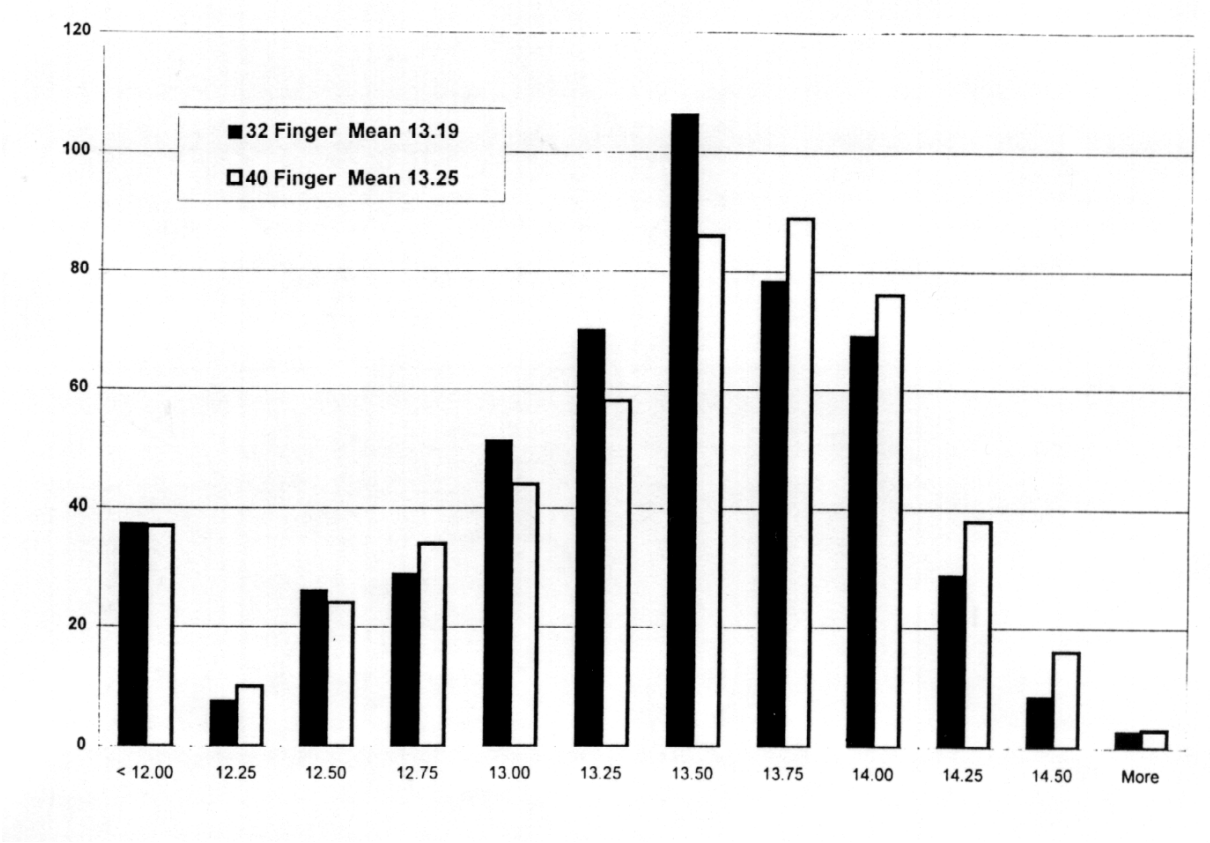
At first, this problem delayed all work on the modified grid design. However, during Phase II a more sophisticated grid modeling program was obtained from Sandia National Laboratories and used to model the standard ASE Americas design, and the results obtained from the new model indicated that an efficiency improvement of about 0.2% absolute should be achievable by increasing the number of grid fingers without changing line width. This allowed the problem to be approached as two independent steps, a change in line width and an increase in the number of fingers, which could be carried out in any order. If the new paste was not available, it followed that the change in the grid design should occur first.

Such a design change is more difficult on the manufacturing line at ASE Americas than it would be for most other cell manufacturers, because the grid on ASE cells is not produced by screen

printing. In order to test a grid with a larger number of fingers, it was necessary to machine a new printing head for the ASE machine, and run tests on the production line itself. The first of those tests, in which over 4,000 cells were printed with the new grid design, was completed at the end of Phase II. The test showed an improvement for the new grid, but it was only about one-half of that predicted by the model, apparently because the additional contact area caused an increase in reverse leakage. Although the improvement in average cell power was small, however, the shift in cell population toward higher performance cell categories was clear (Figure 2).

After the experiment, the production line was converted back to the use of the standard grid design, while permanent conversion to the new grid pattern could be considered. Because changes in the grid design are visually apparent, there are inventory and marketing costs involved in such a conversion. Because of the smaller-than-expected improvement in efficiency, introduction of the new grid was delayed until a new silver paste capable of printing finer lines is introduced in Phase III, so that those costs would be incurred only once, and not twice in a relatively short span of time.

Figure 2. The distribution of efficiencies of EFG cells from the same lot having two different grid patterns. Although the difference in average efficiency is small, there is a noticeable shift in the peak of the distribution toward higher efficiencies for the cells with the greater number of fingers.



3.2.5 Statistical Process Control

During the course of this PVMaT subcontract it became apparent that improvements in average cell efficiency would be difficult to achieve without first putting into place better methods to analyze variations in cell performance on the production line and relate them to production conditions. Accordingly, it was decided to implement a program of Statistical Process Control (SPC), under which data would be collected at each process step and fed into a database for analysis.

One of the first steps in implementing SPC was to acquire software permitting cell test results to be accessed by all members of management and the engineering staff from the ASE personal computer network. Under the previous system, only a few people had access to cell data, which was stored on a minicomputer, and it would often take days for all staff members to become aware of a production problem. The implementation of a few basic programs on the database made it easy for the first time to call up cell data by growth furnace run, for example, and compare it to other runs to obtain such information as the level of degradation in cell efficiency that could be expected as an EFG die approaches the end of its life. Although such studies had been carried out before, the work was tedious and often out-of-date by the time the results were disseminated. Now every staff member had similar information at his or her fingertips immediately.

As another component of the system for collecting information, bar code printers and readers were installed in both the crystal growth and cell fabrication areas. In the crystal growth area, this allowed the collection of critical information on furnace components, such as the reactor used for purification and purification date, for every growth run. This data was then made available for correlation between such variables as purification process and cell efficiency. In the cell area, the use of bar code readers permitted cell processing data, such as sheet resistivity, to be recorded immediately in digital form, instead of on paper. This eliminated the need for tedious searching through paper records to follow trends in production data.

The component of the SPC program most recently initiated is a program of Design of Experiments (DoE). A consultant was used to set up and direct a large-scale optimization experiment, in which we tested eight variables in various parts of the cell manufacturing process. These ranged from humidity during the application of the dopant to the belt speed of the metallization firing furnace, which were set to either high or low values. Over 4,000 cells were then processed according to 16 different combinations of processing conditions, and the results analyzed with the help of DoE software. The results indicated that a number of the variables produced optimal results over a wide range of setpoints, while a few others were more sensitive than had previously been believed. As expected, it was found that the optimum for most of the process conditions lay close to the setpoints established for production. Those variables that were more sensitive than expected will be studied in further DoE experiments which limit the range of those setpoints, to determine optimum conditions more accurately.

3.2.6 High Efficiency Program

As a result of incremental improvements in the production line, cell efficiency improved gradually over the course of Phase II. One of the largest improvements was seen as a result of reducing average wafer thickness to 275 μm, which raised average efficiency by 0.2% absolute on 50% of ASE Americas' production (as of the end of Phase II, the other 50% of wafers are still produced at the former standard thickness of 300 μm).

Improvements in the purity of the silicon available for crystal growth also occurred during the course of Phase II. During Phase I, the high efficiency effort was hobbled by the necessity of using lower quality silicon in crystal growth because of the worldwide silicon shortage. As better grades of silicon became available once again, the improvements made during the program were able to more clearly show their true impact. As of the end of Phase II, many lots of EFG cells are being produced at average efficiencies of 14.1-14.2%. About 30% of the cells in those lots have average efficiencies equal to or greater than 14.35%, which was the cell efficiency goal for Phase II.

3.3 TASK 6 - IMPROVEMENTS IN ASE MODULE PRODUCTION

3.3.1 Increases in Lamination Throughput

One of the goals of this subcontract was to achieve a reduction in the time required for module lamination, which would reduce the need for expensive capital equipment and its associated floorspace requirements. The need for this improvement arose from differences in flow properties between the proprietary encapsulant material used at ASE Americas and the EVA material used by other manufacturers. Although the ASE encapsulant has been demonstrated to possess better resistance to degradation during outdoor exposure than EVA, it burdened ASE with a competitive disadvantage in the form of lower throughput in the lamination process.

At the beginning of Phase I of this subcontract, work was carried out to investigate a number of alternative materials and processes which might permit faster lamination cycles. Tests were performed on the use of an autoclave for lamination, as is done industrially for the manufacture of automotive safety glass, rather than the vacuum equipment currently used by most PV manufacturers. New encapsulants with improved flow properties were also tested. All of this work was successful in that the new materials and equipment produced test laminates which were acceptable visually and electrically. However, further investigation during Phase II revealed significant problems in proceeding to the next level of testing, in which full-size modules would be laminated and subjected to environmental testing. Although the new encapsulant materials flowed more easily during lamination than ASE's standard encapsulant, they were difficult to handle because they were 'sticky'. Plans were made for dealing with this problem in lamination, only to find out that the same property would cause serious problems for the company extruding the material, forcing them to raise the price for this material above that of the standard encapsulant.

Meanwhile, further investigation of autoclave lamination revealed that the equipment required for lamination of full-size modules was very expensive. While such equipment would have the capacity to laminate a number of modules simultaneously, and so would be competitive with vacuum laminators in terms of capital cost per module produced, the financial risk involved in purchasing a production autoclave was very high.

Faced with this situation, renewed attention was focussed on improving the throughput of ASE's current equipment and materials before making the large expenditures required to pursue the new ones. The most promising approach to accomplishing this objective was to modify the lamination process to permit 'hot' lamination, i.e., not cooling the laminator completely between lamination cycles. This holds some risk when working with ASE's encapsulant, because it does not have the thermosetting properties of EVA, and there is a real possibility of delamination when removing a module from the laminator while it is hot. Testing of this approach therefore required the determination of the maximum laminator temperature at which module could be removed without causing delamination. This turned out to be higher than expected, permitting significant shortening of both the heating and cooling portions of the lamination cycle. A process for producing 50-watt modules was eventually demonstrated which shortened total lamination time by 30%, exceeding the goal of 25% originally set for this program.

The new process must now be adapted for production of the 300-watt modules that comprise most of the product manufactured at ASE Americas, to address challenges specific to the processing of such a large product. As of the end of Phase II, therefore, work is continuing on the development of a faster lamination process using ASE's standard lamination equipment and materials which would be usable for all of ASE's products. With the success achieved to date on the smaller modules, confidence is high that this can be achieved without the major development programs on new equipment and materials that had originally been thought necessary.

3.3.2 New Encapsulants

In addition to the work described in the previous section, other investigations were carried out on new or modified encapsulants. Our search for improved encapsulants had two purposes. First, we need to raise the yield of thinner cells in module fabrication; second, we want to extend prospective module lifetime in the field to greater than 20 years, and are searching for an encapsulant that could improve on the one we presently use.

The first of these programs involved an investigation into the use of liquid encapsulants which would harden through the application of high temperatures or light. Such encapsulants were commonly used by manufacturers of photovoltaics twenty years ago, but their use was largely discontinued once vacuum lamination using EVA became standard practice in the industry. Because of the anticipated costs of adding more vacuum laminators as production volume increases, which would not be necessary using this process, and the broad range of new materials developed in the polymer industry during the past two decades, it was considered prudent to reinvestigate this approach.

Work was subcontracted to a consultant to develop a number of test formulations of liquid-based encapsulants to determine the properties of these materials. Sample coupons were prepared using EFG cells and a variety of test formulations. A few of these demonstrated unacceptable properties after setting, such as delamination from the cell surface, but others produced visually acceptable results. Samples of those materials were then subjected to standard environmental test conditions. Delamination or yellowing of the encapsulant occurred in some of those samples, but a few samples survived the testing without apparent degradation. Cost information for production quantities of these materials has not yet been received; costs based on smaller quantities are significantly higher than those for ASE's standard encapsulant. As of the end of Phase II, therefore, it has been found that the use of liquid-based encapsulants appears to be feasible, but no such material has been identified which is cost-competitive with the standard encapsulant. The search for an economical liquid encapsulant is being continued into Phase III.

In parallel with the work on the liquid encapsulants and the new sheet encapsulant material with improved flow properties, testing was also conducted on a variation on ASE's standard encapsulant material. This material, identified during Phase I as a possible improvement over the standard encapsulant, is based on the same base compounds contained in the standard material, but it contains a different package of additives. The two major improvements offered by this new material are higher clarity, with lower haze, and improved resistance to loss of light transmission during exposure to UV light. Test samples of the new material originally prepared during Phase I were continued in accelerated UV lifetime testing and field testing during Phase II along with control samples of the standard ASE encapsulant. The results of this testing demonstrated that while ASE's proprietary encapsulant shows a lower level of transmission loss than EVA under such exposure, the new material shows nearly none. Modules manufactured using the new material were placed in outdoor testing in Florida to attempt to confirm these results, and as of the end of Phase II the reports received on these modules is consistent with the results of the accelerated indoor testing.

An effort is now being made to obtain production quantities of this new material, which has until now has not been manufactured in large volumes. The availability of larger quantities will permit testing of this material using an improved lamination process as described in the previous section. If that testing is successful, ASE Americas may be using a lower-cost process to produce modules containing improved materials before the end of Phase III.

3.3.3 Reduction in Materials and Labor Costs of Module Framing

During Phase I an effort was made to identify frame constructions which would be less expensive than the industry-standard frames made of extruded aluminum and at the same time reduce the time required for assembling frames to modules. The most promising alternative construction found during this search was one in which the frame is made of roll-formed metal, rather than extruded metal. In Phase II this construction was studied in some detail, working with engineers from a company with long experience in roll forming. The company presented a number of candidate designs for new frames, but when studied by ASE engineers, they were found to be insufficiently stiff to withstand the wind forces encountered by PV modules from

time to time. Unfortunately, the increases in metal thickness required to provide improved stiffness eroded the cost advantage of the roll-forming approach. Only one of the proposed designs was found to be sufficiently stiff for ASE's large 300-watt module, and this design required filling the cross-section of the frame with a polyurethane foam. When the roll-forming manufacturer calculated the cost of this design, it was found to be equivalent to that of the conventional frame made of extruded aluminum. Since there was no cost advantage in switching to the new design, this approach was not pursued further.

Another approach to achieving a substantial cost reduction over conventional frames is the concept of eliminating them almost entirely. The logic of this approach is that good structural engineering practice dictates that no structure should contain multiple load-bearing elements that carry the same load. The frames of PV modules are generally designed to provide support for all of the wind loads to which the modules are subjected, but the support structure to which the frames are mounted must carry exactly the same loads. That being the case, small mounting brackets which transfer wind loads from the module to the underlying structure perform the same function as the large frames, but at much lower cost.

Two ASE engineers had an opportunity to observe the application of this concept during a visit to PV installations in Europe, in which this mounting approach was used. The modules in these installations were clearly well supported, using far less material than is used in conventional frames on American PV modules. After this visit, initial design work was carried out to engineer a mounting bracket that would be compatible with ASE modules, and would provide mounting locations compatible with standard ASE frames. As of the end of Phase II, these designs are not yet finalized. It is expected, however, that this approach will be developed sufficiently to be used on ASE modules by the end of Phase III.

3.3.4 Reduction in Cost of Diode Housing

The large 300 W module manufactured by ASE Americas is most commonly supplied with electrical quick connectors to provide connections between modules. Therefore, it does not require a junction box *per se.* However, it does require diode protection to minimize problems associated with hotspot heating due to uneven illumination. The protective diodes are mounted on a circuit board enclosed in a housing on the rear of the module. A large part of the housing cost arises because of the use of an extruded and machined aluminum cover on the housing, which provides a heat sink which dissipates the heat generated by the diodes during the rare instances when they are operating.

A reevaluation of this design was called for in response to new customer demands. This prompted a review of the diode assembly, which resulted in the discovery of an opportunity to change the configuration so as to reduce the heat load. The new design was tested both indoors and outdoors and found to function as predicted, while meeting all requirements for certification. Due to the reduction in heat load, the requirements for heat dissipation using this design were reduced as well. This permits the elimination of the aluminum radiator, to provide a substantial reduction in the cost of such a design.

As of the end of Phase I, a circuit card and preliminary housing design had been developed, and a mockup of the housing was undergoing testing to evaluate its thermal performance. Those tests were completed successfully, and design work was started on the mold for the diode housing itself. In the meantime, a few samples of the new housing were produced by rapid prototyping and distributed to customers to obtain feedback on the new design. That feedback indicated that customers wanted to be able to connect to the housing using any of a number of methods, including cable attached through watertight fittings and various types of electrical conduit, and the design was modified to make this possible. Underwriters Laboratories (UL) determined in their evaluation of the prototype that the circuit card should be modified so that wires would be held by mechanical clamping in addition to the solder bonds, and the circuit card had to be modified to permit this change. Specifications were developed for feedthroughs and strain reliefs, and a special clip was designed to hold the diodes in contact with a heat sink, with the clips in turn locked in place by the lid of the housing. Eight modules were constructed using prototype diode housings and subjected to the standard series of environmental tests, which they passed without difficulty. In order to ensure that the new construction would be accepted by the widest possible range of customers, it was decided that it should be tested as well according to IEEE standard 1262. A number of test modules were sent to Arizona State University for this testing, which is scheduled for completion early in Phase III. Prototypes of the final design were also sent to UL, which is expected to approve the design within the next few months.

Current plans call for introduction of the new diode housing on standard ASE modules midway through Phase III. Due to the elimination of the metal radiator and other components made unnecessary by the new design, use of the new housing reduces the cost of converting a laminate into a framed, customer-ready module by 15%, and reduces the cost of the entire module by 2.5%.

3.3.5 New Flat-Plate Concentrator Design

As was described in section 3.2.1 of this report, an effort was made during Phase I of this subcontract to develop a textured coating that would enhance the collection of light at the cell surface, and this effort was ultimately unsuccessful. At the end of Phase I another concept was developed for improving the collection of light, but on the module level, rather than the cell level, by allowing the efficient collection of light from the spaces between cells in the module. The optical path which the light would follow in this concept was somewhat complicated, and so a consultant was assigned the task of calculating the potential improvement that might be expected from a module design employing the concept. Soon after the conclusion was reached that the cell texturing approach would not work, the consultant reported that his calculations showed that the new module concept would work, and that it had the potential to increase the amount of current collected by a given number of cells by as much as 50% or more, depending on the size and geometry of the cells. Accordingly, the resources that had been earmarked for the completion of the cell texturing work were redirected toward the new module design, which has been designated a Flat-Plate Concentrator (FPC).

The principle of the FPC is that light that strikes in between cells is reflected by a highly reflective surface, and the redirected light rays then strike the interface between the glass and the

surrounding air, which reflects them once again, this final time in the direction of a nearby solar cell. This principle is actually used in most commercial PV modules, where the reflecting medium in between cells is a white or blue layer on the inside of the module backskin. Studies have shown that the additional light collected from the pigmented layer as compared to the use of a black backskin is on the order of two to three percent, and that the light is collected from a distance of a few millimeters from each cell edge. The advantage of the new FPC design is that it collects light from a distance of 20 millimeters or more, and at a much higher efficiency than is possible with conventional backskin materials.

The major task in reducing the FPC concept to practice was in locating a supplier who could produce the required reflective material. Eventually, such a vendor was located, and an order was placed for sample quantities. When the sample arrived, a number of problems were encountered in trying to use it to make test coupons. When it was laminated using ASE's standard module construction, the reflectivity was not as high as had been expected, and some yellowing of the material was observed. Further testing revealed that these problems were due to degradation of the reflective material due to the high temperatures used for lamination. In order to evaluate the true potential of the material, a second set of laminations was carried out using a room-temperature curing encapsulant, and the resulting reflectivity was found to be as high as originally expected. The encapsulant employed for that test, however, was very difficult to use. In order to achieve a reproducible lamination process, it was necessary to switch to yet a third encapsulant system, which could be used at temperatures between those used in the first two tests.

Although it was not possible to eliminate all air bubbles from the laminates made using this encapsulant, the large improvements expected for the FPC design were clearly demonstrated. A first series of coupons exhibited improvements in collected power of an encapsulated cell of as much as 22% over that obtained with the same cell before encapsulation. In the second series, the improvements ranged up to 25%. These samples were sent to NREL as program deliverables.

Work is now being performed to develop full modules employing the new reflective material, and a patent disclosure is being prepared on the new module design.

4.0 PVMaT PROGRAM ACTIVITIES FOR PHASE III

Over the course of the coming year, ASE Americas Inc. will carry out the final phase (Phase III) of the program in Phase 4A2 on the reduction of the cost of EFG modules. During the final year of the program, efforts will be focussed on reaching the primary program goals:

a) a reduction in EFG wafer thickness to 250 microns from the current thickness of 275 microns (down from 300 microns at the beginning of Phase I);
b) implementation of improvements and new processes and manufacturing control systems throughout the cell and module manufacturing areas;
c) implementation of new processing and designs in module manufacturing to reduce module cost.

During Phase I and Phase II, the groundwork was laid for the final accomplishment of these objectives, and that early work has already resulted in a reduction in module cost of 15%. The major overall goal for Phase III is to achieve a further cost reduction of 10%.

The specific tasks to be addressed in Phase III are summarized below.

Task 7: Wafer Manufacturing

- Development of improved laser cutting equipment and processes to permit the cutting of thin silicon tubes with high production yields
- Reduction of EFG wafer thickness to 250 μm

Task 8: Cell Manufacturing

- Reduction in contamination of EFG wafers during cell processing, leading to higher average cell efficiencies
- The establishment of procedures for Statistical Process Control (SPC) of the cell manufacturing line and the writing of a manual describing those procedures
- Implementation of the new HF vapor diffusion glass etch process in production
- Reduction in the width of grid fingers to reduce cell shadowing
- Finalization and testing of a 40 finger metallization grid on the manufacturing line, with the goal of improving cell efficiency

Task 9: Module Manufacturing

- Full introduction of the new diode housing in module manufacturing
- Introduction of an improved encapsulant in module manufacturing

- The introduction into production of a lower cost alternative to ASE's standard glass sheet as the rear side of modules
- The production of full-scale prototypes of Flat-Plate Concentrator (FPC) modules
- The demonstration of module designs with mounting supports other than traditional extruded frames, as a low-cost module construction

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13. ABSTRACT *(Maximum 200 words)*

This report summarizes the progress made at ASE Americas Inc. during Phase II of this subcontract. Accomplishments under *Task 4: Wafers* include optimization of edge-defined film-fed growth (EFG) crystal growth variables, leading to reduced crystal stresses and improved wafer flatness; increased die run length due to improvements in the design of furnace components; construction and testing of EFG growth furnace enclosure; reduction of EFG wafer thickness from 300 μm for 50% of all standard production material; implementation of new equipment to reduce costs of silicon feedstock sorting prior to EFG crystal growth with a 3% increase in silicon feedstock utilization; and development work demonstrating the laser cutting of EFG wafers at higher speeds and with reduced silicon damage. Accomplishments under *Task 5: Cells* include characterization of cells after diffusion as preliminary work toward improving diffusion conditions and improving cell efficiency; demonstration of a continuous process to remove phosphorous glass from diffused wafers, reducing chemical consumption and hazardous waste by 98%; development of statistical process control methods to improve cell production process control; the use of design of experiments to study interactions between processing at various steps in cell manufacturing, and to develop strategies for productivity improvements; improvements in EFG cell efficiency due to the reduction in average wafer thickness; design and construction of equipment for producing cells with an improved grid design; and demonstration of average efficiencies over 14.1% on production lots of EFG cells. Accomplishments under *Task 6: Modules* include production and successful testing of prototypes of a lower-cost module diode housing; successful demonstration of a module design that greatly improves collection of light from space between cells in modules; testing of new encapsulants and lamination processes to demonstrate reduced lamination time, improved yield and enhanced durability; and completion of options study for lower-cost module frames, and development of a frameless module design using mounting clamps.

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