

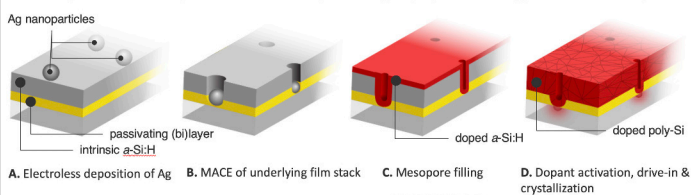
Abstract

- Poly-Si on thick dielectric(s) are passivating contact structures that require pinholes in the dielectric layer(s) for effective charge-carrier transport.
- Poly-Si on SiO_x contacts with thermally induced pinholes have enabled solar cells with > 26% efficiency, but additional thermal processing increases costs
- Pinholes can also be formed via metal-assisted chemical etching (MACE)
- Recently, poly-Si on dielectric(s) with MACE-induced pinholes have enabled certified efficiencies > 22.5% with Voc = 726–729 mV
- We need to determine how the structure and charge-carrier transport of MACE-induced pinholes relates to that of thermally-induced pinholes, then the MACE process may be controlled and optimized to a level that will attract industry adoption

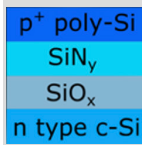
Contact Formation Process

Metal-Assisted Chemical Etching (MACE)

Polysilicon on Locally Etched Dielectrics – processing steps (can also be applied to textured c-Si)



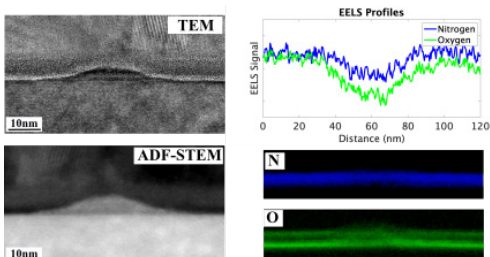
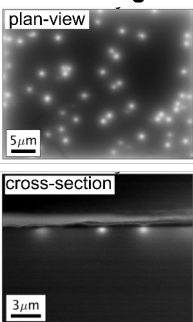
- In this work we study Poly-Si on Locally Etched Nitride and Oxide (PLENO) passivating contact structures
- Electron beam induced current (EBIC), TEM phase contrast imaging, and STEM EELS composition mapping are used to determine the structural and chemical properties of MACE-induced pinholes



Salles, C. L. et al. in *AIP Conference Proceedings*, vol. 2487, no. 1, p. 020011. AIP Publishing LLC, 2022

PLENO on Saw-Damage Etched Wafer

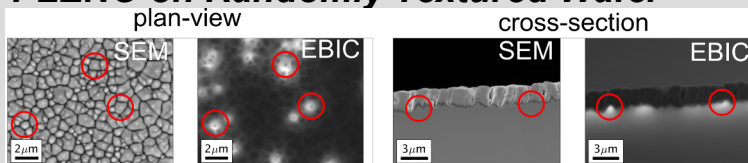
EBIC Images



(left) EBIC images showing pinholes as bright spots (middle) TEM images of region near a bright spot in the EBIC images and (right) horizontal EELS profiles across the bump feature in the TEM images.

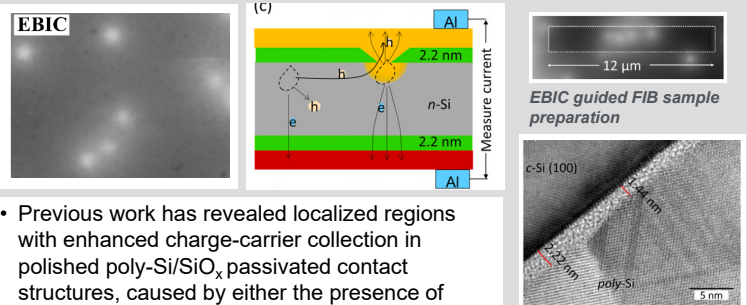
- EBIC images of pinholes in PLENO sample in plan-view orientation appear similar to EBIC images of thermally-induced pinholes
- STEM-EELS analysis reveals a decrease in both the SiO_x and SiN_y indicating pinhole formation in these layers resulting from the MACE process

PLENO on Randomly Textured Wafer



- EBIC images on PLENO sample with random texturing in plan-view orientation may suggest the pinholes are confined to specific pyramids
- In cross-section, the EBIC images suggest that the pinholes may form preferentially at or near the pyramid tips

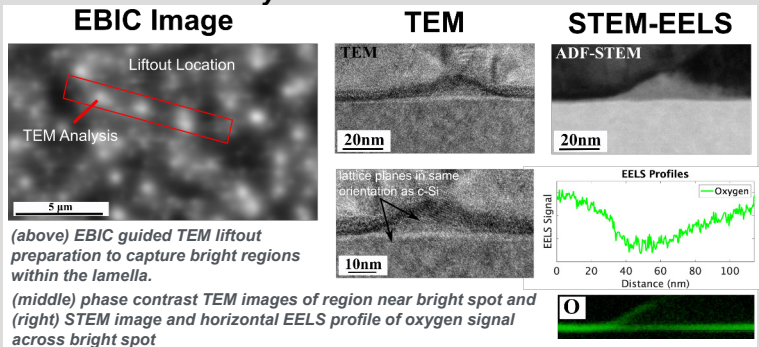
Previous Work on Thermally-Induced Pinholes



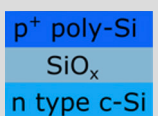
- Previous work has revealed localized regions with enhanced charge-carrier collection in polished poly-Si/SiO_x passivated contact structures, caused by either the presence of pinholes or local SiO_x thinning
- Pinholes in SiO_x layer enable charge-carrier transport on otherwise insulating SiO_x (>2nm)

Kale, A.S., et al *Applied Physics Letters*, 2019, 114, (8), pp. 083902

Correlative EBIC – TEM – STEM EELS PLEO (no SiN_y layer)



- EBIC guided FIB used to target specific bright spots for TEM sample preparation
- Bump observed near the bright spot location exhibits lattice fringes in the same orientation as the c-Si substrate, suggesting epitaxial growth from the substrate during crystallization of the poly-Si
- A decrease in the oxygen signal is observed in horizontal EELS profiles across this feature indicating pinhole formation from the MACE process



Summary

- Enhanced local charge-carrier collection on MACE-processed PLENO on saw-damage etched wafers is similar to EBIC measurements of thermally-induced pinholes
- TEM and STEM-EELS analysis shows that the MACE process effectively creates pinholes not only in SiO_x, but also in SiO_y/SiN_y dielectric bilayers
- This is critical to enable transport through the thick SiO_x/SiN_y, which provides surface passivation and barriers to Boron in-diffusion
- **Inducing pinholes in thick dielectric layers with the MACE process results in similar charge-carrier transport behavior as observed for thermally-induced pinholes**
- **Recent certified efficiencies > 22.5% in solar cells with PLEO and PLENO contacts indicate the MACE process may provide a viable future direction for industrially produced solar cells with passivating contacts as long as MACE processing costs are minimized**