Modeling and Feedback Compensator Design for Power-Hardware-in-the-Loop System for Medium-Voltage Grid-Connected Power Converters

Preprint

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Modeling and Feedback Compensator Design for Power-Hardware-in-the-Loop System for Medium-Voltage Grid-Connected Power Converters

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***Abstract*— Hardware-in-the-loop (HIL) evaluation is a method in which the test subject is split into a physical part and a simulated part, and these parts are connected with interfaces to form a combined physical-numerical system. Power-hardware-in-the-loop (PHIL) systems, where actual hardware is connected to a real-time model, can exhibit issues of instability, inaccuracy and errors when operating in a closed-loop. The challenges of generating a PHIL setup are that, first, because of the limited dynamic response of the different parts of the system, the test results might be inaccurate, and, second, because of the high frequency noise introduced by the sensors to the closed-loop system, it can be difficult to design a compensator for the real-time emulator response, while stabilizing the closed-loop system at the same time. In this paper, different parts of a PHIL system are characterized, and the feedback compensator system design is proposed for the stable operation of the closed-loop PHIL system. The issues as observed in a PHIL system without any compensator are demonstrated using experimental results, and the effectiveness of a first order phase lead compensator is validated.**

Keywords— Power-hardware-in-the-loop (PHIL), medium-voltage converter, compensator design

I. INTRODUCTION

The increasing presence of distributed energy resources in the power grid has resulted in increased power converters as interfaces to these energy resources [1] – [3]. It is estimated that the medium-voltage (MV) grid is utilized for injecting approximately 99% of the power generated by the present photovoltaic (PV) power plants in the world [4] – [7]. The increase in MV power converters on the grid leads to new challenges for ensuring system stability. It becomes absolutely necessary to evaluate these converters and the associated control techniques for most real-life scenarios under laboratory conditions before deployment in the field. To have realistic evaluation techniques, it is important to have well defined and accurate test setups. In this paper, a power-hardware-in-the-loop (PHIL) system is developed and characterized, and a compensation system is developed for the accurate and realistic evaluation of power converters connected to the power grid. PHIL systems with compensation techniques have been used in the past for system evaluations [8]–[11]. Most of these techniques focus on the stable operation of the PHIL system, which does not guarantee an accurate and high bandwidth performance. With the advent of fast-switching power devices, there is a need for high-bandwidth PHIL evaluation techniques. Section II presents the details of the different test configurations used for characterization of different parts of a PHIL system. Section II also discusses the various parts of the model, such as the grid simulator, along with experimental results demonstrating the inaccuracies that can arise in a PHIL setup. Section III presents the developed feedback compensation technique. Section IV includes details of the analytical design and validation results of the lead compensator. It also includes results from the characterization and connection of the PHIL setup to the three-phase, 13.2-kV grid for MV evaluations. Finally, Section V concludes the paper.

II. PHIL SYSTEM CONFIGURATION AND CHARACTERIZATION

Multiple system configurations were used in the modeling and characterization of various parts of the system. This section briefly discusses the test setup used for these evaluations. The full PHIL system configuration created to design the feedback compensator of the system is shown in Fig. 1. This system is a closed-loop PHIL setup comprising of a PV emulator fed PV inverter connected to a grid simulator. The grid simulator acts as the point of common coupling (PCC) in a larger network modeled in a digital real-time simulator (OPAL-RT in this case). The current injected or absorbed from the network is sent as feedback to the network model to generate the voltage reference signals at the PCC.

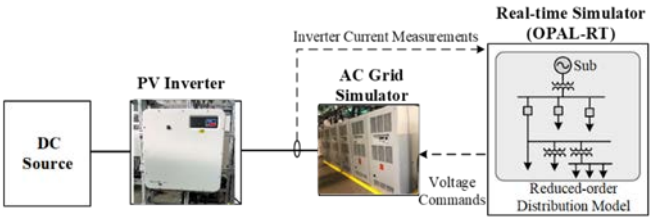

Fig. 1. Schematic of the PHIL setup used for characterization and feedback. Photos by NREL

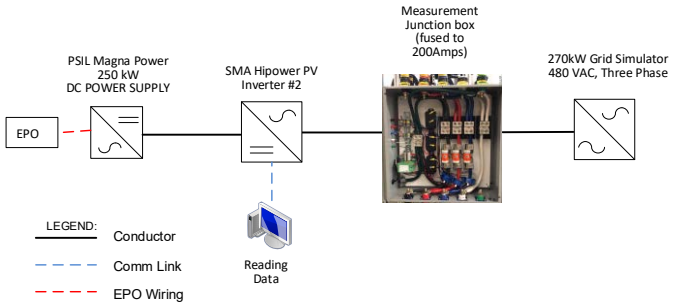

Fig. 2. Simplified system configuration for inverter and sensing characterization. Photo by NREL

To identify the system delays and sensing errors, some baseline tests using the simplified system configuration are shown in Fig. 2. This system includes a PV inverter fed by a PV emulator and connected to a grid simulator and local load. Multiple tests were done to baseline the inverter and other parts of the network such as the grid simulator, communications blocks, and measurement systems for the PHIL system.

Multiple tests were executed using this setup to characterize the different component accuracies, delays, and response of individual components as well as the data acquisition system. These tests included grid voltage changes, active power setpoint changes, reactive power setpoint changes, and power factor command changes. Multiple such tests were done to characterize and quantify system delays and accuracies. Fig. 3 shows the error between the voltage measured at the PCC and the voltage reference. The voltage discrepancies between the reference voltage and the PCC voltage are due to drop across the impedance network between the PCC and the sensing point. These discrepancies will result in incorrect current magnitudes and phase angles when operating in a closed-loop PHIL system. This necessitates mitigating these discrepancies through a compensation system, which is being proposed in this paper.

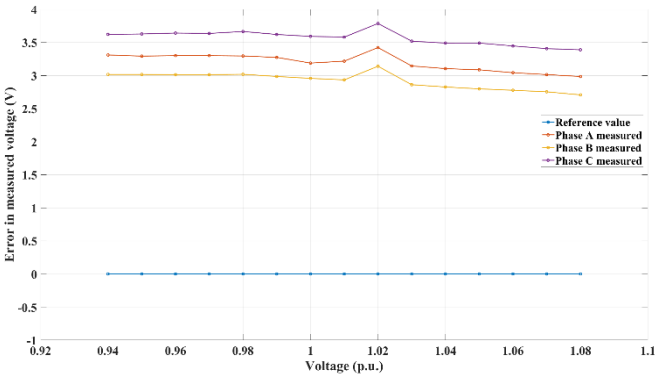

Fig. 3. Voltage sense discrepancies between grid simulator and inverter PCC.

In addition to the voltage magnitude errors, the system delays from the ADCs/DACs and the grid simulator performance need to be identified for the accurate design of the feedback compensation system. The grid simulator used for this characterization and the PHIL setup is a three-phase, 480 V_{LL}, 270 kVA system, as shown in Fig. 2. The grid simulator characterization was performed using variations of the grid simulator output voltages with the injection of harmonics and variation of the loads in the resistive load banks. The grid simulator was injected with 5% harmonic content on top of the fundamental voltage from 2nd harmonic to 72nd harmonic. The loads were operated at 0%, 25%, 50%, and 75%. Each harmonic level was tested at each load point. The frequency domain analysis of the experimental data (see Table I) was used to identify the transfer function of the grid simulator. The obtained transfer function for the grid simulator is presented in (1).

TABLE I. MODEL PARAMETERS FOR THIRD ORDER TRANSFER FUNCTION

$V_{mag}(pu)$	$R_{load}(\Omega)$	G	$f_{p1}(Hz)$	$f_{z1}(Hz)$	$f_{p2}(Hz)$	$f_{p3}(Hz)$	$T_{del}(\mu s)$
1.0	No load	1	819	963	3503	3503	30
1.0	3.4	1	819	963	3503	3503	30
1.0	1.7	1	819	963	3503	3503	30
1.0	1.2	1	819	963	3503	3503	30

$$H_{GS}(s) = \frac{V_{out}(s)}{V_{ref}(s)} = \frac{G\left(\frac{s}{2\pi f_{z1}}+1\right)}{\left(\frac{s}{2\pi f_{p1}}+1\right)\left(\frac{s}{2\pi f_{p2}}+1\right)\left(\frac{s}{2\pi f_{p3}}+1\right)} e^{-sT_{del}} \quad (1)$$

where $f_{p1} = 819\,Hz$, $f_{z1} = 963\,Hz, f_{p2} = f_{p3} = 3503\,Hz, T_{del} = 30\mu s$. The variation of harmonics was injected with the fundamental voltage using analog input to the grid simulator and the output voltage of the grid simulator was used to determine the transfer function of the grid simulator. The Bode plot for the transfer function thus derived is presented in Fig. 4.

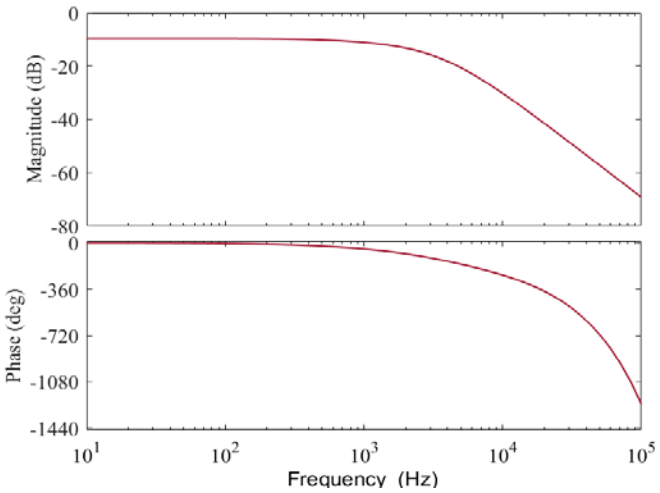

Fig. 4. Bode plot for the grid simulator transfer function as derived from experimental results.

A PHIL setup has been chosen to develop compensation techniques and characterizations techniques to overcome the abovementioned issues. The laboratory single-line diagram for this testcase is shown in Fig. 5. This setup includes a PV emulator fed PV inverter connected to a grid simulator and a local load, with the grid simulator acting as the PCC in a larger

network modeled in the OPAL-RT real-time simulator. The current injected or absorbed from the network is sent as feedback to the network model to generate the reference voltage signals at the PCC. The end goal is for the inverter to have a voltage value at PCC that is representative of the model and not dominated by the characteristics of the measurement equipment including the grid simulator itself.

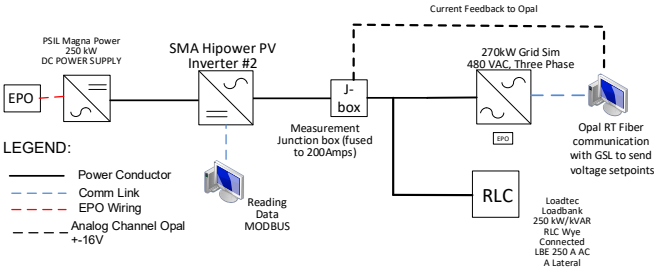

Fig. 5. Test setup for closed-loop PHIL assessment.

III. FEEDBACK COMPENSATION SYSTEM DESIGN

The first steps were to design the feedback compensation system that will help mitigate measurement errors (see Fig. 3) and delays due to the real-time simulator ADCs and DACs. To develop the compensation system, the three phases of the system are considered as three identical single-phase systems. This assumption for the system is valid and does not introduce any error because the cross-coupling between the phases is very weak. The simplified block diagram of the closed-loop PHIL compensation system designed in this paper is shown in Fig. 6. The compensation system is divided into three parts as the real PHIL system. The Feeder Model is the equivalent circuit for the system modeled in the digital real-time simulator. The second block, the PHIL Compensation is the designed feedback compensator. The PV Inverter in the block diagram refers to the hardware setup tested in Fig. 2. All the other blocks in between are derived from the characterization presented in the previous section. The compensation system is designed using proportional-resonance (PR) controllers (see Fig. 6). These help with the overall bandwidth and response of the system compared to the traditional proportional-integral (PI) controllers. For the design, the feeder model is reduced to the Thevenin equivalent circuit as seen by the PV inverter terminal. The Bode plot for the simplified lead version of the feedback compensator is shown in Fig. 7. The compensator is simplified to represent a lead compensator in this case.

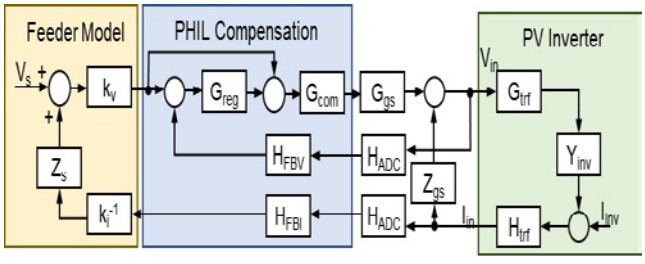

Fig. 6. Block diagram of the designed feedback compensation system.

IV. LEAD COMPENSATOR DESIGN

With the voltage reference to the grid simulator provided by the OPAL-RT system, some delay is introduced into the system, which can be estimated by the time delay between the input and the output signal. To estimate the time delay between the input and output signals, the input signals such as input phase voltage and output phase voltage are stored in the MATLAB workspace.

For estimating the time delay, the input reference signal and the output signal are saved in the MATLAB workspace. The sampling frequency and the number of points are specified to generate a time value. The time value will be used for plotting the signals. From the input and output signals logged in the workspace, the bias is removed from the signals. Then, the fast Fourier transform is performed on the input and output signals. Then, the number of unique points is estimated.

This is followed by plotting of the magnitude and phase response of the signals. The absolute of the maximum magnitude value with its index is determined. This process is performed for both the input and output signals. The output of this index is used to determine the phase lag between the two signals. This is how the estimate of the time delay is determined. This process was estimated for three phases of the voltage waveform, as shown in Table II

TABLE II. ESTIMATE OF TIME DELAY OF VOLTAGE WAVEFORMS FROM THE SIMULINK MODEL.

Time delay – Model based	Phase A (µs)	Phase B (µs)	Phase C (µs)
277V with no harmonics	**149.30**	**156.43**	**142.64**
277V with 5% 120 Hz	**149.51**	**156.76**	**142.28**
277V with 5% 180 Hz	**149.13**	**156.75**	**142.28**
277V with 5% 4260 Hz	**149.17**	**156.53**	**142.52**
277V with 5% 4320 Hz	**149.17**	**156.53**	**142.52**

The time delay is estimated to be approximately 150 µs. This is a non-trivial time delay that must be accounted for. To compensate for the time delay, a lead compensator must be developed, that can account for the time delay. The lead compensator was developed based on the work performed in [13]. The lead compensator is assumed to be a single pole single zero system with a gain. With the estimated delay around 150 µs for all phases, the transfer function calculated for the lead compensator, LD(s), is expressed as follows:

$$LD(s) = \frac{(1.058s + 377)}{(s + 399.9)} \qquad (2)$$

The lead compensator was designed for output lag conditions less than one-fourth of the fundamental cycle. After implementing the lead compensator for each phase, the input and output signals were again stored in the workspace and the time delay between them were re-estimated, shown below in Table iii. The Bode plot of the lead compensator is shown in Fig. 7. Fig. 8 shows the comparison of uncompensated grid output voltage versus the grid output voltage compensated with the lead compensator, plotted with the analog input reference fed to the grid simulator from the OPAL-RT analog outputs.

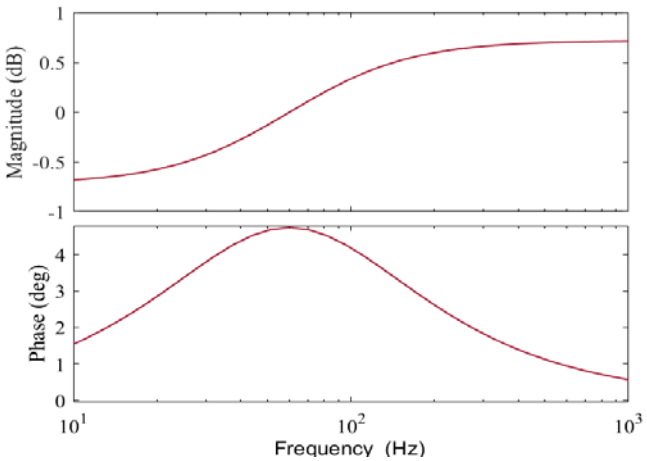

Fig. 7. Bode plot of the simplified feedback compensator

TABLE III. COMPARISON OF DELAY ESTIMATES BETWEEN COMPENSATED AND UNCOMPENSATED SYSTEM

	Uncompensated delay	Compensated delay
Phase A	149.51µs	1.1 µs
Phase B	156.76µs	0.7 µs
Phase C	142.28µs	1.4 µs

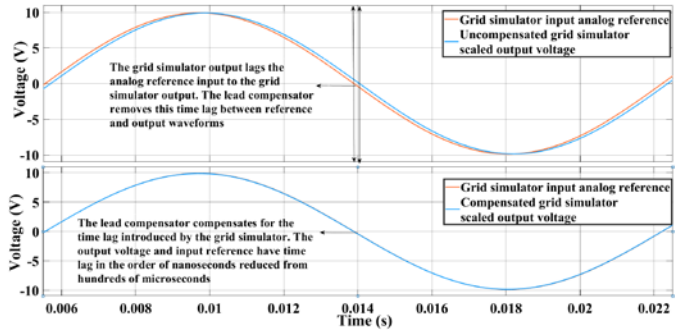

Fig. 8. Comparison of uncompensated and compensated grid simulator output voltage waveform with input reference analog voltage to the grid simulator.

The lead compensator was also validated for the test voltage waveforms with harmonics, and the compensator was able to reduce the lag time between the input reference and the output waveform, shown in Fig. 9.

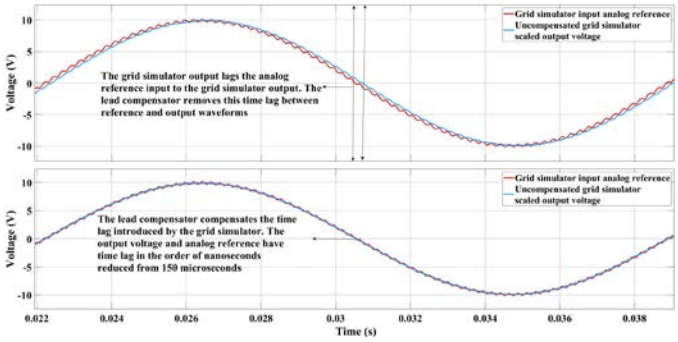

Fig. 9. Comparison of uncompensated and compensated grid simulator output voltage waveform with input reference analog voltage to the grid simulator for input voltage with 70th harmonic

V. CONCLUSION

The paper presents the test setup to characterize different parts of a PHIL setup. The models of different parts of a PHIL setup have been developed and presented. Further, experimental results showing poor voltage tracking and delays in the system have been presented. A feedback compensator that can be used to account for the inaccuracies and instability in the system has been proposed. The paper also includes the details of all the characterizations, the design of the compensator, and the experimental validation of the effectiveness of the compensator.

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