FedIMPACT-Patina Copper Nitride Project

Cooperative Research and Development Final Report

CRADA Number: CRD-16-605

NREL Technical Contacts: Andriy Zakutayev and Sage Bauers

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Contract No. DE-AC36-08GO28308

Technical Report
NREL/TP-5K00-76736
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Golden, CO 80401
303-275-3000 • www.nrel.gov

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Report Date: 2/27/20

In accordance with requirements set forth in the terms of the CRADA agreement, this document is the final CRADA report, including a list of subject inventions, to be forwarded to the DOE Office of Scientific and Technical Information as part of the commitment to the public to demonstrate results of federally funded research.

Parties to the Agreement: FedIMPACT, LLC

CRADA number: CRD-16-605

CRADA Title: FedIMPACT-Patina Copper Nitride Project

Joint Work Statement Funding Table showing DOE commitment:

No NREL Shared Resources

Estimated Costs	NREL Shared Resources a/k/a Government In-Kind
Year 1	$.00
TOTALS	$.00

Abstract of CRADA Work:
There are several areas of interest with regard to advancing renewable energy technology and increasing Participant's use of renewable energy. Participant would like to collectively work with the National Renewable Energy Laboratory on a variety of projects as outlined in part by the statement of work below.

Summary of Research Results:
This project was aimed to synthesize Cu_3N thin films, to evaluate the possibility of fabrication of Cu_3N -based electronic devices, and to assess the potential for their long-tern stability. The corresponding tasks included (1) Growth and Characterization of Doped Cu_3N films, (2) Fabrication of Cu_3N p-i-n photodetectors; (3) Fabrication of functioning Cu_3N transistors, and (4) Metastability Tests. The summary of technical results for each of these tasks is presented below.

1. **Grow and Characterize Doped Cu_3N films.**

Growth conditions for high quality Cu_3N with controllable p- and n-type doping were established by sputtering Cu in activated nitrogen gas (Fig. 1a). This work was achieved using a design-of experiments approach where minimizing the conductivity of the deposited thin films was used as a proxy for the highest-quality (most intrinsic) Cu_3N material. We also found that post-treatment of Cu_3N by storing in a UHV environment resulted in lowering of the conductivity relative to as-deposited samples. With optimal growth and treatment conditions, conductivities under 10^{-3} S/cm and carrier densities on the order of 10^{16} cm^{-3} were achievable at a growth rate of approximately 3nm/min (Fig. 1). These material properties were deemed suitable for device integration.

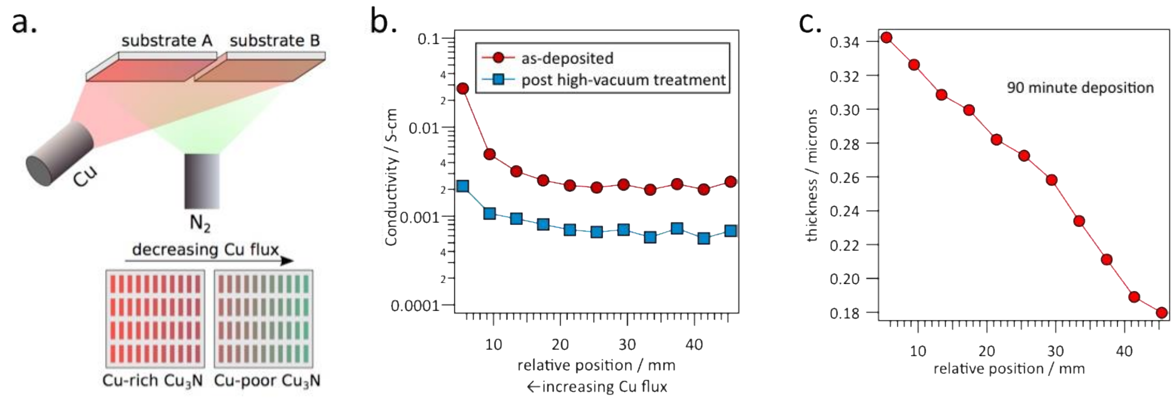

Figure 1:Cu_3N thin film properties. (a) Deposition layout results in graded Cu flux over substrate surface. (b) Conductivity as a function of position / copper flux in Cu_3N thin films both as-deposited and post vacuum treatment. (c) Film thickness as a function of position indicates highly resistive phase-pure Cu_3N can be made at a rate of ~3 nm min^{-1}.

2. Fabricate Cu_3N *p-i-n* photodetectors.

During our materials growth experiments, we found several growth parameters could be used to control the Cu_3N quality and dopant type (e.g. temperature, pressure, Cu flux). We attempted growing Cu_3N diodes on indium tin oxide coated glass substrates by varying these parameters to target a layered n-type/p-type (or vice-versa) Cu_3N stack. An example approach and device layout is shown in Fig. 2. Neither photoconductivity nor rectification in pn-diodes were observed in optimized Cu_3N, so we consulted with FedIMPACT and decided to focus device efforts on thin-film transistors (TFTs). Recent work published by other groups has also documented an inability to prepare high-quality Cu_3N homojunctions (doi.org/10.1016/j.jallcom.2019.02.268).

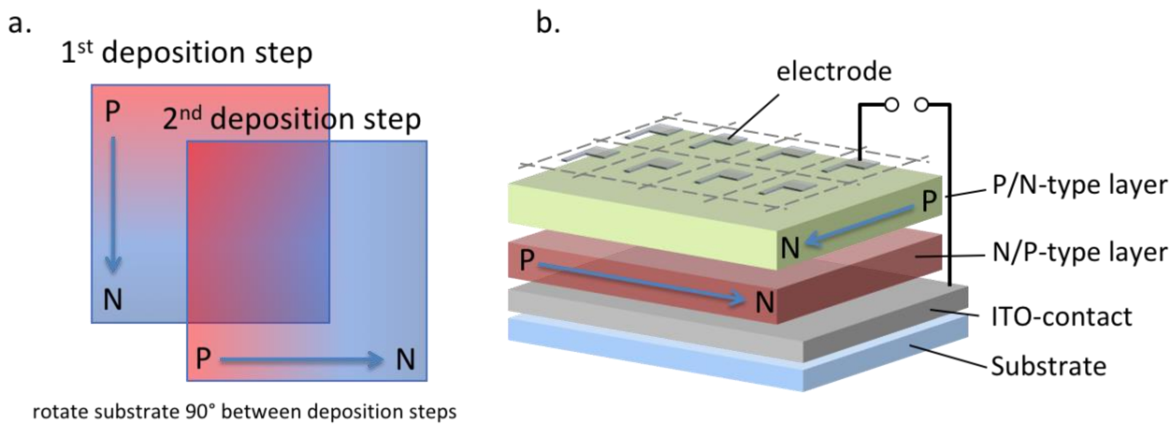

Figure 2: All-Cu_3N diode fabrication approach. (a) pn junctions fabricated by exposing layers to different Cu fluxes. (b) Schematic of complete diode device stack.

3. Fabricate functioning Cu_3N transistor.

Using our optimized Cu_3N recipe, we fabricated TFT transistors using a $Si/SiO_2/Cu_3N/Au$ stack. A semi-automated data collection and analysis routine was also developed for TFT characterization, since our experimental approach resulted in parallel fabrication of 88 distinct devices. The standard Cu_3N TFT device layout is shown in Fig. 3. Several variations to this geometry were attempted, such as different channel lengths, electrode materials, and a planar TFT layout. Additional experiments such as dielectric processing, contact annealing, and adjusting Cu_3N layer thickness were also carried out. Despite our efforts, where over 1500 TFT devices were fabricated, we were unable to fabricate a well-functioning device.

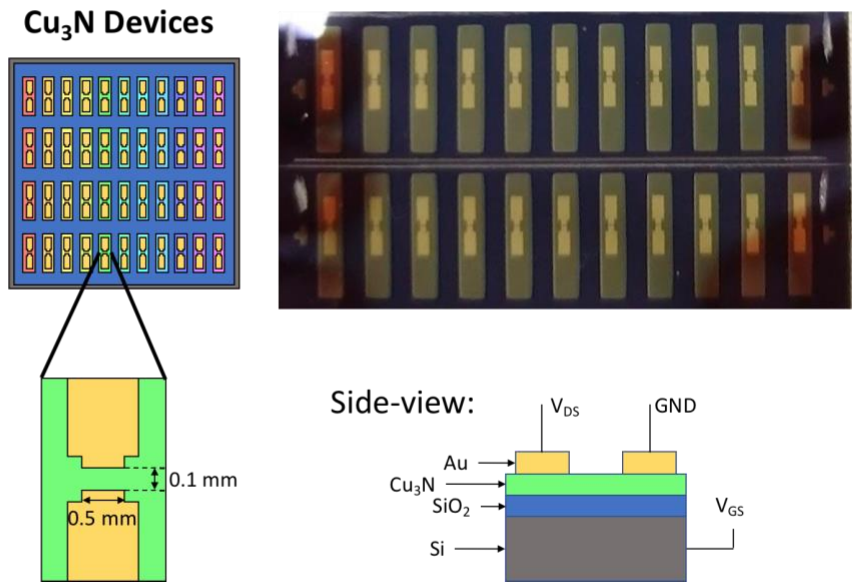

Figure 3: Cu_3N TFTs. Schematic layout and photograph of TFTs fabricated from Cu_3N channel layers.

4. Metastability Test.

Cu_3N was tested for stability by annealing at 100°C in vacuum. Unlike Cu_3N kept in vacuum at ambient temperature, we observed degradation of both the structure and the electrical properties. Fig. 4a shows metallic Cu in the diffraction signal of annealed Cu_3N, while Fig. 4b shows a corresponding increase in conductivity. Annealing Cu_3N in an air atmosphere resulted in similar degradation to copper oxide. These experiments suggest that thermal treatment is unlikely to improve Cu_3N device performance. Furthermore, since semiconductor devices typically operate at elevated temperatures the limited thermal stability of Cu_3N needs to be addressed before it becomes technologically feasible.

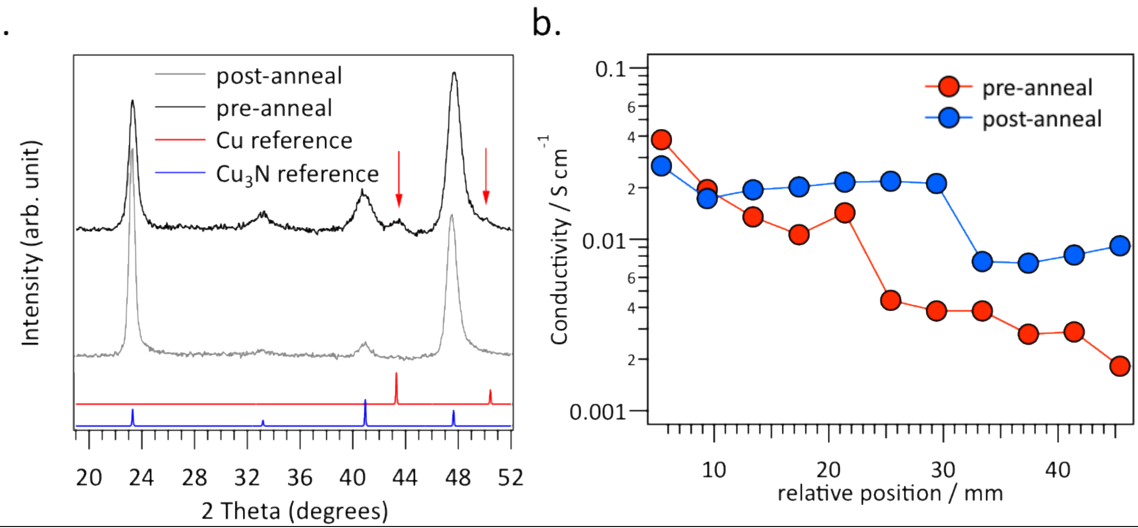

Figure 4: Cu3N thermal degradation. (a) Diffraction of Cu3N before and after annealing in high vacuum environment. Degradation is observed both in poorer signal from Cu3N and emergent peaks from Cu metal. (b) Increase in conductivity from annealed samples due to loss of nitrogen and formation of Cu metal.

<u>Subject Inventions Listing</u>:

None

<u>ROI #</u>:

None

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Office of Energy Efficiency and Renewable Energy (EERE), Solar Energy Technology Office (SETO)