Photovoltaic Inverter Reliability Assessment

Adarsh Nagarajan, Ramanathan Thiagarajan, Ingrid Repins, and Peter Hacke

National Renewable Energy Laboratory

NREL is a national laboratory of the U.S. Department of Energy
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NREL/TP-5D00-74462
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Cover Photos by Dennis Schroeder: (clockwise, left to right) NREL 51934, NREL 45897, NREL 42160, NREL 45891, NREL 48097, NREL 46526.

List of Acronyms

DOE	U.S. Department of Energy
FIT	failure in time
IEC	International Electrotechnical Commission
IGBT	insulated-gate bipolar transistor
MLPE	module-level power electronics
MOSFET	metal-oxide-semiconductor field-effect transistor
MTTF	mean time to failure
PV	photovoltaic
TMY	typical meteorological year
VAR	volt ampere reactive

Executive Summary

As the price of photovoltaic (PV) modules decreases, the price of power electronics becomes more important because they now constitute 8%–12% of the total lifetime PV system cost. As of 2017, the inverter and associated power conditioning components accounted for $0.15/W–$0.17/W of residential applications, significantly more than the U.S. Department of Energy (DOE) benchmark of $0.12/W by 2020. As efforts to reduce PV module costs yield diminishing returns, understanding and reducing inverter costs becomes increasingly critical and is a cost-effective investment toward achieving DOE Solar Energy Technologies Office goals.

With this in mind, this report showcases and describes an approach to help assess and predict the reliability of PV inverters. To predict reliability, thermal cycling is considered as a prominent stressor in the inverter system. To evaluate the impacts of thermal cycling, a detailed linearized model of the PV inverter is developed along with controllers. This research also develops models and methods to compute the losses of the power electronics switches and other components in a PV inverter. The losses are then used to estimate the junction and heat sink temperatures of the power semiconductors in the inverter.

The model is verified by developing an in-house inverter. Additionally, to assess the scalability of the research, the hardware inverter is placed inside a thermal chamber to verify the losses for different ambient temperatures. After the verification of the model, a reduced-order model of the inverter is implemented to translate the profile of the ambient temperature and solar irradiance into the profile of the junction temperatures of the switches. The estimated junction temperature data are used to identify inverter reliability indices and predict the useful lifetime of the inverter system. After developing the models to predict the useful lifetime of the system, the impact of reactive power on the overall reliability of the system is studied.

The first chapter discusses the motivation behind the research on assessing the reliability of PV inverters. The inverter power stage and controller design of the power converter used in this research is explained in detail. The second chapter presents the various losses of the power converter system and the translation of power loss into temperature increase with thermal modeling. The results of the loss modeling and the thermal modeling is also explained in detail.

The third chapter implements the reduced-order model to translate the mission profile of the ambient temperature and solar irradiance into the profile of the junction temperatures of the switches. The final chapter identifies the reliability indices, which are of interest for this system to predict the remaining useful lifetime of the system, and the chapter concludes with a discussion of the impact of reactive power on the overall reliability of the inverter system.

In summary, this paper develops and validates a detailed electrothermal model of an inverter is with the development of a homegrown inverter to make the model scalable. From this validated model, an averaged loss and thermal model is developed to estimate the lifetime of the inverter. This is applied to typical meteorological year (TMY) data for the Phoenix, Arizona, and Ft. Peck, Montana, regions. From the analysis on TMY data for two regions, the effect of reactive power on the lifetime of inverters is studied. The studies show that an inverter's lifetime can be reduced by 7.6% when an inverter is simulated at 0.8 absorbing power factor instead of unity power factor.

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1 Power Electronics Reliability Assessment

1.1 Introduction

As of 2013, the installed cost of residential photovoltaic (PV) systems was $4.69/W [1]. Most research, historically and present, has focused on the production costs and reliability of PV module technology, whereas the cost of the necessary power electronics components has been sparsely considered [2]. As the price of PV modules decreases, the price of power electronics become more important because they now constitute 8%–12% of the total lifetime PV cost [3]. As of 2017, the inverter and associated power conditioning components of residential applications accounted for $0.17/W [4] , significantly more than the U.S. Department of Energy (DOE) benchmark of $0.12/W by 2020. As efforts to reduce PV module costs yield diminishing returns, understanding and reducing inverter costs becomes increasingly critical and is a cost-effective investment toward achieving DOE Solar Energy Technologies Office goals.

A key price driver of power electronics is reliability [5]. PV modules have long lifetimes with warranties up to 20 years [6]. In utility-scale fielded systems, the mean time between failure of inverters has been shown to be 300 to 500 times shorter than modules [7], [8]. In one 27-month study, module failures accounted for only 5% of total energy losses, whereas inverter failures accounted for 36% of lost energy during the same period [9].

Inverter reliability is a layered topic because of its complicated switching/monitoring system and multiple materials bonded together. In addition to providing output power meeting power quality standards, the inverter may be required to manage the power output of the PV module, connect/disconnect from the grid, read and report status, or monitor islanding. Meanwhile, trends in power electronics systems and devices during the past decade have placed increasing demands on the efficiencies of the thermal management and control systems used for metal-oxide-semiconductor field-effect transistor (MOSFET) and insulated-gate bipolar transistor (IGBT) modules. The pressure to decrease the size of power electronics systems and inverter subsystems has resulted in an overall reduction of 50% of the footprint area of many IGBTs during the past 10 years.

This report provides a detailed description of PV inverter reliability as it impacts inverter lifetime today and possible ways to predict inverter lifetime in the future. As a part of this work, we developed detailed inverter hardware and matching models that can potentially predict the lifetime of the inverter when used for different purposes and at different ambient temperatures. Chapter 1 provides the detailed description of the state of knowledge on inverter reliability as well as researched topics relevant to this work. Chapter 2 describes the technical work on inverter losses and thermal modeling. Chapters 3 and 4 enlist model development for practical use and presents a deep dive into inverter lifetime models and their use.

1.2 Existing Literature

In a PV system, the inverter subsystem receives the largest number of service calls for operation and maintenance. This implies increased cost to the end user of the PV system because the usability and profitability of a PV installation is influenced by the costs of operation and maintenance. The breakdown of operation-and-maintenance events from PV operators suggests

that the inverter constitutes 43%–70% of the service calls [9], [10], [11]. The inverter outages contribute to 36% of the energy losses among the total outages [12]. The significant percentage of operation and maintenance and energy loss necessitates understanding the failure mechanisms of various components in the inverter or any other power conversion equipment [13].

Ambient temperature could affect the lifetime of inverter components. The new generation of inverters that use module-level power electronics (MLPE) are more efficient in design and can withstand very high and low temperatures because they are placed on the back of the PV panel. Several studies have performed accelerated testing of MLPE analysis of failure modes of components in MLPE [15], and component-level reliability of MLPE [17], [18].

Up to a certain point in time, the entire lifetime of a PV inverter was predicted based on the failure rates of individual components and handbooks provided by the manufacturers. In recent years, the prediction of the reliability and lifetime of power converters has been done through physics-of-failure assessments. A physics-of-failure assessment is understood through the failure mechanisms of the components of power converters and external physical stressors, such as ambient temperature, solar irradiance, and relative humidity [19], [20], [21]. Some studies included the reliability of inverters with different topologies [22], [23]. Other studies included the detailed prediction of the reliability of IGBTs for medium- and high-power inverter applications [24], [25], [26]. Mission-profile-based studies have involved the translation of ambient temperature, solar irradiance, and relative humidity into the thermal loading of the devices using the electrothermal models of the power converter [27], [28], [29].

1.3 Proposed Steps Involved in Estimating the Lifetime of Inverters

This section provides a quick review of the PV inverter lifetime estimation process used in this report. Figure 1 shows the sequence of steps involved in estimating the lifetime of inverters based on the power semiconductor life estimation. The first step is to develop an inverter from components, which provide flexibility in the choice of topology and component selection, including power semiconductors, heat sink, inductors, and capacitors. The second step is the careful depiction of individual components (capacitors, switches) in a model to accurately represent their thermal lifetime behavior. For this purpose, the data sheets of the passive components are documented and included in the detailed switching model developed using the power electronics modeling tool PLECS, a power electronics platform [30]. The electrothermal model of the inverter is developed using the selected power converter topology and part numbers used in the respective hardware.

The developed model estimates the losses of the power converter using the selected parameters and translates the power losses into increase in temperature using the thermal parameters of the heat sink used in the system. The estimated increase in temperature of the heat sink in the model is verified using actual thermocouple measurements on the developed hardware setup of the inverter.

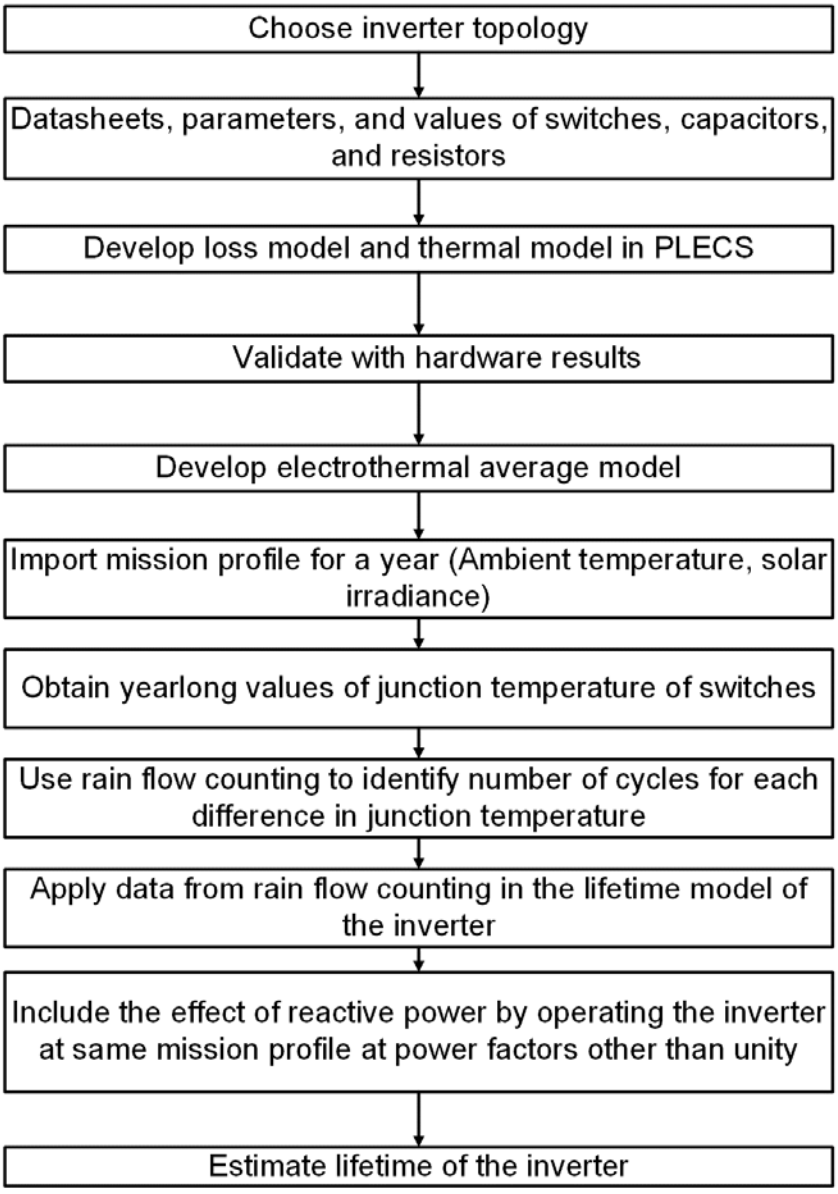


Figure 1. Sequence of steps to calculate lifetime of inverters

After validating the electrothermal model, a multi-timescale model is developed to measure the losses and temperatures during the entire year. Then a physics-based analytic PV model is developed to provide the yearlong mission profile.

This model computes the junction and heat sink temperatures of the devices. Rain flow counting is performed to estimate the difference in junction temperatures, which will be used to estimate the lifetime model of the power semiconductors, the power MOSFETS. Finally, the effect of reactive power is implemented for the yearlong mission profile to study the impact on reliability and lifetime of the inverter. The effects of lifetime on power semiconductors will be assessed along with the lifetime of other components to determine the inverter system lifetime.

1.4 Homegrown Inverter Testing

This section introduces the two-stage inverter hardware developed at the NREL to validate the lifetime estimation model. The design of the inverter and hardware results are discussed in the following subsections.

1.4.1 Design of the Homegrown Inverter

The two-stage 1-kVA inverter built at the laboratory is designed to run in a closed loop for the active power and reactive power set points. The two-stage single-phase inverter consists of a synchronous-boost DC-DC converter at the first stage and an H-bridge inverter at the second stage connected to 120-V AC grid system [31]. On the grid side, a LCL filter is used to control the total harmonic distortion of the output voltage and current waveforms [32]. The inverter schematic and controls are shown in Figure 2.

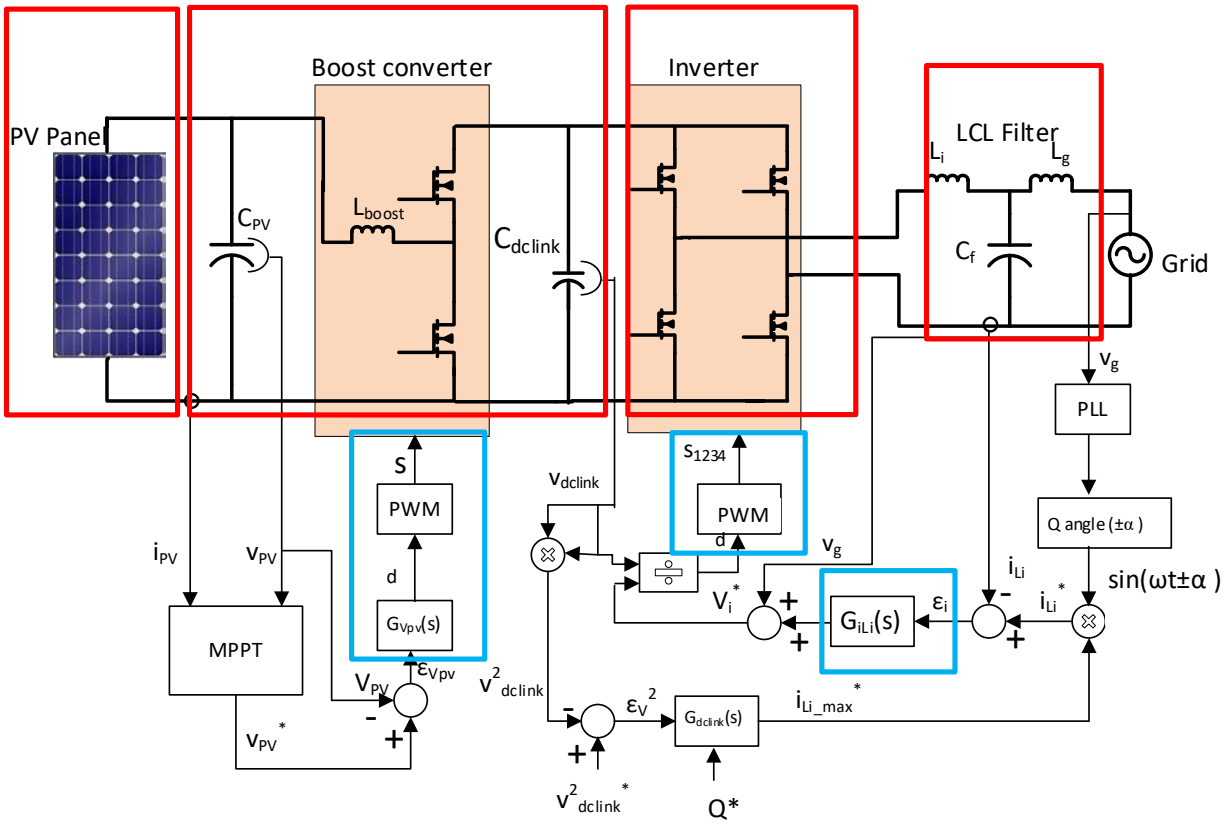


Figure 2. Schematic of the homegrown inverter with the controls

Four controllers are included in the inverter. On the input side, the input power is controlled through the maximum power point tracking algorithm. The input voltage is controlled through the high-bandwidth voltage controller, with a typical bandwidth of 2 kHz. On the output AC side, the phase-locked loop ensures that the inverter output remains synchronous to the grid. The inner current loop is a high-bandwidth proportional-integral or proportional-resonant controller with a bandwidth of few kilohertz [33], [34] .The magnitude of the current reference is derived from the outer DC-link voltage controller, which is a low-bandwidth controller on the order of 5 Hz–10 Hz. Table 1 shows the specification of the homegrown inverter.

Table 1. Specifications of the Two-Stage Inverter

Input DC voltage	110 V
Active power	1 kW
Apparent power	1 kVA
Output AC voltage	120 V RMS
Output frequency	60 Hz
DC-link voltage	220 V
Input boost inductor	500 μH
DC-link capacitor	1.35 mF
Inverter LCL filter	1 mH, 24 μF, 0.2 mH
Switching frequency	30 kHz

The inverter design is initially verified using PLECS. The model is developed in a detailed manner by including the detailed parameters of the power semiconductor, such as the on-state resistance, gate charge, and gate resistance, as well as external series resistance of components, such as the choke coil, electromagnetic interference filters, and inductors. The magnetic parameters of the inductor are also included so that the core losses of the inductor can be computed. Figure 3 shows the schematic of the homegrown inverter developed in PLECS.

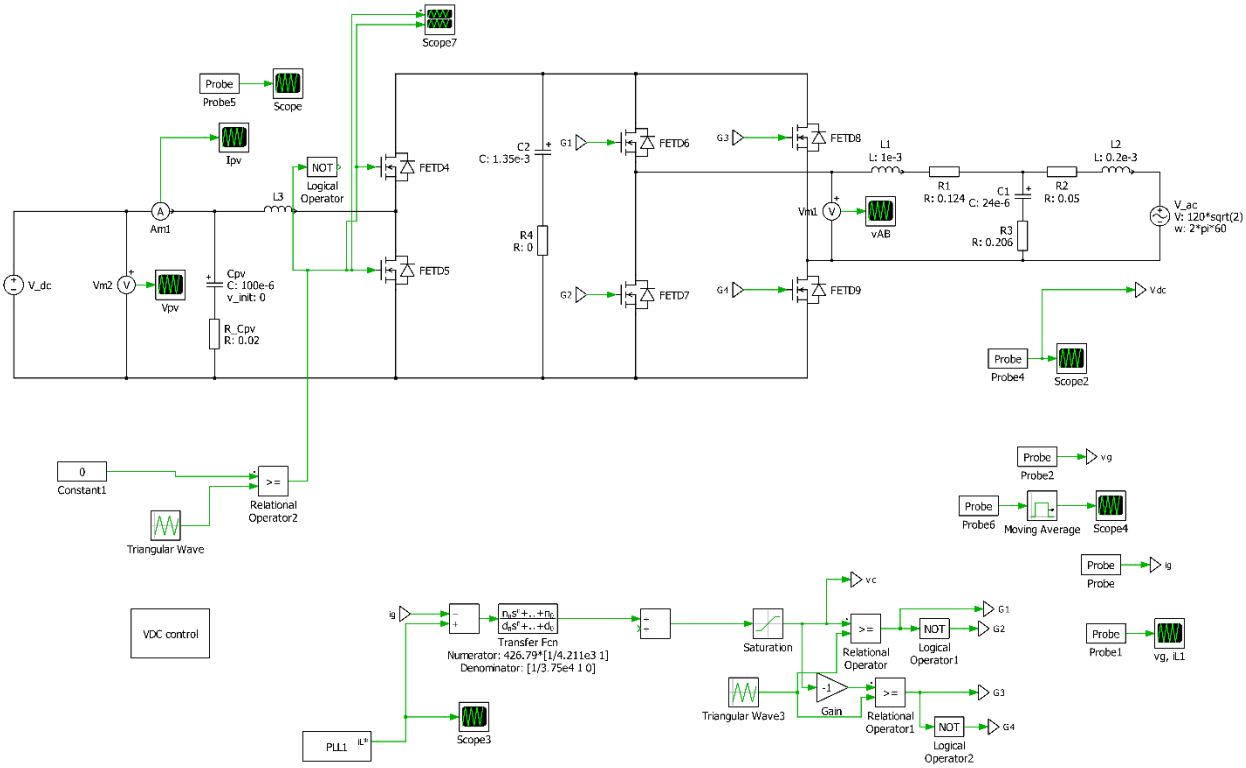


Figure 3. Schematic of the homegrown inverter developed in PLECS

1.4.2 Hardware Setup of the Homegrown Inverter

The inverter circuit board is designed using EAGLE layout software [35] and the PCB etching with assembly designed by Advanced Assembly, Inc. Figure 4 shows the board layout of the inverter.

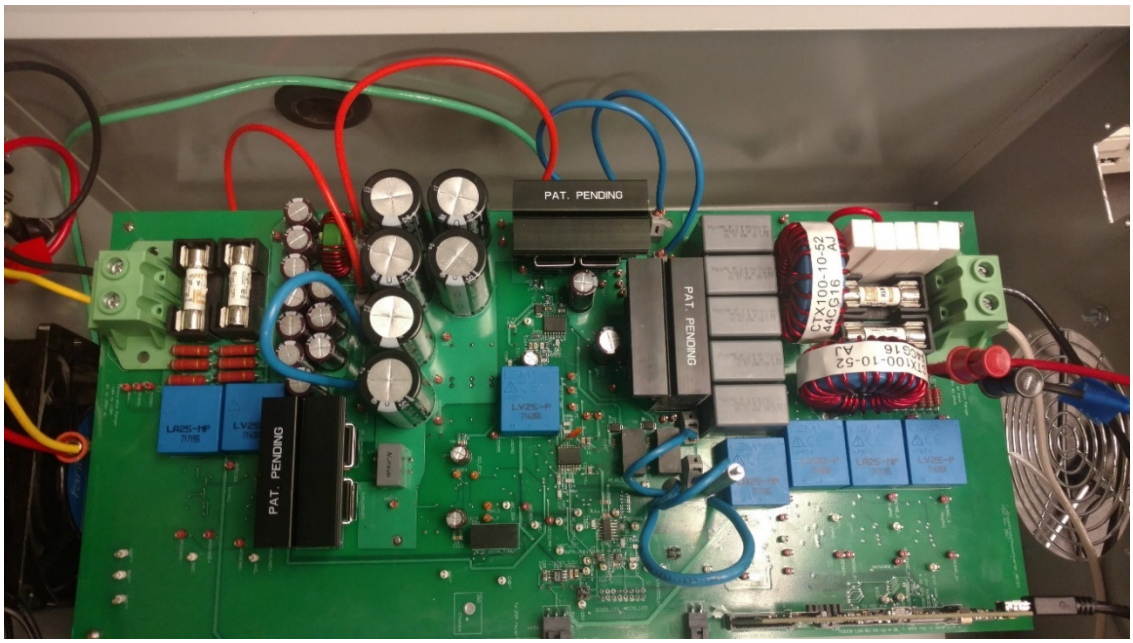


Figure 4. Board layout of the homegrown inverter

The DC side of the inverter is connected to the Magna-Power supply, and the AC side of the inverter is connected to MX45, the AC grid simulator. The Magna-Power supply can act either as fixed DC power supply or as a PV emulator. The MX45 AC grid simulator provides the single-phase, 120-V, 60-Hz AC source. It is capable of four-quadrant operation and can change in per-unit value of voltage or frequency. Figure 5 shows the block diagram of the testing setup.

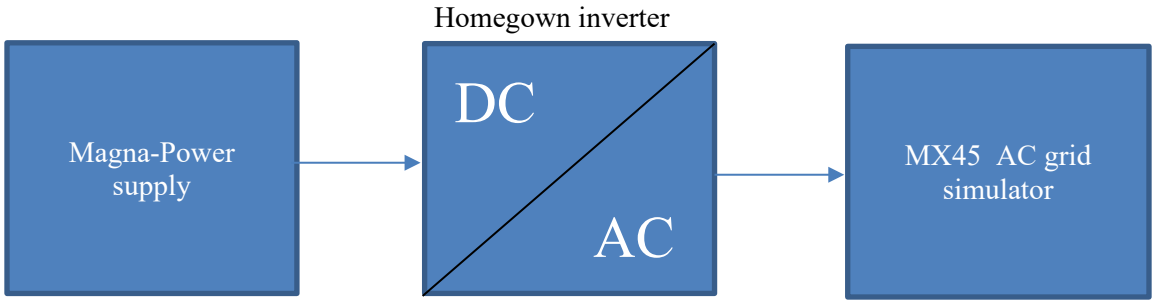
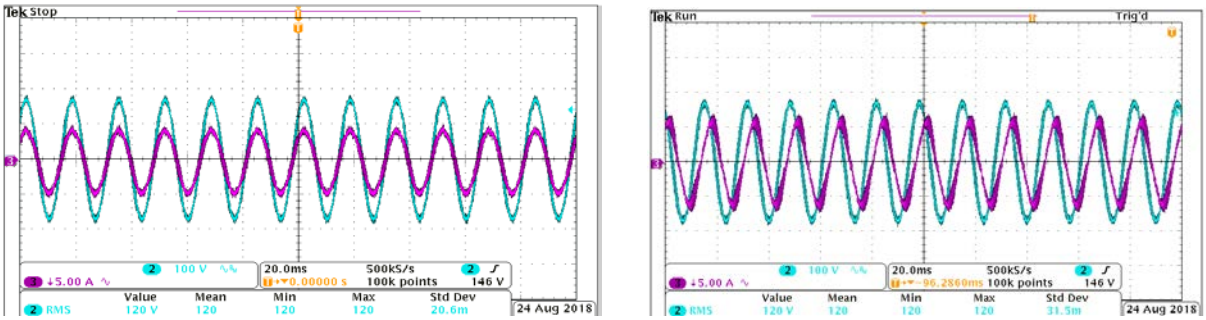


Figure 5. Block diagram of the testing setup

The inverter is initially tested in the open-loop configuration with a resistive load for debugging, and the issues with ringing in the gate driver circuitry are resolved. Then, the inverter is tested using a grid simulator, which emulates the grid source voltage of 120 V at 60 Hz. In this setting, the inverter can operate only in a closed-loop condition because the inverter needs to generate the reference current. The controller is designed to provide a real power command and a reactive power command. Figures 6 (a) and (b) show the hardware results of the output inverter current and the grid voltage for a real power command of P=400 W and real and reactive power commands P =400 W Q=300 volt ampere reactive (VAR), respectively.



(a) (b)

Figure 6. Inverter current and voltage waveforms for (a) P=400 W and (b) P=400 W and Q=300 VAR, respectively

With the hardware designed for operating up to 1 KW, the next sections discuss the loss modeling, thermal modeling, reduced-order models for mission profile translation into junction temperature rise, reliability models, estimation of remaining useful lifetime, and impact of reactive power on the reliability of the power converter.

2 Inverter Losses and Thermal Modeling

2.1 Introduction

PV inverters consist of multiple components, including power semiconductors, sensors, resistors, magnetics, control circuits, and auxiliary power supplies. All these components introduce some amount of power loss in the converter. Most of the time these losses dissipate as heat and lead to an increase in local temperature. The failure modes of the power electronics are complicated and are affected by many factors, but thermal cycling (i.e., temperature swings inside or outside the devices) are one of the most critical failure causes in power inverters. The new generation of PV inverters are becoming more efficient, with efficiencies greater than 97% [36]. The efficiency is brought about by changing the topology of the power converter or control scheme or by better circuit board layout techniques.

With increasing efficiencies, it has become clear to account for all the power losses in the power converter. These losses can be calculated using the existing analytic formula calculations. In the following sections, the power loss calculation will be matched analytically to the actual power loss obtained from the hardware efficiency data.

2.2 Classification of Power Losses

Power losses lead to temperature fluctuations within devices, thus leading to different materials having mismatched coefficients of thermal expansion, causing disconnection in the contacting areas after certain cycles, and ending in the failure of the devices. The power losses are divided further based on the components used in the power converter. Power semiconductors, such as MOSFETs or IGBTs, form the basis of the power stage of the converter [37]. These power semiconductors—typically referred to as switches—introduce losses in the form of conduction losses, switching losses, and gate driver losses. The next component of interest is the magnetics used in the power converter for storage, filtering, and electromagnetic interference reduction. The magnetics include inductors, transformers, and choke coils, and they introduce losses in the form of core losses and conduction losses. All components in the converter, including sensors and control circuitry, have some form of internal resistance introducing conduction losses in the converter. Each loss category is explained in detail in the following sections. The classification of the losses is shown in the Figure 7.

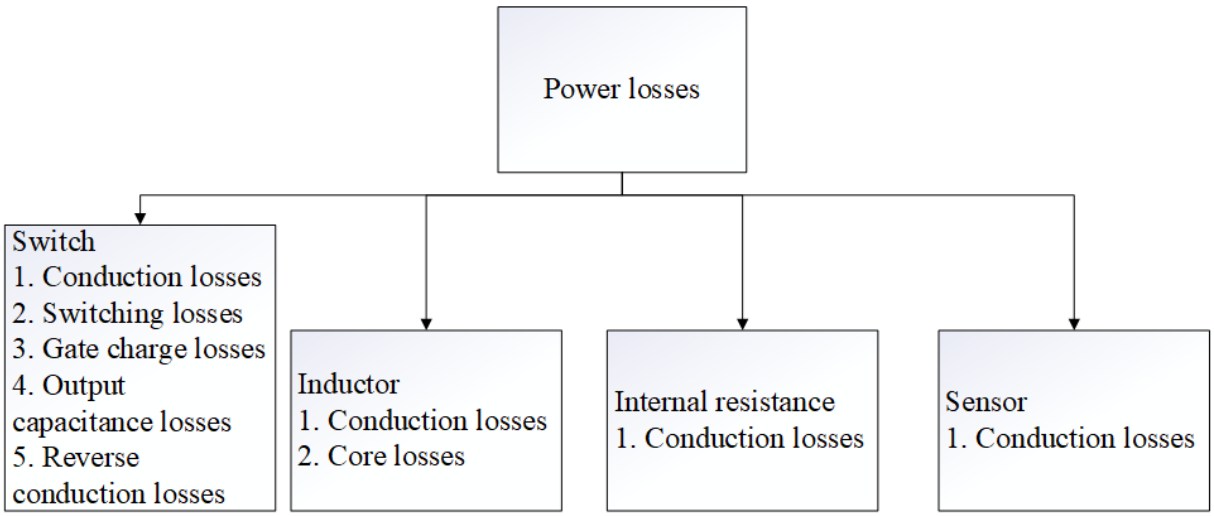


Figure 7. Classification of the power losses of the power converter

2.2.1 Power Semiconductor

Power semiconductors are used in power electronics devices because of their high current-carrying capability and ability to withstand higher voltages than a typical semiconductor device. Power semiconductors include power diodes, power MOSFETs, IGBTs, and a few others such as silicon-controlled rectifiers and their variants. These devices are different in structure than their low-power counterparts, which allows for higher current capability and higher breakdown voltages, which lead to increased power dissipation.

The selection of the power semiconductor devices is based on multiple factors, including the cost, power density, switching frequencies, and operating power ranges. Power MOSFETs are used for low operating power and higher switching frequencies, whereas IGBTs are used for higher operating power and lower switching frequencies. With the advent of silicon carbide power MOSFETs and power diodes, power MOSFETs are also used in medium-power applications [33]. These silicon carbide devices have higher current capability and higher breakdown voltages than silicon-based power MOSFETs. This work focusses mainly on the silicon-based power MOSFETs, and the discussion is limited to that technology.

2.3 Power MOSFET Losses

The MOSFETs have an on-state resistance that determines the conduction losses of the device [38], [39]. These devices also perform continuous on/off operation, which leads to switching losses during the transition from the on state to the off state and vice versa. Each switching device has an associated gate driver circuit to drive these MOSFETs. The switching operation essentially involves continuous charging and discharging of the gate capacitance during each switching cycle. Gate charge losses occur because of the charging and discharging process. Reverse conduction and reverse recovery losses are associated with the body diode of the power semiconductor. The body diode is connected in an antiparallel way to the power semiconductor. All these losses [40], [41] are explained in detail in the following sections. These losses sum to the net losses from the power semiconductor switch, as shown in Figure 8.

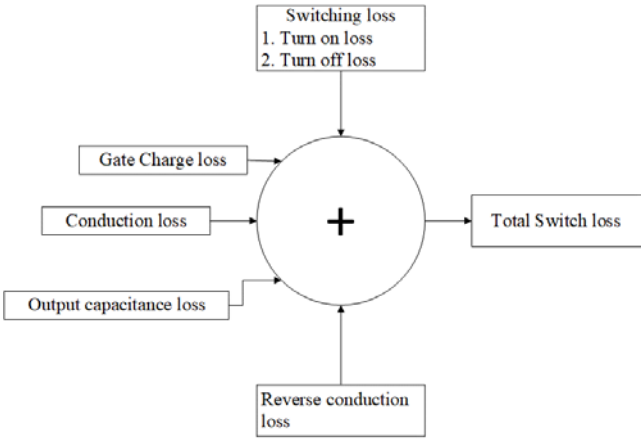


Figure 8. Classification of losses of the power semiconductor switch

2.3.1 Switching Losses

Power semiconductors can be viewed as commutation devices undergoing hundreds of thousands of on and off cycles. With a finite amount of switching time, the dynamics of the voltage and current of the switch creates the switching loss. In a conventional, unipolar inverter controlled by pulse-width modulation, there is a small amount of nonzero current and voltage during the on/off transition, creating the switching loss. This loss can be overcome by using the dead time between the transitions, letting the voltage and current settle to zero, thus nulling the switching loss. The increase in dead time, however, leads to a decrease in the duty cycle range of the converter. Hence, there is a trade-off between the dead time and acceptable switching loss for the designer to choose the appropriate scheme. Figure 9 shows the switching transition occurring at nonzero voltages and currents.

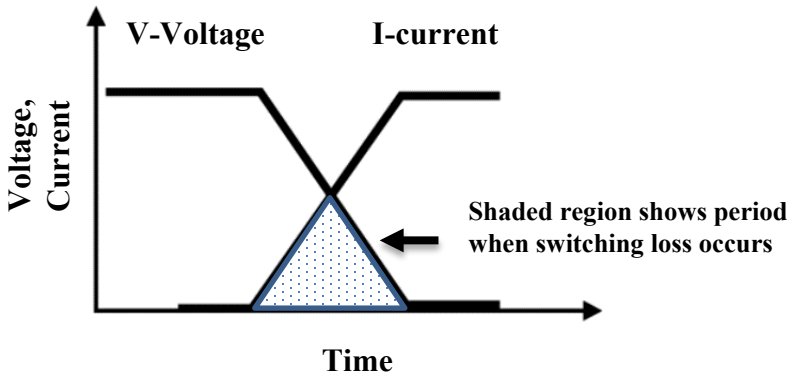


Figure 9. Switching transition at nonzero voltage and current

Switching loss can also be reduced by modifying the topology of the power converter. Often referred to as soft switching, the topology ensures that the switching transition occurs at the zero crossing of the voltage or current. The switching transition at the zero current value is referred to as zero-current switching. This technique is typically used in an IGBT to eliminate the switching loss occurring at the transition and reduce the generation of the electromagnetic interference caused by stray inductances in the circuit. The other obvious technique involves ensuring the

switching transition at the zero crossing of the voltage, referred to as zero-voltage switching). This technique is preferred in power converters based on MOSFETs.

The inverter illustrated in this report uses a full-bridge inverter topology with unipolar pulse-width modulation. The switching loss is calculated based on that assumption. The loss calculation depends on multiple parameters of the selected power MOSFET and operating voltage, current, and switching frequency. Switching losses can be defined as the sum of turn-on and turn-off losses of the power MOSFET [47]. The estimation of the switching loss is provided by the Eq. 1 and Eq. 2. The first equation corresponds to turn-on losses, P_{ON}, occurring at the on transition; and the second equation represents the turn-off losses occurring at the off transition, P_{OFF}.

$$P_{ON} = \frac{V_D \times I_D \times R_G \times f_{sw}}{2}\left[\frac{Q_{GD}}{V_{dr} - V_{plat}} + \frac{Q_{GS}}{V_{dr} - \left(\frac{V_{plat} + V_{th}}{2}\right)}\right] \quad (1)$$

$$P_{OFF} = \frac{V_D \times I_D \times R_G \times f_{sw}}{2}\left[\frac{Q_{GD}}{V_{plat}} + \frac{Q_{GS}}{\left(\frac{V_{plat} + V_{th}}{2}\right)}\right] \quad (2)$$

where V_D is the drain voltage, I_D is the drain current , R_G is the gate resistance, f_{sw} is the switching frequency, Q_{GD} is the gate-to-drain charge, Q_{GS} is the gate-to-source charge, V_{dr} is the gate drive voltage, V_{plat} is the plateau voltage, and V_{th} is the threshold voltage. The parameters V_D, I_D, and f_{sw} are dependent on the operating values; and the rest of the parameters are particular to the selected power MOSFET.

2.3.2 Conduction Losses

Conduction losses in the power semiconductor are straightforward to estimate because they are the I^2R losses in the power semiconductor. The current corresponds to the drain current, I_D, of the MOSFET. The resistance, $R_{DS(ON)}$, is the on-state resistance between the drain and the source of the MOSFET. The $R_{DS(ON)}$ parameter is dependent on the junction temperature of the power MOSFET. Typically, $R_{DS(ON)}$ increases as the temperature increases. The specification sheet from the device manufacturer provides the variation of $R_{DS(ON)}$ with the junction temperature of the device. The conduction loss, P_{COND}, is calculated as shown in Eq. 3:

$$P_{COND} = I_D^2 \times R_{DSON} \quad (3)$$

Figure 10 shows the variation of $R_{DS(ON)}$ with the junction temperature of the device, T_j.

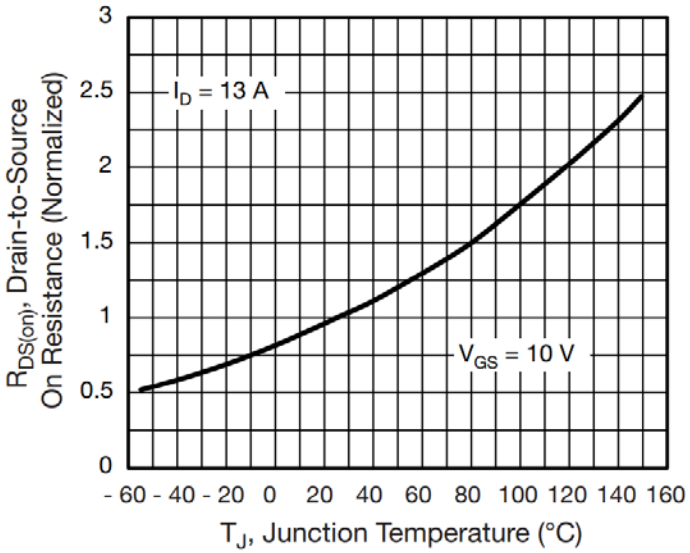


Figure 10. $R_{DS(ON)}$ variation with junction temperature of the device, T_j

2.3.3 Gate Driver Losses

Power semiconductors cannot be driven directly from the controller because of the increased power requirements to drive the power semiconductor. Gate driver circuits are useful for providing the gate signals along with features such as disabling the circuit and setting the dead time for the switching transitions. Gate drivers provide voltage and current signals depending on the power semiconductor type. The power MOSFETs are voltage-controlled devices, whereas the IGBTs are current-controlled devices.

The process of turning on the power MOSFET involves charging the gate capacitance voltage to a value greater than the threshold voltage, V_{th}. Once the gate is charged to the threshold voltage, the device can start carrying current. Then the gate-to-source capacitance, C_{GS}, is charged to the miller gate-to-source voltage, V_{GS_miller}. Then the device acts in the linear region. Now the gate-to-source capacitance is charged to the driving voltage, V_{DR}. Figure 11 (a) shows the entire process of turning on the power MOSFET.

The turn-off procedure involves discharging the gate-to-source capacitance, C_{GS}, from driving voltage, V_{DR}, to the miller gate-to-source voltage, V_{GS_miller}. The gate-to-source capacitance, C_{GS}, is further discharged from the miller gate-to-source voltage, V_{GS_miller}, to the threshold voltage, V_{th}. Once the capacitance is discharged to less than the threshold voltage, the device tuns off. Figure 11 (b) shows the entire process of turning off the power MOSFET [43], [44]. The process of charging and discharging by the gate driver circuit creates some power losses in the form of switch output capacitance loss and gate charge loss. The dead time setting provided by the gate drivers causes the body diode to conduct, causing reverse conduction losses and reverse recovery losses. The reverse recovery losses are not included because of the difficulty of measuring the reverse recovery charge, Q_{rr}, at operating conditions. These losses are explained in the following sections.

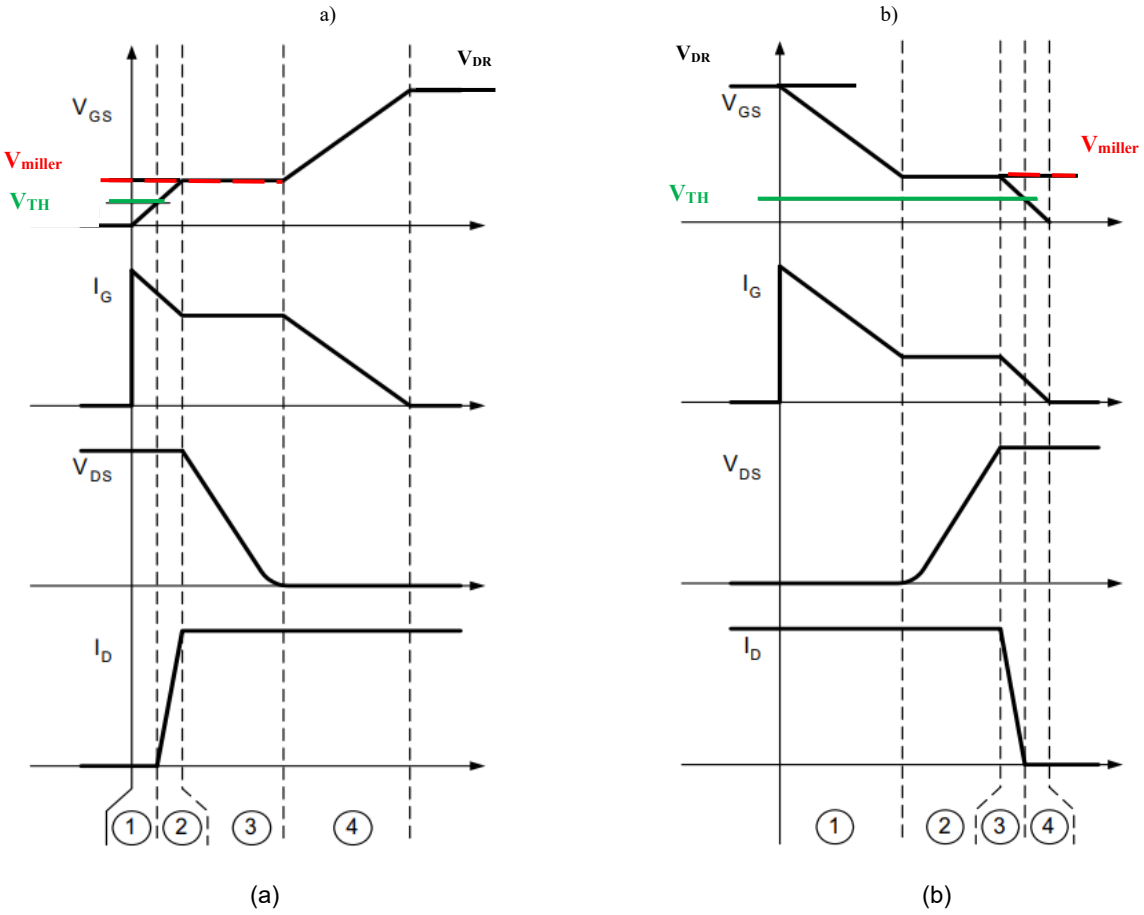


Figure 11. (a) Turning on the power MOSFET and (b) turning off the power MOSFET

2.3.4 Switch Output Capacitance Loss

To charge the output capacitance, C_{OSS}, of the power MOSFET to its bus voltage, some amount of power is consumed. The power needed for charging the output capacitance is referred to as the switch output capacitance loss, P_{OSS}. The power is dependent on the switching frequency, f_{sw}, drain-to-source voltage, V_{DS}, and switch output capacitance, C_{OSS}. The switch output capacitance loss, P_{OSS}, is defined by the following equation:

$$P_{OSS} = \frac{1}{2} \times C_{OSS} \times V_{DS}^2 \times f_{sw} \quad (4)$$

2.3.5 Gate Charge Loss

The gate-to-source capacitance, C_{GS}, is charged and discharged during the switching transitions. The power consumed for the charging and discharging of the capacitance is referred to as the gate charge loss, P_G. The gate charge loss, P_G, is dependent on the switching frequency, f_{sw}, gate drive voltage, V_{DR}, and gate-to-source capacitance, C_{GS}. The gate charge loss is defined by the following equation:

$$P_G = Q_G \times V_{DR} \times f_{sw} \quad (5)$$

2.3.6 Reverse Conduction Loss

The dead time setting provided by the gate driver causes the body diode to turn on, making it conduct during the switching transitions. This creates a diode conduction loss, referred to as reverse conduction loss, P_{SD}. The reverse conduction loss, P_{SD}, is dependent on the body diode voltage, V_{SD}, drain-to-source current, I_{DS}, dead time setting of the gate driver, t_{SD}, and switching frequency, f_{sw}. The reverse conduction loss, P_{SD}, is defined by the following equation:.

$$P_{SD} = V_{SD} \times I_{DS} \times t_{SD} \times f_{sw} \tag{6}$$

2.3.7 Inductor Losses

The inductors experiencing power loss, P_{copper}, can be classified into two categories. They experience conduction loss because of the current flow through the copper windings. These windings have associated external series resistance. This is akin to the I^2R loss equation:

$$P_{copper} = I_{RMS}^2 \times \text{ESR} \tag{7}$$

The second category is the core loss, which occurs in a magnetic core because of the alternating magnetization. The core loss can be further classified into eddy current loss and hysteresis loss.

The manufacturer of the magnetics typically provides the constants and coefficients necessary to compute the core loss power density using the Steinmetz equation:

$$P_v = Cm \times f^x \times B^y \times (Ct_2 \times T^2 - Ct_1 \times T + Ct)/1000 \tag{8}$$

The core losses can be estimated by the core loss power density, P_v, with the volume of the core material, V_{core}.

2.4 Thermal Modeling

Thermal models of power electronic converters describe the transient thermal behavior of power converters or power devices to estimate the temperatures of the power devices. The thermal behavior is typically described using lumped elements in the form of thermal resistances and thermal capacitances. The thermal model developed for measuring temperatures has an analogous relationship with an electrical circuit representing a voltage source connected to a resistor. The relationship is described in Table 2 and Figure 12.

Table 2. Relationship Between Electrical and Thermal Domain

Electrical domain		Thermal domain	
Voltage	V	Temperature	˚C or K
Current	A	Power loss	W
Resistance	Ω	Thermal resistance	˚C/W
Capacitance	F	Thermal capacitance	J/˚C

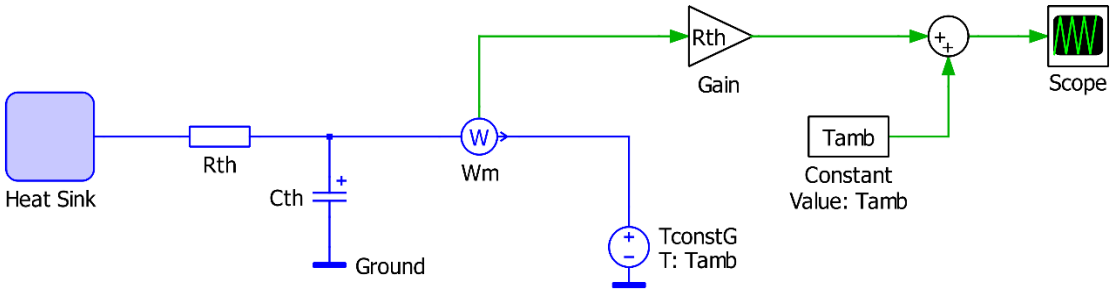


Figure 12. Electrical equivalent circuit in thermal domain

Thermal resistance determines the increase in temperature of the system with respect to power loss. It can also be defined as the increase in temperature per 1 W of power loss. The total thermal resistance of a MOSFET connected to the heat sink includes three thermal resistances of three components: heat sink thermal resistance, thermal interface material, and power MOSFET [42]. The thermal resistance of the heat sink depends on the airflow or the cooling method implemented in the heat sink system. The thermal interface material is used for the efficient transfer of heat from the power MOSFETs to the heat sink. The thermal resistance of the thermal interface material depends on the pressure applied on the thermal interface material between the heat sink and the MOSFET. The thermal resistance of the MOSFET is determined by the Foster and Cauer network values provided by the manufacturer. The total resistance of the heat sink system is represented by the following equation:

$$R_{TOTAL} = R_{MOSFET} + R_{TIM} + R_{HS} \tag{9}$$

Thermal capacitance determines the time it takes for the temperature to reach a steady-state value. This is akin to the time constant in the electrical circuits, which is the product of resistance and capacitance. Thermal capacitance, C_{th}, is defined as the product of volume of the material , density of the material, and specific heat of the material at constant pressure [48]. The product of volume and density can be rewritten as mass:

$$C_{th} = V \times \rho \times \text{cp [J/K]} = \text{m} \times \text{cp [J/K]} \tag{10}$$

The thermal impedance of a power converter or a semiconductor device is typically expressed as a chain of thermal resistor-capacitor network [49], [50]. Thermal networks are represented in two configurations: tank and filter. The tank configuration is a chain of resistor-capacitor circuits connected in parallel, referred to as a Foster circuit. The filter configuration is a chain of resistor-capacitor circuits connected as low-pass filters, referred to as Cauer circuit. The Foster and Cauer representations are shown in figures 13 (a) and (b).

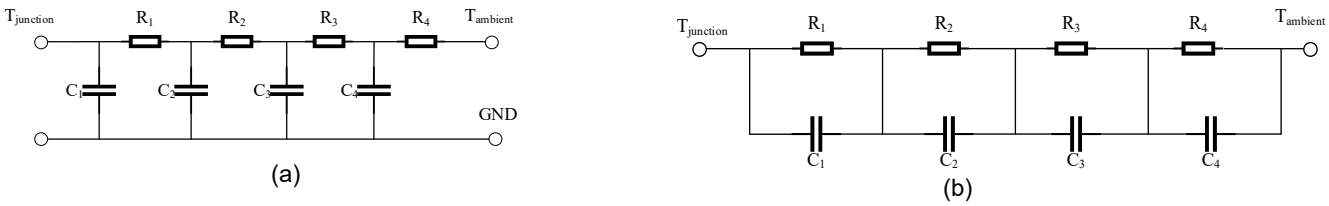


Figure 13. (a) Cauer/filter and (b) Foster/tank thermal resistor-capacitor networks

Figure 14 shows the how the thermal resistor-capacitor constant determines the final steady-state temperature value and the settling time.

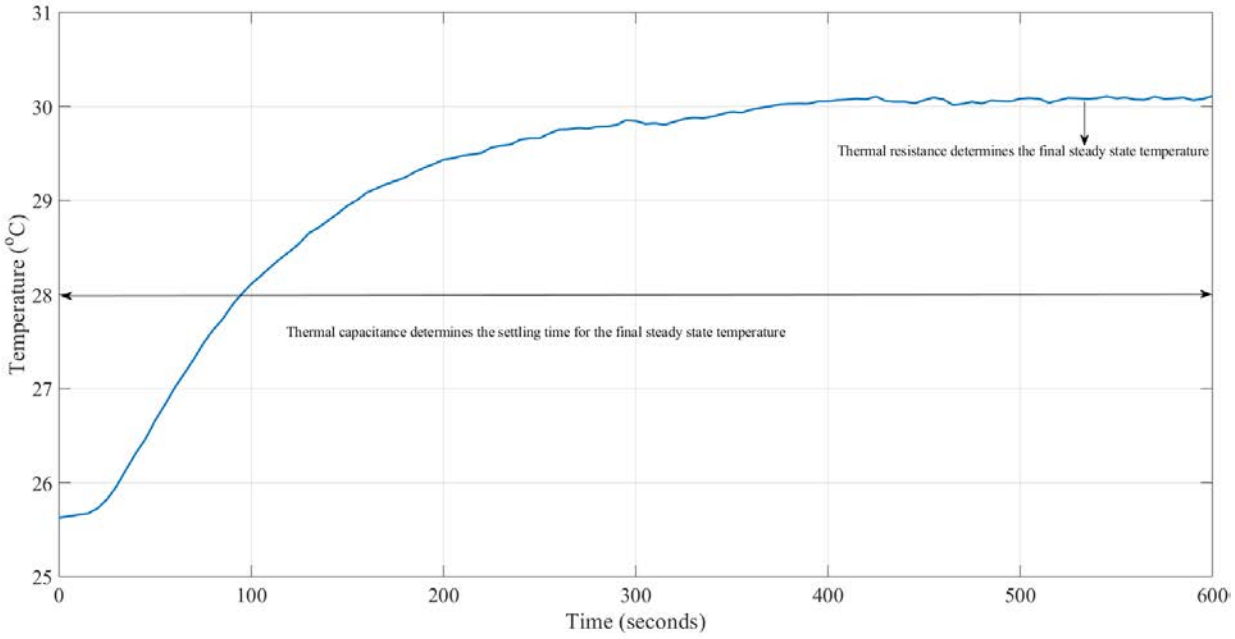


Figure 14. Significance of thermal resistance and thermal capacitance

2.4.1 Implementation of Thermal Model

The thermal model of the power converter is developed in parallel with the electrical model. The electrical model estimates the losses of the power semiconductors, and power loss translates into an increase in temperature in thermal domain. This is implemented in PLECS, a power electronics simulation platform.

The simulation platform lets the user provide the necessary parameters for loss estimation of power semiconductors [45]. These parameters include the on-state resistance, switching frequency, gate voltage, gate resistance, threshold voltage, plateau voltage, and the Foster and Cauer thermal resistor-capacitor network. These parameters can be useful for formula-based estimation of losses. The parameters can also be implemented in the form of lookup tables. These parameters are often provided by the device manufacturer. A lookup table-based implementation for power loss of a MOSFET for conduction loss is shown in Figure 15.

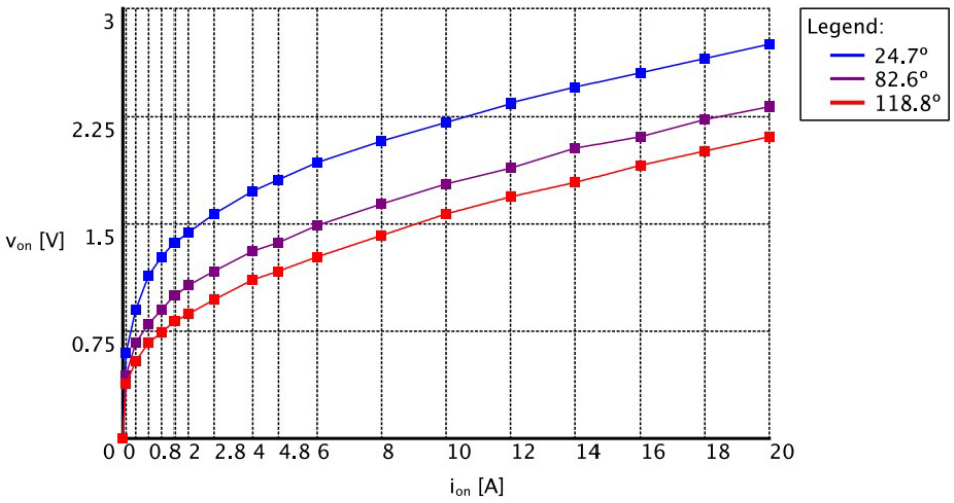


Figure 15. Lookup table implementation for power loss estimation

The thermal model of the inverter is implemented using the data obtained from the data sheets entered in the form of variables, parameters, and lookup tables. Figure 16 shows the thermal model of a generic H-bridge-based PV inverter with current source at the input and AC grid voltage source at the output connected through an inductor filter.

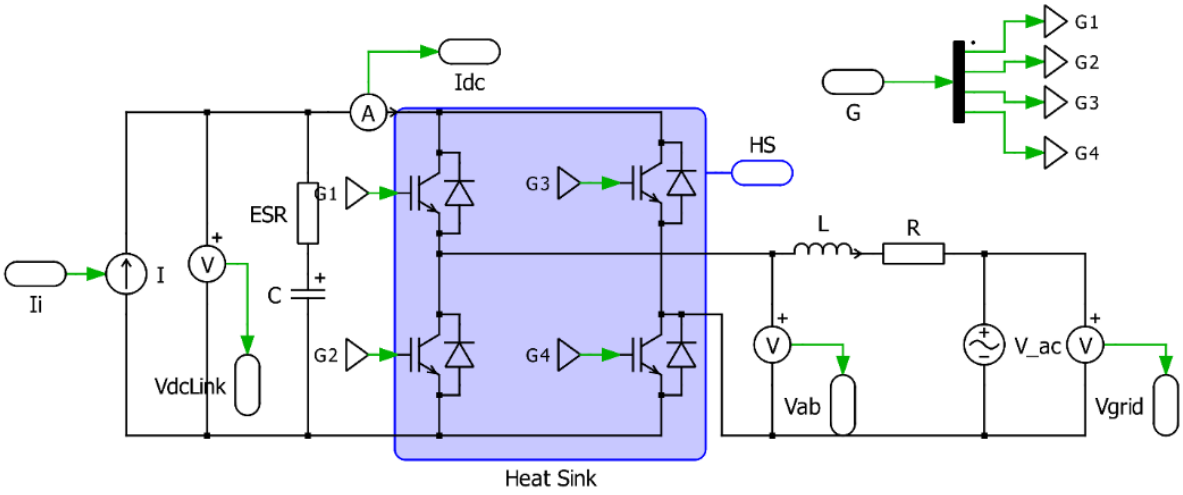


Figure 16. Thermal model of a generic H-bridge-based PV inverter

The switches of the inverter are modulated using unipolar pulse-width modulation. The losses of the switches include conduction losses and switching losses. Figure 17 shows the switch losses of the top and bottom MOSFETS. The figure shows that the loss waveforms follow the sinusoidal waveform of the output grid AC voltage.

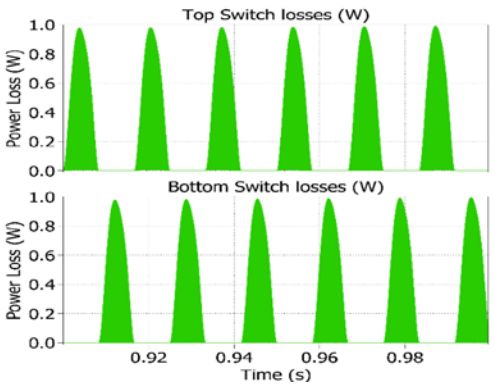


Figure 17. Switch losses of the top and bottom inverter MOSFETS

2.5 Results from the Loss Model

The homegrown inverter, as explained in Chapter 1, is a two-stage inverter with a DC-DC boost converter followed by an H-bridge inverter. The thermal model is developed for all six switches of the power converter, which include all the losses as described previously for the power MOSFETs. The simulation developed in PLECS also includes the losses of the inductors and conduction losses with the external series resistances of the inductors, chokes, and coils. Figure 18 shows the implemented PLECS model of the homegrown inverter.

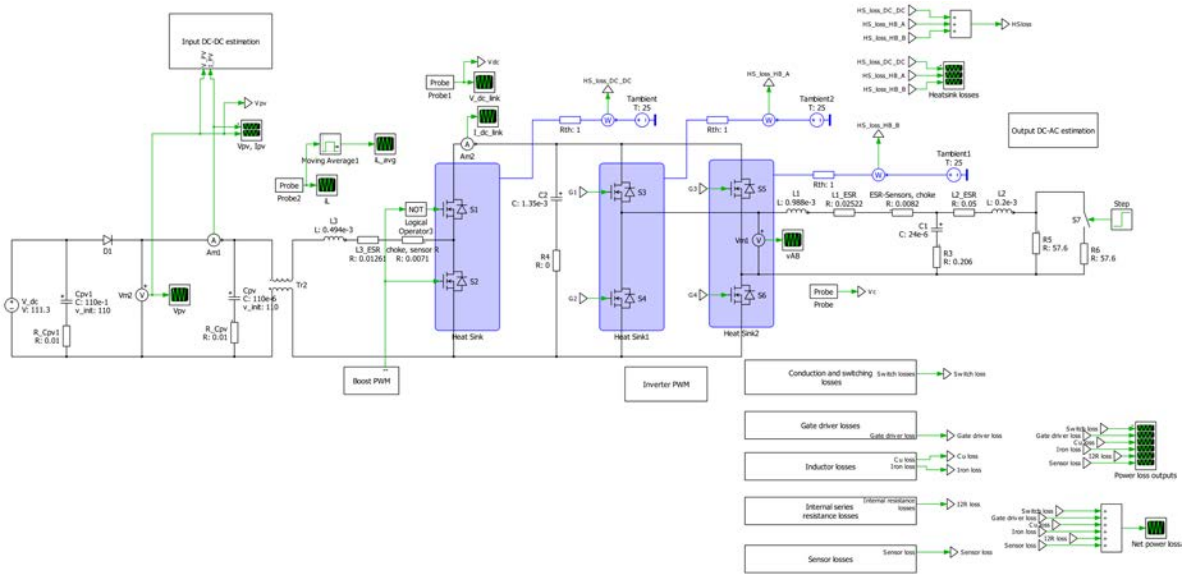


Figure 18. PLECS simulation model of the homegrown inverter

Figure 18 that the losses of the power converter are calculated separately based on the components used in the system. The heat sink is represented in Figure 18 by a blue box around the power MOSFETs. The software calculates the losses and temperatures of the components under the area of the heat sink. These losses simulated by the software have a settling time associated with the thermal capacitances of the MOSFET. Simultaneously, these losses are averaged over a few switching cycles using analytic formulae. Figure 19 shows compares analytically calculated heat losses without the settling time and the simulated heat losses including the thermal capacitances for a step change in load from 250 W to 500 W.

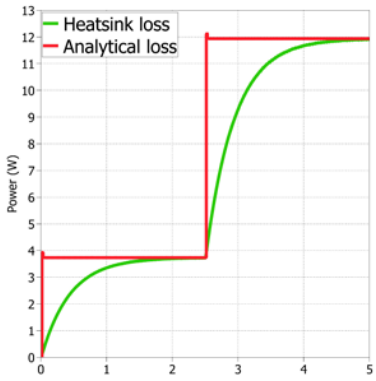


Figure 19. Comparison of analytic heat loss with simulated heat sink loss (with settling time) for step power change from 250 W to 500 W

Figure 20 also shows the calculation of individual losses and net losses of the system. The individual component losses are calculated and plotted together with net losses. These graphs are plotted for the power converter operating at 250 W and 500 W. Figures 20 (a) and (b) show the averaged individual and net losses of the power converter for a step change of load from 250 W to 500 W.

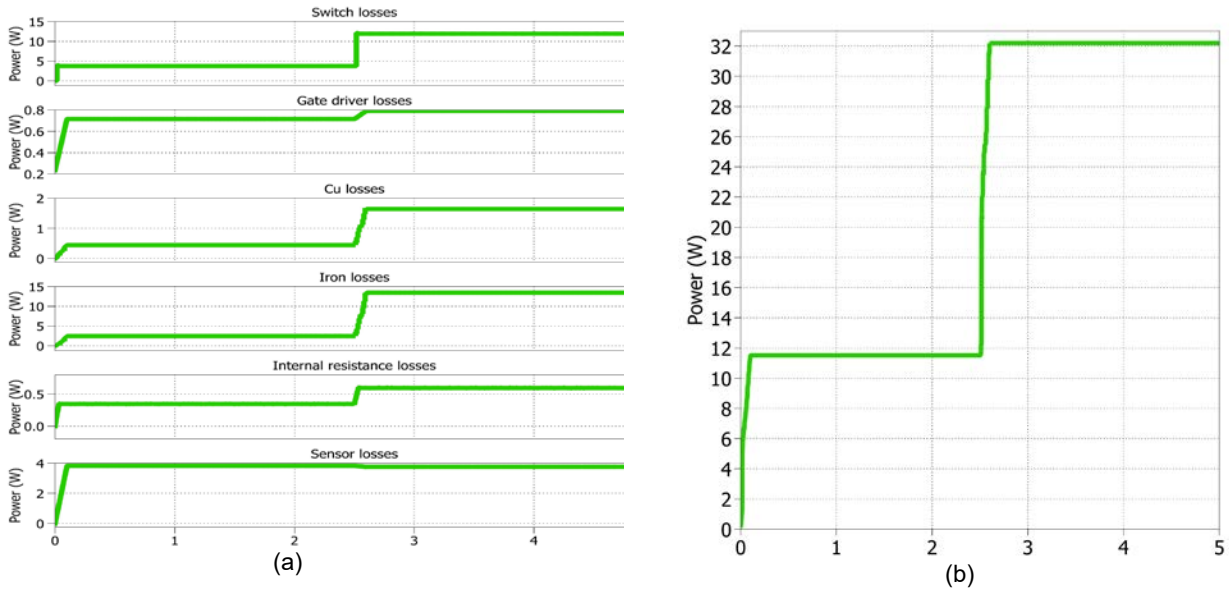
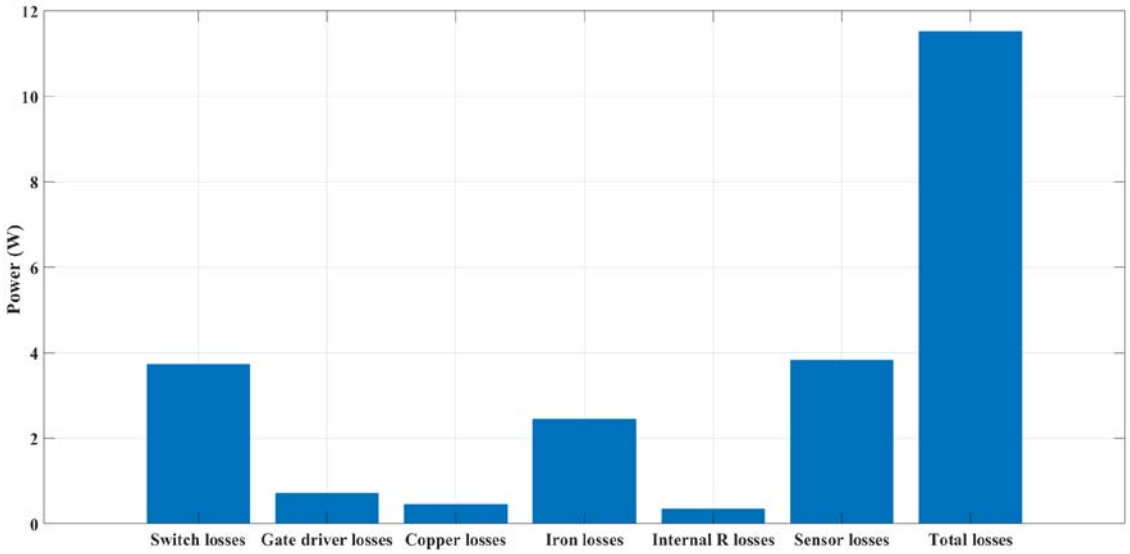
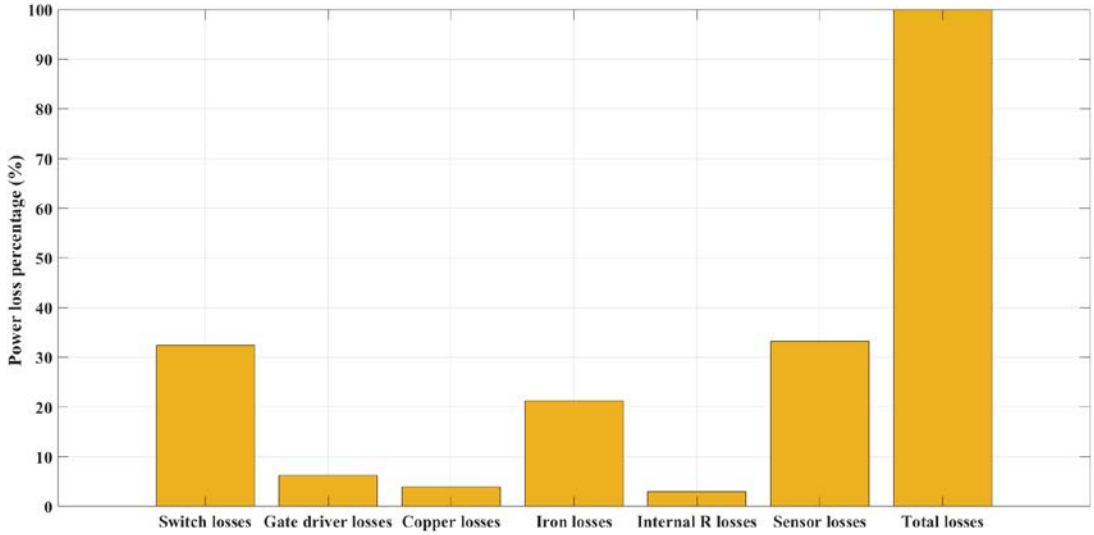


Figure 20. Individual and net losses of power converter for step power change from 250 W to 500 W

With the individual loss components of the power converter obtained from the model, the separation of the power losses for operation at 250 W and 500 W are plotted as absolute numbers and percentages. Figures 21 (a) and (b) show the power loss separation for operation at 250 W.



(a)



(b)

Figure 21. Power loss separation for converter operation at 250 W represented as numbers and percentages, respectively

2.6 Results of Thermal Model

The semiconductor power losses obtained from the developed model can be translated into an increase in temperature using the thermal resistance values obtained from the data sheets of the heat sinks, thermal interface material, and MOSFETs. The simulated increase in temperature is compared with the actual increase in temperature of the heat sink. The thermocouple data is acquired from the temperature acquisition system, which is then compared to the temperature data with thermal capacitance for measuring settling time. Figure 22 shows the experimental setup with thermocouples placed on top of the heat sink.

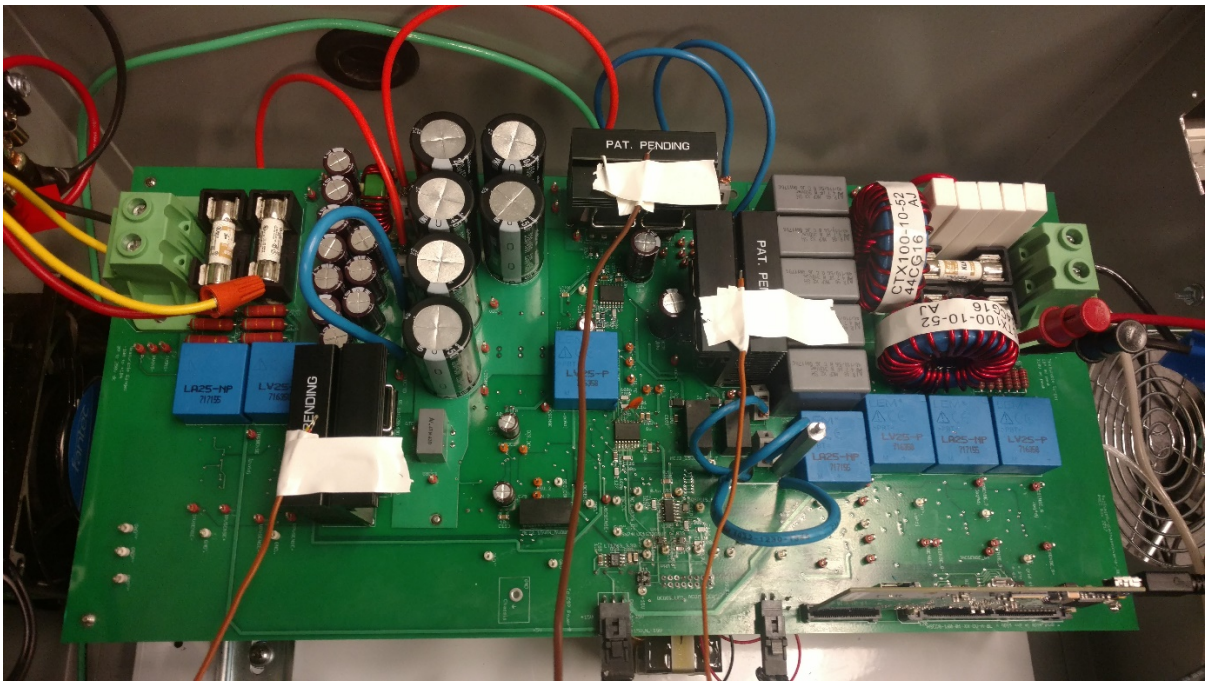


Figure 22. Experimental setup of homegrown inverter with thermocouples

The thermal resistances and thermal capacitances are calculated using the formulae from the previous sections. The inverter is operated at 250 W, and the temperatures of the heat sink connected to the DC-DC converter. The simulated model includes the thermal capacitance to determine the settling time. The hardware temperature data are captured using a thermocouple data acquisition system for a sample of 0.2 Hz or 1 sample for every 5 s. The simulation data are acquired instantaneously and compared with the hardware data. Figure 23 compares the experimental and simulated temperature rise of the heat sink connected to the DC-DC converter.

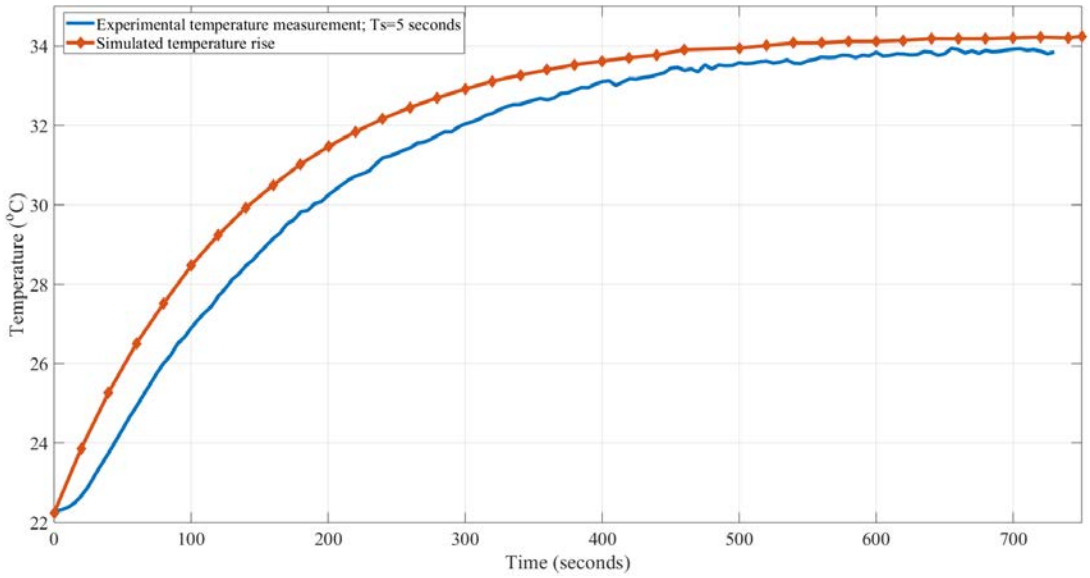


Figure 23. Comparison of experimental and simulated temperature rise of the heat sink connected to DC-DC converter

The thermal model is also verified by repeating the experiment at different ambient temperatures in a thermal chamber. The inverter setup running at 500 W is placed inside the thermal chamber for ambient temperatures of 25°C, 35°C, and 45°C. The conditions are simulated in the PLECS and the temperatures are plotted against the hardware results shown in Figure 24.

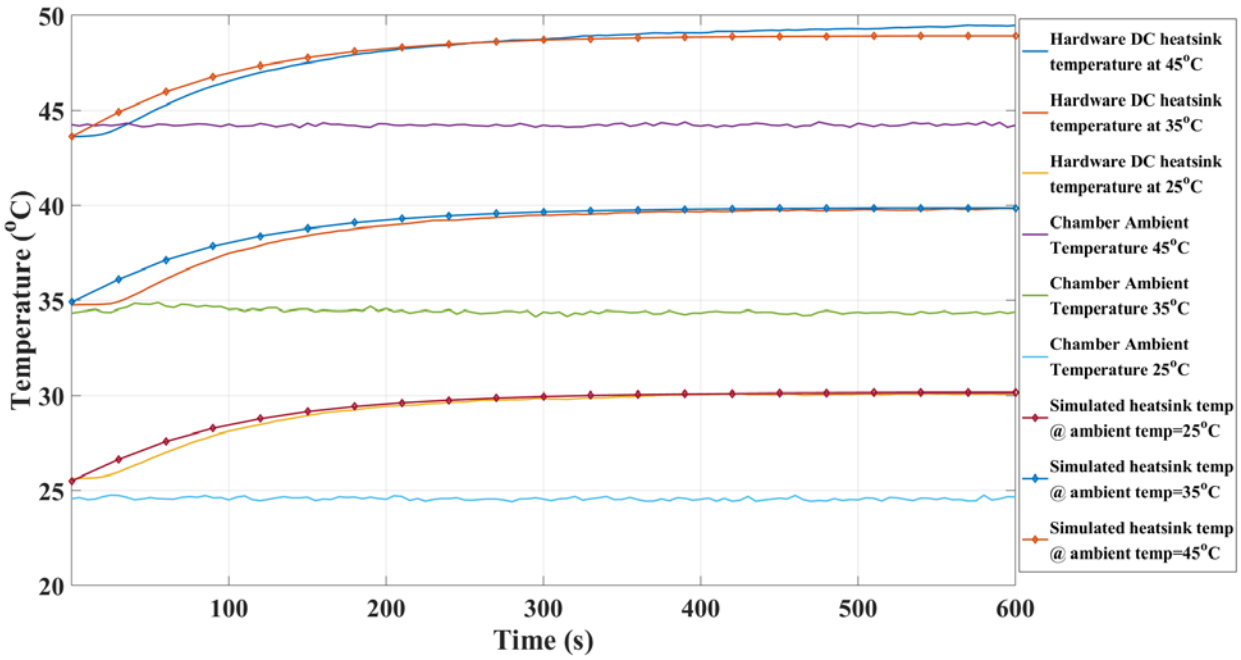
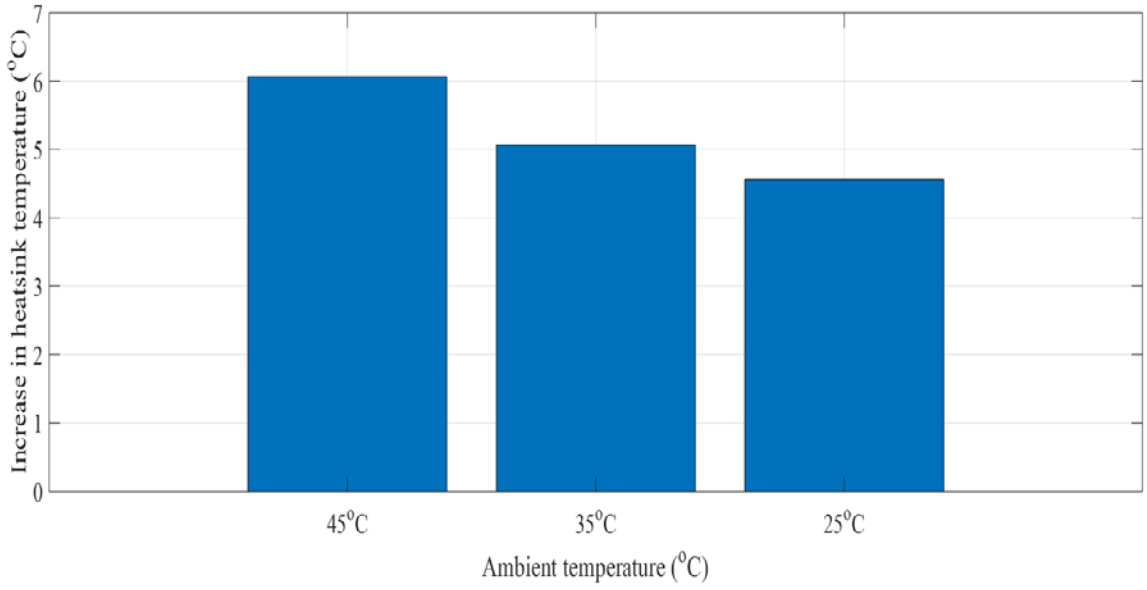


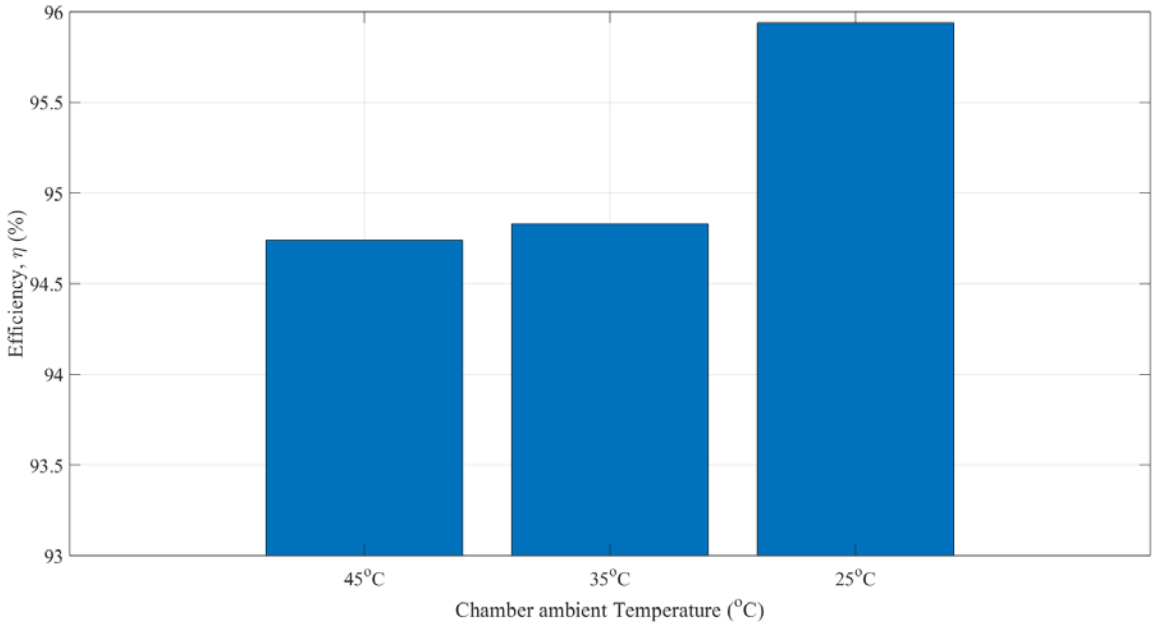
Figure 24. Comparison of hardware and simulated temperatures of inverter running in thermal chamber at different ambient temperatures

The power loss and efficiency data are also recorded for the thermal chamber experiment. As expected, the efficiency of the power converter decreases, and the power loss of the converter increases as the ambient temperatures increases. With the same experimental setup, the thermal

resistance of the heat sink remains constant. The increasing power loss translates to increasing temperature of the junction temperature of the switches and heat sinks. Figures 25 (a) and (b) show the increase in heat sink temperature and decrease in efficiency of the power converter as the ambient temperature increases.



(a)



(b)

Figure 25. Effect of ambient temperature on the power converter efficiency and junction temperature of the MOSFET

3 Reduced-Order Models for Annual Temperature Estimation

The models developed in the previous chapter to measure the losses and heat sink temperatures are suitable for short time periods, such as a few minutes, because of computational limitations. The computational limit for a few minutes is caused by the switching model and passive components, such as inductors and capacitors, which slow down the processing time. This model cannot be used to measure temperatures on an annual basis. Hence there is a need to use average models with analytic calculations to measure loss and temperature rise for time periods within a range from thousands of hours to a year. The following sections discuss the existing switching model and the simplification of these models to average models with formulae-based loss and temperature estimation.

3.1 Switching Model of the Inverter

The switching model of the inverter contains the electrical models of the switches along with the topology of the power converter, passive components, electrical model of a PV panel, and the closed-loop control for a grid-controlled inverter and maximum power point tracking of the inverter. Figure 26 shows the detailed electrical switching model of the inverter along with the topology and controls.

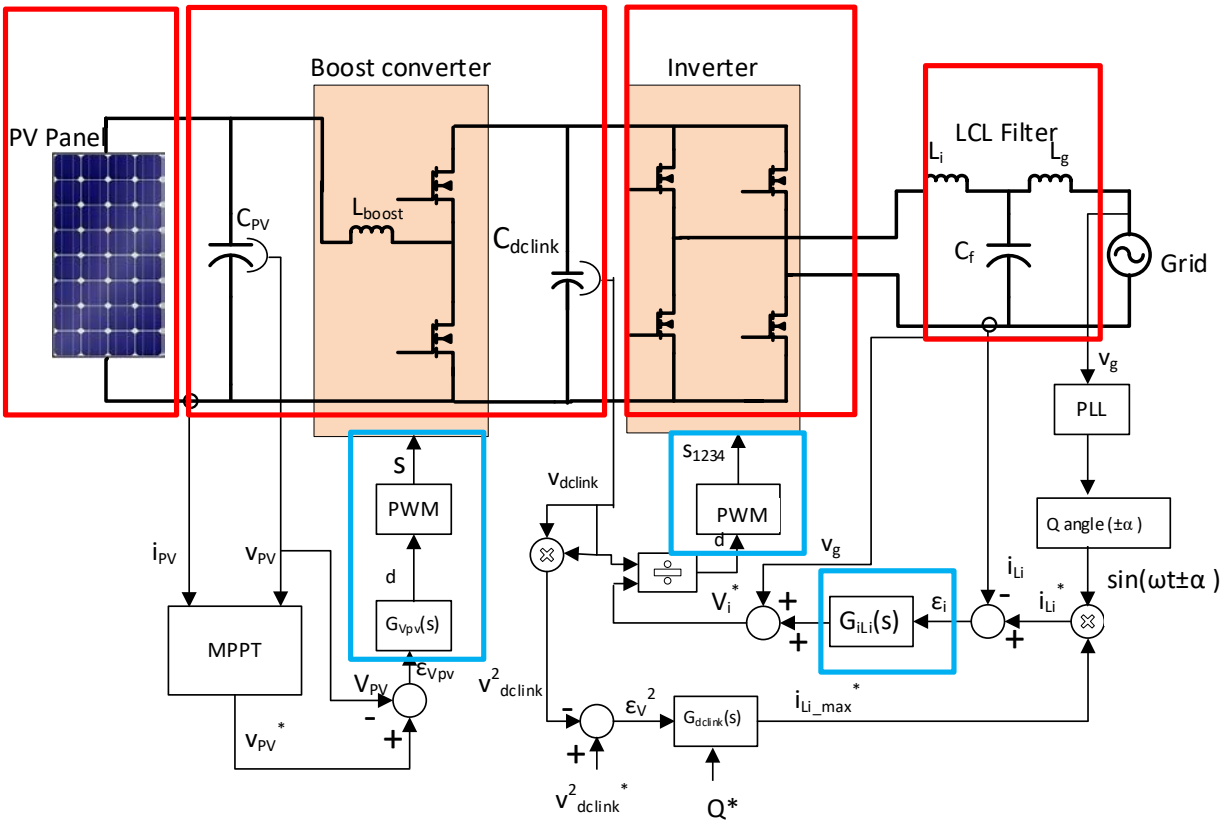


Figure 26. Detailed electrical switching model of two-stage inverter with controls

The power converter circuit consists of the electrical model of the PV module, synchronous boost converter, and H-bridge-based inverter with an LCL filter and grid source at the output. The controllers in the circuit include a maximum power point tracking controller for input power-side control, input voltage control, pulse-width modulations for the power switches, phase-locked loop for grid-following control, internal inverter current-control loop for generating the current reference, and an external DC-link voltage control for controlling the voltage of the DC-link capacitor along with its ripple requirements.

3.2 Development of Average Model

As mentioned previously, the computational time of a switching model of the power converter is very large because of the presence of the electrical model of the PV panel, passive components, power semiconductors, and high-speed controllers. These components must be further simplified into average analytic models to reduce computational time. Figure 27 shows the highlighted portions of the power converter model, which must be simplified to reduce computation time. The portions highlighted in red include the electrical models that must be simplified, and the blue portions are the controller blocks that must be eliminated.

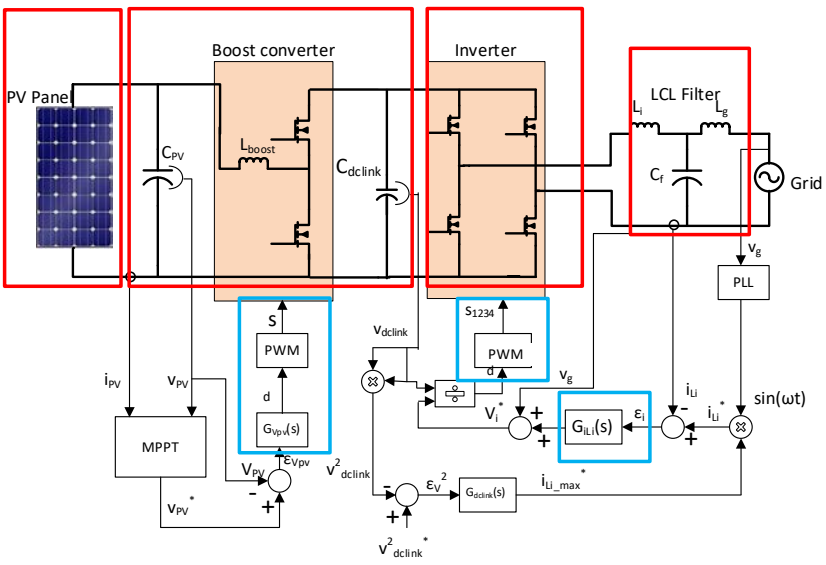


Figure 27. Simplification of the power converter model

The highlighted controller blocks in Figure 27 include the input voltage controller, inverter current reference controller, and pulse-width modulation of the power semiconductors. The two controllers are high-bandwidth controllers on the order of few kilohertz, which increases the computation time. The pulse-width modulation block includes the reference generation and its comparison with the duty cycle value, which, again, has a high computation time.

Among the power converter blocks to be reduced, the electrical model of the PV panel [51] [52] can be replaced with a physics-based analytic model, which estimates the output current of the PV module. The output current of the PV module is expressed by the following equation:

$$I_{PV} = N_p I_{sc}\left(\frac{G}{1000}\right) - N_p I_o\left(e^{\frac{qV_{PV}}{nN_s kT}} - 1\right) \quad (11)$$

where:

- I_{PV} is the PV array current expressed in amperes
- V_{PV} is the PV array voltage expressed in volts
- I_{sc} is the short current at an irradiance of 1000 W/m^2 expressed in amperes
- G is the solar insolation level expressed in percentages
- I_O is the dark saturation current expressed in amperes
- q is the charge of an electron expressed in coulomb
- n is the ideality factor
- N_s is the number of cells in series
- N_p is the number of cells in parallel
- K is the Boltzmann constant expressed in joules per kelvin
- T is the panel temperature expressed in kelvin.

The rest of the highlighted portions can be reduced using an averaged-switch model developed in [51], [46]. The paper uses the insolation or the irradiance and ambient temperature to represent

the equivalent of the electrical model of a PV panel, and the paper also develops the average model of the power converter along with its control. Figure 28 shows the averaged model of a single-phase PV inverter with its controller design.

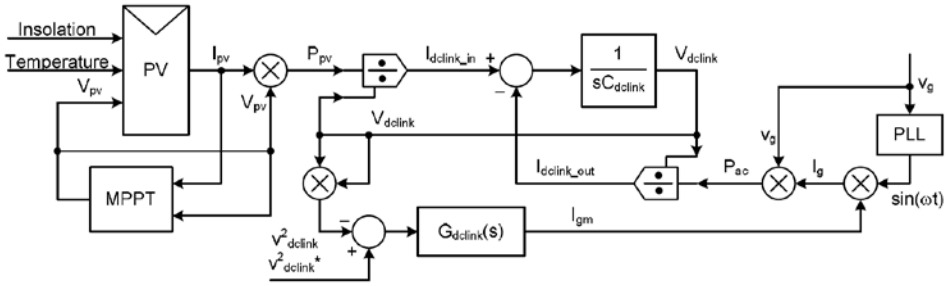


Figure 28. Averaged model of a single-phase PV inverter

The average model is implemented in PLECS. The model uses the same parameters as the homegrown inverter except for the input voltage source, which is replaced with the PV current source. The model is designed for the same switching frequency, DC-link voltage and AC grid voltage. Figure 29 shows the average model for the PV inverter developed in PLECS.

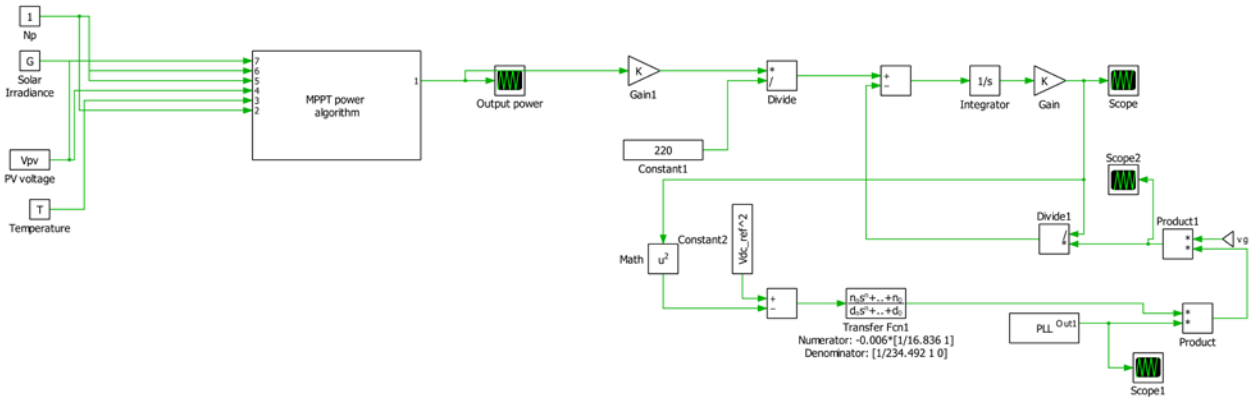


Figure 29. Averaged model of inverter developed in PLECS

3.3 Development of Averaged Loss Models

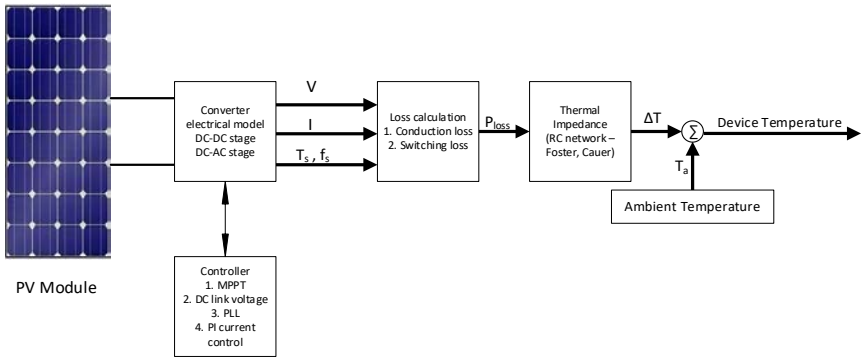


Figure 30. Loss model derivation from the PV Inverter electrical model

The average models developed for the PV inverter do not include the loss models of the power semiconductors, which help us estimate the junction temperatures [46]. The power conductor

loss models need parameters such as operating voltage, current, and switching frequency of the converter as well as specific parameters of the power semiconductor such as the on-state resistance, capacitance values related to the gate, drain and source of the MOSFET, and reverse recovery time. These parameters are used to estimate the switching and conduction losses of the power converter. The losses calculated are translated into an increase in temperature using the thermal impedance network (Foster and Cauer) of the power semiconductor. The obtained difference in temperature, ΔT, is added with the ambient temperature, T_a, to obtain the device temperatures. Figure 30 shows the development of the loss models from the electrical model of the power converter.

The same procedure explained is repeated to estimate the junction temperature of the power semiconductor from the average model of the semiconductor. Figure 31 shows the implementation of the average loss models from the average PV inverter model.

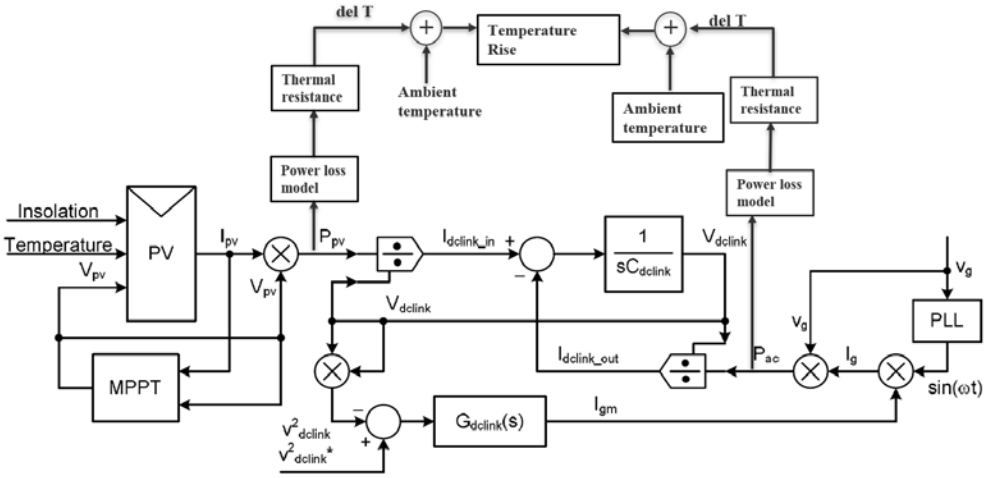


Figure 31. Implementation of averaged loss models from average PV Inverter model

3.3.1 Implementing Annual Simulation Models

Using the average inverter and loss models, junction temperature data in the range of thousands of hours can be estimated with the same computation made available for the switching model. Using the combined average model, with solar irradiance and ambient temperature as input during an entire year, the junction temperature profile throughout the year can be obtained from the model shown in Figure 32.

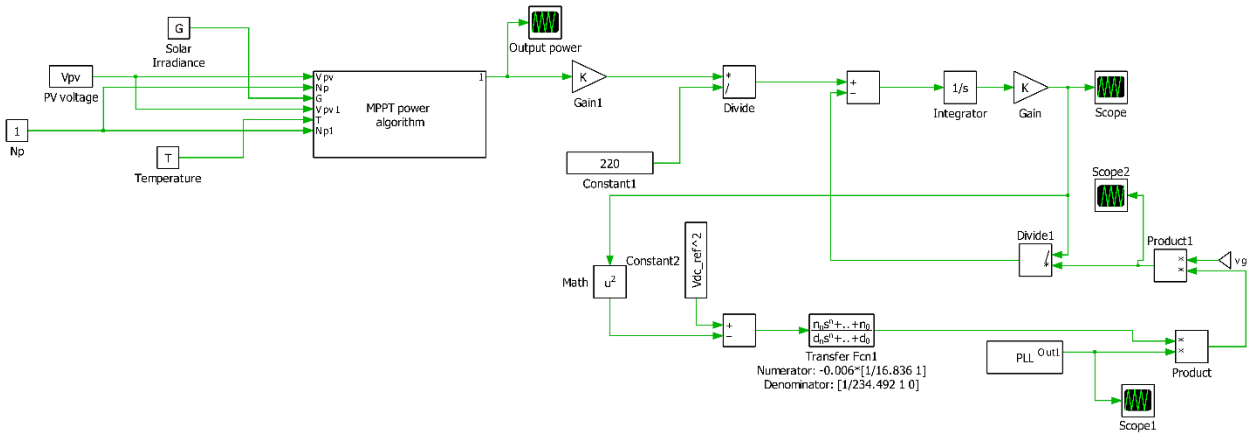


Figure 32. Implementation of yearlong average inverter loss model

To account for variations in temperature and irradiance at a location throughout many years, temperature and irradiance inputs from the typical meteorological year (TMY) data are used as input for the data. To account for the diversity in weather, two locations with extreme temperatures are chosen: Phoenix, Arizona, a hot location; and Ft. Peck, Montana, a cold location [53], [54]. The ambient temperature data are provided in degrees Celsius. The irradiance data are chosen from the global horizontal irradiance data. Figure 32 shows the implementation of the yearlong model from the TMY data. The irradiance and temperature variations at the two locations contribute to different annual PV power production at two locations. Figures 33 (a) and (b) show the power production at Ft. Peck and Phoenix, respectively. As shown, Ft, Peck has less annual PV power production and Phoenix has more power production.

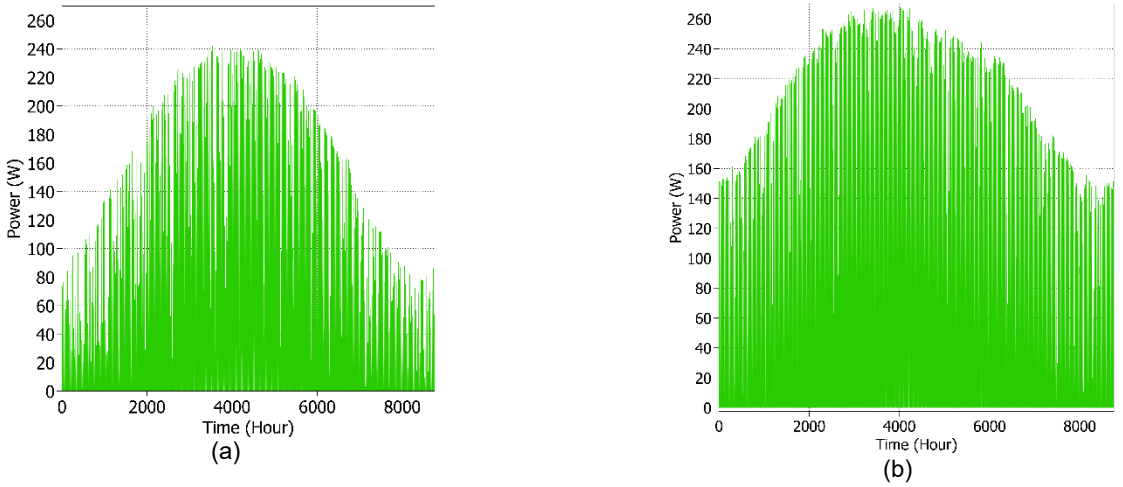


Figure 33. Annual PV power production at (a) Ft. Peck and (b) Phoenix

With the input PV power obtained from the irradiance and temperature data, the average inverter loss model can be used to measure the junction and heat sink temperatures of the DC-DC converter and H-bridge inverter. The inverter model also includes an efficiency block after the PV power production stage to account for the power losses. Figures 34 (a) and (b) show the annual temperature increase of the heat sink at Ft. Peck and Phoenix.

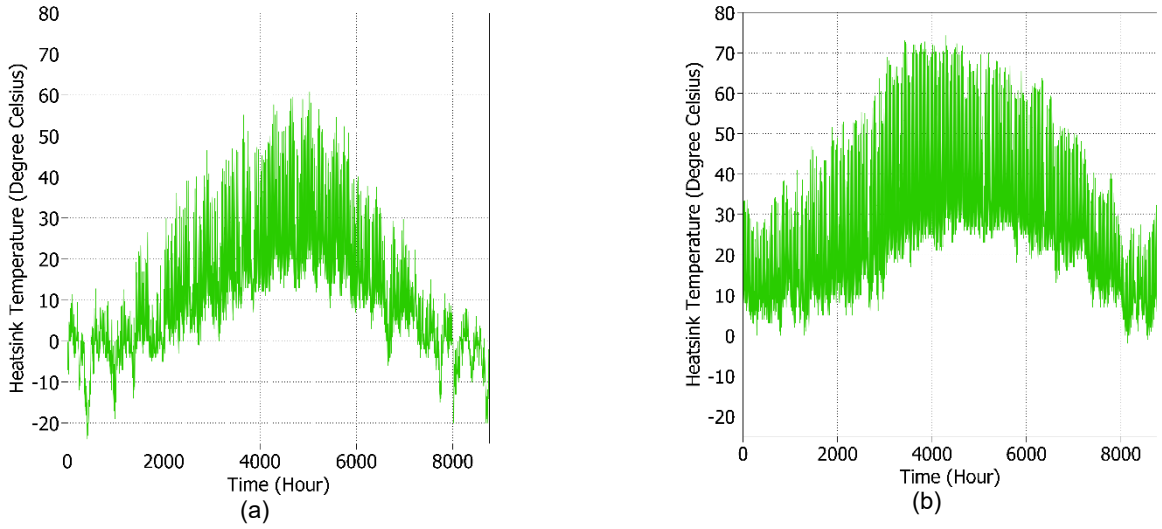


Figure 34. Annual heat sink temperatures of the DC-DC converter at (a) Ft. Peck and (b) Phoenix

3.4 Rain Flow Counting

Rain flow counting data are used process the data with varying stress levels into a data set of simple intervals [55]. This is useful for processing the annual temperature data obtained in the previous section. Figure 35 shows the rain flow counting results of the temperature data obtained from Ft. Peck

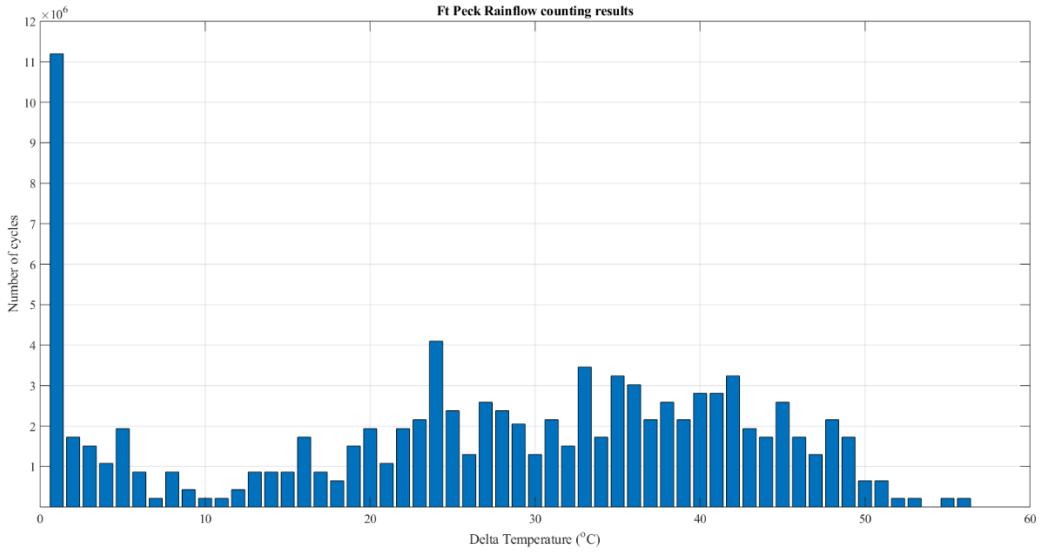


Figure 35. Rain flow counting results of the junction temperature data at Ft. Peck

4 Estimation of Reliability and Useful Lifetime

The results of the yearlong model give us the junction temperatures of the power semiconductors and the relative variations in the temperature of the heat sinks. The junction temperature data are fed through a rain flow counting algorithm to record the number of device cycles under each difference in junction temperature, ΔT_j. Applying the number of cycles and ΔT_j to the lifecycle model gives us the lifetime of the power semiconductors. This chapter describes the research performed in evaluating existing lifetime models in the literature as well as the proposed lifetime model. Finally, the lifetime prediction framework will be extended to assess the impacts of reactive power on the inverter system using the same analysis.

4.1 Survey of Lifetime Models of Power Semiconductors

4.1.1 Coffin-Manson Model

The Coffin-Manson model is frequently used to predict failures caused by deformation or cracks induced by thermomechanical stress or change in temperature. The thermomechanical stress is used to predict solder joint failures caused by temperature cycling in electronic components [56], [57], [58].

The Coffin-Manson model predicts the number of kilocycles subjected to stress at different junction temperatures, ΔT_j, and mean junction temperatures, T_m. The number of kilocycles to failure, N_f, is given by the following equation:

$$N_f = a \times (\Delta T_j)^{-n} \times e^{\frac{E_a}{k.T_m}} \tag{12}$$

where a is the experimental coefficient; n is the Coffin-Manson coefficient, which depends on the chosen failure mechanism; E_a is the activation energy, and k is the Boltzmann constant.

A simplified Coffin-Manson model eliminates the exponential term and neglects the effect of mean junction temperature. It is expressed as:

$$N_f = a \times (\Delta T_j)^{-n} \tag{13}$$

The Coffin-Manson model does not include parameters such as frequency of cycling and geometry of the solder joint. These are included in a semiempirical model developed by Engelmaier [59], [60], [61].

4.1.2 Norris-Landsberg Model

The Norris-Landzberg model [62], [63], [64] is an analytic model that includes the effect of the frequency of cycling along with the parameters included in the detailed Coffin-Manson model. It is expressed in the following equation, where f is the frequency of cycling, and n_2 is an additional experimental coefficient:

$$N_f = a \times f^{-n_2} \times (\Delta T_j)^{-n_1} \times e^{\frac{E_a}{k.T_m}} \tag{14}$$

4.1.3 Bayerer Model

The Bayerer [62], [65], [66] model is the detailed analytic model available to estimate the kilocycles to failure using parameters in addition to those in the Coffin-Manson equation, such as the heating time, t_{on}, applied current, I_{DC}, diameter of the bond wire, D, and blocking voltage, V_{block}:

$$N_f = a \times (\Delta T_j)^{-n_1} \times e^{\frac{E_a}{k.Tm}} \times {t_{on}}^{\beta_3} \times {I_{DC}}^{\beta_4} \times {V_{block}}^{\beta_5} \times D^{\beta_6} \quad (15)$$

where, a, n, and β are experimental parameters derived from large data of power semiconductor cycling.

4.2 Cumulative Stress

The stress accumulated during the mission profile of a power semiconductor at different power levels, irradiance, and ambient temperatures is translated into different ΔT_j using the multi-timescale thermal model developed in Chapter 3. The lifetime model equations give the number of cycles to failure, N_f, at a difference in junction temperature of the power semiconductor, ΔT_j. The rain flow counting of the yearlong junction temperatures gives the number of cycles accumulated during the mission profile, N_i. To estimate the cumulative stress, an assumption of linear damage is considered, typically referred to as the Miner's rule [56], [67], [68]. The cumulative stress calculated by Miner's rule is expressed as:

$$Q = \sum_{i=1}^{n} \frac{N_i}{N_{fi}} \quad (16)$$

where, i=1,2, 3, …, n represents the various differences in junction temperature of the power semiconductor, ΔT_j.

The cumulative stress has a value less than one. The reciprocal, $\frac{1}{Q}$, gives the number of mission profiles the device can survive for the same mission profile. In our case, each mission profile represents a TMY, and the number of mission profile refers to the number of years the power semiconductor device can survive.

4.3 Reliability Indices

The cumulative stress rate and lifetime estimation are expressed in terms of number of mission profiles or number of cycles the power semiconductor is estimated to fail; however, these estimations are calculated for a particular condition or sample size. To account for the variations in conditions and the uncertainty in manufacturing more than a million devices, the failure rates must be characterized using a probability density function [69].

The failure function, F(t), estimates the probability of a device failure at or before time, t. This is expressed as:

$$F(t) = \int_o^t f(\tau).d\tau \quad (17)$$

where F(∞)=1. As time tends to infinity, the probability of device failure goes from 0 to 1 or 0% to 100%. The reliability function, R(t), is expressed as:

$$R(t) = 1 - F(t) \tag{18}$$

implying that the reliability function tends to zero as time increases to infinity.

In commercial applications, the device manufacturer provides a failure rate term called failure in time (FIT), typically referred to as the FIT number [70]. The FIT number estimates the number of failures that happened during a million hours. FIT is expressed by the following equation:

$$FIT = \frac{10^9 \times F}{SS \times t} \tag{19}$$

where F is the number of observed failures, SS is the sample size of the devices under test, and t is the number of hours the devices were subjected to. The manufacturer provides the FIT number, the product of the number of sample size, and the number of hours the devices were subjected to. The FIT number provided by the manufacturer is calculated for a single junction temperature, with a activation energy and confidence value, according to the JEDEC Standard JESD 85: Methods for Calculating Failure Rates in Units of FITs [71].

To account for the variations in an entire component population, the statistical confidence factor, $\frac{\chi^2}{2}$, must be included to estimate the normalized FIT. The statistical confidence factor, $\frac{\chi^2}{2}$, depends on the failure rate, F, and confidence level provided by the manufacturer. The normalized FIT is calculated as:

$$FIT_{norm} = \frac{\chi^2}{2} \times \frac{10^9 \times F}{SS \times t} \tag{20}$$

The estimation of normalized FIT value can be related to another reliability term, mean time to failure (MTTF). MTTF is expressed as a ratio of million hours and normalized FIT value:

$$MTTF = \frac{10^9}{FIT_{norm}} \tag{21}$$

4.4 Proposed Lifetime Model

The simplified Coffin-Manson model uses the difference in junction temperature, ΔT_j:

$$N_f = MTTF \times \Delta T_j \text{^} - m \tag{22}$$

The power semiconductor manufacturer provides the Coffin-Manson coefficients for various failure modes. Among the failure mechanisms, aluminum wire bond failure is the most common failure mechanism, and its coefficient is used in Eq. 22. The MTTF obtained from the normalized FIT values is used in the equation.

The proposed model was compared with an avalanche-based lifetime model [56] to estimate the remaining useful lifetime. Table 3 shows compares the avalanche-based lifetime model and MTTF-based model for the inverter power semiconductor temperatures.

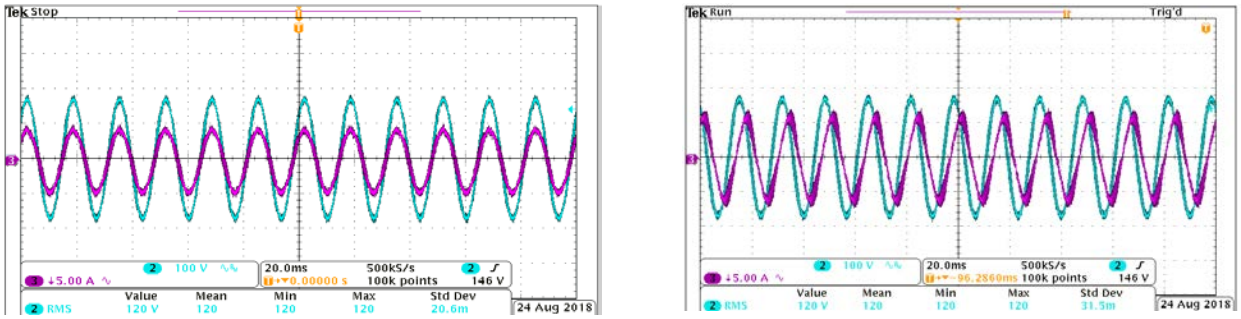
Table 3. Lifetime Model Comparison of Avalanche-Based Model and MTTF-Based Model

Mission Profile	Avalanche-Based Lifetime Model	MTTF-Based Lifetime Model
Ft. Peck, MT	140.2 yr	138.1 yr
Phoenix, AZ	66.6 yr	64.4 yr

4.5 Influence of Reactive Power

Historically, most PV inverters tried to operate at unity power factor, i.e., zero reactive power absorbing or supplying. With the new grid codes as well as utility requirements, however, inverters must operate at a nonunity power factor or absorb and supply reactive power for change in voltage or frequency [72].

With the additional reactive power, the total apparent power of the inverter will increase, which will translate into increased currents flowing through the inverter switches. To validate this experimentally, the inverter was operated in grid-connected mode with two operating set points. One set point was real power, P=400 W, and reactive power, Q= 0 VAR. The other set point was real power, P=400 W, and reactive power, Q=300 VAR. Figures 36 (a) and (b) show the inverter current and voltage waveforms at the two set points.



(a) (b)

Figure 36. Inverter current and voltage waveforms for (a) P=400 W and (b) P=400 W and Q=300 VAR, respectively

The reactive power leads to increased currents in the inverter switches, which translates to increased power losses and an increase in heat sink temperature. Figure 37 shows compares junction temperature for two set points: P=400 W and P=400 W, Q=300 VAR.

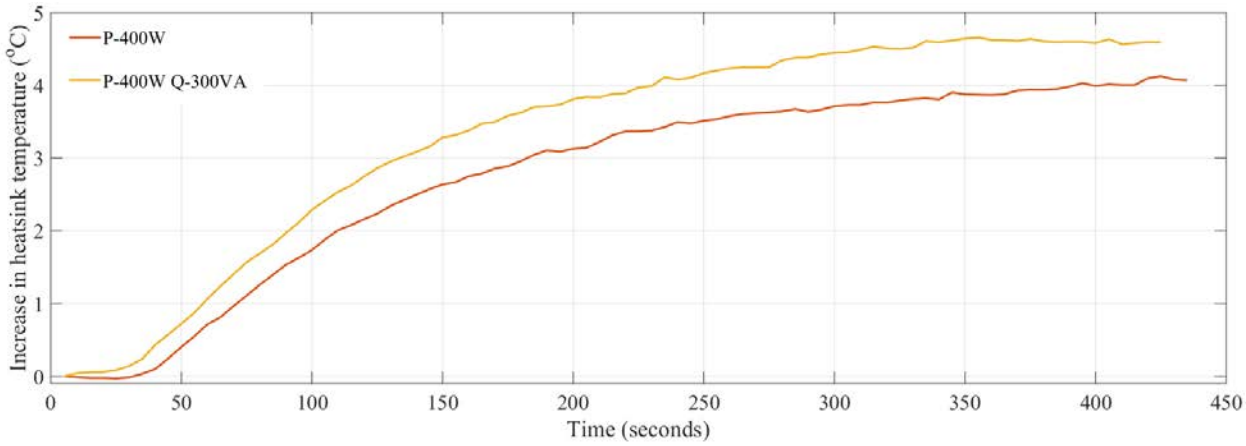


Figure 37. Comparison of heat sink temperatures for P=400 W, Q=0 VAR, and P=400 W, Q=300 VAR

Few papers have studied the effect of reactive power on thermal performance and inverter reliability. Reference [73] considered the impact of reactive power injection outside the feed-in operating hours. In this paper, real power is equal to zero when reactive power is injected into the grid. Reference [74] studied the impact of reactive power injections on the thermal performance of the PV inverters. Reference [75] discussed the effect of nonunity power factor in PV inverters for grid support functions.

The yearlong mission profile was repeated for the Phoenix TMY conditions, with a constant reactive power injection of 20 VAR into the grid. The yearly AC power output for the Phoenix TMY with and without the reactive power injection is shown in figures 38 (a) and (b).

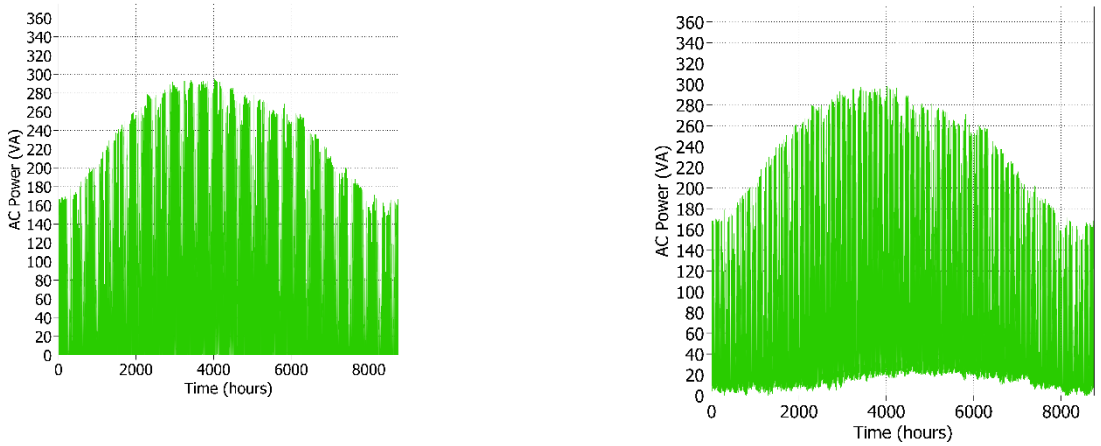


Figure 38. Annual AC power output for Phoenix TMY (a) without reactive power injection and (b) with reactive power injection

After sorting the data through rain flow counting, we see minor differences in the number of cycles at each ΔT_j of the power semiconductor. Figure 39 shows the bar graph comparison for the number of cycles at each ΔT_j for the Phoenix TMY with and without reactive power injection.

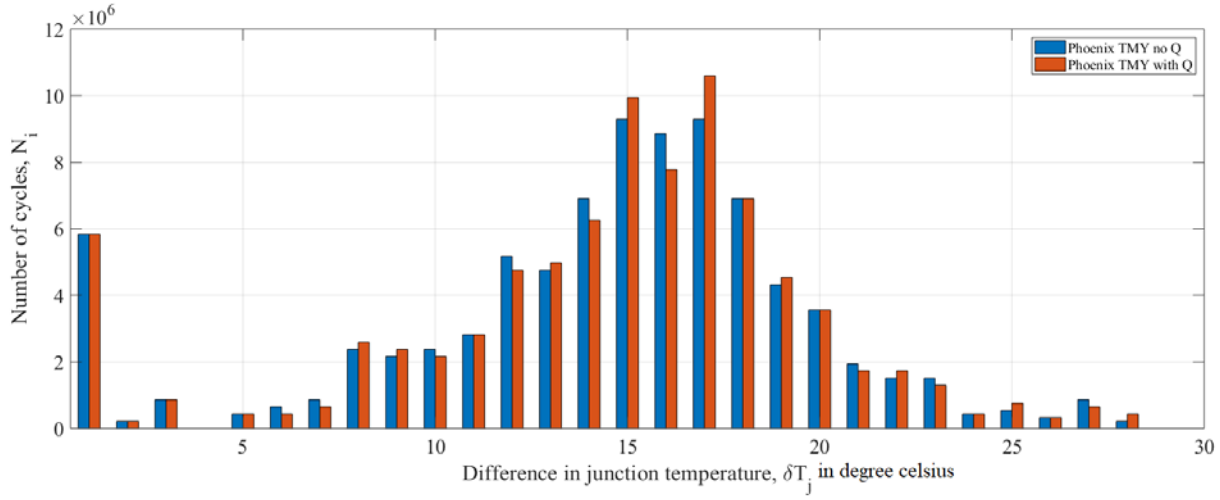


Figure 39. Bar graph comparison of number of cycles at each ΔT_j for the Phoenix TMY with and without reactive power injection

The yearlong mission profiles for the Phoenix TMY are also repeated for power factors at 0.95 p.u., 0.90 p.u., and 0.80 p.u [76] [77]. Reactive power, Q, increases as the power factor decreases from unity power factor. Figure 40 shows the bar graph of the number of cycles with various ΔT_j for power factors 1 p.u., 0.95 p.u., 0.90 p.u., and 0.80 p.u.

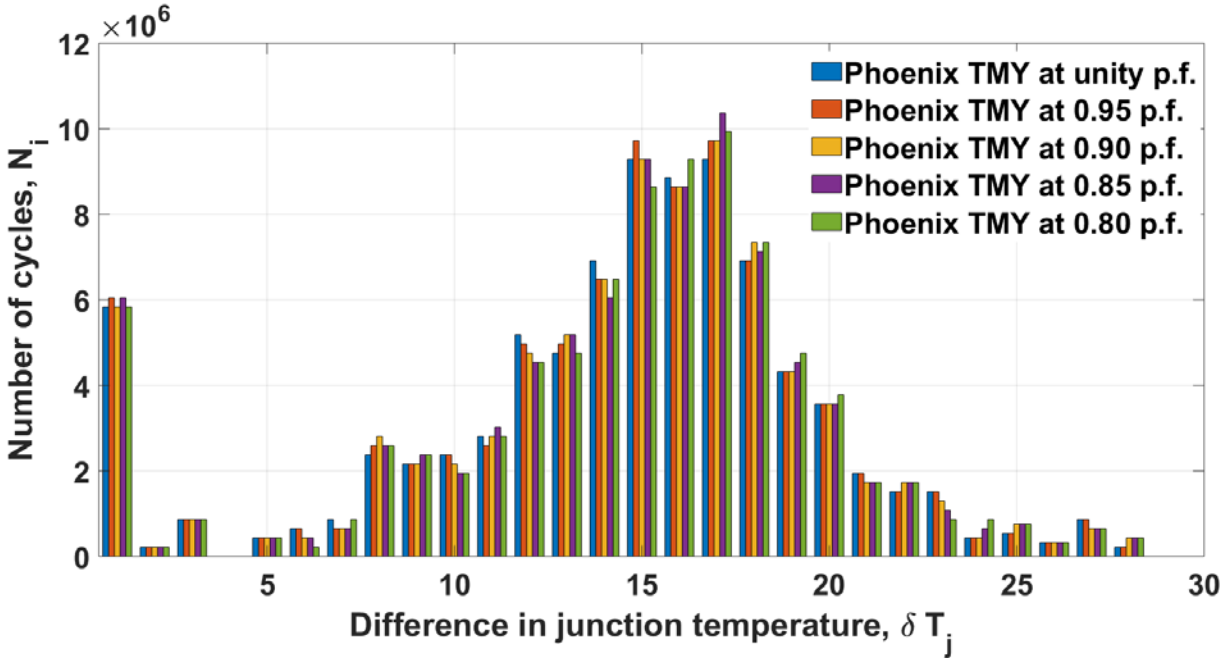


Figure 40. Bar graph comparison of number of cycles at each ΔT_j for the Phoenix TMY at power factors 1 p.u., 0.95 p.u., 0.90 p.u., and 0.80 p.u.

The remaining useful lifetime is estimated from the rain flow counting data. Figure 41 shows the remaining useful lifetime versus the power factor operation for the Phoenix TMY. The remaining useful lifetime decreases as the operating power factor deviates from unity power factor.

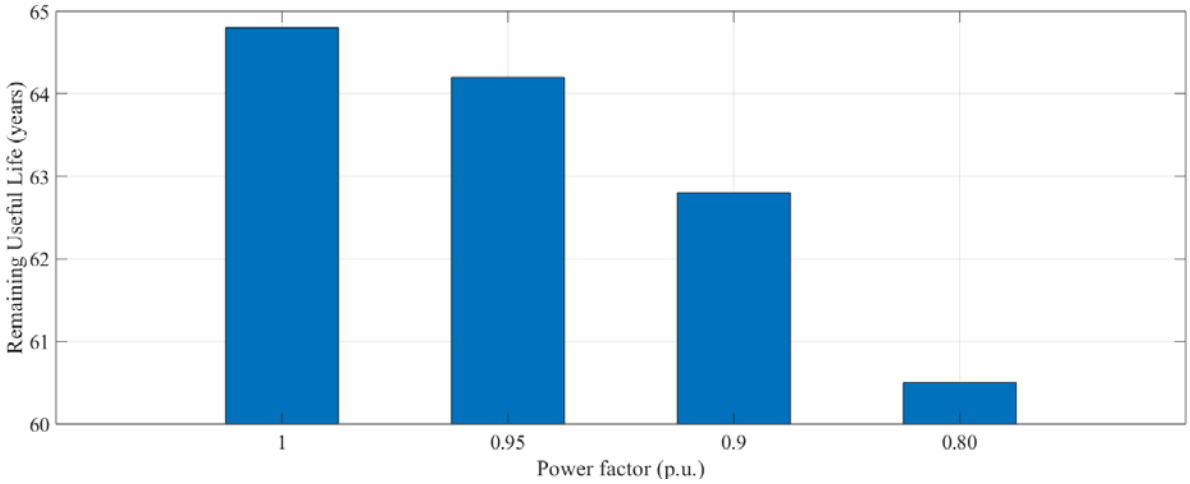


Figure 41. Comparison of remaining useful lifetime versus the operating power factor for the Phoenix TMY

4.6 Inverter System Reliability and Lifetime

The system reliability of the inverter depends on the number of components. In a system with n components, the system cannot perform if one of the n components fails. The total unreliability is given by:

$$F_{total}(x) = 1 - \prod_n (1 - F_n(x)) \tag{23}$$

This report considers only the thermal cycling effect on the power semiconductors in the power stage of the PV inverter. The overall system reliability and lifetime also depends on the DC-link capacitors, gate driver circuitry, inductors, and other power stage components. The effects of these components are not included in the current model; however, Eq. 23 helps calculate the total reliability once the other components effects are included.

This report also does not include effects of other external phenomenon, such as humidity on the inverter reliability and lifetime. Unlike thermal cycling, which causes the power stage devices to derate and have one-time failure events, humidity causes other effects on the inverter, including corrosion from diffusion through potting and ion migration. These effects will be studied in future and models will be developed to include effects such as humidity, and they will be validated with experiments. The observations and results from these studies will be passed to the International Electrotechincal Commission (IEC) standards development committee currently involved in developing the new draft on IEC 62093: Balance-of-system components for photovoltaic systems – Design qualification natural environments [76].

5 Conclusions

This research was motivated by the fact that as the price of PV modules decreases, the price of power electronics becomes a topic of research. The cost of power electronics is mostly increased by frequent hardware failures when compared with the long lifetime of PV modules. Additionally, as efforts to reduce PV module costs yield diminishing returns, understanding and reducing inverter costs becomes increasingly critical and is a cost-effective investment toward achieving DOE Solar Energy Technologies Office goals.

Inverter reliability is a layered topic because of its complicated switching/monitoring system, and many things can cause a failure. In addition to providing output power meeting power quality standards, the inverter might be required to manage the power output of the PV module, connect/disconnect from the grid, read and report status, or monitor islanding.

With these motivations, the research described in this report evaluated and predicted inverter life. Because finding individual component part numbers from off-the-shelf inverters is cumbersome, an inverter hardware was built in-house. Subsequently, electrothermal inverter models were built to match the in-house hardware. The electrothermal model of the inverter was developed to perform a detailed study of losses and thermal impacts on inverter life. The electrothermal model was validated with the in-house inverter's heat sink temperatures at different ambient temperatures with the goal to make the model scalable.

An inverter averaged-switch model was built from the detailed switching model to enable annual simulations to assess the cumulative effect of ambient temperatures. The multi-timescale model was simulated for TMY data in Phoenix, Arizona, and Ft. Peck, Montana, to capture diverse weather conditions. The junction temperatures from the simulation were measured during the entire year and processed using rain flow counting to obtain the number of cycles under each junction temperature. The number of cycles were then used to evaluate the existing lifetime of the transistors within the inverter. The new lifetime model was compared with existing avalanche lifetime model. Finally, the influence of reactive power on the reliability of the PV inverters was studied. Results showed that transistor lifetime decreased as the operating power factor decreases. The lifetime of an inverter—which is the number of useful cycles the inverter can survive for the same mission profile—was calculated using existing approaches, and a comparison was made between the avalanche-based and MTTF-based inverter models for the Phoenix and Ft. Peck regions. Additionally, the impact of lifetime was evaluated for inverter use with and without reactive power set points for multiyear analysis, and it was found that using an inverter for reactive power support on a regular basis reduces the lifetime. An inverter's lifetime was reduced by 7.6% when an inverter was simulated at 0.8 absorbing power factor instead of unity power factor.

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