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Preprint

David L. Young, San Theingi, Vincenzo LaSalvia, Kejun Chen, William Nemeth, Dawn Findley, Matthew Page, and Pauls Stradins

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Self-Aligned, Selective Area Poly-Si/SiO₂ Passivated Contacts for Enhanced Photocurrent in Front/Back Solar Cells

David L. Young, San Theingi, Vincenzo LaSalvia, Kejun Chen, William Nemeth, Dawn Findley, Matthew Page and Pauls Stradins

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Abstract — Poly-Si/SiO₂ passivated contact front/back solar cells suffer low J_{sc} due to parasitic absorption in the front poly-Si layer. We demonstrate a self-aligned, selective area front contact dry-etch technique that retains the as-deposited poly-Si beneath the metal grid lines but thins it elsewhere. J_{sc} improves by 0.7 mA/cm² over our standard 40 nm thick poly-Si. Greater improvements are expected with thicker poly-Si needed for fired metal contacts. Surface passivation is slightly diminished with poly-Si thinning but can be partially restored with re-hydrogenation.

Index Terms —silicon devices, photovoltaic cells, Ohmic contacts.

I. INTRODUCTION

Poly-Si/SiO₂ passivated contacts are a promising route to high efficiency, high V_{oc} cells due to their excellent J_0 values[1, 2], high-temperature impurity gettering properties[3] and wide process window. Record IBC polySi-Si/SiO₂ contact structures have been formed[4], but industry is more likely to adopt the less complex front/back cell configuration in the near term. Thus far, front/back poly-Si/SiO₂ devices have suffered from low J_{sc} values due to parasitic absorption in the front poly-Si layer and in the often-implemented front TCO layer.[5-8] Thinning of the poly-Si layer[9] or growing C- or O-containing polySi alloys[10, 11] to increase the bandgap have been shown to decrease this loss. However, maintaining the passivation during metal grid formation is difficult as the poly-Si thickness decreases. This is true for laboratory deposition techniques like thermal and e-beam evaporation of metals, but even more severe for fired screen-printed contacts. Thus, a tradeoff exists between growing thin enough front poly-Si to minimize J_{sc} loss and thick enough poly-Si to allow passivated metal contacts. Ideally, forming a selective area passivated contact region only under the contacts would remove this trade-off. Indeed, Ingenito et al. showed an improvement in J_{sc} by wet chemically etching the front poly-Si/SiO₂/c-Si region between the metal fingers using a photolithography-based patterning technique.[9]

Here, we report self-aligned, selective-area poly-Si/SiO₂ contacts without the need for photolithography techniques using a simple dry reactive ion etch process using the pre-formed front metal grid as an etch mask. Our preliminary studies show that the process can remove poly-Si gently enough to preserve surface passivation and increase J_{sc} with minimal V_{oc} and FF loss.

II. EXPERIMENTAL

We based this experiment on our previously reported TCO-free rear junction, front/back poly-Si/SiO₂ device[12] to capitalize on carrier transport to the front contacts through the wafer rather than through the highly resistive poly-Si:P layer. The goal was to thin the poly-Si between the grid fingers without detrimental effects on the FF. n-Cz single-side textured Woongjin wafers were piranha and RCA cleaned and then etched in 1% HF until hydrophobic before loading into a clean tube furnace to grow a low temperature oxide on both sides of the samples at 700 °C for 5 mins. Next, p/n a-Si:H layers were grown over the oxide using PECVD and SiH₄ and H. The textured side of the wafer received 40 nm of P-doped a-Si:H over the full area, while the non-textured side of the wafer received 40 nm of B-doped a-Si:H deposited through a 4 cm² opening in a mask held between the sample and the plasma to define rear emitter regions. Next, samples were annealed in a tube furnace at 850 °C for 30 mins to crystallize the a-Si into poly-Si and to diffuse dopants. Hydrogenation of the samples was accomplished by deposition of 15 nm of Al₂O₃ using atomic layer deposition of trimethylaluminum (TMA) and water followed by a 400 °C forming gas anneal (FGA).

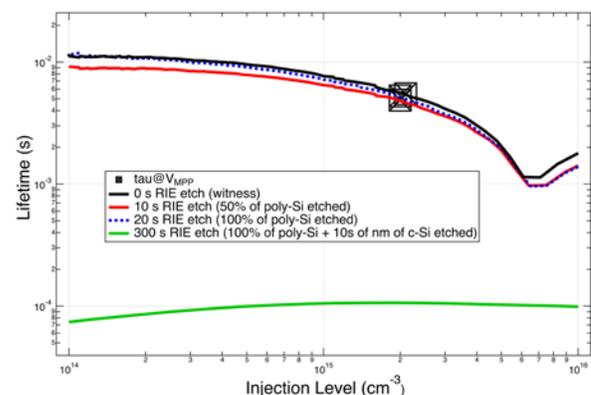


Fig. 1. Lifetime vs injection level for samples RIE etched to remove n⁺ poly-Si between Al grid lines. Lifetime is preserved for up to 100% of the poly-Si removed.

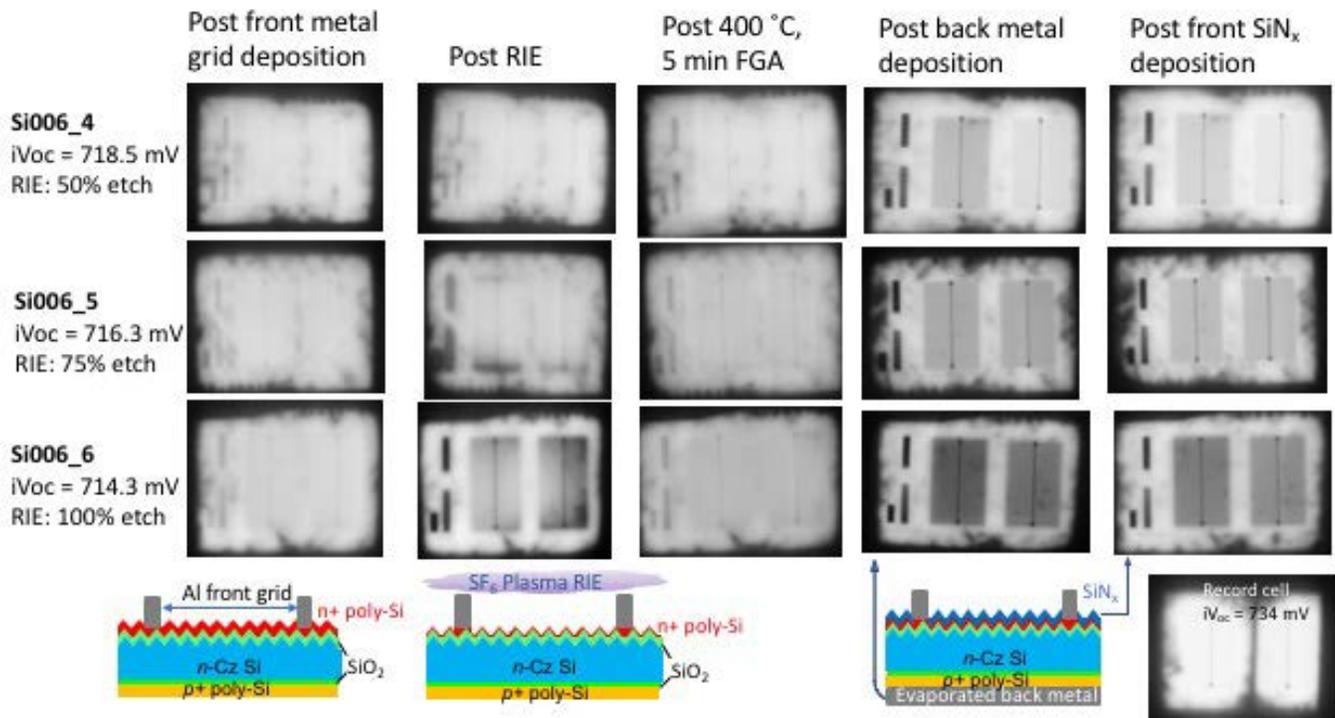


Fig. 2. $\frac{1}{4}$ second exposure photoluminescence images of samples RIE etched to remove 50%, 75% and 100% of the front, n^+ poly-Si layer between Al grid lines. Images in rows show the progression of the sample from post front metal deposition to a final SiN_x coating. The bottom right image is a record device not processed with the other samples in this series.

Thermally evaporated Al through a shadow mask formed the front grid and single bus bar on the n-type poly-Si:P side of the device.

Next the samples were RIE-etched using SF_6 and a low-power plasma to remove the n-type poly-Si material between the Al grid fingers (See schematics in Fig. 2). The Al fingers acted as a plasma etch mask and were not affected by the plasma etching atmosphere either in appearance or contact resistivity. Calibration of the etch rate was done with poly-Si films grown on quartz substrates using optical transparency models to determine layer thicknesses. A re-passivation of the cell was conducted using only a FGA followed by full-area thermal evaporation of Al on the p-type poly-Si:B mesa back side of the device. Finally, a SiN_x antireflection coating was added to the textured side of the device.

III. RESULTS

Fig. 1 shows photoconductive decay effective lifetime vs injection level data for a series of n-type symmetric passivated contact samples etched by RIE to remove 0%, 50% and 100% of the 40 nm poly-Si and one sample that was etched for longer to remove the poly-Si and a few 10s of nm into the c-Si wafer. The data show no change in lifetime for the samples where only the poly-Si was etched, but a drastic drop for the sample that was etched into the wafer. No re-passivation processing was done on these samples. For all of the data shown here the

“100%” etch refers to the longest etch time before passivation failed. Some poly-Si may still remain on the sample either as a very thin layer or as islands, as was observed by cross-sectional TEM (not shown). Moving to devices, Fig. 2 shows $\frac{1}{4}$ second exposure photoluminescence (PL) images for a series of devices etched between 0 and 20 seconds in the plasma RIE to remove 0% to 100% of the poly-Si. The RIE removal percentages are listed along with pre-metal implied open circuit voltages (iV_{oc}) for each device on the left. The first column of images show that the devices have excellent luminescence after grid metallization, even under the grid. After the RIE etch the PL signal dims with increasing etch time in the field area and even under the metal grid lines, but recovers significantly after a FGA - especially under the metal areas. However, after the evaporation of the back metal on the p-type emitter, the PL signals are much lower for the longer etch time samples and does not improve much with the addition of the SiN_x layer. We speculate that the thinner front poly-Si is not able to withstand the back metallization process without loss of passivation. Standard, thick layers of poly-Si are able to maintain excellent passivation during the evaporation of the back metal possibly by helping to protect the sensitive poly-Si/ SiO_2 /c-si interface. Adding the SiN_x layer to the front *before* depositing the back metal may help to protect the thin poly-Si. NOTE: The PL for the witness sample with no RIE etching was unusually low for this particular series, so our record device was used for

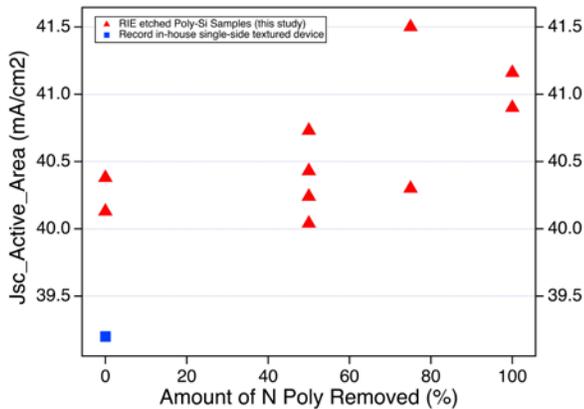


Fig. 3. Active-area J_{sc} values vs the percent amount removed from 40 nm of n+ poly-Si by RIE etch as calibrated by etch time.

comparison in Fig. 2. The record device had a much higher pre-metal iV_{oc} than the samples used in this experiment, so its PL signal is significantly brighter. Overall, the RIE etching with a FGA on the tested samples does not severely affect the PL signal despite removing most of the heavily doped poly-Si layer.

We next recorded current vs voltage data under 1-sun AM1.5 conditions and found that, as expected, J_{sc} improved with removal of the front poly-Si layer. Fig. 3 shows the active area J_{sc} for devices with 0 – 100% of the front poly-Si removed by RIE as calibrated by etch time. We used active area current densities to account for variations in the metal grid area coverage from sample to sample. There is quite a bit of scatter in the data, but comparing the 0% to the 100% cells, we see about a 0.7 mA/cm² increase with the removal of the poly-Si. We see a similar increase for double-side textured samples (data not shown here). This boost in current is only about 40% of what we expected from our SunSolve modeling where the front poly-Si n+ layer parasitically absorbs about 1.6 mA/cm² of current.[12] The record cell's data are also shown in Fig 3. Using an active area current density, our record cell would have an efficiency of 22.6% with a V_{oc} of 722 mV. The boost in current density by forming selective-area contacts could well push this device beyond 23%.

As implied in Fig 2. thinning the poly-Si layer did lower the passivation in the devices and resulted in reduced V_{oc} and FF by values larger than typically seen after metallization. Fig. 4 shows iV_{oc} , V_{oc} and FF values for samples etched to remove 50 – 100% of the poly-Si layer. The $iV_{oc} - V_{oc}$ difference for the 50% thinned sample is better or typical (~ -10mV) for devices following this process procedure. As a larger percentage of the poly-Si layer is thinned, the $iV_{oc} - V_{oc}$ difference increases and is close to 20 mV for the 100% poly-Si thinned sample. Fig 4 also shows FF follows a similar decrease with increasing etched poly-Si percentage with FF loss analysis showing 1% loss due to series resistance and 5-6% loss due to J_{02} . This indicates that passivation loss, rather than an increase in resistance, is the main contributor to efficiency loss.

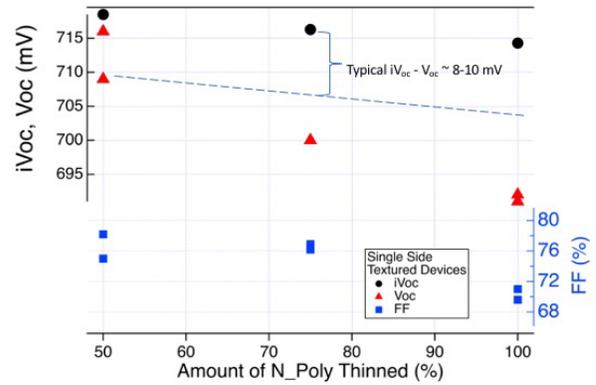


Fig. 4. iV_{oc} , V_{oc} and FF vs percent of poly-Si removed by RIE. Typical $iV_{oc} - V_{oc}$ values are 8-10 mV after metallization, but RIE etched samples showed a larger drop.

Despite these negative trends, the V_{oc} and FF values for the 50% sample (~ 20 nm of poly-Si left on the sample) are actually quite acceptable and may indicate a window where this technique could be used on much thicker poly-Si layers to allow passivated contacts under the metal while providing a significant boost to J_{sc} without affecting V_{oc} or FF.

Work is ongoing to passivate the etched surface with Al_2O_3 and/or SiN_x to decrease the V_{oc} and FF losses.

IV. CONCLUSION

We explored the use of reactive ion etching to thin the front doped n-type poly-Si layer between Al contact fingers in order to form self-aligned, selective-area passivated contacts on a front/back rear junction device. Our results show that Al contacts are preserved in an SF_6 plasma environment and that passivation is mostly preserved after low-power RIE etching plus a FGA. However, passivation is lowered during the deposition process of the back metal contact possibly due to a lack of protection by thicker n-type poly-Si at the SiO_2/c -Si interface. Devices showed slightly higher $iV_{oc} - V_{oc}$ loss with increased etching time, but with corresponding increase in J_{sc} , as expected. Work is ongoing to protect the etched surface to improve passivation and device efficiency.

REFERENCES

- [1] M. Rienacker, A Merkle, U. Romer, H. Kohlenberg, J. Krugener, R. Brendel, R. Peibst, "Recombination Behavior of photolithographic-free back junction back contact solar cells with carrier-selective polysilicon junctions for both polarities" Energy Procedia 92 412-418, 2016
- [2] D. L. Young, W. Nemeth, V. LaSalvia, M. R. Page, S. Theingi, J. Aguiar, B. G. Lee and P. Stradins "Low-Cost Plasma Immersion Ion Implantation Doping for Interdigitated Back Passivated Contact (IBPC) Solar Cells," Solar Energy Materials & Solar Cells, 158, 68, 2016.
- [3] A. Liu, D. Yan, S. P. Phang, A. Cuevas and D. Macdonald "Effective impurity gettering by phosphorus- and boron- diffused

- polysilicon passivating contacts for silicon solar cells," *Solar Energy Materials & Solar Cells*, 179, 136, 2018.
- [4] F. Haase, C. Hollemann, S. Schäfer, A. Merkle, M. Rienäcker, J. Krügener, R. Brendel and R. Peibst "Laser contact openings for local poly-Si-metal contacts enabling 26.1%-efficient POLO-IBC solar cells," *Solar Energy Materials and Solar Cells*, 186, 184, 2018.
- [5] Y. L. R. Peibst, S. Reiter, N. Orlowski, S. Schäfer, M. Turcu, B. Min, R. Brendel, D. Tetzlaff, J. Krügener, T. Wietler, U. Höhne, J.-D. Kähler, H. Mehlich, S. Frigge "Industrial, Screen-Printed Double-Side Contacted Polo Cells," in 35th EU-PVSEC, 2017, .
- [6] C. R. Frank Feldmann, Ralph Müller, Martin Hermle "The application of poly-Si/SiO_x contacts as passivated top/rear contacts in Si solar cells," *Solar Energy Materials & Solar Cells*, 159, 265-271, 2017.
- [7] N. K. Sina Reitera, Rolf Reineke-Kocha, Yevgeniya Larionovaa, Mircea Turcu,, D. T. Jan Krügenerb, Tobias Wietlerb, Uwe Höhnec, Jan-Dirk Kählerc, and d. Rolf Brendela, Robby Peibst "Parasitic absorption in polycrystalline Si-layers for carrier-selective front junctions," *Energy Procedia*, 92, 199, 2016.
- [8] M. Nicolai, M. Zanucoli, F. Feldmann, M. Hermle and C. Fiegna "Analysis of silicon solar cells with poly-Si/SiO_x carrier-selective base and Emitter contacts," *IEEE Journal of Photovoltaics*, 8, 1, 103, 2018.
- [9] A. Ingenito, G. Limodio, P. Procel, G. Yang, H. Dijkslag, O. Isabella and M. Zeman "Silicon solar cell architecture with front selective and rear full Area ion-implanted passivating contacts," *RRL Solar*, 1, 2017.
- [10] G. N. Andrea Ingenito , Josua Stuckelberger , Philippe Wyss, Luca Gnocchi, Christophe Allebé, and M. D. Jörg Horzel, Franz-Josef Haug, Philipp L'oper, and Christophe Ballif "Phosphorous-Doped Silicon Carbide as Front-Side Full-Area Passivating Contact for Double-Side Contacted c-Si Solar Cells," *Journal of Photovoltaics*, 2018.
- [11] J. Stuckelberger, G. Nogay, P. Wyss, Q. Jeangros, C. Allebé, F. Debrot, X. Niquille, M. Ledinsky, A. Fejfar, M. Despeisse, F.-J. Haug, P. Löper and C. Ballif "Passivating electron contact based on highly crystalline nanostructured silicon oxide layers for silicon solar cells," *Solar Energy Materials & Solar Cells*, 158, 2, 2016.
- [12] David L. Young, Bill Nemeth, San Theingi, Abhijit Kale, Dawn Findley, and M. P. Jake Atkins, Pauls Stradins "Front/back poly-Si/SiO₂ passivated contact device with Voc >720 mV" in 35th European Photovoltaic Solar Energy Conference and Exhibition, 2018, 700 -703.