



Electrothermal Modeling and Analysis of Gallium Oxide Power Switching Devices

Preprint

Ramchandra M. Kotecha,¹ Andriy Zakutayev,¹ Wyatt K. Metzger,¹ Paul Paret,¹ Gilberto Moreno,¹ Bidzina Kekelia,¹ Kevin Bennion,¹ Barry Mather,¹ Sreekant Narumanchi,¹ Samuel Kim,² and Samuel Graham²

*1 National Renewable Energy Laboratory
2 Georgia Institute of Technology*

*Presented at ASME 2019 International Technical Conference and Exhibition
on Packaging and Integration of Electronic and Photonic Microsystems
(IPACK2019)
Anaheim, California
October 7–9, 2019*

**NREL is a national laboratory of the U.S. Department of Energy
Office of Energy Efficiency & Renewable Energy
Operated by the Alliance for Sustainable Energy, LLC**

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications.

Contract No. DE-AC36-08GO28308

Conference Paper
NREL/CP-5400-73791
December 2019



Electrothermal Modeling and Analysis of Gallium Oxide Power Switching Devices

Preprint

Ramchandra M. Kotecha,¹ Andriy Zakutayev,¹ Wyatt K. Metzger,¹ Paul Paret,¹ Gilberto Moreno,¹ Bidzina Kekelia,¹ Kevin Bennion,¹ Barry Mather,¹ Sreekant Narumanchi,¹ Samuel Kim,² and Samuel Graham²

1 National Renewable Energy Laboratory

2 Georgia Institute of Technology

Suggested Citation

Kotecha, Ramchandra M., Andriy Zakutayev, Wyatt K. Metzger, Paul Paret, Gilberto Moreno, Bidzina Kekelia, Kevin Bennion, Barry Mather, Sreekant Narumanchi, Samuel Kim, and Samuel Graham. 2019. *Electrothermal Modeling and Analysis of Gallium Oxide Power Switching: Preprint*. Golden, CO: National Renewable Energy Laboratory. NREL/CP-5400-73791. <https://www.nrel.gov/docs/fy20osti/73791.pdf>.

**NREL is a national laboratory of the U.S. Department of Energy
Office of Energy Efficiency & Renewable Energy
Operated by the Alliance for Sustainable Energy, LLC**

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications.

Contract No. DE-AC36-08GO28308

Conference Paper
NREL/CP-5400-73791
December 2019

National Renewable Energy Laboratory
15013 Denver West Parkway
Golden, CO 80401
303-275-3000 • www.nrel.gov

NOTICE

This work was authored in part by the National Renewable Energy Laboratory, operated by Alliance for Sustainable Energy, LLC, for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. Funding was provided by the Laboratory Directed Research and Development (LDRD) Program at NREL. The views expressed herein do not necessarily represent the views of the DOE or the U.S. Government. The U.S. Government retains and the publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes.

This report is available at no cost from the National Renewable Energy Laboratory (NREL) at www.nrel.gov/publications.

U.S. Department of Energy (DOE) reports produced after 1991 and a growing number of pre-1991 documents are available free via www.OSTI.gov.

Cover Photos by Dennis Schroeder: (clockwise, left to right) NREL 51934, NREL 45897, NREL 42160, NREL 45891, NREL 48097, NREL 46526.

NREL prints on paper that contains recycled content.

ELECTROTHERMAL MODELING AND ANALYSIS OF GALLIUM OXIDE POWER SWITCHING DEVICES

Ramchandra M. Kotecha, Andriy Zakutayev,
Wyatt K. Metzger, Paul Paret, Gilberto Moreno,
Bidzina Kekelia, Kevin Bennion, Barry Mather,
Sreekant Narumanchi,
National Renewable Energy Laboratory
Golden, CO

Samuel Kim, Samuel Graham
Georgia Institute of Technology
Atlanta, Georgia

ABSTRACT

Gallium oxide is an emerging wide band-gap material that has the potential to penetrate the power electronics market in the near future. In this paper, a finite-element gallium oxide semiconductor model is presented that can predict the electrical and thermal characteristics of the device. The finite element model of the two-dimensional device architecture is developed inside the Sentaurus environment. A vertical FinFET device architecture is employed to assess the device's behavior and its static and dynamic characteristics. Enhancement-mode device operation is realized with this type of device architecture without the need for any selective area doping. The dynamic thermal behavior of the device is characterized through its short-circuit behavior. Based on the device static and dynamic behavior, it is envisioned that reliable vertical transistors can be fabricated for the power electronics applications.

Keywords: Wide Band-Gap Devices, Gallium Oxide Devices, Power Semiconductor Devices, Power Electronics, High-Voltage Devices, Ultra, Wide Band-Gap

NOMENCLATURE

ac	alternating current
Al ₂ O ₃	aluminum oxide
C-V	capacitance vs. voltage
dc	direct current
FinFET	fin-shaped field effect transistor
Ga ₂ O ₃	gallium oxide
GaN	gallium nitride
MOSFET	metal-oxide field effect transistor
N _d	donor concentration
Si	silicon
SiC	silicon carbide
SiO ₂	silicon dioxide
TCAD	technology computer-aided design

1. INTRODUCTION

Wide band-gap devices such as SiC and GaN have started to penetrate in power electronics systems and have demonstrated

strong performance benefits compared to Si-based power semiconductor devices. SiC devices have demonstrated significant performance benefits in high blocking voltage metal-oxide field effect transistors (MOSFETs) with high current conduction and better thermal conductivity compared to Si devices while GaN devices have demonstrated extremely high-current conduction in a small footprint with high-frequency operation up to 10 MHz [1]–[3]. While SiC and GaN devices have disrupted the semiconductor industry with significant gains in performance benefits, many technical challenges remain to be solved with respect to their wide-spread adoption in existing Si-based power electronics systems. The cost and the quality of wafer is still a major challenge for SiC devices [4]. Besides the cost, the reliability of the oxide layer and the low threshold voltage are major challenges for SiC devices with respect to device fabrication. Due to its small footprint, the dynamic electrothermal capability of the SiC device has also posed a challenge for high-power applications wherein the junction temperature can rise to significant levels that can damage the device module or package [1]. On the other hand, GaN devices have the potential for much cheaper costs compared to SiC devices. This is mainly because many device manufacturers have successfully demonstrated and supplied lateral GaN devices grown on Si wafers [5]. However, device and package reliability challenges remain to be fully addressed for GaN devices as well. The first main challenge is the difficulty in achieving selective area doping required for vertical GaN devices with higher blocking voltages. Due to its high-electron mobility combined with a wide band-gap of 3.4 eV, GaN power transistors could see significant amounts of electromagnetic interferences when used in fast switching circuits. Also, with a small footprint size, dynamic electro-thermal stability is also a concern for GaN, which also poses major packaging-related changes [2].

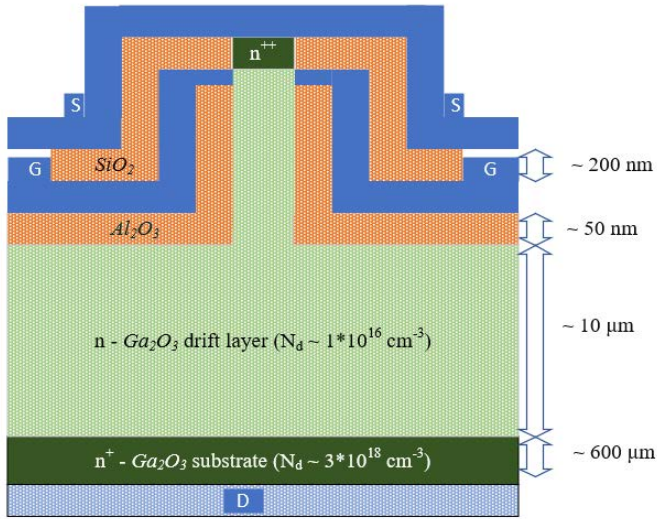


FIGURE 1: Ga₂O₃ VERTICAL FinFET DEVICE STRUCTURE

With all the challenges in existing wide band-gap technologies, a lot of motivation has emerged to explore other wide band-gap materials beyond SiC and GaN. Gallium oxide (Ga₂O₃) is one such material that has theoretical physical properties that make it a potential choice for power electronics applications. Ga₂O₃ has an ultrawide band-gap of 4.8 eV as well and has a very low intrinsic carrier concentration in the range of $1.79 \cdot 10^{-23} \text{ cm}^{-3}$. Also, it has a very high breakdown field in the range of 8 MV/cm. With such superior material properties, the theoretical Baliga Figure of Merit is estimated to be close to 3,444, which is about 10 times higher than SiC and 5 times higher than GaN [6]–[9]. The biggest challenge with respect to the Ga₂O₃ material is its low thermal conductivity compared to SiC and GaN, which poses a significant challenge for its adoption in power electronics applications. Despite the challenge posed by its low thermal conductivity, Ga₂O₃ material has attained wide-spread attention due to the possibility of mitigating the effect of low thermal conductivity by modifications in the semiconductor process and through innovative package designs.

Regardless of the advantages and the challenges offered by this new material, it is essential to develop the models for various levels of complexities depending on the intended consequences of its applications. In this paper, a technology computer-aided design (TCAD) model is presented for a Ga₂O₃ vertical transistor to assess the feasibility and performance of this device for power electronics applications and designs. This kind of model also aids in the fabrication process that can result in significant savings in terms of cost and time [10]. Section 2 describes the modeling methodology employed to develop the TCAD model while section 3 describes the results from the electrical and thermal analyses of the TCAD model. Finally, conclusions derived from the model are summarized in section 4.

2. Modeling Methodology

To explore the device behavior, a vertical fin-shaped field effect transistor (FinFET) device architecture is used for model

development. The model is developed inside the Sentaurus TCAD environment. The physics-based device architecture is first constructed using the SDE tool within the Sentaurus environment as shown in Figure 1 [11]. The doping profiles and meshing are defined appropriately for the vertical 2-dimensional transistor architecture. Once the model is built inside the Sentaurus environment, the device characteristics are extracted using the SDevice tool within the environment. In order to characterize the device behavior, drift-diffusion model for carrier transport is implemented. The temperature and field-dependent carrier mobility model is implemented. To characterize the device's self-heating effects, the thermodynamic model is activated in the Sentaurus environment. After the entire model is built in the Sentaurus environment, various modes of dc, C-V, ac, and transient analyses are performed to analyze the device's behavior and extract the device's characteristics of interest.

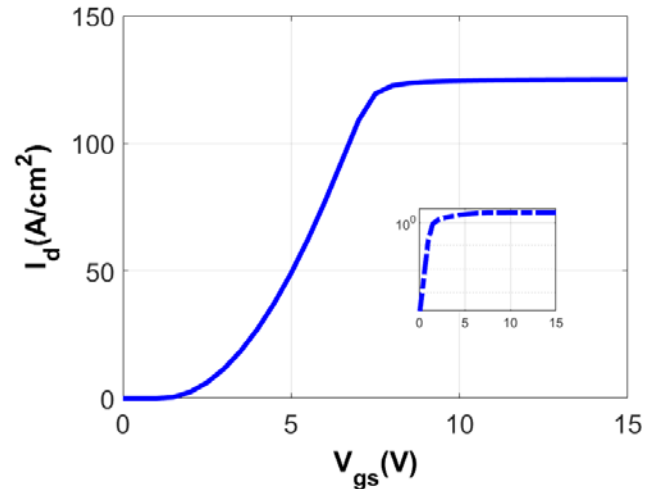


FIGURE 2: Device transfer characteristics with drain current density (I_d) as a function of gate-source voltage (V_{gs})

2.1 Vertical FinFET Device Behavior

The vertical FinFET device architecture was recently demonstrated for both GaN and Ga₂O₃ devices [11]. Selective

area doping has been found to be challenging for emerging wide band-gap materials; thus, alternative device structures to vertical, planar MOSFETs are explored [11]–[13]. In the vertical FinFET device structure shown in Figure 1, no p-type doping is required when the FinFET architecture is fabricated from an n-type substrate. An n-drift layer is grown on top of the substrate. Depending on the type of process, interfacial layers are also grown before the drift layer is grown on the substrate. The thickness and the doping concentration of the drift region are determined based on the desired breakdown voltage and the on-resistance of the device. For model development, a 10- μm -thick drift region is designed with a donor concentration of $1 \cdot 10^{16} \text{ cm}^{-3}$. The double-sided gate is insulated from the channel region by a 50-nm Al₂O₃ dielectric. The width of the fin and the doping concentration of the channel region are important device parameters in the design of the threshold voltage and the current

gain. The work function difference between the gate metal and the n-type channel region results in the total depletion in the fin region. Thus, an enhancement-mode vertical transistor can be realized using FinFET architecture [11].

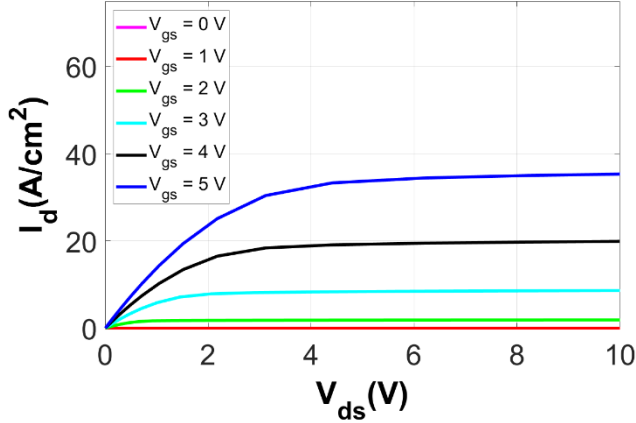


FIGURE 3: Device output characteristics with drain current density (I_d) as a function of drain-source voltage (V_{ds})

3. MODELING RESULTS AND DISCUSSION

Based on the qualitative description of the device behavior in the previous section, the modeling results from the TCAD analyses are found to be on the expected lines. First, the dc transfer characteristics are extracted to determine the appropriate device threshold for desired normally-off concentration.

The dc transfer characteristics for the vertical FinFET structure are shown in Figure 1. From the figure, it can be observed that the threshold voltage of the device is close to 1.5 V, which is an acceptable range of voltage for power electronics applications. Another planar vertical device reported in [13] demonstrates a threshold voltage close to -50 V. A recently reported vertical planar device with nitrogen (N^-) as the p-type dopant instead of magnesium (Mg^{++}) has a threshold voltage close to -55 V.

Most Si-based power semiconductor devices have a positive threshold voltage in excess of 5 V. Emerging wide band-gap devices such as SiC have threshold voltages in excess of 2 V, and emerging GaN devices have threshold voltages in excess of 1.3 V. Thus, almost all the power electronics applications are based on enhancement-mode devices with positive threshold voltages. Therefore, deep depletion-mode devices such as the ones presented for vertical planar architectures are not acceptable for present day power electronics applications. The vertical FinFET device structure provides a pathway to maximizing the benefits offered by the Ga_2O_3 material.

The key reliability concerns related to the Ga_2O_3 devices such as the dynamic thermal stability must be addressed for any device architecture employed for fabrication.

The dc output characteristics and the device self-heating characteristics are presented in Figures 3 and 4.

It can be observed from the dc characteristics that there is a significant reduction in the channel current due to the increase in

the device on-resistance with the rise in the junction temperature. As the channel current is conducted from drain to source, there is an increase in junction temperature due to lattice-heating. This effect is characterized in the model by activating the thermodynamic model in the Sentaurus environment.

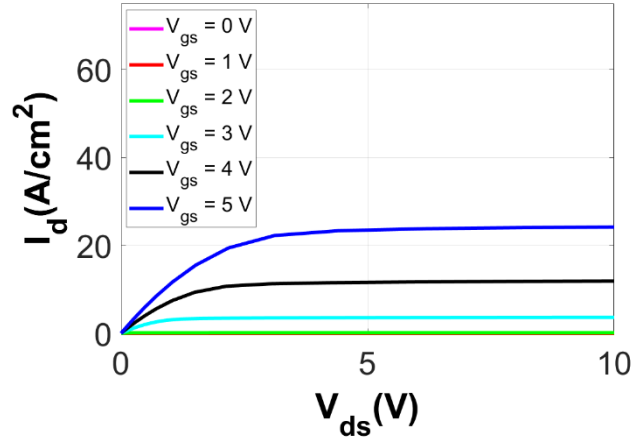


FIGURE 4: Device transfer characteristics with drain current density (I_d) as a function of gate-source voltage (V_{gs})

Due to the low thermal conductivity of the Ga_2O_3 material, the assessment of dynamic thermal stability is very important. In active power electronics systems, it is expected that semiconductor devices will be subjected to transient faults under various operating conditions. One of the most severe transient conditions is the short circuit in a switching device. During this condition, the device undergoes severe electrical and thermal stress due to a sudden rise in the device current. The junction temperature can reach unreasonable levels and has the potential to permanently damage the device and the packaging surrounding the device.

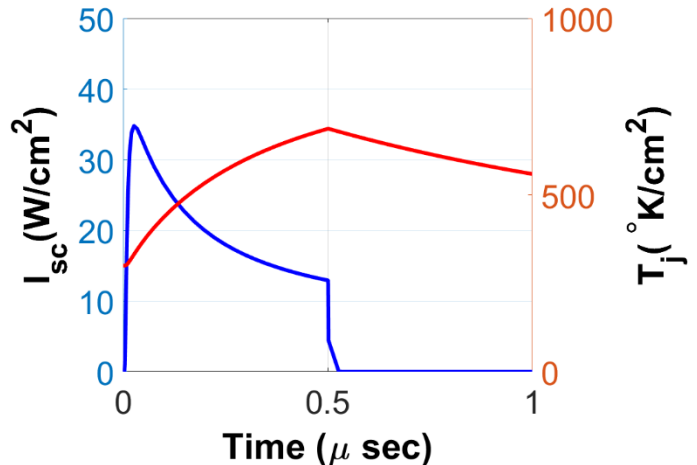


FIGURE 5: Device short-circuit current and the junction temperature under short-circuit current.

Figure 5 shows the device short-circuit current and the resulting junction temperature with an applied reverse voltage of 800 V when the device is subjected to a short circuit transient.

It can be observed that the self-heating in the device is significant as observed from the tailing current after device turn-off and the steep rise in junction temperature up to 685 K. Such a steep rise in temperature is expected due to the low thermal conductivity of Ga₂O₃. Although the heat absorption capacity of Ga₂O₃ is higher compared to SiC and GaN, the packaging around these devices may not be able to sustain such a steep rise in the junction temperature during transient faults. The most susceptible components of packaging during high-temperature events are bond wires, interface materials, and solder joints. It is important to conduct simultaneous research in packaging along with the device research to achieve an immediate target of 250°C in the operation of power electronics.

Although the results from finite-element modeling presented in this paper are related to vertical FinFET device architecture, it is important to explore various device architectures as well as diode structures to assess the viability of the Ga₂O₃ material for power electronics systems.

4. CONCLUSION

A physics-based model for the vertical FinFET Ga₂O₃ device is presented in this paper. The two-dimensional device model is developed in the Sentaurus TCAD environment. Based on the device's *I-V* characteristics, it can be observed that enhancement-mode device operation can be achieved through proper design of the fins and the channel doping concentration. In order to achieve desired enhancement-mode operation, the current gain of the transistor is compromised to some extent, which is a major design trade-off. It is possible to achieve lower on-resistance with this material due to its wide band-gap. The short-circuit performance of the device must be addressed in conjunction with the package design as the junction temperature can rise to significant levels depending on the time-domain performance of the device.

ACKNOWLEDGEMENTS

This work was authored by the National Renewable Energy Laboratory (NREL), operated by Alliance for Sustainable Energy, LLC, for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. Funding was provided by the Laboratory Directed Research and Development (LDRD) Program at NREL. The views expressed in the article do not necessarily represent the views of the DOE or the U.S. Government. The U.S. Government retains and the publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes. The author would like to acknowledge the help and support provided by Nelson Braga at Synopsys Inc. in several aspects of the model development.

REFERENCES

[1] Baliga, B. Jayant. *Fundamentals of Power Semiconductor Devices*. Springer International Publishing, Switzerland (2010). DOI: 10.1007/978-3-319-93988-9.

- [2] Baliga, B. Jayant. "Gallium Nitride Devices for Power Electronic Applications." *Semicond. Science and Technology*, VOL. 28, No. 7, (2013): pp. 074011.
- [3] *Gallium Oxide: Technology, Devices*. Elsevier, 2019.
- [4] Reese, S. B., Remo, T., Green, J., and Zakutayev, A. "How Much Will Gallium Oxide Power Electronics Cost?" *Joule* (2019). DOI: 10.1016/j.joule.2019.01.011
- [5] Kotecha, R. M., Zhang, Y., Rashid, A., Vrotsos, T., and Mantooth, H. A. "A Physics-Based Compact Device Model for GaN HEMT Power Devices." in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. pp. 108–113. Fayetteville, AR, Nov. 7-9, 2016. <https://doi.org/10.1109/WiPDA.2016.7799919>
- [6] Pearton, S. J., Jiancheng, Y., Cary, H. P., Ren, F., Kim, J., Tadjer, M. J., and Mastro, A. M. "A Review of Ga₂O₃ Materials, Processing, and Devices." *Applied Physics Reviews* VOL. 5, No. 1 (2018): pp. 011301.
- [7] Kumar, A., Pratiyush, A. S., Muralidharan, R., and Nath, D. N. "A Performance Comparison Between β -Ga₂O₃ and GaN High Electron Mobility Transistors." (2018) arXiv preprint arXiv:1802.02313.
- [8] Higashiwaki, M., Kuramata, A., Murakami, H., and Kumagai, Y. "State-of-the-Art Technologies of Gallium Oxide Power Devices." *Applied Physics* (2017): pp. 13.
- [9] Kotecha, R. M., W.K. Metzger, W.K., Mather, B. A., Narumanchi, S., and Zakutayev, A. "Modeling and Analysis of Gallium Oxide Vertical Transistors." *ECS Journal of Solid-State Science and Technology* VOL. 8, No. 7 (*JSS Focus Issue on Gallium Oxide Based Materials and Devices*) (2019).
- [10] Synopsys. "Sentaurus Device Simulator Guide." Version J–2014.09. (2014).
- [11] Hu, Z., Nomoto, K., Li, W., Tanen, N., Sasaki, K., Kuramata, A., Nakamura, T., Jena, D., and Xing, H. G., "Enhancement-Mode Ga₂O₃ Vertical Transistors with Breakdown Voltage > 1 kV." *IEEE Electron Device Letters* VOL. 39, No. 6 (2018): pp. 869–872.
- [12] Higashiwaki, M., Sasaki, K., Kuramata, A., Masui, T., and Yamakoshi, S. "Gallium Oxide (Ga₂O₃) Metal-Semiconductor Field-Effect Transistors on Single-Crystal β -Ga₂O₃ (010) Substrates." *Applied Physics Letters* VOL. 100, No. 1 (2012): pp. 013504.
- [13] Wong, M. H., Goto, K., Murakami, H., Kumagami, Y., and Higashiwaki, M. "First Demonstration of Vertical Ga₂O₃ MOSFET: Planar Structure with a Current Aperture." *2017 75th Annual Device Research Conference (DRC)*. pp. 1–2. South Bend, IN, date 25-28 June 2017.