Decentralized Carrier Interleaving in Cascaded Multilevel DC-AC Converters

Preprint

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Decentralized Carrier Interleaving in Cascaded Multilevel DC-AC Converters

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Abstract—Cascaded dc-ac converters with interleaved carriers are commonly used in applications where elevated voltages and low-distortion multilevel waveforms are needed. Example applications include modular multilevel converters and solid-state transformers. In such systems, carrier interleaving is generally achieved via communication among the stacked converters or a centralized controller. Due to the large number of converters in such a system, existing approaches entail significant wiring complexity and communication may limit resilience to failures. In this paper, we introduce a control strategy which achieves communication-free carrier interleaving among series-connected converters. The proposed controller is embedded within each converter control loop and only requires measurements available at each set of converter terminals. We formulate a dynamical system model and show that the system converges to the interleaved condition irrespective of the number of converters in the stack. After outlining a practical method for digital implementation, experiments are shown on a hardware-in-the-loop setup.

Index Terms—Switch interleaving, cascaded H-bridges, phase-shifted PWM.

I. INTRODUCTION

Carrier interleaving is used to obtain multilevel waveforms in cascaded converter architectures such as modular multilevel converters (MMCs), solid-state transformers (SSTs), and numerous other topologies which contain cascaded H-bridges [1]–[4]. This approach is advantageous since it yields high-quality waveforms and relaxed filtering requirements, as well as reduced common-mode noise [5]. As applications evolve to higher voltage levels and topologies become increasingly complex, the number of cascaded converters can become large. In such settings, it is desirable to obtain communication-free implementations where multi-converter systems can be assembled in a modular plug-and-play fashion with minimal wiring between units. Towards that end, we propose a control method that enables decentralized PWM carrier interleaving in cascaded H-bridge systems. After deriving a small-signal

model which shows how the cascaded converters interact, we show that the proposed controllers converge to the interleaved state irrespective of how many converters are in the system. The paper concludes with a hardware-in-the-loop validation on DSP hardware.

As illustrated in Fig. 1, symmetric carrier interleaving can be implemented via centralized, distributed, or decentralized means. In the centralized setup, one platform executes closed-loop control and manages carrier timing for interleaving. Although this approach is most straightforward and has been extensively used for voltage and current balancing in MMCs [1]–[3], it entails practical challenges associated with wiring, common-mode noise on sensed signals, and isolation requirements between the controller and N converters. Setups with longer distances between converters are particularly challenging due to the long cable runs from each converter to the centralized controller. A centralized controller also acts as a single point of failure.

To enhance modularity, another approach is to install a controller at each converter while PWM timing among converters is managed on a single communication bus [6] or in a chain of neighbor-to-neighbor signal exchanges [7]. Although

Fig. 1. A comparison of various control architectures for cascaded systems.

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these methods enhance resiliency, the communication bus is still vulnerable to common-mode noise, packet drops, and communication faults as discussed in [8], [9]. To address this, the work in [8] proposes a supervisory communication unit that functions to synchronize all the PWM carriers. Decentralized interleaving controllers do exist for parallel-connected setups [10], [11] but is unclear if such methods are applicable for cascaded architectures. To date, the only known decentralized method for cascaded systems is reported in [12]. However, this approach requires significant computational resources to oversample the current, precisely detect zero crossings, and take control action.

In this paper, we propose a new controller that fills these gaps for cascaded systems. In particular, the control design does not require foreknowledge of the number of converters and it takes the form of a simple first-order control law suitable for digital implementation. Furthermore, the implementation is computationally efficient with only one sample-and-hold operation per switch cycle. The paper is structured as follows: In Section II, we describe the system structure and associated notation. A dynamical model and control design procedure are given in Section III. We provide simulation and hardware-in-the-loop (HIL) experimental results in Section IV and conclude the paper in Section V.

II. SYSTEM DESCRIPTION AND NOTATION

The system under consideration in Fig. 2(a) is composed of N series-connected H-bridge inverters which collectively deliver common current, $i + i_\omega$, into the grid voltage, v_g , via an output inductance L . The fundamental component (e.g., at 50 or 60 Hz) of this current is denoted as i_ω and i denotes the remaining high frequency ripple. As illustrated in Fig. 2(a), each controller has a high-pass filter (HPF) to extract the ripple signal which is processed by the controller. Furthermore, we assume that there is a sufficiently large gap between the HPF cutoff frequency and the high switching frequency such that the HPF's dynamics can be neglected.

Each instance of the proposed controller contains an autonomously triggered sample-and-hold operation where i_k^s denotes the sampled value of i at the k -th converter. Each sampled ripple component is processed by the proposed *carrier phase shift controller* whose logical output is denoted as $q_k \in \{0, 1\}$. Here, q_k denotes the state of the top-switch in the k -th H-bridge positive terminal leg where 0 and 1 denote an open and closed switch, respectively. The complement of q_k is $\bar{q}_k := 1 - q_k$, and the nominal switching frequency is ω_{sw}^* .

Our proposed controller is designed such that the falling edge of q_k triggers a measurement of i to obtain i_k^s at the k -th converter. As shown in Fig. 2(b), this implies that i_k^s coincides with the *local current peak* associated with the k -th converter switch transition. Consider the scenarios in Fig. 2(b) with arbitrary, interleaved, and synchronized sampling. As depicted, i_k^s and i_j^s for $j \neq k$ may be unequal over a given switch cycle for arbitrary phase shifts. However, the scenarios with interleaved and synchronized carriers both give $i_k^s = i_j^s, \forall j, k$ with the key

Fig. 2. N cascaded H-bridge inverters with the proposed control are shown in (a). The ripple current and its sampled values are shown in (b) for various carrier configurations.

difference that ripple is minimized in first case and maximized in the latter. Evidently, the sampled magnitudes are a key indicator of whether the N carriers are interleaved. We will leverage this property to engineer decentralized controllers that collectively converge to the interleaved operating point. The challenge is that each local controller must achieve this without global timing information.

The controller is depicted in Fig. 2(a) where the k -th sampled current is processed by a time-varying proportional gain $K(t)$. In Section III, we will show how $K(t)$ is computed to guarantee interleaving. This controller yields a small adjustment, $\tilde{\omega}_k$, on the k -th converter switching frequency that is subsequently added to the nominal value, ω_{sw}^* . Finally, we integrate the actual switching frequency, ω_k and obtain the angle $\phi_k \in [0, 2\pi)$ which is scaled by $1/(2\pi)$ to produce a saw-tooth carrier that swings between ± 1 .

Note that the proposed controller can flexibly co-exist with any generic ac-side controller that produces a modulation signal $-1 < m < 1$. Hence, m is regarded as an exogenous input

Fig. 3. The original cascaded structure is in (a) whereas its decomposed counterpart in (b) is obtained via superposition. Waveforms in (c) relate the waveforms in the original and decomposed models.

signal in our model. The unipolar PWM implementation and switch-level logic are illustrated in Fig. 2(a). For convenience, we define $d := |m|$ which captures the effective duty ratio seen across the H-bridge ac terminals. Furthermore, m and by extension d are assumed identical among all converters.

III. SYSTEM MODELING AND CONTROL DESIGN

To uncover how local control actions give rise to networked interactions, decompose the original system in Fig. 3(a) into the N circuits in Fig. 3(b). Referring to Fig. 3(b), denote the current that would flow if the k -th converter existed alone as i_k . Application of the superposition principle (see Fig. 3(c)) allows us to recover variables in the original system given the states of the decomposed system.

As shown in Fig. 4(a), the k -th current component has a phase shift, ϕ_k , with respect to a global angular reference which evolves with angle $\theta = \omega_{sw}^* t$. By extension, the nominal switching frequency defines a system-wide reference frame for analysis. The peak ripple magnitude is denoted i_{pk} and the phase angle, ϕ_k , coincides with both the local ripple minimum and saw-tooth carrier edge. The k -th current waveform rises and falls with slope h_+ and h_- , respectively. Furthermore, the k -th logic switch function, q_k , can be defined in terms of the local carrier angle.

$$q_k = \begin{cases} 1, & \text{for } 0 \leq \theta - \phi_k < 2\pi d, \\ 0 & \text{for } 2\pi d \leq \theta - \phi_k < 2\pi \end{cases} \quad (1)$$

Given these definitions, i_k is the piecewise linear function

$$i_k(\theta, \phi_k) = q_k(-i_{pk} + h_+(\theta - \phi_k)) + \bar{q}_k(i_{pk} - h_-(\theta - \phi_k - 2\pi d)). \quad (2)$$

Applying superposition, it is evident the current in the actual stacked system is $i = \sum_{k=1}^N i_k(\theta, \phi_k)$ (see Fig. 3(c)).

A. Closed-loop system model

To facilitate analysis, we isolate *self-coupling* and *mutual-coupling* dynamics between the controllers where the locally sampled peak has the following small-signal representation:

$$i_k^s(t) = \hat{i}_k^s + \tilde{i}_k^s(t), \quad (3)$$

Fig. 4. (a) Nomenclature for decomposed current waveform of k -th converter. (b) System dynamical model.

where $\hat{i}_k^s$ would be the locally sampled peak under periodic steady-state conditions (i.e., static $\tilde{\omega}_k$), and $\tilde{i}_k^s(t)$ encapsulates the impacts due to all N controllers taking action. To parse out the self and mutually-coupled contributions on $\tilde{i}_k^s(t)$, we obtain

$$\tilde{i}_k^s(t) = \tilde{i}_{k,k}^s(t) + \sum_{j \neq k}^N \tilde{i}_{k,j}^s(t), \quad (4)$$

where the first term captures the change in the sampled peak current at the k -th converter due to the k -th controller taking action (i.e., self-coupling), and the second term accounts for the $(N - 1)$ remaining converters and the impacts of their control actions on the k -th measurement (i.e., mutual coupling). Figure 4(b) illustrates the networked interactions within the small-signal model.

From Fig. 4(b), we see that control action manifests itself as a small signal adjustment in the switching frequency, $\tilde{\omega}_k$, at the k -th converter. This change induces a corresponding phase shift $\tilde{\phi}_k$ in the position of the locally sampled current peak $\tilde{i}_k^s$. To isolate the self-coupling contribution (i.e., impact of k -th controller taking action on i_k^s), multiply the slopes of the $N - 1$ other current components, i_j , $\forall j \in \{1, \dots, N\}, j \neq k$, by the phase shift of the k -th converter, ϕ_k , and summing up contributions to obtain

$$\tilde{i}_{k,k}^s = \sum_{j \neq k}^N (q_{k,j} h_+ - \bar{q}_{k,j} h_-) \tilde{\phi}_k, \quad (5)$$

$$= \sum_{j \neq k}^N (q_{k,j} - d) h \tilde{\phi}_k, \quad (6)$$

$$= - \sum_{j \neq k}^N (q_{k,j} - d) h \int \tilde{\omega}_k dt, \quad (7)$$

where $q_{k,j}$ is used to compactly denote the whether the j -th converter and its decomposed current component has a positive

Fig. 5. Controller on/off action over an ac line cycle.

slope when the k -th converter takes a sample. In particular, $q_{k,j} = 1$ if $q_j = 1$ at the instant the k -th converter takes a sample and is zero otherwise. Denote the complement of $q_{k,j}$ as $\bar{q}_{k,j} = 1 - q_{k,j}$ and define $h := h_+ + h_- = v_{dc}/(\omega_{sw}^* L)$ where it is noted that the slopes sum to a constant. Finally, in (7) we replace $\tilde{\phi}_k$ with the time integral of $\tilde{\omega}_k$.

We now switch focus to the mutual coupling terms in (4). The change in $\tilde{i}_k^s$ due to the switching frequency adjustment of the j -th converter, $\tilde{\omega}_j$, is equivalent to the k -th converter producing an equal and opposite change, $-\tilde{\omega}_j$, in its own switching frequency. Using a sequence of manipulations along the lines of (5)–(7) eventually gives

$$\tilde{i}_{k,j}^s = -(q_{k,j} - d)h\tilde{\phi}_j = (q_{k,j} - d)h \int \tilde{\omega}_j dt. \quad (8)$$

Substitute (7) and (8) into (4) and simplify to obtain

$$\tilde{i}_k^s = - \sum_{j \neq k}^N (q_{k,j} - d)h \int (\tilde{\omega}_k - \tilde{\omega}_j) dt. \quad (9)$$

To reveal the closed-loop system dynamics, differentiate both sides and substitute the control law, $\tilde{\omega}_k = -K(t)\tilde{i}_k^s$, to get

$$\frac{di_k^s}{dt} = hK(t) \sum_{j \neq k}^N (q_{k,j} - d)(i_k^s - i_j^s), \quad (10)$$

where (10) defines the nonlinear multi-converter model for the system in Fig. 2.

Fig. 6. Two sets of simulation results are shown in (a) and (b) for systems with 5 and 12 cascaded H-bridges, respectively. Both systems are initialized with random carrier phase shifts and a fixed sinusoidal modulation signal, m , it utilized.

TABLE I
PARAMETERS FOR SIMULATIONS

Symbol	Description	Value	Units
V_{dc}	Dc-link voltage	200	V
ω_{sw}^*	Nominal switching frequency	$2\pi 5 \times 10^3$	rad/s
L	Filter inductance	2.5	mH
K_o	Controller gain magnitude	400	rad·A/s

B. Control design

Inspecting (10), the signs inside the right-hand-side summation depend on the effective duty and switch signals. Hence, the plant exhibits time-varying gains which are difficult to stabilize. However, after careful analysis it can be shown that $q_{k,j} - d$ in (10) is negative $\forall k$ when $d \in (0, \frac{1}{N}]$, and positive $\forall k$ when $d \in (\frac{N-1}{N}, 1]$. For those particular duty-ratio ranges, denoted as $d^\dagger := \{(0, \frac{1}{N}] \cup (\frac{N-1}{N}, 1]\}$, (10) boils down to

$$\frac{di_k^s}{dt} = hNK(t)d' \left(i_k^s - \frac{1}{N} \sum_{j=1}^N i_j^s \right), \text{ for } d \in d^\dagger, \quad (11)$$

where $(1/N) \sum_{j=1}^N i_j^s$ is the average of all sampled ripple amplitudes, $d' = -d < 0$ when $d \in (0, \frac{1}{N}]$, and $d' = 1-d > 0$ when $d \in (\frac{N-1}{N}, 1]$.

Since the plant gain polarity is well-defined and uniform for all converters when $d \in d^\dagger$, we can adjust the sign of $K(t)$ in real-time to ensure convergence of all sampled ripple amplitudes to the global average (i.e., $i_k^s \rightarrow (1/N) \sum_{j=1}^N i_j^s, \forall k$). Most importantly, this also implies convergence to the interleaved state. Given a constant $K_o > 0$, we achieve this by toggling $K(t)$ between $\pm K_o$ such that $K(t)d' < 0$ when $d \in d^\dagger$. For duty ratios $d \notin d^\dagger$ where the plant might not be stabilizable, K_o is set to zero and the switching frequencies all revert to the nominal value. Figure 5 illustrates how the time-varying control gain is toggled in real-time over a sinusoidal line cycle. Since d is locally available at each converter, this gives a fully decentralized implementation.

Fig. 7. Experimental setup where the proposed controller in Fig. 2(a) was implemented on a DSP. The HIL platform emulates a system of 3 cascaded H-bridges where one of the control loops is carried out on the TI F280049C DSP.

It can be inferred from (10) that the convergence rate to the interleaved state is proportional to the factor $hNK(t)$, where $h = v_{dc}/(\omega_{sw}^* L)$. Therefore, convergence time varies with $\omega_{sw}^* L/(v_{dc} K_o N)$ which is tuned by choosing an appropriate value of K_o given the physical parameters, N , and nominal switching frequency. A practical upper bound on K_o is dictated by the maximum allowable switching frequency deviation from the nominal value ω_{sw}^* .

IV. SIMULATION AND EXPERIMENTAL RESULTS

The proposed control scheme was simulated for a system of $N = 5$ and $N = 12$ H-bridge inverters for different modulation amplitudes, M , where $m(t) = M \cos(\omega t)$ and $\omega = 2\pi 60 \text{ rad/s}$. These two case studies are illustrated in Figs. 6(a)–(b), respectively, and both systems utilize the parameters in Table I. As shown, the 5 and 12 converter systems, which operate with modulation amplitudes $M = 0.3$ and $M = 0.8$, respectively, start with random carrier phase shifts and converge to the interleaved state as evidenced in their output voltage and current waveforms. Notice that the 5 converter system has a slower convergence speed due to the reduced number of converters. However, this could be negated by increasing the control gain, K_o , as appropriate.

Next, we validated the controller on digital control hardware with a PLECS brand HIL platform (see Fig. 7). The HIL

numerical plant model was executed with a time step of $3.5 \mu\text{s}$ and the controller was implemented on a Texas Instruments F280049C LaunchPad. A system of 3 cascaded H-bridges was assembled where one controller was implemented on a F280049C DSP and the remaining two controllers are contained within the emulated HIL subsystem. All three power stages and ac load are embedded within the HIL real-time model. Although the proposed control method works for an arbitrary number of cascaded converters and switching frequencies, we deliberately limited the experiment to 3 converters switching at 5 kHz due to limitations on the HIL time-step size. Referring to Fig. 8, we observe convergence to the interleaved state for worst-case initial conditions with synchronized carriers.

V. CONCLUSIONS AND FUTURE WORK

In this paper, we proposed a novel method to achieve communication-free carrier interleaving in series-connected converters. The proposed controller is embedded within each converter control loop and only requires local measurements available at the converter terminals. We derived a dynamical model of the multi-converter system and showed that it asymptotically converges to the interleaved state irrespective of the number of converters and initial conditions. Finally, the proposed approach was validated in simulation and HIL experiments. Future work includes analysis of heterogeneous systems with mismatched dc-links and modulation amplitudes among converters. A fully hardware-based validation is also needed.

REFERENCES

- [1] R. Darus, G. Konstantinou, J. Pou, S. Ceballos, and V. G. Agelidis, "Carrier interleaved PWM techniques in modular multilevel converters: A comparison based on same voltage level waveforms," in *IEEE Energy Conversion Congress and Exposition*, pp. 3725–3730, IEEE, 2014.
- [2] G. Konstantinou, G. J. Capella, J. Pou, and S. Ceballos, "Single-carrier phase-disposition PWM techniques for multiple interleaved voltage-source converter legs," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4466–4474, 2017.
- [3] W. van der Merwe, P. Hokayem, and L. Stepanova, "Analysis of the n -cell single phase MMC natural balancing mechanism," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, pp. 1149–1158, Dec. 2014.

Fig. 8. Real-time experimental results: (a) stack voltage and current at start-up for $N = 3$ converters, and (b) PWM switch signals for all the 3 units at startup and at the final interleaved state.

- [4] L. Bede, G. Gohil, T. Kerekes, and R. Teodorescu, "Optimal interleaving angle determination in multi paralleled converters considering the DC current ripple and grid current THD," in *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, pp. 1195–1202, IEEE, 2015.
- [5] J. W. Kimball and M. Zawodniok, "Reducing common-mode voltage in three-phase sine-triangle PWM with interleaved carriers," *IEEE Transactions on Power Electronics*, vol. 26, no. 8, pp. 2229–2236, 2010.
- [6] D. J. Perreault and J. G. Kassakian, "Distributed interleaving of paralleled power converters," *IEEE Transactions on Circuits and Systems I*, vol. 44, pp. 728–734, Aug. 1997.
- [7] M. Cousineau, M. Le Bolloch, N. Bouhalli, E. Sarraute, and T. Meynard, "Triangular carrier self-alignment using modular approach for interleaved converter control," in *European Conference on Power Electronics and Applications*, pp. 1–10, IEEE, 2011.
- [8] T. Xu and F. Gao, "Global synchronous pulse width modulation of distributed inverters," *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6237–6253, 2015.
- [9] T. Xu and F. Gao, "Self-synchronization operation of global synchronous pulsewidth modulation with communication fault tolerant and simplified calculation capabilities," in *Applied Power Electronics Conference and Exposition*, pp. 921–927, IEEE, 2016.
- [10] J. Poon, B. B. Johnson, S. V. Dhople, and S. R. Sanders, "Minimum distortion point tracking: Optimal phase shifting for input-or output-parallel connected DC-DC converters," in *Workshop on Control and Modeling for Power Electronics*, pp. 1–6, IEEE, 2018.
- [11] M. Sinha, J. Poon, B. B. Johnson, M. Rodriguez, and S. V. Dhople, "Decentralized interleaving of parallel-connected buck converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4993–5006, 2019.
- [12] L. Du and J. He, "A simple autonomous phase-shifting PWM approach for cascaded h-bridge converters," *IEEE Transactions on Power Electronics*, 2019.