Effect of Reactive Power on Photovoltaic Inverter Reliability and Lifetime

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NOTICE

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Abstract — **This paper performs research on predicting Photovoltaic (PV) inverters reliability and lifetime based on thermal cycling. Thermal cycling is considered the most important stressors in an inverter system. In order to achieve this, a detailed electrothermal model of the PV inverter will be developed along with their controllers capable of providing voltage support through reactive power. An in-house inverter was built, and a PV inverter model was developed to match the physical inverter. The PV inverter electrothermal model was validated for different ambient temperatures to match the in-house inverter hardware. The in-house inverter was placed inside a thermal chamber to emulate different ambient temperatures and their losses and temperature rises within the system were measured. After the validation of the model, a reduced order model of the inverter will be implemented to translate the mission profile of ambient temperature and solar irradiance into load profile of junction temperatures of the switches. The junction temperature data will be used to identify the reliability indices and hence predict the useful lifetime of the inverter system. Along with the model to predict useful lifetime of the system, the impact of reactive power on the overall reliability of the system will be studied. The key observation in this paper shows that lifetime of the inverter decreases as the operating power factor moves away from unity.**

Index Terms — **Inverter reliability, lifetime estimation, thermal model, loss model, rain flow counting.**

I. INTRODUCTION

Research on PV systems has multiple facets to it, however a lot of them focuses on the production costs, reliability of PV module technology. With the reduction in price of PV modules, the price of power electronics become more relevant, power electronics now constitute 8- 12% of the total lifetime PV cost [1]. As efforts to lower PV module costs yield diminishing returns, the importance of understanding and lowering inverter costs become increasingly critical.

One of the key price drivers of power electronics is reliability [2]. In a utility-scale PV installations, the mean time between failure of inverters has been shown to be 300 to 500 times shorter than modules [3]. In one 27-month study, module failures accounted for only 5% of total energy losses, while inverter failures accounted for 36% of lost energy over the same period [4][5]. In another study, inverter subsystem is found to have received the largest of service calls for operation and maintenance. These studies present the motivation for this study on prediction of lifetime of inverter system addressed in this paper. One way for assessing inverter lifetime is based on failure rates of individual components and handbooks provided by the manufacturers. In recent years, prediction of reliability and lifetime of power converters are done through physics of failure assessments. The physics of failure assessment is understood through the failure mechanisms of the components of power converters and external physical stressors like ambient temperature, solar irradiance, and relative humidity [6].

Several studies have addressed the reliability and lifetime estimation of inverters from thermal cycling perspective. But new grid codes have brought additional requirements to provide reactive power support. In the recently updated IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces, IEEE 1547-2018 [7], PV inverters are expected to support the grid by supplying or absorbing reactive power which leads to increase in the total apparent power of the inverter. This paper addresses the effects of reactive power on PV inverter reliability and lifetime.

In this paper, a mission-profile based approach will be used for predicting the lifetime and reliability of inverter. For this purpose, an in-house inverter was built with detailed knowledge on the parameters and values of the components used in the inverter. These parameters and values are used to develop a detailed electrothermal model which estimates the power losses and junction temperatures of the switches, explained in section II. The detailed model is extended to a reduced order model to estimate the junction temperature of switches from the mission profile of ambient temperature and irradiance, as explained in section III. The junction temperature data from the year-long model is analyzed using rain flow counting to identify the number of cycles for each difference in junction temperature. The data obtained from rain flow counting is used to estimate the reliability indices and lifetime of the inverter, as explained in section IV. Section V details the impact of reactive power on lifetime of the inverter, due to the operation of PV inverter at non-unity power factors. The workflow utilized for further sections is represented in Fig. 1.
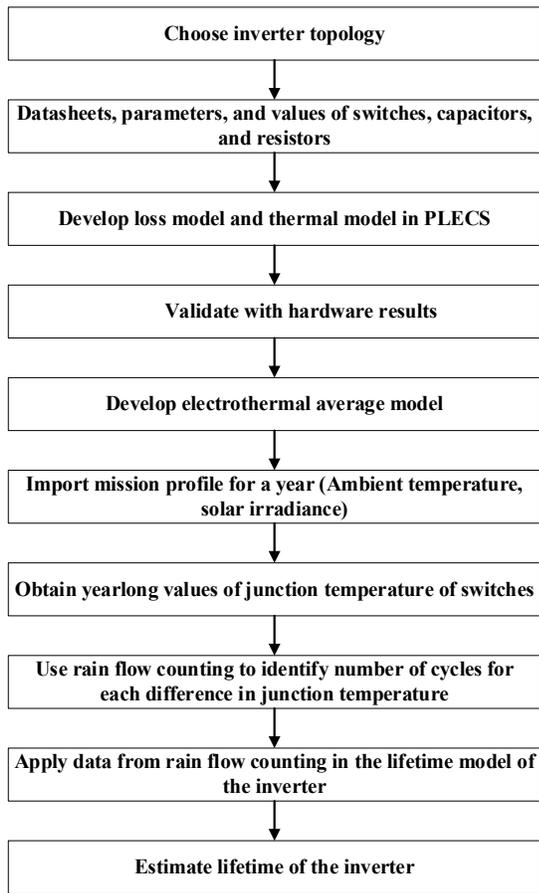
Fig. 1.   Workflow to calculate the lifetime of inverters

II. ELECTROTHERMAL MODEL

The first step in this study is to develop a home-grown inverter. The built home-grown inverter, shown in Fig. 2, is a two-stage single phase grid connected inverter with a boost DC-DC converter at the first stage and a H-bridge inverter at the second stage connected to 120V AC grid system. The inverter is designed to run at closed loop and is capable of supplying or absorbing reactive power.

Fig. 2.   Board Layout of the home-grown inverter

The inverter design was validated using PLECS, a transient power electronics simulation software. The model developed in PLECS includes the detailed parameters of the power semiconductor like the ON-state resistance, gate charge, gate resistance, and temperature dependent parameters used in the inverter hardware. The model also includes the external series resistances and magnetic parameters of components like choke coil, EMI filters and inductors. These were used to develop a detailed electrothermal model.

A. Loss model

The loss model includes semiconductor associated losses like switching losses, conduction losses, Gate charge losses, reverse recovery losses, Gate driver losses, reverse conduction losses, and inductor associated losses like core losses and conduction losses, shown in Fig. 3. The internal resistances of the inductors, choke coils, and sensors were modelled using conduction losses.
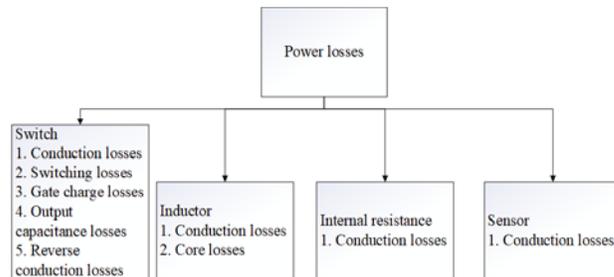
Fig. 3.   Classification of losses of the power converter

The switch used in the power converter is a Power MOSFET. The Power MOSFET has a resistance between the drain and source of the device during the ON-state, $R_{DS(ON)}$. The $R_{DS(ON)}$ parameter is dependent on the junction temperature of the power MOSFET, with $R_{DS(ON)}$ increasing as temperature increases. When the MOSFET is switched on, the current flowing between the drain and source contributes to conduction losses. The conduction loss, P_{COND} is calculated as shown below.

$$P_{COND} = I_D^2 \times R_{DSON} \qquad (1)$$

The Power Semiconductors can be interpreted as commutation devices undergoing thousands of ON and OFF cycles. In a conventional unipolar PWM controlled inverter, there is a non-zero current and voltage during the ON-OFF transition creating the switching loss. Fig. 4. shows the switching transition occurring at non-zero voltages and currents.
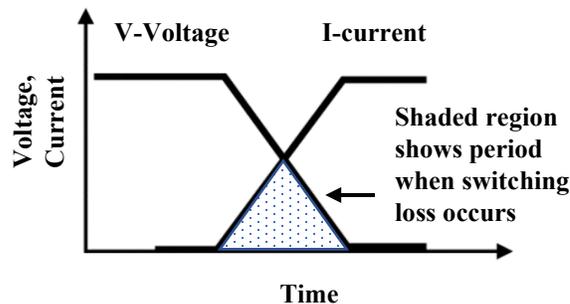
Fig. 4.   Switching transition at non-zero voltage and current

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The loss calculation depends on multiple parameters of the selected power MOSFET and operating voltage, current and switching frequency. Switching losses can be defined as the sum of turn-on and turn-off losses of the power MOSFET [9].

For turning the switch on and off, the gate to source capacitance, C_{GS} is charged and discharged during the switching transitions. The power consumed for the charging and discharging of the capacitance is referred to as gate charge loss, P_G. The gate charge loss, P_G is dependent on the switching frequency, f_{sw}, gate drive voltage, V_{DR} and gate to source capacitance, C_{GS}. The gate charge loss is defined by the following equation below:

$$P_G = Q_G \times V_{DR} \times f_{sw} \tag{2}$$

To charge the output capacitance, C_{OSS} of the power MOSFET to its bus voltage, some amount of power is consumed. The power needed for charging the output capacitance is referred to as switch output capacitance loss, P_{OSS}. The power is dependent on the switching frequency, drain to source voltage, V_{DS} and switch output capacitance, C_{OSS}. The Switch Output capacitance loss, P_{OSS} is defined by the equation below:

$$P_{OSS} = \frac{1}{2} \times C_{OSS} \times V_{DS}^2 \times f_{sw} \tag{3}$$

The dead time setting provided by the gate driver causes the turning on of body diode making it conduct during the switching transitions. This creates a diode conduction loss, referred to as reverse conduction loss, P_{SD}. The reverse conduction loss, P_{SD} is dependent on the body diode voltage, V_{SD}, drain to source current, I_{DS}, dead time setting of the gate driver, t_{SD} and switching frequency. The reverse conduction loss, P_{SD} is defined by the equation below.

$$P_{SD} = V_{SD} \times I_{DS} \times t_{SD} \times f_{sw} \tag{4}$$

The inductors experience power loss, P_{copper} which can be classified into two categories. They experience conduction loss due to the current flow through the copper windings. These windings have their associated External Series Resistance (ESR). This is similar to I^2R loss equation shown below.

$$P_{copper} = I_{RMS}^2 \times ESR \tag{5}$$

The second category is the core loss, which occurs in a magnetic core due to the alternating magnetization. The core loss is classified into Eddy current loss and Hysteresis loss. The manufacturer [10] typically provides the constants and coefficients necessary for computing the core loss power density using the Steinmetz equation below.

$$P_v = Cm \times f^x \times B^y \times \frac{Ct_2 \times T^2 - Ct_1 \times T + Ct}{1000} \tag{6}$$

The core losses can be estimated by the core loss power density, P_v with the volume of the core material, V_{core}.

B. Thermal model

The losses explained above were implemented in a switching model developed in PLECS, a power electronics simulation platform. This electrical model can estimate the losses of the power converter. With loss modeling completed, a thermal model was developed to describe the transient thermal behavior and to estimate the temperatures of the power devices. The

thermal behavior is typically described using lumped elements in the form of thermal resistances and capacitances. The thermal model developed for measuring temperatures has an analogous relationship with an electrical circuit representing a voltage source connected to a resistor. Fig. 5 describes the relationship between electrical and thermal domain.
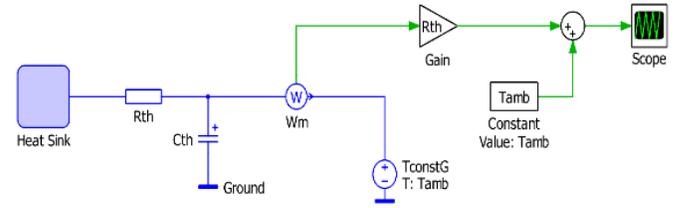

Fig. 5. Electrical equivalent circuit in thermal domain

Thermal resistance determines the increase in temperature of the system with respect to power loss. It can also be defined as increase in temperature per one watt of power loss. The total thermal resistance of a MOSFET connected to the heatsink is the sum of thermal resistances of heatsink thermal resistance, Thermal Interface Material (TIM), and power MOSFET. The thermal resistance of the MOSFET is determined by the Foster / Cauer network values provided by the manufacturer. The total resistance of the heatsink system is represented by the equation below

$$R_{TOTAL} = R_{MOSFET} + R_{TIM} + R_{HS} \tag{7}$$

Thermal capacitance determines the time taken for the temperature to reach a steady state value. The product of thermal resistance and thermal capacitance is equivalent to the time constant in a RC electrical circuit, which is the product of resistance and capacitance. Thermal capacitance, C_{th} is defined as the product of volume of the material (V), density of the material (ρ) and specific heat of the material at constant pressure(cp). The product of volume(m^3) and density (Kg/m^3) can be rewritten as mass, m (Kg).

$$C_{th} = V \times \rho \times cp \ [J/K] \ = \ m \times cp \ [J/K] \tag{8}$$

C. Results

The switches of the inverter are modulated using unipolar Pulse Width Modulation. The losses of the switches include conduction losses and switching losses. Fig. 6. shows the switch losses of the top and bottom MOSFETS. It can be observed from the figure that the loss waveforms follow the sinusoidal waveform of the output grid AC voltage.
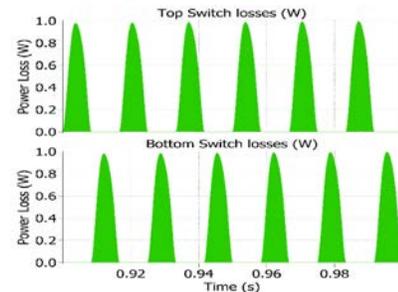

Fig. 6. Switch losses of the top and bottom inverter MOSFETS

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The thermal model of the inverter is implemented using the data obtained from the datasheets entered in the form of variables, parameters and lookup tables. Fig. 7. shows the thermal model of the two-stage home-grown inverter simulated in PLECS.
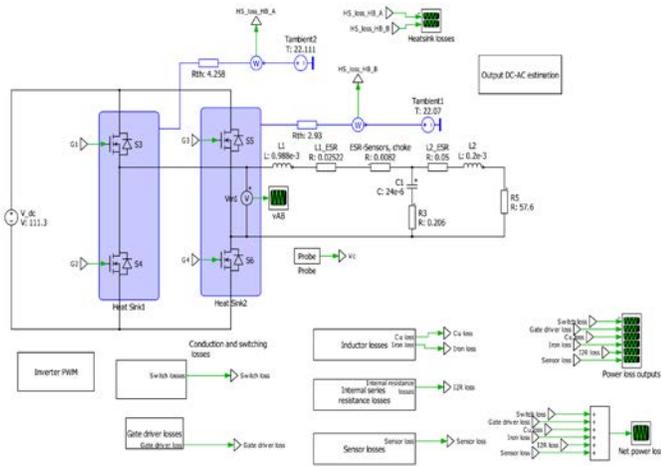

Fig. 7.   Detailed Electrothermal model of home-grown inverter

From Fig. 7, it can be observed that the losses of the power converter are calculated separately based on the components used in the system. The heatsink is represented by a blue box around the power MOSFET's. The software calculates the losses and temperatures of the components under the area of the heatsink. These losses simulated by the software have a settling time associated with the thermal capacitances of the MOSFET. In the simulation, these instantaneously calculated losses are averaged over few switching cycles using analytical formulae.

Fig. 8. shows the comparison of analytically calculated heat losses without the settling time and the simulated heat losses without including the thermal capacitances.
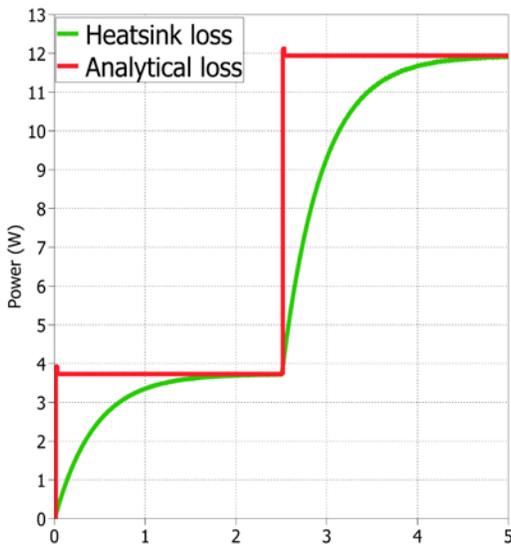

Fig. 8.   Comparison of analytical heat loss with simulated heatsink loss (with settling time)

The electrothermal model was also validated with hardware temperature measurements on the power switches. The temperatures of the power MOSFET were acquired using thermocouples placed on the switches, shown in Fig. 9.

Fig. 9.   Experimental setup of homegrown inverter with thermocouples

The temperature raise in the MOSFET was compared between the hardware and simulated model, shown in Fig. 10. The temperature values from the simulation matches the actual hardware.
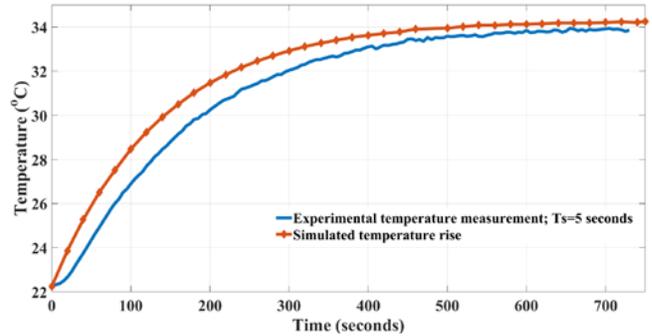
Fig. 10.   Comparison of experimental and simulated temperature rise of the MOSFET

The thermal model was also verified by repeating the experiment at different ambient temperatures in a thermal chamber. The inverter setup running at 500W was placed inside the thermal chamber for ambient temperatures of 25°C, 35°C, and 45°C. The conditions were simulated in the PLECS and the temperatures were plotted against the hardware results shown in Fig. 11.

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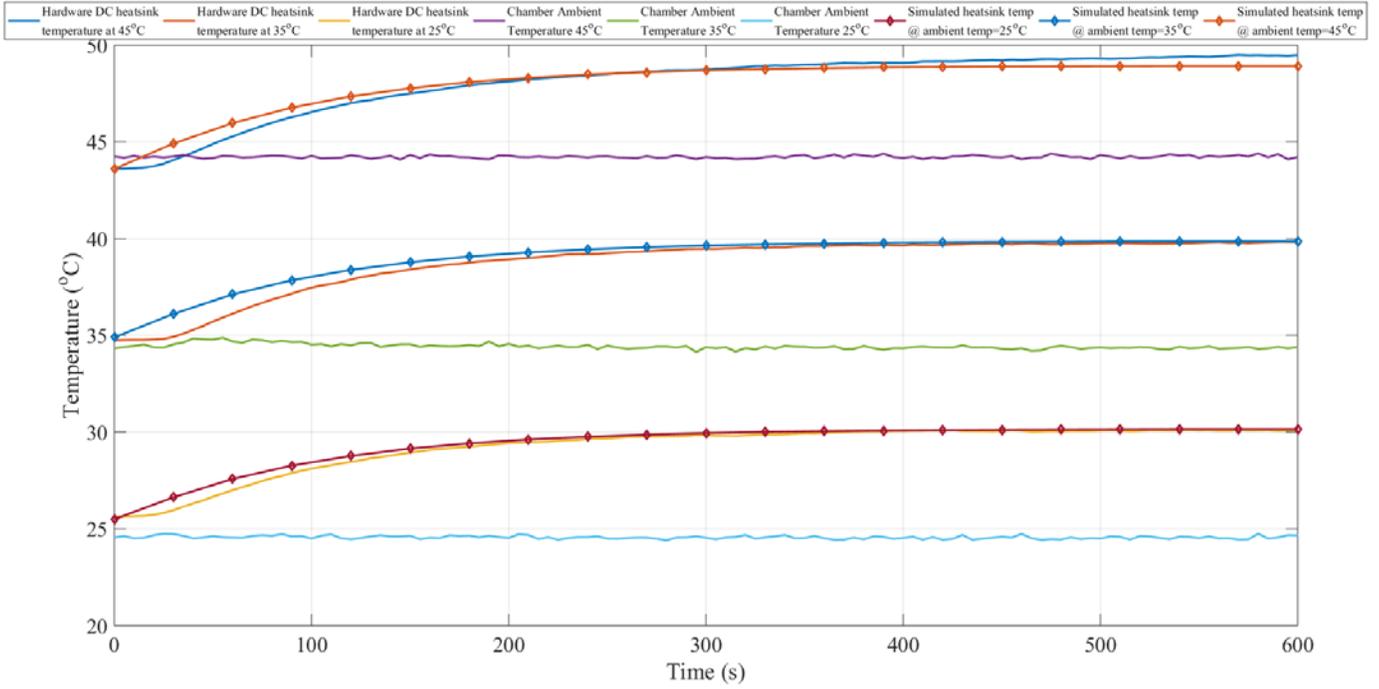
III. Reduced Order Model

For measuring temperatures over an entire year, the computational time of a switching model of the PV inverter is very large due to the presence of electrical model of the PV panel, passive components, power semiconductors, high speed controllers. The highlighted portions in red and blue, shown in Fig. 12. should be reduced using an average model [12].
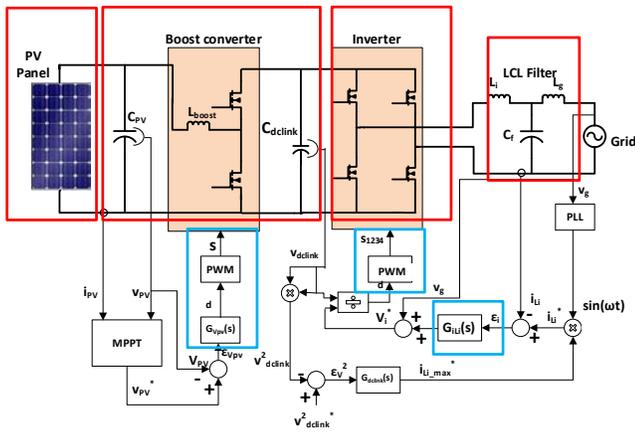

Fig. 12.   Simplification of the power converter model

The losses are averaged using analytical formulae to reduce computational time. The losses calculated are translated into increase in temperature using the thermal impedance network (Foster, Cauer) of the MOSFET. The obtained difference in temperature, ΔT_j is added with the ambient temperature, T_a to obtain the device temperatures shown in Fig. 13.
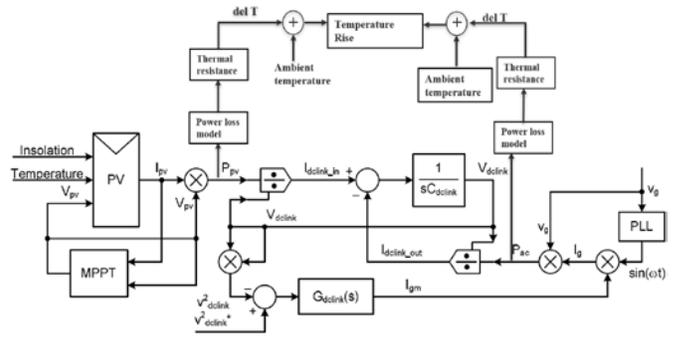
Fig. 13.   Implementation of average PV inverter loss models

To account for variations in temperature and irradiance at a location over many years, the typical meteorological year (TMY) data is used as input for the model [13]. The two locations are Phoenix, Arizona and Ft Peck, Montana, with former a hot location and latter being a cold location. The ambient temperature data is provided in degree Celsius (°C). The irradiance data is chosen from the Global Horizontal Irradiance (GHI) data. The model computes the annual PV power production and translates it to junction temperature of the semiconductors. Fig. 14. a) includes the annual PV power production and Fig. 14. b) shows the annual junction temperatures for TMY of Phoenix.

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Fig. 14. a) and b) showing annual PV power production and annual junction temperatures for Phoenix

IV. RELIABILITY AND LIFETIME MODEL

The results of the yearlong model provide the junction temperatures of the power semiconductors. The junction temperature data is fed through a rain flow counting algorithm [15] to record number of device cycles, N_i, under each difference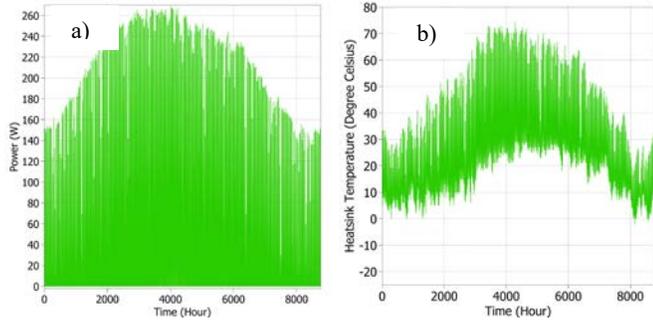 in junction temperature, ΔT_j. Applying the number of cycles and ΔT_j to the lifecycle model gives us the lifetime of the power semiconductors. With the coefficients provided by the device manufacturer, a simplified Coffin-Manson model [14] is considered for evaluating the number of cycles to failure, N_f, shown in the equation below.

$$N_f = a \times (\Delta T_j)^{-n} \qquad (9)$$

Where, 'a' refers to the experimental constant and n is the Coffin-Manson model coefficient. For the Coffin-Manson model coefficient, n, this work utilizes the coefficient provided by the manufacturer for Aluminum wire bond failure. For constant 'a', this work utilizes the Mean Time To Failure (MTTF) value. This value is calculated using the Failures in Time (FIT) number and confidence value provided by the manufacturer.

The number of cycles to failure, N_f, is related with the number of cycles the device is already consumed, N_i, based on the assumption of linear damage is considered, typically referred to as the Miner's rule. The cumulative stress calculated by Miner's rule is expressed below.

$$Q = \sum_{i=1}^{n} \frac{N_i}{N_{fi}} \qquad (10)$$

Where, i=1,2,3,…,n represents the various differences in junction temperature of the power semiconductor, ΔT_j. The cumulative stress, Q, has a value less than one. The reciprocal, $1/Q$ gives the number of mission profiles the device can survive for the same mission profile, referred to as Remaining Useful Lifetime (RUL).

The cumulative stress rate and lifetime estimation are calculated for a single condition for a defined sample size. To account for the variations in conditions and the uncertainty in manufacturing over a million devices, the failure rates must be characterized using a probability density function [16].

The failure function F(t) estimates the probability of a device failure at or before time, t. This is expressed as

$$F(t) = \int_o^t f(\tau).d\tau \qquad (11)$$

The lifetime calculation performed using the above Coffin-Manson model was compared with existing avalanche-based lifetime model [17]. The proposed model was compared with avalanche-based lifetime model and the lifetime estimations were found very close to each other, as shown in Table 1.

TABLE I
LIFETIME MODEL COMPARISON OF AVALANCHE MODEL AND COFFIN MANSON MODEL

Mission Profile	Avalanche based lifetime model	Coffin Manson lifetime model
Ft Peck	140.2 years	138.1 years
Phoenix	66.6 years	64.4 years

V. IMPACT OF REACTIVE POWER

With support of reactive power, the apparent power of the inverter increases which translates into increased currents and increased temperatures of the power semiconductors. To study the effect of reactive power, the yearlong mission profile for Phoenix TMY shown in section IV is repeated for non-unity power factors of 0.8 p.u., 0.85 p.u., 0.9 p.u., and 0.95 p.u. The simulations were repeated for this power factors and junction temperature profiles were obtained. The rain flow counting algorithm was repeated for each power factor and the number of cycles for each difference in junction temperature, ΔT_j were computed. A bar graph was plotted for number of cycles under each ΔT_j or power factors from 1 p.u. to 0.8 p.u. in Fig. 15.
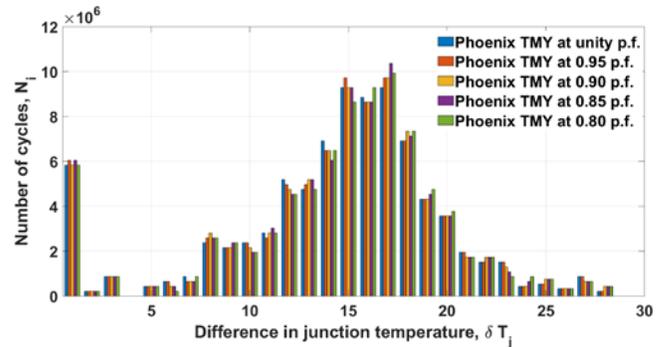
Fig. 15. Bar graph comparison of number of cycles at each ΔT_j at Phoenix TMY at power factors 1 p.u., 0.95 p.u., 0.90 p.u., 0.85 p.u. and 0.80 p.u.

Using this data from rain flow counting, the number of cycles to failure, Nf and Remaining Useful lifetime was calculated for each power factor. Fig. 16. shows the remaining useful lifetime (RUL) decreasing as the power factor moves away from unity for the same mission profile.
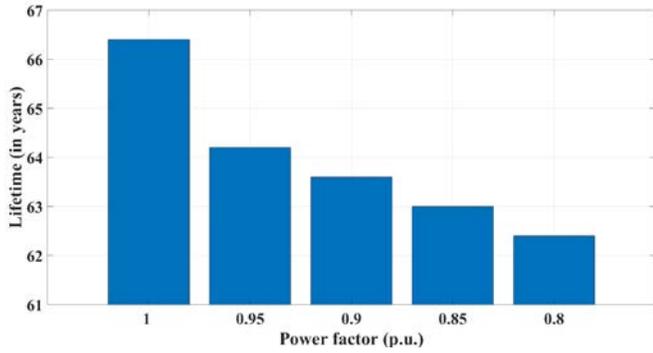
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Fig. 16.   Comparison of RUL versus the operating power factor for Phoenix TMY

VI. CONCLUSION

A detailed electrothermal model was developed for a PV inverter and the loss models and thermal models were verified using an in-house inverter. The results from the detailed electrothermal model was validated by operating the in-house inverter at different ambient temperatures inside a thermal chamber and the junction temperatures from hardware and simulation matched closely. From this detailed model, a reduced order model was developed to translate the year-long mission profile of ambient temperature and solar irradiance into junction temperature of the switches. The junction temperature data from year-long model was used to estimate the reliability and lifetime of the inverter. Further, the model was extended to study the impact of reactive power on lifetime of the inverter. The results from the study show that inverter lifetime decreases for operation of inverter at power factors other than unity.

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