Techno-Economic Analysis for Grid Edge Intelligence: A Preliminary Study on Smart Voltage Regulator Controls

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Adverse impacts of variability in PV generation on the life/maintenance of tap changers can be reduced by adding intelligent autonomous controls for voltage regulators. Applications of a framework that can perform techno-economic analyses on smart voltage regulator control algorithms are presented in this work. The framework was developed at NREL and regulator control applications developed by Eaton Corporation were assessed with this framework to quantify performance improvements with grid edge intelligence.

Leverages a Python-based techno-economic analysis tool (SPEED-DER) that uses OpenDSS as a power flow solver
SPEED-DER can conduct quasi-static time-series simulations while integrating advanced control applications in a plug-and-play fashion
Pluggable control applications, provided by Eaton, come as black box control modules

Control application scenarios:
I. Legacy control with default, location-independent delays
II. Legacy control, with modified location-coordinated time delays
III. Adaptive time delay control
IV. Adaptive voltage bandwidth control

Cost-benefit analyses are designed based on three maintenance policies for control devices:
- Policy-1: Replace its switching contacts
- Policy-2: Alternate replacing its contacts and replacing the entire device
- Policy-3: Replace the entire device

After a regulator has operated a predetermined number of times (100,000 for this study), a maintenance request can be issued.

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Figure: Capability description of SPEED-DER framework

Figure: Tap change counts for voltage regulator clusters and LTC for selected 5-day simulation

Figure: Differences in net present values for O&M costs between the legacy and other two control techniques for different maintenance policies

Figure: Long-term flicker severity indices results for selected 5-day simulation (< upper limit of 0.8)

Figure: Daily regulator tap change counts for Reg-3 with a) legacy control, b) adaptive time delay control, and c) adaptive voltage bandwidth control; from 1-year simulation

Figure: Topology of the test circuit (J1 feeder) with distributed PVs and locations of LTCs and line voltage regulators

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