

Manufacturing and Reliability Science for CIGS Photovoltaics

Lorelle Mansfield

National Renewable Energy Laboratory

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Final Report

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Principal Investigator:	Lorelle Mansfield Scientist Phone: 303-384-7884 Email: <u>lorelle.mansfield@nrel.gov</u>

Executive Summary: The purpose of this program was to overcome the largest challenges to investor confidence and long product lifetime in Culn_xGa_{1-x}Se₂ (CIGS)based photovoltaic products: metastability, shading-induced hot spots, and potentialinduced degradation (PID). Key findings were made in each of these areas by studying CIGS reliability at the cell level, which very few groups are currently doing. Metastability was thought to be a function of the CIGS absorber. We have challenged the state-of-theart by showing that the metastability seen in commercial products is likely to be caused by the buffer layer. Solar Cell Capacitance Simulator (SCAPS) device modeling confirmed that the buffer layer has a significant influence on metastability in CIGS devices, and it also led to a processing change-the introduction of CdS islands to Zn(O,S) buffer layers-that dramatically reduced metastability in CIGS solar cells. In the reverse-bias shading task, modeling showed us that 19% solar cells are possible with thin CIGS layers of 0.5 µm. We were able to fabricate 15.2% solar cells in this project, which is the highestreported efficiency of devices in the ultra-thin class. We also discovered that the best way to dissipate less power in reverse bias was to eliminate the intrinsic ZnO laver that is often used in CIGS devices. Lower power dissipation led to devices that allowed two times the maximum power-point current density in reverse without damage. PID is caused by the drift of Na+ ions from the back glass to the CIGS/Mo interface, followed by diffusion into the solar cells and to the CdS region. We found that PID can be slowed by using lowconductivity borosilicate glass that contains higher K and lower Na than soda-lime glass. Based on significant progress in each of the three reliability challenges, the CIGS celllevel reliability project was very successful. We have also proved that module-level degradation mechanisms can be tested and solved at the cell level.

Background: The novelty of this work is evidenced by the few updates in the literature in the field of cell-level reliability. Of the three areas of study, metastability has the most activity. Several papers document techniques for measuring metastability, such as photoluminescence [7-10]. Most cite the Lany-Zunger V_{Se}-V_{Cu} complex (LZ) [11] as an absorber defect that is likely responsible for metastable behavior. These are different from our work because we have shown the metastable behavior to be more buffer-related than absorber-related. Some studies did look at buffer changes such as surface treatments [12] and varying chemistry [13-15] to reduce metastability in devices with Zn(O,S) buffers. Oftentimes they still site the LS model for defect states in the CIGS at the buffer/absorber interface. One notable experiment is the addition of Si to the CIGS growth [16], which enables the *elimination* of the buffer layer and also reduces metastability.

Studies related to partial-shading damage include those by Steve Johnston's project, where sites likely to break down were identified using thermal imaging techniques [17-19]. Another group looked at differences in reverse breakdown behavior depending on the buffer layer used and modeled it according to Fowler–Nordheim tunneling and also Poole–Frenkel conduction [20]. They think that Fowler–Nordheim tunneling is the main contributor to the breakdown current. This paper could be useful when we begin device modeling for reverse-bias behavior. Of course, there are also reports of partial-shading damage in modules [21, 22], and Marco Nardone was able to model the difference between bare and encapsulated modules [23]. Experimentally, we have shown that encapsulated devices break down at smaller reverse voltages, but that will not be reported publicly. Studies on ultra-thin devices are covered below in the Project Results and Discussion under Task 2.

Potential-induced degradation (PID) had few literature reports, and we are the main group studying it at the cell level. Several deal with PID test procedures for modules [24-26], documentation of failure in CdTe [27], and a review of module PID [28]. *In-situ* dark current-voltage measurements were performed on our cells, and maximum power calculations were done similar to reference [29] with the results submitted to the IEEE Journal of Photovoltaics for publication [30].

Introduction: As costs of Si-based modules have dropped rapidly, the projected large price advantage of CIGS over Si has not been realized. Without a substantial price difference between Si and CIGS modules, and long product lifetime required to achieve low levelized cost of electricity (LCOE), investors have little incentive to choose CIGS, the less mature technology. Thus, with a short product history, addressing product lifetime and reliability issues (or perceived reliability issues) is critical for CIGS. This program was significant because it investigated the three main challenges for reliability in CIGS modules. They correspond to the project tasks: Task 1: Metastability, Task 2: Reverse-Bias Shading, and Task 3: Potential-Induced Degradation. We took an innovative approach by investigating module-scale problems at the cell level and attempting to solve the problems at the cell level. We found ways to mitigate all three reliability challenges, and they are detailed in the Project Results and Discussion section. The project milestones are listed in Table 1.

Table 1 Milestones

Year #	Task #	Milestone	Milestone Description	Planned End Date	Milestone Type: Annual or Quarterly
1	1	1	Outline for publication that draws conclusion whether datasets are consistent with hypothesis that metastability is controlled by the density of (V_{Se} - V_{Cu}) defects and their population.	3/31/2016	Quarterly
1	3	2	Demonstrate that small-cell module test coupons show no degradation under standard damp-heat test (85°C, 85% relative humidity, 1000 hours) and have electrical leads appropriate for PID stress and electrical testing.	6/30/2016	Quarterly
1	2	3	Demonstrate an improved state-of-the-art thin device exhibiting \geq 15% efficiency at \leq 0.5-µm CIGS absorber thickness. Device should exhibit larger reverse current flow at a fixed reverse voltage compared to the standard 2.5-µm-thick device. Quantify, on a research-cell scale, the magnitude of metastability and PID in CIGS devices, and identify routes to mitigate these effects.	9/30/2016	Annual
2	1	1	Identify at least one CIGS metastability mechanism by demonstrating at least one absorber-processing variation and at least one buffer-processing variation that significantly affects metastability.	12/31/2016	Quarterly
2	2	2	Using unencapsulated scribed partner absorbers, document individual cell voltage at which damage from shading occurs, i.e., V _{damage} .	3/31/2017	Quarterly
2	3	3	Identify at least two populations resulting in differing amounts of PID in CIGS cells.	6/30/2017	Quarterly
2	2	4	Demonstrate high-efficiency (\geq 15%) research cell that flows at least I _{mp} in reverse current at a reverse voltage bias of V _{damage} or less. Submit at least three publications to peer-reviewed journals.	9/30/2017	Annual
3	2	1	Using <i>encapsulated</i> NREL cells, document individual cell reverse voltage at which damage from shading occurs, V _{damage} , and current density allowed before damage occurs.	12/31/2017	Quarterly
3	1	2	Show that buffer metastability is reduced in devices with Cd partial-electrolyte (CdPE) treatment plus Zn(O,S) buffer layer when compared to devices with only a Zn(O,S) buffer layer.	3/31/2018	Quarterly
3	3	3	Confirm the hypothesis that migrating Na is the cause of PID and that K mitigates PID because it migrates less than Na. Stress samples with at least three different alkali levels or incorporation methods, including at least one K-containing sample and one Na- containing sample.	6/30/2018	Quarterly

		-			
3	1	4	 Provide specific process and device design guidelines to eliminate or significantly reduce metastability, shading degradation, and PID in CIGS. Two out of three of the following metrics should be achieved: (Task 1) Reduce metastability to a change in Voc less than or equal to 1 mV over the time period of 500 s to 1200 s of light soaking. State-of-the-art: The most-stable devices with Zn(O,S) buffers had a change in Voc of 1.8 mV to 2.5 mV over the time period of 500 s to 1200 s of light soaking. (Task 2) Encapsulated devices should allow 1.5 x JMPP to flow in reverse-bias without damage. State-of-the-art: Greater than 62% of encapsulated mini-modules were damaged by reverse currents less than 1.5 x JMPP. To measure progress, the behavior of encapsulated standard NREL devices will be measured in Q1. (Task 3) Limit PID to 7% relative change in efficiency after 25 hours of accelerated stressing in the most damaging configuration of back-grounded with +1000 V applied to devices. State-of-the-art: Devices on soda-lime glass degrade by 100% (from original efficiency to 0% efficiency) after 25 hours of accelerated stressing in the most damaging 	9/30/2018	Annual
			 configuration of back-grounded with +1000 V applied to devices. State-of-the-art: Devices on soda-lime glass degrade by 100% (from original efficiency to 0% efficiency) after 25 hours of accelerated stressing in the most damaging configuration. Publication and/or documentation of communication of these results to an industrial partner, preferably, with results on 		
			implementation.		

Project Results and Discussion:

Task 1 Metastability – Summary

Some commercial CIGS modules show large changes in current-voltage (JV) parameters with light soaking. Although such changes do not necessarily indicate a performance problem, the associated uncertainty may be disadvantageous in a highly competitive market. Thus, it is beneficial to understand the origin of large metastabilities to define what processing changes might diminish metastability without impacting other desirable aspects of high-performance devices. We have attempted to reproduce large metastabilities such as those in some commercial products through both absorber and buffer processing variations in small devices. Although variations of both types were found to affect metastability, only buffer variations could reproduce large metastability in high-efficiency devices. Device modeling confirms that buffer effects alone are sufficient to explain the large metastability seen in these devices. The device model has guided us toward a processing change that reduces metastability without increasing current loss in the buffer.

Background

In CIGS cells and modules, changes in JV behavior with light exposure are most typically observed to be metastable, (i.e., the change can be reversed by periods of dark storage) and positive (i.e., module efficiency increases with time). Some products are observed to undergo large metastable increases in fill factor and voltage with light exposure. Figure 1 shows an example of parameter changes with light soaking in a commercial CIGS module. JV parameters are shown as a function of one-sun light-soaking time at 50°C.

Buffer Variations

Several works have reported larger JV metastability in CIGS with non-CdS buffers compared to CdS buffers [31-35]. Results from this study support that trend. Figure 2 shows the change in opencircuit voltage (V_{oc}) with light soaking for an experiment involving only buffer variations. Data from all 45 different samples are shown. with the mean value for each buffer type marked with an "X."



Figure 1: Power, V_{oc}, and fill factor as a function of 1-sun light-soak

time for an example of a commercial CIGS module.

Absorber Variations

The goal was to induce large metastable device behavior via multiple variations in absorber processing, without changing the CdS buffer. 37 samples incorporating processing variations were expected to affect metastable defect concentration. However, for high-efficiency samples (i.e., efficiency > 15%), large metastability did not occur. This result is shown by the gray + signs in Figure 3. On the other hand, some absorber process variations resulted in low-efficiency devices with significant metastability. The low-efficiency, metastable devices occurred for process variations that produced low carrier density. The black circles in Figure 3, read to the bottom axis, show how the metastable change in Voc anticorrelates with zero-bias, dark-state carrier density (p).

An anti-correlation between carrier density and metastable change in V_{oc} is to be expected from the modest metastable defect concentrations reported. Specifically, following the derivation of Obereigner, the change in V_{oc} , ΔV_{oc} , can be derived to be

$$\Delta V_{oc} \approx \frac{AkT}{2q} \ln \left(1 + \frac{\Delta p_{meta}}{p_{shallow}} \right),$$

where k is Boltzmann's constant, T is temperature, q is the electron charge, A is the diode quality factor, $p_{shallow}$ is the shallow acceptor density, and Δp_{meta} is the change with light-soaking and a subsequent increase with light soaking due to metastable defects. The solid line in Figure 3 is a least-squares fit using the form of this equation and p_{meta} as the fit parameter. The extracted value for Δp_{meta} is 8.5×10¹⁴



Figure 2: Voltage metastability in CIGS devices for different buffer deposition chemistries, with mean value marked as "X."



Figure 3: Metastable change in V_{oc} as a function of dark carrier density (lower axis, black circles) or stabilized device efficiency (upper axis, gray +'s). The solid line is a least-squares fit to the carrier-density data.

cm⁻³, in approximate agreement with the low 10^{15} cm⁻³ values of Δp_{meta} observed in the literature. The correlation coefficient is 0.6, implying that this relationship explains most of the variation in metastability in the dataset.

JV Curves and Device Modeling of Buffer Variations

JV curves exhibiting metastability were modeled to determine what ranges of materials parameters might reasonably lead to the observed effects. А few representative JV curves from this study were chosen for modeling and are shown in Figure 4 as solid lines. Because the CdS devices are much more stable, Figure 4 contains only one experimental JV curve for this device, whereas both relaxed-state and light-soaked curves are shown for the other devices.

Device modeling was used to understand the possible origins of the observed behaviors, using Solar Cell Capacitance Simulator (SCAPS)



Figure 4: Measured JV curves (solid lines) and modeled JV curves (dashed lines with x's) for samples with different buffer variations.

software [36]. Literature or measured materials properties values were used to describe each layer. The values employed in the SCAPS model are well-documented in the paper (drafted, to be submitted) so that other groups may use them to replicate our results and compare to their own devices. Four ZnOS parameters—free-electron density, deep-trap density, buffer/absorber surface recombination velocity, and buffer/absorber conductionband offset—were varied to fit the experimental JV curves. These modeled JV curves are overlaid with the experimental data in Figure 4. The modeled curves reproduce the features of the experimental data (including inflection, voltage, and fill factor increases with light soaking) and curve shape. Thus, it is concluded that buffer effects alone are sufficient to explain the large metastability seen in these devices.

Implications for Processing Changes

The insights provided by the SCAPS device model have suggested some processing changes that might mitigate metastability. One such change has been proven experimentally. Tiny islands of CdS were deposited adjacent to the buffer layer. These islands enable hole injection into the buffer layer, and thus, they decrease metastability without increasing buffer absorption. Figure 5a compares quantum efficiency (QE) from devices with a standard CdS buffer, one with a standard Zn(O,S) buffer, and a third with a Zn(O,S)buffer with CdS islands. The addition of the CdS islands does not appreciably decrease the blue response of the device. Figures 5b and 5c compare the change in Voc of these three devices as a function of time, over two different timescales. From the small change in Voc of the devices with Zn(O,S) + CdS islands (red traces), it can be seen that the presence of the CdS islands dramatically decreases metastability.

During the course of this project, we have made excellent progress in understanding CIGS device metastability. We have challenged long-held the theory that metastability is solely a function of defects in the CIGS absorber by proving that the metastability seen in commercial products is likely to be caused by the buffer layer. Our discovery has been supported by SCAPS modelina and confirmed device bv experimental devices. A dramatic reduction of metastability in CIGS solar cells was realized by introducing CdS islands adjacent to Zn(O,S) buffer layers.



Figure 5: Comparison of devices with three different buffer designs, in terms of a) QE, b) voltage increase over 20 minutes of light soak, and c) voltage increase 500–1200 seconds after initial exposure.

Task 2 Reverse-Bias Shading – Summary

Partial shading can degrade module performance by forcing reverse current through the shaded cells. Our original hypothesis was that fabricating devices with a thinner CIGS layer would confine the electric field and allow the reverse current to flow at lower voltages, thus reducing the power dissipated and the likelihood of damage. We modeled thin devices to determine how to attain the highest efficiency and were able to fabricate devices with 0.49-µm CIGS that had 15.2% efficiency. However, reverse-bias behavior was not significantly improved. Taking a cue from previous reverse biasing of Zn(O,S) devices, we improved reverse-bias behavior in CdS devices by removing the i-ZnO layer from the device stack. Both the CdS devices without i-ZnO and the Zn(O,S) devices were able to survive twice the maximum power-point current in reverse without damage.

Background

Partial shading can degrade module performance by forcing reverse current through the shaded cells. Silverman et al. found that modules lost 4%–7% of their maximum power due to shunting caused by partial shade [21]. The damage is observed as visible "worm trails" in Figure 6. We have been able to reproduce this damage in small-area cells by subjecting them to reverse bias in the dark.

Thin CIGS Devices – Modeling and Performance

It is difficult to evaluate changes to current and voltage separately by device fabrication trials, especially

when determining how Ga content should change through the device thickness. Therefore, we used device modeling to investigate the effect of Ga content in ultra-thin CIGS devices. We first wanted to determine the optimum "height" of the Ga/(Ga+In) (Ga/III) at the rear of the film near the CIGS/Mo interface, which can act as an electron reflector at the back of the device. In Figure 7a, at a thickness of 2 μ m, the efficiency can be greater than 20% for rear Ga/III ratio of 0.3 and higher, with the best efficiency coming from rear Ga/III = 0.6. For thinner CIGS films, the highest efficiencies also occur at rear Ga/III = 0.6, but the efficiency numbers are lower. This modeling indicates that it is



Figure 7: (a) Efficiency versus rear Ga/(Ga+In) and (b) efficiency versus bandgap-gradient start for three different film thicknesses. Insets show, by red arrows, the portion of the bandgap that is changing.



Figure 6: Image of visible damage ("worm trails") to a CIGS module caused by partial shading.

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possible to achieve 19% efficiency for 0.5- μ m devices. The device model also leads to the conclusion that the rear Ga/III of the 0.5- μ m CIGS films should be at least 0.5 to 0.6. This is a difference in Ga/III of at least 0.3 over the rest of the film. In general, the efficiency is also increased when the start of the bandgap-gradient is farther from the film surface (Figure 7b). The dependency of efficiency on bandgap-gradient start depth is particularly strong for the ultra-thin CIGS films with a thickness of 0.5 μ m. Optimization would result in a very thin layer of high-Ga CIGS. It also means that the rear Ga gradient should be as steep as possible to increase the device efficiency. More than 19% efficiency could be achieved if the bandgap-gradient start depth is greater than 0.35, or stated alternatively, if the high-Ga region is less than 0.15 μ m thick.

To aid in fabricating the Ga gradients that were modeled, we developed a prediction tool for Ga gradients. As shown above, the gradients are important to device performance, and they vary as a function of growth recipe. Predicting Ga profiles using classic diffusion equations is not possible for a couple of reasons. First, In and Ga atoms occupy the same lattice sites—thus, they diffuse interdependently. Second, there is not yet a detailed experimental knowledge of the chemical potential as a function of composition that describes this interaction. We showed how diffusion equations can be modified to account for site sharing between In and Ga atoms [37]. The analysis was implemented in an Excel spreadsheet, and outputs predicted Cu, In, and Ga profiles for entered deposition recipes. A single set of diffusion coefficients and activation energies was chosen such that simulated elemental profiles track with published data and our own experiments.

diffusion Device modeling and modeling guided our attempt to high-efficiency achieve ultra-thin CIGS solar cells. The best devices from this study are plotted in Figure 8, along with best results from some other studies [1-6]. The devices most similar to ours in performance are from Kim et al., with efficiency of 13.7% at 0.5 µm [6]. Vermang et al. used rear passivation to attain devices of 13.5% efficiency at 0.4 µm [3]. In our experiments, we did not use additional passivation like Vermang's, light-management schemes as reviewed by Schmid [38], or the increasingly popular postdeposition alkali treatments. This



Figure 8: Efficiency versus thickness for several previous studies [1-6] on ultra-thin CIGS. The best efficiencies from this study are shown by red triangles pointing toward the upper right.

indicates that even higher device performance is possible. We were able to increase the efficiency of our ultra-thin CIGS for thicknesses between 0.43 and 0.65 μ m. Our best cell was measured at 15.15% efficiency and had a CIGS thickness of 0.49 μ m. It had the highest voltage of our samples at 0.733 V, plus good current at 26.4 mA/cm² and fill factor of 78.2%. The official JV measurement was taken by NREL's Solar Cell/Module Performance Group. Full details can be found in reference [39].

Reverse-Bias Behavior

We reverse-biased devices with a variety of Cu(In,Ga)Se₂ absorber thicknesses from 0.4 μ m to 2.5 μ m, with the expectation that larger reverse current would be allowed to flow at lower voltages. Our initial experiments showed promise. However, as the efficiency of thin devices was improved, the reverse current allowed at a given voltage decreased. To display this phenomenon, we tried several different metrics. Originally, we calculated reverse breakdown voltage after the method of Puttnins et al. [40], but our CdS devices did not always show a turn-on voltage in reverse before becoming damaged. We also looked at voltages to reach a given current density, such as



Figure 9: Power dissipated at J_{mpp} in reverse bias versus CIGS film thickness.

maximum power-point current (J_{mpp}) or -30 mA/cm². The best metric was to calculate the power dissipated (P = I * V) for those devices that reached the J_{mpp} in reverse. This makes sense as a comparison between devices because we can easily understand that more power dissipated will indicate device damage. The power in mW versus CIGS absorber thickness is shown in Figure 9. The orange box is to indicate that most of the devices are within that power range regardless of thickness. We should note that not all devices were able to allow J_{mpp} in reverse without damage and the devices that failed are not on the graph.

Processing Changes

We did discover one processing change that improved reverse-bias behavior. Lee et al. showed that Zn(O,S) buffers were able to allow more current flow in reverse at lower voltages [22]. We saw similar results in our Zn(O,S) devices and wanted to find out if the i-ZnO and AZO layers affected the device's ability to reach J_{mpp} in reverse bias. Comparisons of the device stacks of Zn(O,S) and CdS devices are shown in Figure 10. We did several iterations of CdS devices with thinner i-ZnO layers, with AZO only (no i-ZnO layer), and with thicker AZO layer. A comparison of the power dissipated at J_{mpp} in

reverse for CdS with AZO only, standard CdS with bi-layer ZnO, and Zn(O,S) devices is shown in Figure 11a. The orange box is the same power range as in Figure 9, indicating the common range of power dissipated at J_{mpp} for standard CdS devices. This set does not include devices that were damaged before reaching J_{mpp} in reverse, which was about 50% of the CdS devices. We are pleased to report that devices without an i-ZnO layer—the CdS with AZO only and the Zn(O,S) devices—were consistently able to reach J_{mpp} (and even $2 \times J_{mpp}$, Figure 11b) in reverse bias without damage.





The reverse-bias and partial-shading task led to some important conclusions. Device models confirmed that 19% devices are possible with 0.5- μ m CIGS layers. We were able to fabricate 15.2%-efficiency devices with thin absorber layers, significantly improving upon the previous efficiency of ultra-thin CIGS devices. With these best-in-class devices, we also found that the reverse-bias characteristics do not depend on absorber thickness. We discovered that the best way to dissipate less power in reverse bias was to eliminate the intrinsic ZnO layer that is often used in CIGS devices. Lower power dissipation led to devices that allowed $2 \times J_{mpp}$ in reverse current without damage.



Figure 11: (a) Power at J_{mpp} versus device type and (b) power at $2 \times J_{mpp}$ versus device type. The orange box in (a) indicates the common range of power dissipated at J_{mpp} for standard CdS devices.

Task 3 Potential-Induced Degradation – Background

Studying potential-induced degradation (PID) can add value to photovoltaic (PV) modules by helping to accurately predict power output and mitigate degradation. CIGS absorbers are known to benefit from alkali-metal dopants, which can diffuse out from soda-lime glass (SLG) substrates to enhance carrier concentration and reduce recombination [41]. On the other hand, transport of Na⁺ from SLG into the semiconductors is the cause of PID in Si, CdTe, and CIGS modules [28]. Therefore, alkali metals can both benefit and deteriorate PV performance, depending on their particular distribution and bonding. Careful study of these characteristics is needed to optimize the initial efficiency and degradation of CIGS modules.

Samples

To study CIGS PID, a method for packaging seven small-area solar cells (0.42 cm² each) into module-like encapsulated samples was developed [42]. Standard CIGS device stacks were grown on various substrates: SLG, two borosilicate glasses (BSG), and SLG with an Al₂O₃ diffusion barrier. A KF post-deposition treatment (PDT) was additionally performed on SLG substrates. KF PDTs are known to enhance initial efficiency [41], but studies have connected alkali metals with degradation in damp heat [41], so more work is needed to understand how KF PDTs affect power produced over the lifetime of the PV module. The present study also employed K-rich borosilicate glass substrates instead of Na-rich SLG as a means to achieve comparable initial performance with reduced PID.

Multiple BSGs were explored at first, and Schott D263 BSG was the best of all investigated because of its high K content and thermal expansion coefficient of 7×10^{-6} K⁻¹, which was well-matched to that of CIGS (~7–9×10⁻⁶ K⁻¹). The SLG with an Al₂O₃ diffusion barrier was chosen to be similar to substrates used in industry.

Diffusion (85°C; no bias)

Before PID studies were performed, thermal anneals were examined as control samples—these samples endured long-term exposure to 85° C without bias. Independent of the thermal anneals' duration, samples of every type exhibited a decrease in carrier concentration by 2x to 3x (Figure 12). As expected, this coincided with small V_{oc} and

efficiency reductions. These changes may be attributable to diffusion, possibly through a redistribution of alkali metals. Na is smaller than K, so it should have a higher diffusivity at 85°C. Na's smaller atomic radius should also make its grain-interior defect formation energies more favorable than K, likely making it a more active dopant [41]. For these reasons, the redistribution of Na may dominate the observed carrier concentration and efficiency losses after thermal diffusion.

Drift and Diffusion (-1000 V and 85°C)

Previous studies of CIGS PID have shown that it is crucial to separate moisture and potential effects [28], so the present study employed encapsulation. Bias can be applied across the substrate glass or the cover glass, and both have been shown to cause PID [28]. In this study, four configurations were initially tested on SLG substrates: positive or negative 1000 V, in each case applied either across the substrate or across the cover glass. Bias across the cover glass with both polarities had little or no effect after 100 h of stress. Applying positive bias to the cells with the back of the substrate grounded, which establishes an



Figure 12: (a) Carrier concentration and (b) efficiency means and standard deviations (error bars) as a function of time at 85 °C and 10% relative humidity (no bias) for SLG (gray squares), SLG + KF PDT (black squares), BSG (orange circles), and repeated BSG (red circles) substrates.

electric field from the device toward the back (and should drive Na⁺ the same direction), did not cause PID in 100 h, and may have even improved performance. Applying negative bias to the cells to establish an electric field from the back toward the device (driving Na⁺ from the substrate into the device) caused catastrophic PID. In some cases, the PID (efficiency and carrier concentration losses) could be recovered by reversing the voltage polarity, in agreement with former reports [28]. However, the drops in efficiency and carrier concentration diffusion (Figure 13) were not restored by the polarity switch. The most damaging configuration (-1000 V on the substrate) was carried on for the rest of the experiments.

Initial PV performance of the BSG devices was almost as good as the standard SLG devices (Figure 12) because high levels of K diffused out from the BSG into the growing absorbers (Figure 13). This caused the absorber K secondary-ion mass spectrometry (SIMS) signal on BSG substrates to be similar to the absorber Na SIMS signal on SLG substrates. This relatively high apparent concentration of K established majoritycarrier hole concentrations approaching those established by Na on SLG substrates (Figure 12). In this way, K can achieve similar effects to Na with respect to absorbers' initial PV performance. The SLG PID absorber had increased Na after 25 h of PID, and likewise, the BSG PID sample had more K in the absorber than the BSG control. However, the gain in BSG absorber K was less pronounced than the Na gain on SLG due to the BSG's 35x lower leakage current. The present results suggest that PID occurred through harm to the p-n junction itself (SIMS not shown [43])as opposed to ZnO corrosion, which has been observed in previous CIGS PID studies [28].



Figure 13: (a) Na and (b) K SIMS intensity with depth through the cored device stack for the SLG (triangles) control (black) and PID (red) and BSG (circles) control (gray) and PID (orange) samples. PID duration was 25 h.

ZnO corrosion is much faster in the presence of moisture, highlighting the importance of encapsulation for PID testing.

After 25 h of stress, the SLG and KF PDT (not shown) samples exhibited catastrophic PID to 0% efficiency, while the BSG and SLG/Al₂O₃ substrates suffered much less degradation (Figure 14). Much longer stressing durations were carried on, and slow PID was observed out to 700 h. Figure 14 summarizes the contrast in stability among the samples: on average, the SLG, SLG/Al₂O₃, and BSG solar cells degraded to <50% of their initial efficiency within 6, 30, and 500 h, respectively.

PID was also compared on the basis of Coulombs transferred. After physically driving equal amounts of cations into the devices, the SLG, BSG, and SLG/Al₂O₃ showed different trends. BSG substrates had the least PID with respect to time, but the SLG/Al₂O₃ substrates had the least PID with respect to Coulombs transferred. The Al₂O₃ diffusion barrier did not alter the leakage current of SLG substrates, and the Na driven through the Al₂O₃ diffusion barrier initially improved carrier concentration and efficiency. After 15 h (or 0.05 C), too much Na had accumulated and PID occurred. The Al₂O₃ samples may have different slopes than SLG in Figure 14 and Figure 15 because they received more time at 85°C, light soaking, and bias sweeping, all of which can reverse PID [25]. The BSG samples also had much longer durations at 85°C, so roughly 24x more diffusion should





Figure 15: (a) Efficiency means and standard deviations (error bars) and (b) champions as a function of time at -1000 V bias, 85 °C, and 10% relative humidity for SLG (black squares), SLG/Al₂O₃ (gray squares), and BSG (red circles).

Figure 14: (a) Efficiency means and standard deviations (error bars) and (b) champions as a function of cumulative charge transferred at - 1000 V bias, 85 °C, and 10% relative humidity for SLG (black squares), SLG/Al₂O₃ (gray squares), and BSG (red circles) substrates.

have occurred relative to SLG. Diffusion could be reducing the K⁺ accumulation in the junction that high bias causes, which could also explain the recovery after PID that has been reported to occur even at room temperature [44]. The possibility of test-specific degradation in Figure 14 and Figure 15 must be checked in future work by approximating field conditions more closely (e.g., combining high-voltage stress with light soaking and device bias).

Processing Changes

This study examined the effect of switching from SLG to BSG substrates on PID of CIGS. The high K levels in BSG led to increased K in the absorber layer, which led to initial PV performance similar to devices on standard SLG substrates. High-voltage stressing led to catastrophic PID of solar cells on SLG substrates after just 6 h. In contrast, solar cells on BSG substrates required 500 h of stress for catastrophic PID. The SLG PID was associated with increased Na in the absorber, especially near the buffer interface. The had reduced leakage current, which diminished less-conductive BSG PID. Unencapsulated experiments have observed ZnO corrosion-based PID, but encapsulated PID is due to physical accumulation of ions in the junction. These cations initiate PID by compensating to reduce charge-carrier concentration, built-in voltage, Voc, and efficiency, although catastrophic PID could also relate to shunting or interface recombination. In contrast to the PID-diminishing BSG substrates, SLG with Al₂O₃ diffusion barriers reduced PID without altering leakage current. Further experiments are needed on SLG with Al₂O₃ diffusion barriers with added alkali to increase the device efficiencies.

These laboratory studies emulated field PID using smaller sample areas and shorter timescales. PID of encapsulated CIGS was due to alkali-metal ion drift from the glass substrate, followed by catastrophic accumulation of alkali metal in the junction. These findings indicate that PID testing can be accelerated by using a basis of Coulombs transferred. Similar studies of CdTe modules in the Photovoltaic Quality Assurance Task Force (PVQAT) project have shown that Coulombs transferred in the chamber for a given power-loss level relate well to Coulombs transferred in the field. For this project, two methods for mitigating PID were identified: using less-conductive glass and using a diffusion barrier on the glass to limit initial absorber alkali-metal content. Our results show that less-conductive BSG substrates reduce the Coulomb transfer rate and offer a processing solution for dramatically reducing PID.

Conclusions: Most milestones in the project were met, although some took slightly longer to complete than others. In particular, fabricating an ultra-thin CIGS solar cell with efficiency of 15% was more difficult than expected. This caused the annual milestones 1.2.3 and 2.2.4 to be completed later in the project than planned. Reducing metastability by using a Cd partial-electrolyte before the Zn(O,S) buffer layer was an unmet Quarterly Performance Indicator (QPI). We were able to do this once earlier in the project, but we were unable to replicate the results. The QPI dealing with reverse-biasing encapsulated NREL cells (3.2.1) also did not go as planned because NREL devices tended to break down at the grid lines unlike our partner cells, which did not have grids.

This project did demonstrate that investigating cell-level reliability is an effective way to solve module reliability problems. We were able to reduce metastability by adding CdS islands to our Zn(O,S) buffers. Reverse-bias damage was mitigated by removing the i-ZnO layer from devices, when using either a Zn(O,S) buffer or a CdS buffer. Potential-induced degradation was also slowed by replacing the soda-lime back glass with a low-Na, high-K borosilicate glass. These changes could be implemented in modules to help solve the three main reliability problems in CIGS PV.

Budget Categories per SF-424a	BP 1		BP 2		BP 3		Total	
k. Total Charges	\$	926,586	\$	1,175,121	\$	1,218,293	\$	3,320,000
DOE Share	\$	926,586	\$	1,175,121	\$	1,218,293	\$	3,320,000
Cost Share							\$	-
Cost Share Percentage		0.0%		0.0%		0.0%		0.0%

Budget and Schedule:

Path Forward: Open questions still exist in the field of cell-level reliability. We found that CdS islands reduce the metastability of CIGS devices with Zn(O,S). However, we did not explore other materials that may be able to perform a similar function. Reducing the Cd in the device stack is always a priority, so there are research opportunities in finding materials that can inject holes into the Zn(O,S) buffer layer, or alternative buffer layers that would provide stability without the use of Cd. The definition of metastability used in this project was of *reversible* changes. Other degradation mechanisms, such as *irreversible* performance decreases caused by heat and light-soaking, could be studied in a similar fashion. Reverse-bias behavior in solar cells is not commonly explored, and the field could benefit from having a device module that attempts to describe it. This would allow predictions of reverse-bias behavior in modified device structures before the actual

fabrication occurs. Another area for study in PID is whether or not a device with only K and no Na will degrade as quickly as the devices on soda-lime glass. In addition, the front-grounded PID stress configuration should be explored because it has also been identified as a cause of degradation in modules. Finally, the framework we have used for studying cell-level reliability and using it to solve module-level problems could be expanded to other solar cell technologies. This is by no means an exhaustive list, but there is certainly room for additional discoveries in the little-studied field of cell-level reliability.

Publications Resulting from This Work: Not all of the publications resulting from the project work were able to be referenced in the text. Those already referenced will appear again in the following references list. Some of the included references are collaborations between two SuNLaMP projects.

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