Thermal and Thermomechanical Modeling to Design a Gallium Oxide Power Electronics Package

Preprint

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Thermal and Thermomechanical Modeling to Design a Gallium Oxide Power Electronics Package

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Abstract— **There is significant interest in the power electronics industry in transitioning from silicon to wide-bandgap devices. Gallium oxide devices have the potential to offer comparable or even superior performance than other wide-bandgap devices, but at a much lower cost. Recent breakthroughs include demonstration of a laboratory-scale gallium oxide transistors and diodes; however, a functional power electronics package for these devices is yet to be developed. In this paper, the research methodology in designing an electronics package for gallium oxide devices is outlined. Finite element-based thermal and thermomechanical modeling simulations were conducted to realize a package design that meets the combined target of minimal thermal resistance and improved reliability. Different package designs that include various material combinations and cooling configurations were explored, and their thermal and thermomechanical performance are reported. Furthermore, the short-circuit withstanding capabilities of gallium oxide devices were studied and compared with silicon carbide.**

Keywords—gallium oxide; wide-bandgap devices; power electronics; high-temperature packaging; thermal modeling; thermomechanical modeling; finite-element

I. INTRODUCTION

Wide-bandgap devices are at the heart of a new paradigm shift in the power electronics industry that is motivated by demands of improved performance, higher efficiency, and higher power density. In large industry sectors such as automotive, aerospace, and the defense where power electronics devices and related packaging play a significant role in the power conversion and transmission process, silicon carbide (SiC) and gallium nitride (GaN) devices have become the frontrunners in replacing silicon devices [1]. Higher device temperatures can be an important enabler for compact, power-dense power electronics. Research efforts to develop compact, high-performance electronics packages that can support the high-temperature operation capabilities of SiC and GaN devices are ongoing. Compared to SiC and GaN devices, gallium oxide (Ga_2O_3) devices can offer the same and even superior electrical performance but at a much lower cost; however, this device technology and packaging are still at a nascent stage with significant challenges and questions due to the lower thermal conductivity of Ga_2O_3 as compared to SiC and GaN. While initial work [2] has been done on fabrication and characterization of Ga_2O_3 devices on a wafer, significant effort is still necessary towards all aspects of packaging the device—especially thermal, thermomechanical and reliability aspects—into a functioning power electronics module/component.

Power electronics packaging designs to utilize the full potential of wide-bandgap devices is currently a major research focus area in renewable energy and energy-efficiency applications. Ga_2O_3, being an ultra-wide-bandgap material, can operate as a device at temperatures higher than 200°C, thereby introducing challenges in the packaging design. In addition to efficiently dissipating heat from the device to the coolant, the package must reliably function at high temperatures without any catastrophic failure. Moreover, the electrical design of the package must be given due attention and needs to be executed together with the thermal and thermomechanical design. Current power electronics packages, particularly in energy-efficient electric vehicles, are rated for operation up to a maximum of 175°C even with the use of SiC devices. Novel design architectures are essential for enabling compact, power-dense, and reliable wide-bandgap device-based-packages that can sufficiently withstand higher operating temperatures. In this paper, the thermal and thermomechanical modeling efforts at the National Renewable Energy Laboratory (NREL), in collaboration with the Georgia Institute of Technology (Georgia Tech), in designing a robust, reliable power electronics package for mounting and operating Ga_2O_3 devices are described. Thermal and thermomechanical modeling simulations were conducted using select materials for each component layer of the package and are described in the following sections. Additionally, the short-circuit withstanding capability of Ga_2O_3 devices were investigated through modeling and compared with other wide-bandgap devices such as SiC.

II. PACKAGE DESIGN

A. Thermal Modeling

Steady-state finite element analyses (FEA) were conducted to compute the thermal performance impact of Ga_2O_3 devices. The FEA evaluated the effects of different cooling strategies and materials on the junction-to-coolant thermal resistance. The thermal performance of Ga_2O_3 power modules were then compared to the performance of Si and SiC modules under equivalent package and cooling configurations.

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Fig. 1 shows a computer-aided drawing model that consists of a 5×5×0.18-mm Ga_2O_3 device, direct-bond copper (DBC) substrate and baseplate. The extent of the model domain (dimension *l* in Fig. 1) represents one device and its associated packaging within a power module. In the model, the *l* dimension was varied from 6 to 25 mm and represent the spacing between the devices. Adiabatic boundary conditions were applied to the lateral sides of the packaging (DBC, baseplate) to mimic the model symmetry. The size of the Ga_2O_3 device was based on the dimensions of commercially available 1.2-kV SiC devices since there are no commercially ready Ga_2O_3 devices. Various DBC ceramics (aluminum nitride (AlN), alumina (Al_2O_3), and silicon nitride (Si_3N_4)) and baseplate materials (copper (Cu), aluminum (Al), and aluminum silicon-carbide (AlSiC)) were modeled to compute their effect on the thermal performance.

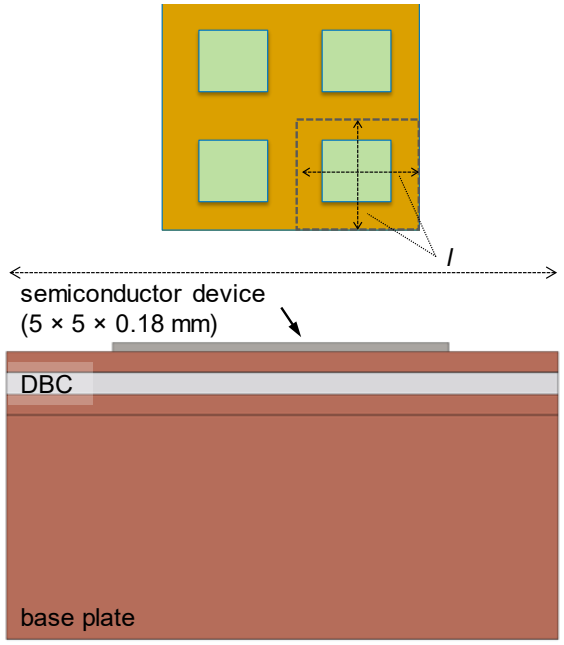

Fig. 1. Schematic of the power module model used in the FEA

The material properties and thickness dimensions used in the FEA were taken from various sources and are provided in Table I. Anisotropic and temperature-dependent thermal conductivity values taken from [3] were used for the Ga_2O_3 device. Temperature-dependent properties were also used for SiC, Si, Cu, and AlSiC. A thermal contact resistance of 2.3 mm^2-K/W was imposed on the baseplate-to-DBC and the device-to-metallization interfaces to simulate the bonding/adhesion layer (i.e., solder or sintered silver). Volumetric heat generation values were imposed on the semiconductor devices to simulate the heating effects. The semiconductor heat generation was adjusted so that the maximum junction temperatures reached 250°C for every case evaluated. The 250°C junction temperature condition is intended to simulate high-temperature operating conditions for wide-bandgap-based devices.

Convective cooling effects were simulated by applying heat transfer coefficient (HTC) boundary conditions on the cooled surfaces (e.g., baseplate, DBC, or device surface). The HTC values were varied to evaluate the effect of the convective cooling performance on the junction-to-coolant thermal resistance. A 65°C fluid temperature (T_f) was used for all cases.

The effects of three cooling configurations (baseplate-cooled, DBC-cooled, and device-cooled) on the thermal resistance was modeled. The baseplate-cooled configuration applies cooling to the bottom surface of the baseplate. The 2014 Honda Accord Hybrid [4] and 2015 BMWi3 [5] cool the power electronics devices using a baseplate-cooling strategy. In the DBC-cooled configuration, the baseplate is removed, and cooling was provided directly on the bottom surface of the DBC. In the device-cooled configuration, cooling was provided on the top side of the device and also on the exposed surfaces of the top metallization layer. The device-cooled case would require the use of a dielectric fluid because the fluid would be in contact with electrically active surfaces.

TABLE I. POWER MODULE MATERIAL PROPERTIES USED IN THERMAL FEA

Component	Material	Thickness (mm)	Thermal Conductivity (W/m-K)
Device	Ga_2O_3	0.18	anisotropic, temperature-dependent [3]
	SiC	0.18	temperature-dependent [6]
	Si	0.18	temperature-dependent [7]
DBC	Cu	0.3	temperature-dependent [7]
	Al_2O_3	0.38	24 [8]
	AlN	0.63	170 [8]
	Si_3N_4	0.32	90 [8]
Baseplate	Cu	3.25	temperature-dependent [7]
	Al	3.25	166 [9]
	AlSiC	3.25	temperature-dependent [10]

Fig. 2 compares the Ga_2O_3 junction-to-coolant thermal resistance of AlN, Al_2O_3, and Si_3N_4 ceramics for the baseplate- and DBC-cooled configurations. The junction-to-coolant thermal resistance ($R_{th,j\text{-}f}$) is defined according to Equation 1.

$$R_{th,j-f} = \frac{(T_{j,maximum} - T_f)}{Q_{device}} \quad (1)$$

where $T_{j,\,maximum}$ is the maximum junction temperature and Q is the heat output of the semiconductor device. Cu was the baseplate material used for the results shown in Fig. 2. The convective thermal resistance dominates at lower HTC values, and thus all cases provide nearly identical performance. As the HTC increases, package thermal resistance becomes more significant, and the variations in power module design begin to have a larger influence on the thermal performance. As expected, the DBC-cooled configuration has a lower thermal resistance as compared with the baseplate-cooled configuration. The use of Al_2O_3 ceramic provides the highest thermal resistance—a result of its lower thermal conductivity. AlN and Si_3N_4 ceramics are predicted to provide the lowest thermal resistance and have nearly identical performance. Tradeoffs between the thermal conductivity and thickness of AlN (higher thermal conductivity) and Si_3N_4 (thinner) are the reasons for their similar performance. These results indicate that the DBC-cooled configuration with either AlN or Si_3N_4 ceramic will offer the best thermal performance. Si_3N_4 may be the better option for high temperature operation based on its thermomechanical performance (see *Thermomechanical Modeling*). FEA simulations (baseplate-cooled) comparing the performance of Cu, Al, and AlSiC baseplates predicted similar thermal performance for AlSiC and Al. Cu baseplate was found to have the lowest thermal resistance—about 10% lower than AlSiC at an HTC of 10,000 W/m^2-K.

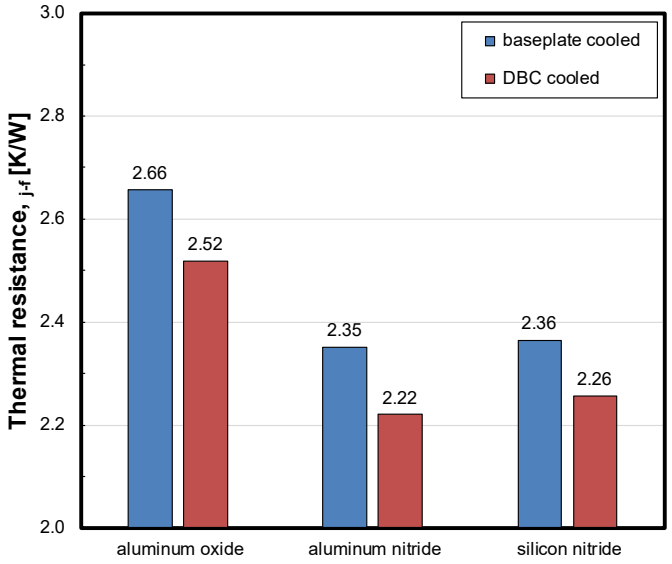

Fig. 2. Ga_2O_3 junction-to-coolant thermal resistance showing the effects of varying the ceramic material and cooling configuration.

The effect of cooling the power modules on both sides (double-side cooling) was also modeled, and the results were compared to the single-side cooled cases. Planar packaging of the Ga_2O_3 devices would enable double-side cooling and can be conducted for both the baseplate-cooled and DBC-cooled configurations. The 2013 Toyota Camry Hybrid [11] and 2016 Chevy Volt [12] use double-side cooled planar power modules. Fig. 3 compares the performance for the single- and double-side cooled modules with Ga_2O_3 devices. Cu baseplate and Si3N4 substrate were used to obtain the results shown in Fig. 3. Cooling both sides of the modules reduces the thermal resistance by about 50% as compared with the single-side case.

Directly cooling the semiconductor device (device cooling) using a dielectric fluid eliminates the thermal resistance associated with the packaging materials and can provide a higher thermal performance. The performance of this cooling strategy is shown by the device-cooled results in Fig. 3. As shown, the device-cooling configuration outperforms the DBC and baseplate single-side cooled cases. Compared with the DBC single-side cooled case, the device-cooled configuration reduces thermal resistance by about 14% and 50% at HTC values of 10,000 W/m^2-K and 100,000 W/m^2-K, respectively. At higher HTC values of >100,000 W/m^2-K (typical of two-phase cooling), the device cooling performance is comparable with double-side cooling strategies.

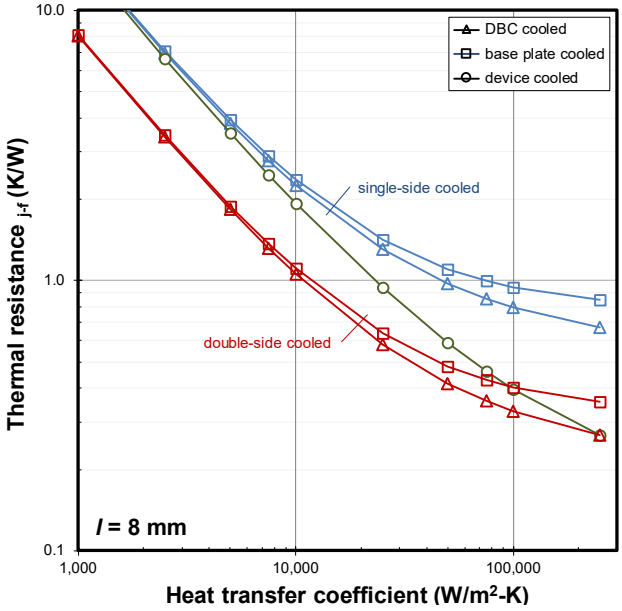

Fig. 3. Junction-to-coolant thermal resistance versus the HTC plot comparing different cooling strategies

Fig. 4 compares the thermal performance of Ga_2O_3, SiC, and Si semiconductor materials for the baseplate (single-side) and device-cooled configurations. The semiconductor materials were compared under equivalent cooling conditions and package configurations (materials and dimensions). Semiconductor dimensions of 5×5×0.18 mm was used for all cases, and the thermal conductivity was adjusted to represent the semiconductor material (e.g., Ga_2O_3, SiC, or Si) per Table I. In reality, heat generation within a device is not uniformly distributed, and the distribution may vary among the different semiconductor materials (due to different internal structure), which will affect the junction-to-coolant thermal resistance values. Moreover, the semiconductor dimensions may vary (e.g., different dimensions for the same voltage and current rating) for the different materials (Ga_2O_3, SiC, and Si) based on their electrical characteristics. However, a uniform heat distribution and equivalent device dimensions were used here because the internal structure of Ga_2O_3 is not known and to compare the effects of the semiconductor thermal conductivity on the package thermal resistance.

The FEA results predict that the use of Ga_2O_3 will result in an increase in the thermal resistance as compared with SiC and Si. The thermal resistance of Ga_2O_3 devices is predicted to be about 11% (baseplate-cooled case) and 4% (device-cooled case) higher than the thermal resistance of SiC when compared at an HTC of 10,000 W/m^2-K. At a higher HTC of 100,000 W/m^2-K, the thermal resistance of Ga_2O_3 is about 36% (baseplate-cooled case) and 31% (device-cooled case) higher as compared with SiC. The higher resistance of the Ga_2O_3 modules is associated with its low thermal conductivity (~11 W/m-K at 250°C). The lower thermal performance of Ga_2O_3 compared to other wide-bandgap materials, is not as significant considering its relatively low thermal conductivity. However, the computed thermal resistance values (and its performance relative to other wide-bandgap materials) will likely change if the detailed source, drain, and gate geometries are modeled. Si and SiC are predicted to have similar thermal performance because the thermal conductivities of the two semiconductors are nearly identical at 250°C junction temperature (see Table 1).

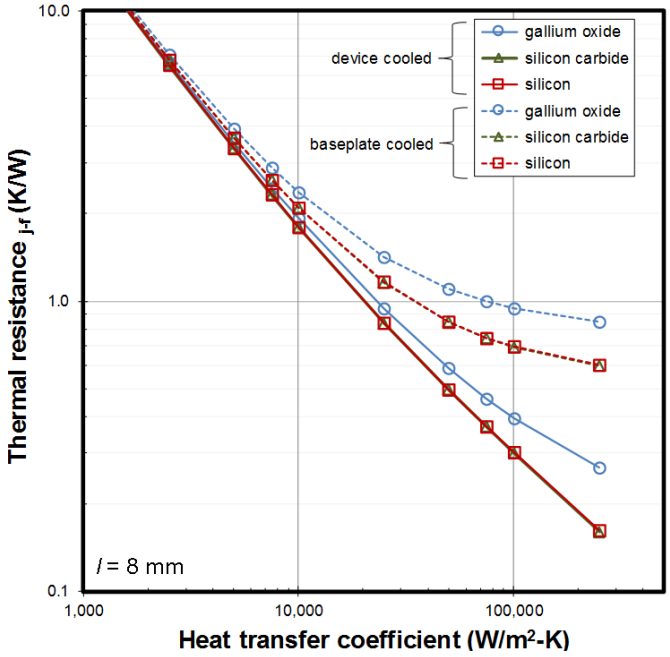

Fig. 4. Steady-state thermal FEA comparing the performance of Ga_2O_3, SiC, and Si semiconductor power modules

B. *Thermomechanical Design*

The objective of conducting different thermomechanical simulations in this study was to design a reliable power electronics package for mounting and operating Ga_2O_3 devices. As bonded interfaces such as die-attach and substrate-attach are considered as critical components within a package [13], the first step in this study was to realize a package that would ensure excellent reliability at these interface attachments. A few different materials were considered for each component layer and non-linear FEA were conducted to quantify their impact on stress and strain distribution at the die-attach and substrate-attach.

A traditional packaging design, as shown in Fig. 5, was chosen as the structural layout for conducting the FEA and is equivalent to the baseplate-cooled configuration in the thermal analysis. The footprint of the package was 50 x 50 mm^2. The thickness of the materials considered in this study match the values listed in Table I. Subsequent changes made to this model in optimizing the package design included removing the baseplate to replicate a DBC-cooled configuration. The quarter-symmetry of the model was utilized to reduce the computational time. Unlike in the thermal analysis, this model was sized to be representative of a commercially available power electronics package. This is important because the thermomechanical FEA results are size-dependent and could yield different conclusions between packages of significantly different footprints. In other words, the optimal selection of materials for a 10 x 10 mm^2 package may not result in the best performance for a 50 x 50 mm^2 package.

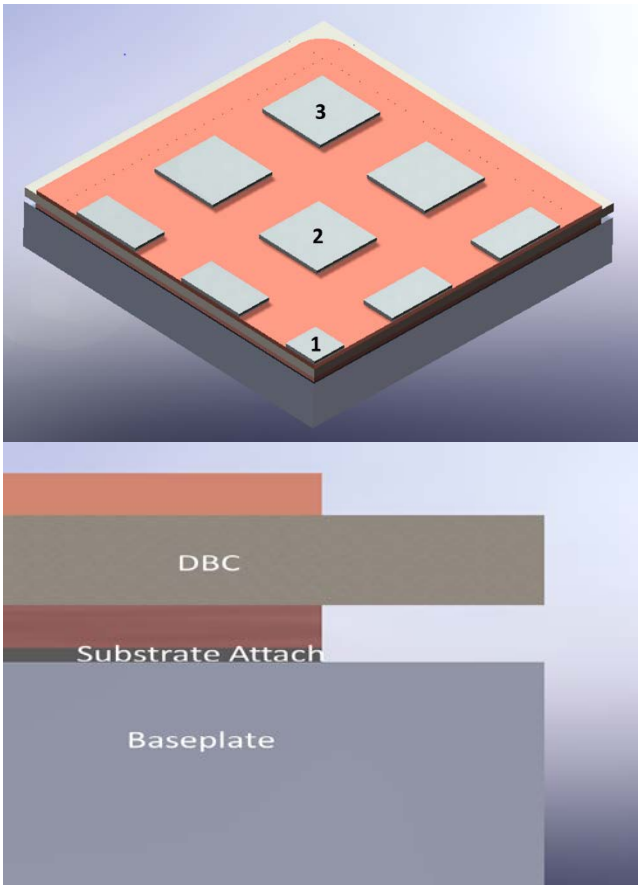

Fig. 5. Package design chosen for thermomechanical analysis (top), side-view of the package; devices and die-attach are not shown (bottom)

Multiple Ga_2O_3 devices were populated on the top to investigate the impact of location on the die-attach deformation behavior. Using this model, various materials commonly used in the power electronics industry were simulated for the different component layers such as baseplate and DBC. In all simulations, sintered silver and high-lead solder (95Pb5Sn) were selected as the die-attach and substrate-attach, respectively, as these materials are rated to operate at elevated temperatures. Anand viscoplasticity model [14] parameters obtained from the literature [15], [16] were given as inputs to define the deformation nature of die-attach and substrate attach layers,

while linear elastic material properties were applied to all other component layers. Temperature-dependent properties were used to the extent possible. Based on the data reported in [17], Ga_2O_3 devices were modeled to be anisotropic in nature. A thermal cycle of -40°C to 200°C with a ramp rate of 5°C/min and 10-min dwell at both extreme temperatures was applied as the loading condition.

Volume-averaged strain energy density values computed at the corner region of the substrate-attach and across the entire die-attach regions were obtained as the major outputs. In this study, the impact of each component material on the reliability of the package was determined based on these strain energy density outputs—the higher the strain energy density value, the less reliable the package. In other words, from a reliability perspective, the combination of materials that yields the lowest values of strain energy density at the substrate-attach and die-attach regions is preferred. It is to be noted that the conclusions obtained from the modeling study should be considered as design recommendations and any packaging engineer who chooses to rely on the material combinations presented in this paper for their package design should conduct experimental validation tests before constructing the package.

Multiple simulations with Cu and AlSiC as the baseplate and Si_3N_4, AlN, and Al_2O_3 as the ceramic were conducted; however, the results obtained with AlN as the ceramic were not included in this paper. While AlN ceramic is widely used in power electronics packages that are rated for operation up to 150°C, experiments conducted as part of another project at NREL revealed interfacial delamination between the AlN ceramic and the Cu metallization under a thermal cycle load of -40°C to 175°C. The inability of a DBC substrate with AlN as the ceramic to operate at high temperatures would not be captured by the thermomechanical FEA in this study as it focused on a package design based on die-attach and substrate-attach reliability. Hence, simulations with AlN ceramic would show comparable performance with other ceramics and including them in this paper would lead to inaccurate design recommendations.

a) Baseplate-Cooled Configuration: Fig. 6 shows the effect of different material combinations on the strain energy density values of substrate-attach layer. It is clear from the figure that the AlSiC baseplate offers a significant improvement over the Cu baseplates in substrate-attach reliability regardless of the ceramic material used. AlSiC has a coefficient of thermal expansion (CTE) of around 6 -7 ppm/°C and is highly compatible with the CTE of ceramic materials. However, the lowest value of strain energy density is obtained between AlSiC and Si_3N_4 despite the CTE mismatch in that combination being higher than when Al_2O_3 is used as the ceramic. A hypothesis for this trend is that in the event of a negligible CTE mismatch between the baseplate and the ceramic material, the substrate-attach may be more prone to the local CTE mismatch that exists between itself and the baseplate or the substrate metallization (Cu in this case). Additionally, the slightly thicker Al_2O_3 ceramic could be inducing larger stresses on the substrate-attach, leading to higher values of strain energy density than the Si_3N_4 ceramic. Experimental tests would need to be conducted to validate this assumption.

Strain energy results at the die-attach regions for the different material combinations simulated using the baseplate-cooled model configuration are presented in Fig. 7. Although the quarter-symmetric model had a total of nine die-attach regions, only the ones along the diagonal are shown here for clarity. The X-axis labels denote the baseplate used and the location of the die-attach, as shown in Fig. 5. AlSiC baseplate resulted in lower values of strain energy density than the Cu baseplate, but the difference is minimal and does not translate to a significant improvement in the reliability of the die-attach. This is because the reliability of the smaller die-attach is determined to a larger degree by the local CTE mismatch between itself the devices. The DBC substrate has a secondary effect on the die-attach reliability. Changing the baseplate material only serves to affect the global deformation behavior of the package and does not cause much of an impact at the die-attach level.

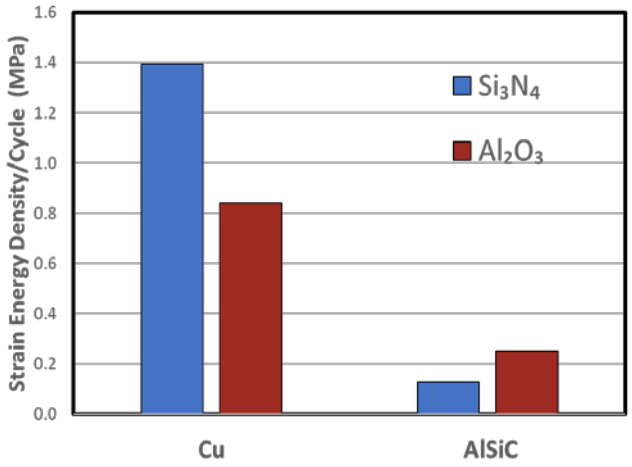

Fig. 6. Strain energy density per cycle values at the substrate-attach in the baseplate-cooled configuration

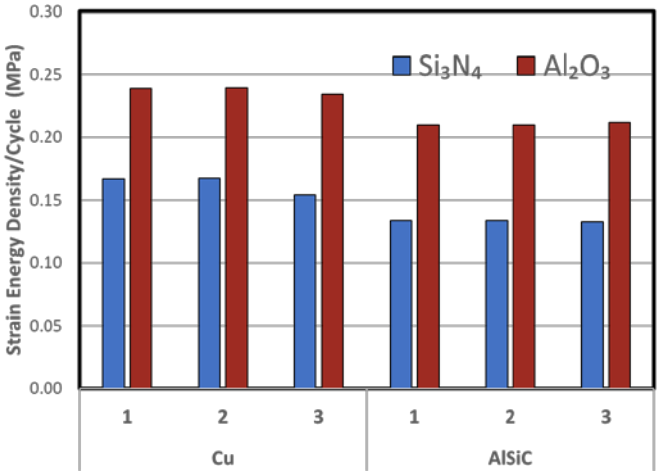

Fig. 7. Strain energy density per cycle values at the die-attach in the baseplate-cooled configuration

Among the different combinations modeled in the baseplate-cooled configuration, selecting AlSiC as the baseplate and Si_3N_4 as the substrate resulted in the lowest value of strain energy densities, both at the substrate-attach and die-attach. Thus, from a thermomechanical perspective, choosing AlSiC and Si_3N_4

should result in the longest lifetime of the package under harsh thermal cycling environments.

b) DBC-cooled Configuration: The model for the DBC-cooled configuration was obtained by removing the baseplate and the substrate-attach from the baseplate-cooled configuration. In this case, the DBC had a 0.5 mm-thick Cu metallization on its either ends. Simulations with Si_3N_4 and Al_2O_3 as ceramic material were conducted and the strain energy density results are plotted in Fig. 8.

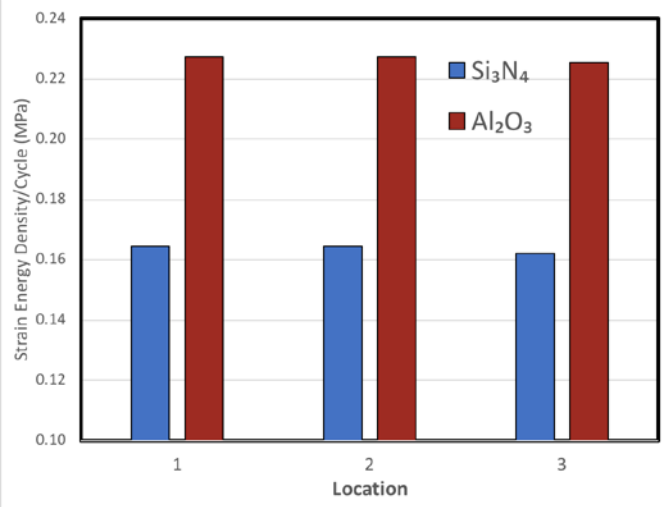

Fig. 8. Strain energy density per cycle values at the die-attach in the DBC-cooled configuration

Strain energy density results obtained at the die-attach in the DBC-cooled configuration follow a similar pattern as in the baseplate-cooled configuration. With the CTE mismatch between the devices and the die-attach remaining the same in all the cases plotted in Fig. 8, the DBC ceramic becomes the material of interest. The CTE of Si_3N_4 is closer to that of Ga_2O_3 than Al_2O_3 and results in lower values of strain energy density. Also, the similarity in the absolute values of results between Fig. 7 and Fig. 8 further elucidates the negligible impact the baseplate has on the die-attach reliability.

c) Comparison of Ga_2O_3 with SiC: The effect of changing the device material on the thermomechanical performance of substrate-attach and die-attach was investigated. In a baseplate-cooled configuration, the material properties of the devices at the top were changed to that of SiC but the dimensions were kept the same. SiC was modeled as an isotropic material. Predictably, no difference in the strain energy density results at the substrate-attach was observed. At the die-attach, strain energy density results were observed to be slightly lower than with Ga_2O_3 devices, with the local CTE mismatch being the dominant factor.

It is worth noting that the die-attach reliability with Ga_2O_3 and SiC devices was evaluated in this study under a thermal cyclic loading condition. In actual power electronics packages, failure at the die-attach occurs mainly due to the thermal transients that develop with the switching behavior of the device. As part of the future work, the heat dissipation data from Ga_2O_3 and SiC devices will be obtained from device models and incorporated into the thermomechanical FEA to study the deformation behavior of various die-attach materials.

C. Short-Circuit Modeling

Power semiconductor devices are prone to various failure mechanisms when operated in switching applications. Especially, when the operating conditions involve high instantaneous power levels at elevated junction temperatures, the device could be subjected to severe electrical, thermal, and mechanical stresses. The short-circuit withstanding capability of a power device is another useful parameter in determining its reliable and safe operation area and is particularly important for emerging wide-bandgap devices. When a large amount of heat is generated in the device active region under short-circuit conditions, an abrupt rise in junction temperature may lead to a permanent damage of the device. For evaluation of wide-bandgap device ruggedness, especially their ability to cope with thermal runaways from higher operating temperatures, short-circuit event simulations were performed for a vertical slice of SiC and Ga_2O_3 devices with 5-µm copper metallization at the top and horizontal surface dimensions of 10 x 10 μm^2 (Fig. 9).

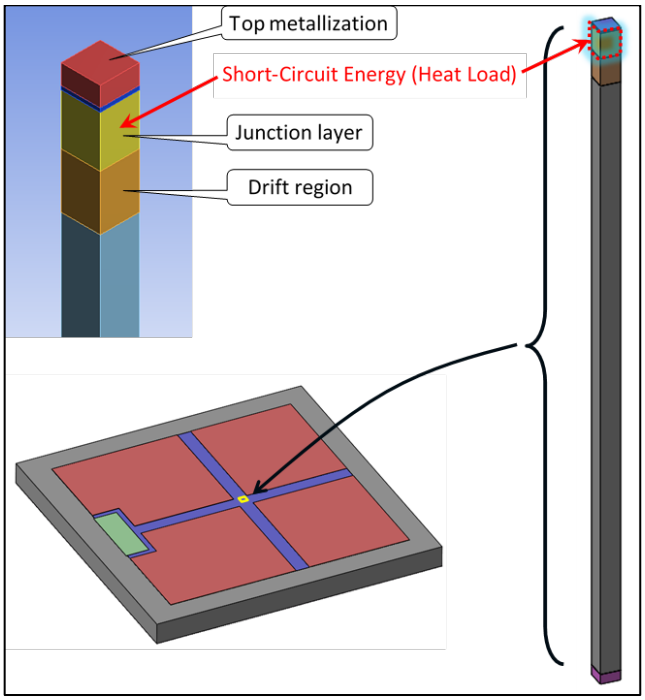

Fig. 9. Vertical slice of a power device used for short-circuit modeling FEA

The parameters that significantly affect the device behavior under short-circuit conditions are thermal conductivity, initial operating temperature, surface heat transfer coefficient (cooling method), and heat absorption capacity of the semiconductor material. It is important to note that the metal contacts and bond wires must be able to sustain any mechanical or thermal stresses exerted by the device. If the device temperature surpasses the melting temperature of the metal contacts, the device could fail even if the semiconductor chip itself survives the temperature spike.

Due to the lack of availability of any short-circuit heat-generation and junction temperature data for Ga_2O_3 devices, the

estimated heat load from a high-power SiC MOSFET device was used to perform FEA for both devices. The transient temperature rise was recorded while applying short-circuit internal heat generation waveforms to the junction layer with the assumption of one-dimensional heat propagation in the vertical axis direction (Fig. 9). Simulations were conducted in ANSYS Workbench.

Various combinations of contact materials, cooling methods, and thermal properties of the semiconductor device regions were analyzed. Most commercial devices are rated for operation only up to 175°C junction temperature for steady state operation [18], but as Ga_2O_3 devices are expected to operate at higher junction temperatures, the initial device temperature was set to 250°C. The recommended short-circuit withstand time for Si devices is 10 µs [19]. Even though applied heat load was an approximation based on SiC power MOSFET short-circuit data and the times presented below may not reflect exact behavior of a real device, the simulations clearly illustrated similarities (initial temperature rise slopes) and differences (final temperatures) between SiC and Ga_2O_3 devices. FEA results showed that both SiC and Ga_2O_3 devices have much lower than 10-µs short-circuit withstand times. Analyzed scenarios yielded safe short-circuit withstand times only on the order of 2–3 µs (see Fig. 10). After about 2.7 µs, both device temperatures surpass melting temperature of aluminum (660°C), which indicates potential damage in case aluminum is used for contact fabrication. At about 5.2 µs, temperature of the Ga_2O_3 device reaches the melting point of copper (1084°C), which is another threshold for safe operation of the power device with copper top surface metallization and wire contacts.

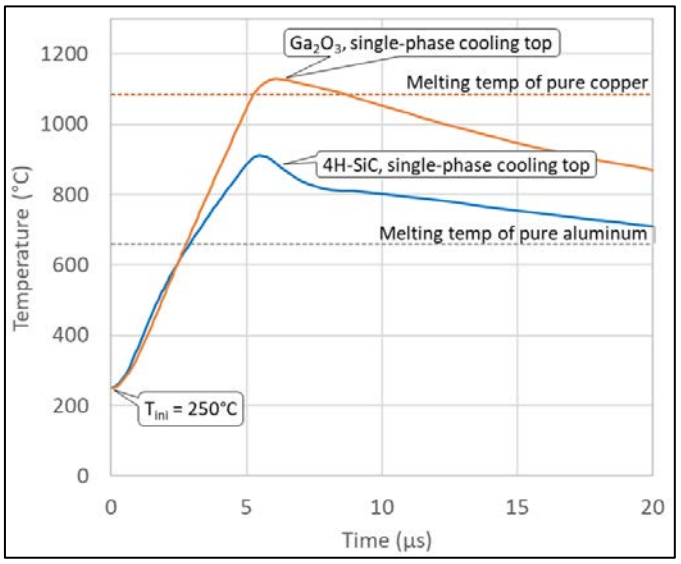

Fig. 10. Maximum temperatures in SiC and Ga_2O_3-based devices during 4.7-µs short-circuit event simulations.

As seen in Fig. 10, the lower thermal conductivity of the Ga_2O_3 material poses a challenge for proper heat dissipation from the device under short-circuit conditions.

III. Future Work

Thermal and thermomechanical modeling efforts to investigate additional package design variations are ongoing. Through FEA, the feasibility of compact, novel packaging architectures for mounting and operating Ga_2O_3 devices will be explored. The thermal performance of additional cooling strategies and package configurations will be evaluated and compared. In addition to die-attach and substrate-attach, substrate reliability aspects will be incorporated into the thermomechanical FEA. Simulations with plasticity models applied to the substrate metallization layers will be conducted. Another key focus area of thermomechanical FEA will be electrical interconnects and their design. Various interconnect strategies such as wire bonds, ribbon bonds, and flex foils for planar packaging will be studied. Thermal and thermomechanical modeling results will be combined to select the best package and cooling configuration. Computational fluid dynamics simulations will be run to design and optimize the heat exchanger for a Ga_2O_3-based power electronics package. Finally, the optimized package will be selected for fabrication to conduct experimental validation.

On the short-circuit modeling front, the actual short-circuit behavior of the Ga_2O_3 power semiconductor device will be used to evaluate the internal heat generation from the switching device under various conditions such as short-circuit or thermal cycling in power converter. It is expected that real Ga_2O_3 semiconductor devices will have lower thermal conductivity compared to SiC or GaN devices. Therefore, any device package consideration must also determine the best trade-off between the electrical behavior and the thermal behavior of the device. In no circumstances, the junction temperature of the device must exceed the maximum allowable temperature for the device/package system or the module/package system. If there is an abrupt rise in the junction temperature due to a short-circuit transient, the device must be able to withstand the sudden rise in the junction temperature for the short period of time that is enough for protective circuitry to react and shut down the power device.

The detailed electro-thermal behavior prediction of Ga_2O_3 devices through FEA using tools such as ANSYS or using compact electro-thermal modeling is currently being explored. The compact electro-thermal device model may be implemented in any Hardware Description Language (HDL) such as Verilog A or in the SPICE. The electro-thermal modeling will involve analyzing the heat generation and propagation within the device under various transient scenarios that can provide insights for a better package design. The optimized package design should ensure that the benefits of Ga_2O_3 devices are fully captured and possibly exceed the performance offered by other wide-bandgap or Si devices.

IV. Summary

In this paper, research efforts at NREL, in collaboration with Georgia Tech, to design a Ga_2O_3-based power electronics package are described. The design framework is oriented towards enabling the package to operate at elevated temperatures that are typical of wide-bandgap devices. Through thermal and thermomechanical FEA, various material combinations and cooling strategies were explored for their effectiveness in offering optimal thermal performance and improved reliability.

In general, aggressive cooling strategies such as device cooling and DBC cooling exhibited lower values of package thermal resistance than conventional baseplate-cooled configurations. Also, the potential of double-sided cooled packages in lowering the thermal resistance even further than single-sided cooled packages was demonstrated. A comparative analysis of equivalent package designs with different device materials revealed that novel packaging architectures would be required for Ga_2O_3 devices to offer similar thermal performance as SiC and Si devices. The lower thermal conductivity of Ga_2O_3 device is a limiting factor and needs to be compensated with innovations in the package design.

Among the different baseplate and ceramic materials considered for packaging, thermomechanical FEA predicted the combination of AlSiC and Si_3N_4 to be the most beneficial for substrate-attach reliability. The CTE of AlSiC is highly compatible with that of DBC ceramics and resulted in significantly lower values of strain energy density than Cu baseplates. Die-attach reliability was found to be dictated to a greater extent by the local CTE mismatch between itself and the devices or DBC. For a given package design, replacing Ga_2O_3 devices with SiC devices resulted in improved reliability at the die-attach.

The short-circuit withstanding capabilities of Ga_2O_3 devices were investigated and compared with SiC devices. In the event of a short-circuit scenario such as a thermal runaway, the safe withstand times for Ga_2O_3 and SiC devices were found to be in the range of 2–3 µs, which is much lower than the recommended time of 10 µs for Si devices.

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