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Alessandro Cavalli, Steve Johnston, Dana Sulas, John Simon, Kevin L. Schulte, David L. Young, and Aaron J. Ptak
National Renewable Energy Laboratory

Brett Ley and Corinne E. Packard
Colorado School of Mines

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GaAs Solar Cells Grown on Unpolished, Spalled Ge Substrates

Alessandro Cavalli[1], Brett Ley[2], Steve Johnston[1], Dana Sulas[1], John Simon[1], Kevin L. Schulte[1], Corinne E. Packard[1, 2], David L. Young[1], and Aaron J. Ptak[1]

[1]National Renewable Energy Laboratory, Golden, Colorado, 80401, USA
[2]Colorado School of Mines, Golden, Colorado, 80401, USA

***Abstract* — We spalled 2-inch Ge wafers using a Ni stressor layer and grew GaAs solar cells by hydride vapor phase epitaxy on the spalled Ge surface without other surface treatments. The controlled spalling procedure leaves behind arrest lines, which are parallel surface striations, perpendicular to the crack front, caused by the crack propagation repeatedly halting and restarting during the fracture. We show that small arrest lines do not significantly affect device performance, but larger lines act as regions for carrier recombination. We demonstrate a 12.8% efficient single-junction device, without anti-reflection coating, grown on a spalled surface containing arrest lines. The quantum efficiency of this device is similar to devices grown on non-spalled GaAs and Ge substrates.**

I. Introduction

III-V solar cells have demonstrated the highest efficiency of any photovoltaic device to date, but high costs have restrained their applications to niche markets consisting mainly of space power systems [1]. A major portion of the price is the deposition cost, which can potentially be lowered using hydride vapor phase epitaxy (HVPE) [2], [3], a technique that has demonstrated single-junction GaAs solar cell efficiencies > 25% [4]. However, the cost of the single-crystal substrate used for device growth remains very high. One possible path to reduce substrate-related costs is to use epitaxial liftoff using controlled spalling [1], [5]. Spalling uses a stressor layer deposited on a substrate, so that when a crack is initiated it propagates parallel to the surface, allowing for device exfoliation. This process takes less than a second to occur, can be integrated in a straightforward manner in fabrication lines, and has been shown to work well with Ge (100) wafers [6]. The spalling approach, compared to traditional chemical epitaxial lift-off [7], potentially has higher throughput and scalability, and thus can be a feasible process in large scale manufacturing of photovoltaic devices. However, spalling does leave behind arrest lines. Arrest lines are morphological features on spalled surfaces that consist of localized roughness that deviates above and below the average spall depth plane, with micrometer-scale depth and width[8], [9]. Between arrest lines, the RMS roughness of spalled Ge wafers is comparable to that of pristine Ge wafers[8]. Arrest lines form as fracture stops and restarts, propagating discontinuously, during controlled spalling. The orientation of the arrest lines is not a result of crystallography; it aligns perpendicular to the crack propagation direction[8], [9]. In this work, devices are grown on the as-spalled surface without any further alterations to surface quality. Devices are large enough to sample a large number of arrest lines of differing size [8], [9].

Chemo-mechanical polishing (CMP) could be used to remove these features before growth, but current price predictions indicate that this is cost-prohibitive for the use of III-V devices in much larger markets than where they exist today. In fact, CMP may account for $8-16 per reuse [1]. We showed previously that we can successfully grow devices on spalled surfaces without using a CMP step [10], but the effect of arrest lines on device performance is currently unknown. Therefore, here we investigate the growth of GaAs solar cells on spalled Ge surfaces, without additional processing or polishing, to study the impact of the unpolished surface on device performance.

II. Experimental Methods

The first step to obtain a spalled surface is to clean a 2-inch diameter (100)-oriented Ge substrate [p-type doped, 6° offcut toward the (111) plane] for one minute, using a 2:1:10 volumetric solution of NH_4OH:H_2O_2:H_2O. For this experiment, a nickel stressor layer was electroplated in a solution consisting of 0.6 M $NiCl_2 \cdot 6H_2O$ and 5.0 mM H_3PO_3, on the polished surface of the wafer using a circular jig with front contacts and plating diameter of 4.36 cm (1.71 inch). The bath was heated to 60 ºC with continuous filtration and agitation applied during deposition [8]. The plating time and current density were t = 2.75 min and J = 80 mA/cm^2, respectively. The sample underwent a 3-min post-plating etch step in a freshly made 2:1:10 solution [10]. We initiated the controlled spall using a mechanized roller and Kapton tape that acted as a handle for the spalled film [11]. The spalled wafer, after film exfoliation, was cleaned using agitated Transene TFG etchant to remove any possible traces of Nickel, then loaded directly into the growth reactor for III-V epitaxy without further surface processing. A control sample was grown on a standard non-spalled, epi-ready Ge wafer. In the control sample, the only difference was the addition of a small amount of In in the GaAs layers to improve the lattice match to Ge. Results from a GaAs device grown on a GaAs substrate are also included in certain figures for reference and represent our target efficiency.

Fig. 1 shows the device structure used in this work. Growth was conducted at 650 °C in a custom-designed dual chamber Dynamic HVPE (D-HVPE) reactor [3], [12], [13]. Hydrogen selenide and diethylzinc were used as the n- and p-type dopant precursors, respectively. A 1 μm-thick GaAs buffer layer was

grown first on the substrate, followed by a 300 nm thick GaInP stop-etch layer. These two layers were followed by an inverted GaAs rear heterojunction solar cell, grown at a rate of ~ 1.1 μm/min, that uses GaInP cladding layers. The samples were processed following a procedure similar to the one described previously in Ref. [14]. The only substantial difference is the use of an $HF:H_2O_2:H_2O$ 1:1:2 solution for the etching of the Ge substrates. The III-V layer grown on the rough spalled Ge has a morphology that follows the undulations of the substrate, so that a planar view of the top of the sample reveals the presence of ridges and undulations. As a result of the sample inversion during the device fabrication, though, the arrest lines that were imprinted as ridges in the III-V layers are now imaged as depressions. No anti-reflection coatings (ARC) were deposited on the samples presented here. The cell size was 0.25 cm^2. The quantum efficiency (QE) and specular reflectance measurements were obtained via a custom-built QE setup, while the current density-voltage (*J-V*) performance was measured on an XT10 solar simulator, calibrated to simulate the AM1.5G spectrum at 1000 W/m^2. The dark lock-in thermography (DLIT), photoluminescence (PL), and electroluminescence (EL) were performed in a custom-built setup previously described, using a 532nm laser diode and RG750 long-pass filters for PL imaging [15].

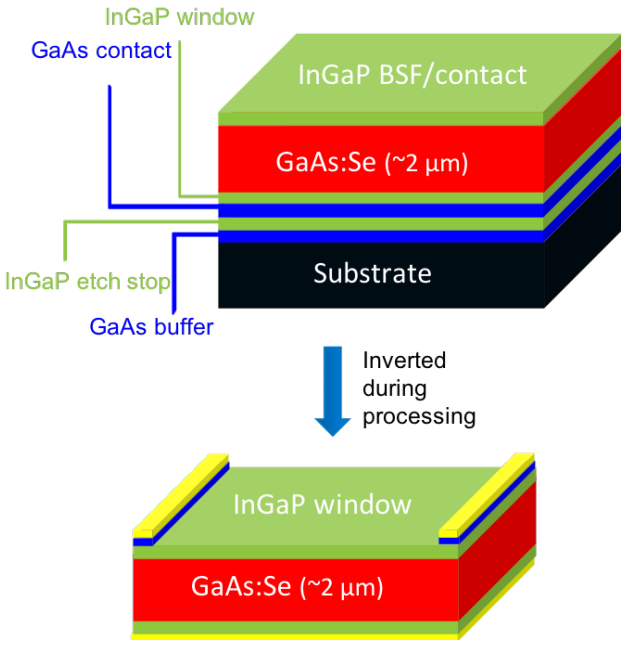

Figure 1. Device schematic of the rear heterojunction GaAs solar cells (layer thicknesses not to scale).

III. Results and Discussion

In this manuscript, we consider the performance of three samples, all rear heterojunction solar cells, made of similar materials grown on different substrates to understand the achievable quality and limitations of growth on the unprocessed spalled material. The three samples were: GaAs (E_g=1.41 eV), grown on unpolished spalled Ge (sp-Ge); $In_{0.016}Ga_{0.984}As$ (E_g=1.39 eV) grown on standard epi-ready bulk Ge (epi-Ge); and GaAs grown on epi-ready GaAs (epi-GaAs). Fig. 2a shows the internal QE (IQE) of the three samples. The IQE of the sample on epi-Ge is very similar to the best GaAs cells grown by HVPE on epi-GaAs, as expected. There is some degradation, indicating that the carrier collection efficiency for devices grown on epi-Ge is slightly lower than for homoepitaxial growth of GaAs. The sample on sp-Ge exhibits a lower IQE, indicating a lower minority carrier diffusion length.

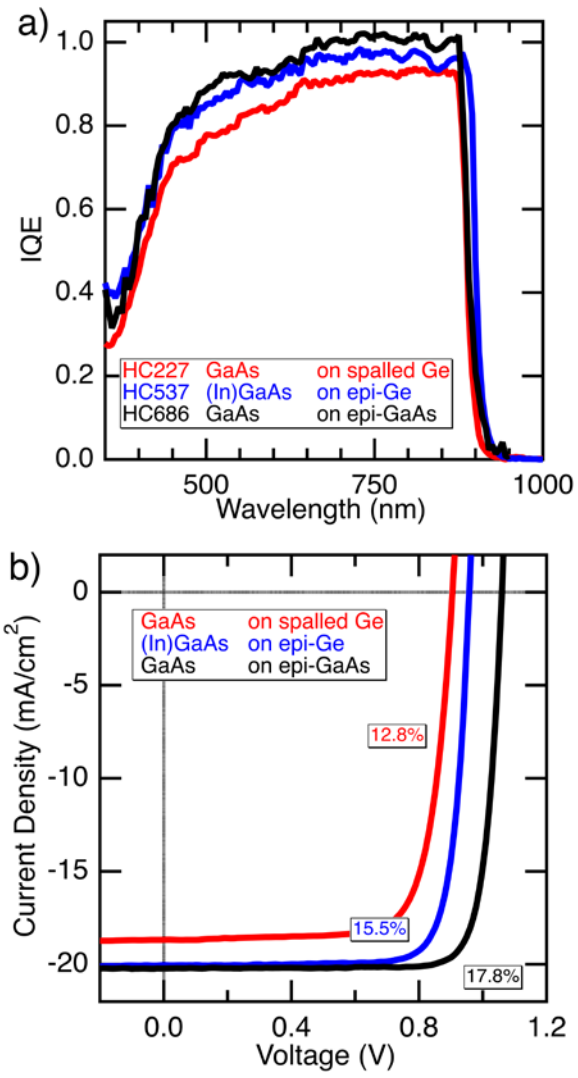

Figure 2. (a) Internal QE measurements of a GaAs rear heterojunction solar cell grown on a spalled Ge wafer. The IQE of a reference (In)GaAs cell grown on an epi-ready Germanium wafer, as well as a GaAs cell grown on GaAs, are included for comparison. (b) *J-V* measurement of the cells grown on spalled Ge, on bulk Ge, and on bulk GaAs, highlighting the relatively high short-circuit current and the limited V_{OC} on sp-Ge. The conversion efficiencies (without ARC) are listed in the figure for each device.

Fig. 2b shows the *J-V* characteristics under a simulated AM1.5G 1-sun spectrum of all three samples tested. The short

circuit current density (J_{sc}) is 18.7 mA/cm^2 for the sp-Ge sample, equivalent to that expected from integrating the EQE measurements with the AM1.5G solar spectrum. The J_{sc} values of the epi-Ge and epi-GaAs devices are somewhat higher, slightly exceeding 20 mA/cm^2. The J_{sc}, open circuit voltage (V_{oc}), fill factor (FF), and the efficiency of the devices are presented in Table 1. The efficiency expected once a good ARC is deposited is also included. For ideal materials, we would expect a slightly higher current (~0.75 mA/cm^2) in the device on epi-Ge than the epi-GaAs device, due to the slightly lower bandgap. The measured J_{sc} is negligibly different between these two, however, which is consistent with the lower IQE measured. While not as high as solar cells grown on epi-GaAs, the level of performance on epi-Ge provides a sufficient baseline for comparison with the sp-Ge device.

Table 1. Comparison of the performance of the solar cells grown on sp-Ge, epi-Ge, and epi-GaAs.

Substrate	J_{sc} (mA/cm^2)	FF	V_{oc} (V)	η (%)	η_{ARC} (%)
sp-Ge	18.7	0.76	0.90	12.8	18.0
epi-Ge	20.0	0.81	0.96	15.5	21.8
epi-GaAs	20.2	0.83	1.07	17.8	25.0

Clearly, the performance of the device on sp-Ge is lower than the control devices. We can probe the causes that limit the efficiency in more detail by investigating the dark *J-V* characteristics of the devices. Fig. 3 shows that while all cells are dominated by a J_{02} characteristic current density, the dark current of the sp-Ge device is clearly higher than the others, limiting the performance of the device at 1-sun illumination. An increase of J_{02} current density is correlated with a decrease in V_{oc} and is typically a result of non-radiative recombination that happens at material impurities, structural defects such as dislocations generated by stress relaxation, or defects due to processing damage.

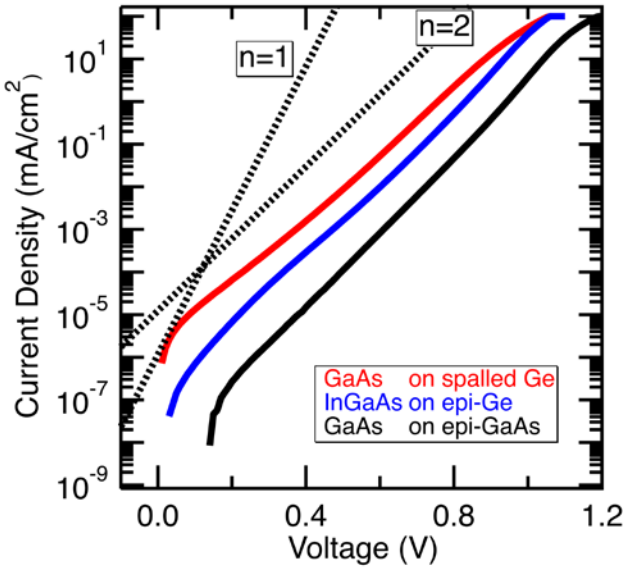

Figure 3. Dark *J-V* characteristics of GaAs heterojunctions grown on a spalled Ge wafer, as well as of (In)GaAs on epi-Ge and GaAs on epi-GaAs, plotted on a semi-logarithmic scale, highlighting the J_{02}-limited performance of all the cells. The dashed lines represent the expected slopes for diodes with n=1 and n=2 ideality factors and are presented as a guide to the eye.

To discover the causes for the high dark current, we performed forward and reverse-bias DLIT. DLIT spatially images shunts, processing damage, and resistive regions by measuring the heat dissipated through carrier recombination and resistive current flow. Lock-in amplification allows high-sensitivity detection of weak heat signatures by pulsing the current at a given frequency, although the spatial resolution (and thus the ability to detect defect morphology) is limited when the current modulation frequency becomes slower than heat diffusion [15]. Nevertheless, we identify several defect regions using DLIT. Comparing the forward and reverse-bias images of a 5 mm x 5 mm device on sp-Ge (Fig. 4a and 4b) allows us to determine the defect character. In forward bias, we observe two prominent heat signatures at the corners of the device (Fig. 4a), but these defects do not heat up in the reverse-bias measurement (Fig. 4b). We therefore conclude that these defects are not ohmic shunts but are more probably regions of higher recombination. These lines are related to the presence of wide (20-50 μm width, 1-5 μm depth) arrest lines caused by the spalling procedure [8]. In the same sample, we additionally identify many smaller spots that appear to be similar to heat signatures in samples grown on epi-Ge (Fig. 4c-d). Although these spots are less numerous on epi-Ge, we can conclude that these are not defects specific to devices grown on spalled substrates.

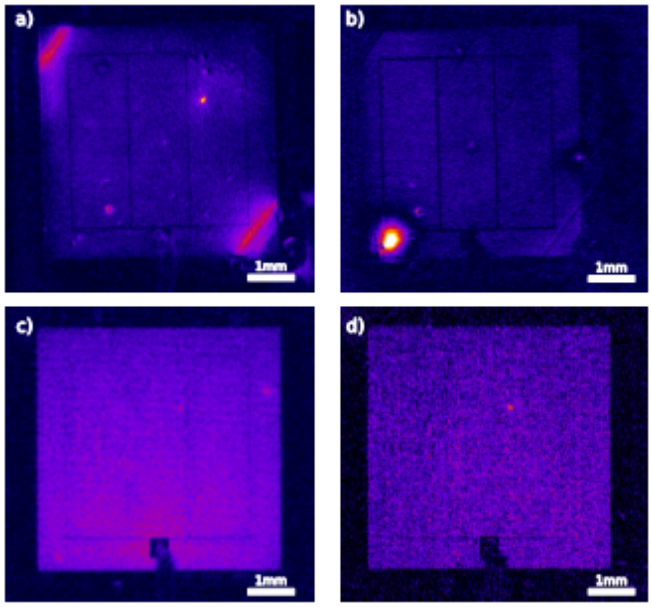

Figure 4. DLIT of solar cell devices, on sp-Ge in forward (a) and reverse (b) bias, and on epi-Ge in forward (c) and reverse (d) bias.

To further investigate these defects, we performed EL and PL on the same device on sp-Ge that was shown in Fig. 4a-b. Fig. 5a shows the EL measurement of this device. The weak EL in the device corners that are separated by the arrest lines seems to suggest a problem with electrical connectivity that prevents current injection into these corners. The PL signature (see Fig.

5b) is roughly constant in intensity across the sample, even in the corners, suggesting that the material separated from the rest of the device by the arrest lines is still in good condition. It is thus possible that the large arrest lines act as carrier recombination centres, lowering the V_{oc} and reducing the J_{sc}. We additionally observe several smaller (<5 μm width, <200 nm depth) spalling arrest lines with correlated intensity variations in both the EL and PL images, which may suggest that the arrest lines act as recombination centres, thus increasing the dark current in the device. However, because these lines do not heat up during DLIT measurements, it is also possible that the variation in morphology can result in a different directionality of emission, such that the luminescence collection efficiency varies across the rough surface.

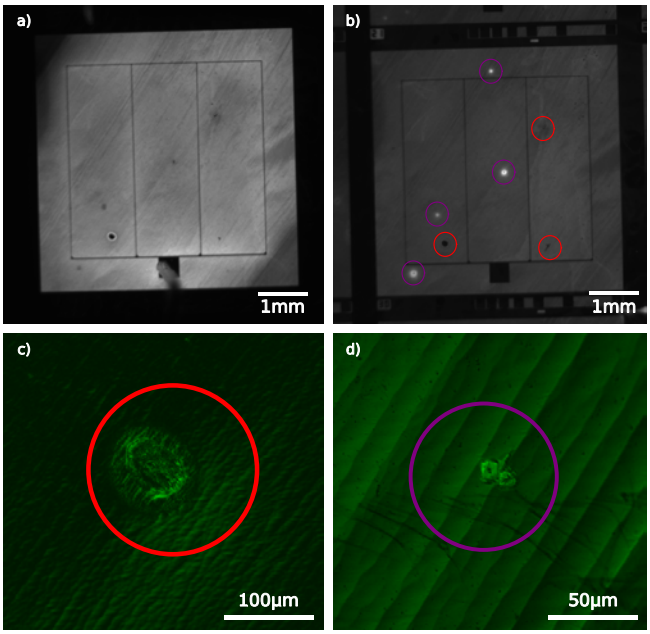

Figure 5. EL (a), PL (b), and false-colour Nomarski microscopy on sp-Ge (c-d), for the identification of different kinds of defects such as shunts and pin-holes.

The PL measurement shown in Fig. 5b highlights two additional kinds of defect spots (both bright and dark), which all appear dark in the EL image. We find that the defect spots that are dark in both PL and EL images dissipate heat in both forward and reverse-bias DLIT, and we attribute these defects to local shunts that heat up under current flow. In Fig. 5c, we show that these defects have irregular shapes, which are either due to a particle deposited before or during the growth procedure, or generated during the device processing. Bright defects in PL, instead, are related to pin-holes caused by the device processing (Fig. 5d), in which the back-gold metal contact layer is exposed when the active layer above is removed by chemical wet etching. The metal then reflects the PL laser light, which is thus collected by the detector. These two kinds of defects are not specific to sp-Ge samples, because they are found on epi-Ge and epi-GaAs samples as well, suggesting that they are not caused by the unpolished surface of the substrate.

IV. Conclusion

We demonstrate a GaAs heterojunction solar cell grown on an unpolished, spalled Ge substrate, with an efficiency of 12.8% without an ARC. The IQE is somewhat degraded compared to typical GaAs solar cells grown by HVPE on GaAs, and the FF and the V_{OC} must be improved substantially to achieve high efficiency. We explain the limited performance as a result of the presence of large arrest lines observed by PL, EL and DLIT. Shallow arrest lines do not seem to have a significant effect on performance, but deep arrest lines cause non-radiative recombination centres, as well as introduce disconnected regions that prevent carrier collection. However, the performance of solar cells grown on epi-Ge is still not as high as on epi-GaAs, suggesting that there are further issues with growth on Ge in general. Additional measurements such as cathodoluminescence, atomic force microscopy, and transmission electron microscopy, are thus still necessary to find out if nucleation and growth on Ge is optimized. Nevertheless, these results show that CMP may not be required after controlled spalling to achieve acceptable performance: with a better control of the spalling process to eliminate deep arrest lines, the combination of HVPE growth and spalling could grant a path to III-V cost reduction.

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