Validating the Test Procedures Described in UL 1741 SA and IEEE P1547.1

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Validating the test procedures described in UL 1741 SA and IEEE P1547.1

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***Abstract*— This paper investigates the test procedures specified in UL 1741 SA and the upcoming revision to IEEE P1547.1. A 550 kVA photovoltaic inverter was chosen for the tests. This research reveals some of the key components to consider while doing certification tests for UL 1741 SA and IEEE P1547.1. This paper also identifies some issues requiring consideration for future releases of the standard, i.e. IEEE P1547.1.**

Keywords—Inverter testing, UL 1741 SA, IEEE 1547.1, Photovoltaics

INTRODUCTION

The IEEE Standard 1547 [1] is the primary document providing requirements for interconnecting distributed energy resources (DERs) such as photovoltaic (PV) systems to the power system. In 2005, IEEE 1547.1 [2] was published containing test procedures to verify the conformance of DERs with interconnection requirement in IEEE 1547. Since the first publication of IEEE 1547 in 2003, a lot has changed in the distributed generation area, e.g. DER penetration levels and operation and control functionalities, requiring a full revision of the standard [3], which was published on April 6, 2018 [4]. Especially in recent years the percentage of DER generation in the grid has reached the point in many U.S. states, e.g. Hawaii and California, where safe and reliable operation of the grid demands the active participation of DERs in terms of grid support functions [5]. To manage very high levels of PV in California, the Public Utilities Commission modified its Rule 21 tariff which requires DERs to participate in grid support functions in abnormal situations in order to stabilize the grid [6]. This led to an amendment to the Underwriters Laboratories (UL) 1741 inverter certification standard [7], which accommodates not only the new requirements of Rule 21 but also other documents specifying interconnection requirements, known as Source Requirements Documents (SRDs). The amendment, known as UL 1741 Supplement A (SA), published in September 2016, can be seen as stop-gap until adoption and completion of the more inclusive IEEE 1547-2018 and subsequent IEEE P1547.1 revisions.

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Ideally these standards should facilitate easy integration of DERs into the grid instead of creating roadblocks, while ensuring that grid operator needs are met. Keeping this idea in mind, it is prudent to examine the recently-published UL 1741 SA and upcoming IEEE P1547.1 for any issues that might arise in certification tests. The National Renewable Energy Laboratory (NREL) with the sponsorship of Department of Energy (DOE) Solar Energy Technologies Office took the initiative to evaluate the UL 1741 SA and IEEE P1547.1 test procedures in NREL's Energy Systems Integration Facility (ESIF). The lessons learned from testing the test procedures are used as feedback for the IEEE P1547.1 Working Group.

A utility scale 550 kVA inverter was used at NREL to examine the testing procedures of UL 1741 SA and IEEE P1547.1. Evaluation of conformance test procedures focused on tests most likely to be problematic specifically for large-scale DERs, such as ride-through tests, which require very high power and voltage slew rates. This paper presents selected findings resulting from this effort.

TEST PROCEDURE VALIDATION

In order to ensure that the conformance test procedures can be applied to different classes of inverters, the NREL team began evaluation of key conformance tests against a large commercial inverter to complement the previous testing done on the smaller micro, residential and small commercial inverters. It is important to note that the inverter under test was manufactured in 2014, prior to the publication of UL 1741 SA (and well before the current IEEE P1547 draft was developed). NREL engineers installed updated inverter control firmware that provided improved functionality for grid support functions. However, neither the inverter nor the firmware was certified to UL 1741 SA. Therefore, any tests that the inverter "failed" should not be taken to reflect poorly on the inverter, nor should they be taken to reflect poorly on the test procedure necessarily. The objective here was to evaluate the test procedures themselves, not to test the inverter compliance.

A. Test equipment and setup

Figure 1 shows the test setup developed for this project.

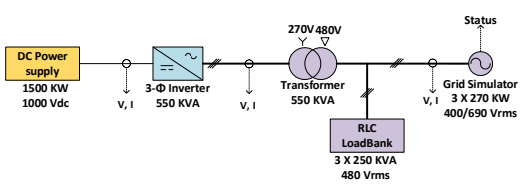

Figure 1:Test setup

All the equipment shown in this setup are located at different locations in ESIF at NREL.A list of testing procedures validated is shown in Table I.

TABLE 1: GRID INTERCONNECTION FUNCTIONS TESTED AT NREL

Main function	Document
Voltage ride through (VRT)	UL 1741 SA
Frequency ride through (FRT)	UL 1741 SA
Anti-islanding (AI) with advanced grid functions, i.e., frequency-watt (F-W), volt-var (V-Var), specified power factor (SPF), VRT, FRT	Draft IEEE P1547.1
V-Var	UL 1741 SA
F-W including time response	UL 1741 SA and Draft IEEE P1547.1

B. *Voltage ride-through (VRT)*

The inverter was programmed to ride through voltage excursions encompassing several VRT operating regions defined in California Rule 21. Two tests were performed for each operating region; in one test, the change in voltage was applied to all three phases simultaneously, and in another test the change in voltage was applied on phase A only. The dwell time between voltage excursions is supposed to be provided by the manufacturer per UL 1741 SA; however, as the inverter used in this test was manufactured before the publication of UL 1741 SA, this information was not available. For the preliminary test, the value of dwell time was assumed as 1 second. The manufacturer's stated accuracy (MSA) of voltage was taken into consideration as prescribed by UL 1741 SA. To allow the test to be run with 540 kVA of supply (grid simulator), a load bank was connected in parallel with the inverter. Figure 2 shows the inverter output for the test voltage applied on three phases simultaneously.

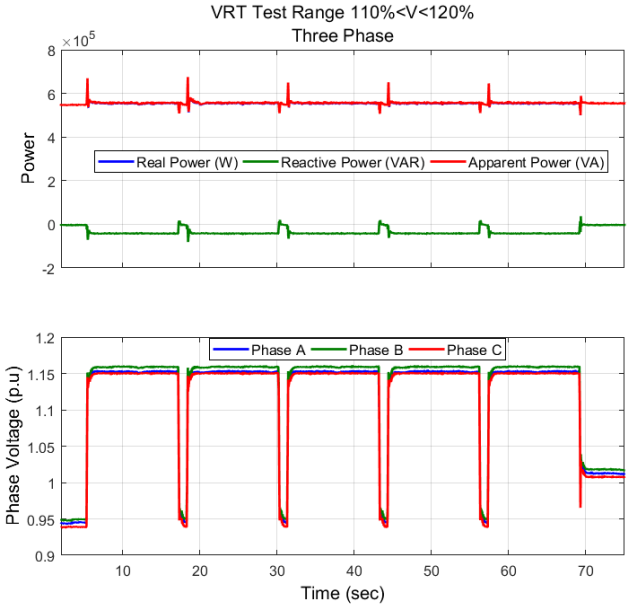

Figure 2: Voltage ride-through test in the operating region of 110%<V<120% with test voltage applied on all three phases simultaneously

Lessons learned from VRT tests

- In general, the VRT tests performed as expected. However, the grid simulator tripped for some low voltage ride through (LVRT) tests when the voltage returned from low to high. Figure 3 shows the grid simulator tripping behavior. LVRT tests were performed four times keeping all the parameters same. The grid simulator trips at different times of the pulse train. The cause of the intermittent grid simulator tripping is not known, but may be related to saturation of the grid simulator's internal output transformer due to residual magnetic flux.

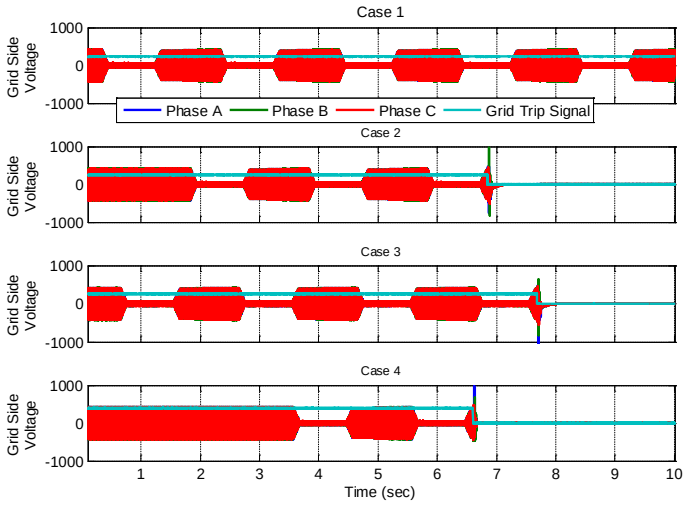

Figure 3: Intermittent tripping of grid simulator during LVRT recovery

C. *Frequency ride-through (FRT)*

The FRT test procedures described in UL 1741 SA were tested for combinations of different frequency rise- and fall-time slopes and power levels for all the high and low frequency ranges specified in UL 1741 Table SA8.4 considering MSA of frequency. Each region was tested with two different slopes for rise time and fall time of frequency, 1 Hz/s and 3 Hz/s, and two different power levels, 100% and 20% of nominal power. Dwell time of 1 second between frequency events was assumed.

Lessons learned from FRT tests

- The FRT testing procedure of UL 1741 SA assumes rectangular FRT requirements. No testing method has been provided for SRDs having a non-rectangular testing region. However, most FRT requirements that apply to DERs (including the IEEE 1547-2018 requirement) are rectangular, so this may not be a major issue.

D. *Anti-islanding (AI) with grid support functions*

The unintentional islanding test procedure specified by section 5.7.1 of draft 3 of IEEE P1547.1 was used with the test conditions specified in Table 2. The historical islanding test procedure in IEEE 1547.1-2005 requires the test be re-run many times with minor variations in load tuning to ensure that at least one run uses a load that is well-balanced, creating a very difficult condition for island detection. The proposed new test procedure allows the total number of tests to be reduced while increasing confidence in the results by using the following generalized test sequence:

1. Disable the inverter's AI controls and confirm that a stable island can be created.

2. Using the same island load tuning verified in step 1, re-enable anti-islanding controls and confirm that the inverter detects the island.

If a stable island cannot be created in step 1, the test must be repeated many times, as in 1547.1-2005.

TABLE 2: : INVERTER GRID SUPPORT FUNCTIONS FOR AI TESTS

Test condition	Functions active during AI test
1	Default settings with all grid support functions off
2	SPF, F-W, VRT, and FRT
3	V-Var, F-W, VRT, FRT

As per the draft of IEEE P1547.1, worst-case configuration of grid support functions for islanding detection must be identified by the manufacturer. As such information was not available for the inverter under test, parameters shown in Table 3 were used for AI tests.

TABLE 3: GRID SUPPORT PARAMETERS FOR AI TESTS

Functions	Parameters
VRT, FRT	CA Rule 21 settings
F-W	db_{OF} = 0.017 Hz and K_{OF} = 0.05
V-Var	Most aggressive V-Var curve characterized by deadband = 0, slope = maximum
SPF	SPF = 0.9 and 0.95, Under- and overexcited

The test set-up depicted in Figure 1 was developed to be compliant with the set-up shown in Figure 4 recommended by draft IEEE P1547.1.

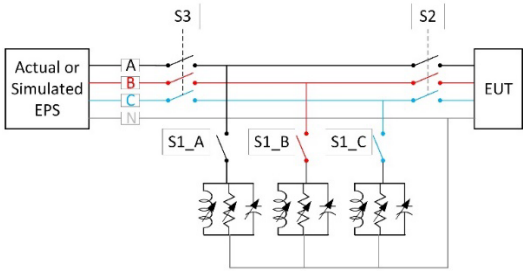

Figure 4: Test set-up for islanding detection test

Since the inverter used in this test requires a transformer, the transformer was considered a part of the equipment under test (EUT) and the measurements to verify the performance were taken on the grid side of the transformer. AI tests were performed for two quality factors (QF), 1.0 and 1.5, and two inverter power levels, 100% and 20% of nominal power. For all combinations of QF and power level, the inverter was tested first with the AI function disabled to verify that the load was well tuned. For a well-tuned load, when switch S3 in Figure 4 is opened to create an island condition with AI controls disabled, the inverter may continue to operate at near-nominal voltage and frequency. This confirms the load tuning and hence allows a significant reduction in the number of tests that must be run.

When AI controls were disabled in the specific inverter under test, it did continue to operate in a well-balanced island. When the AI function was enabled, for the same load and parameter settings the inverter tripped shortly after creation of an islanding condition. Figure 5 shows one example of the result.

Lessons learned from AI Tests

- The primary lesson from this testing was that the new IEEE P1547.1 unintentional islanding test procedure successfully confirmed a well-tuned load, allowing a reduction in the number of tests with an increased confidence that the DER's behavior has been validated.

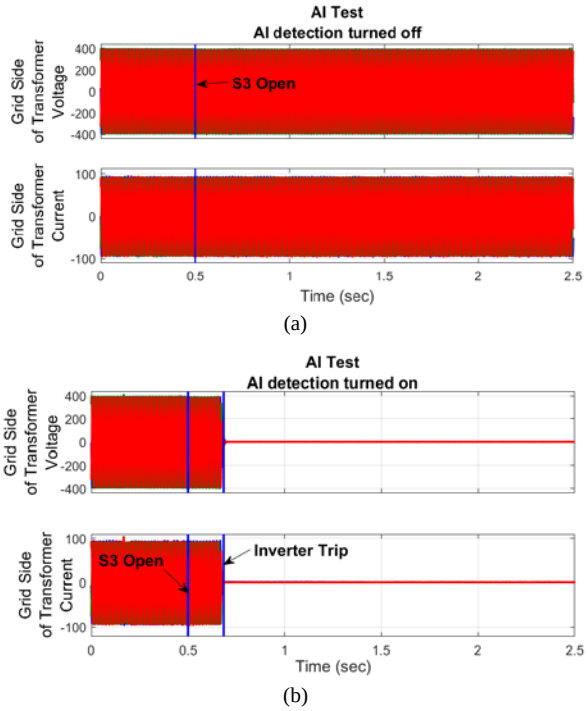

Figure 5: Example of successful AI test result: a) The inverter didn't trip for a tuned load when AI function was off., b) The inverter tripped for the same load when AI function is on.

- While creating the island condition for a 3-phase inverter by opening the switch S3 in Figure 4, the switch must disconnect all the three phases simultaneously otherwise the certification tests may produce an erroneous result. Figure 6 shows one event where a malfunctioning grid simulator output contactor was opened to create an island in an unbalanced way. This could give the false impression that the inverter detected the island if test results are not examined carefully.

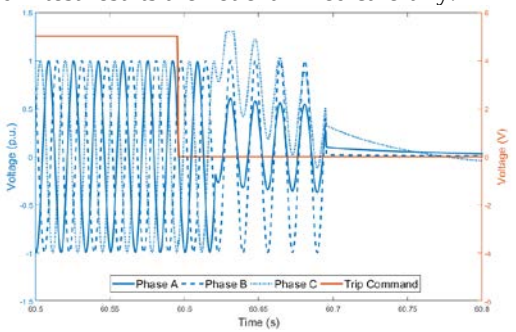

Figure 6: Unbalance in the grid simulator voltage phases due to a malfunctioning contactor for a few cycles before the grid simulator output ceases.

- The effort to create a sustained island for tuned load with over-excited SPF was unsuccessful for the inverter under test, though a sustained island with under-excited SPF was

successfully created. If a similar problem occurred in certification testing, a larger number of tests would be required, per the draft P1547.1 procedure.

E. Volt-Var (V-Var)

The volt-var test procedure specified in UL 1741 SA was followed. The procedure requires some information from the manufacturer to define the volt-var slope and minimum step size for voltage change to accommodate measurement error. Some tests were performed on the inverter to find some of these parameters as not all the information was available. Three different volt-var curves (designated most aggressive, average, and least aggressive) were tested on the inverter for two different power levels: 100% and 20% of nominal power. The inverter was tested for both Watt priority and var priority mode. Figure 7 shows one test result for the "most aggressive" volt-var curve.

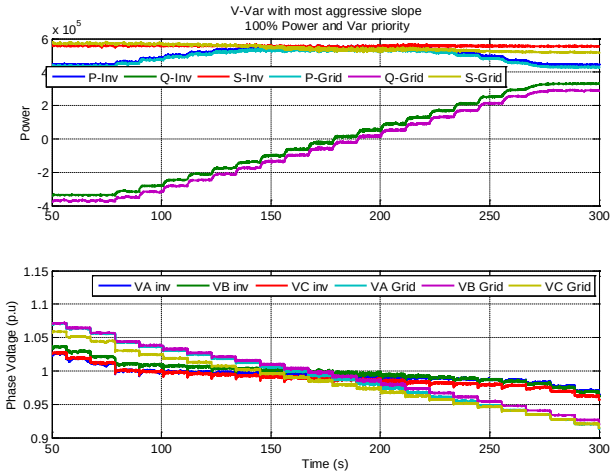

Figure 7: Result of volt-var test with var priority

Lessons learned from V-Var tests

- The transformer introduces some unbalance in voltage though the applied voltage from grid simulator is balanced. As can be seen Figure 7, the difference between the voltages at different phases was observed to be as high as 1.5%. This unbalanced voltage creates some error in validating the experimental result with the expected result.
- The inverter used for this test changes its reactive power based on the voltage at the inverter side of the transformer. However, the voltage change across the transformer is different for the case when the reactive power output changes with respect to voltage than the case when the inverter reaches its maximum or minimum reactive power limit. Figure 8 shows the voltage on both sides of the transformer when the grid simulator voltage was changed from one level to another level. Per IEEE 1547-2018, most large DERs will be required to comply with volt-var curves and other requirements at the point of common coupling (i.e. the connection point to the utility system, typically on the grid side of the transformer), which most currently do not.

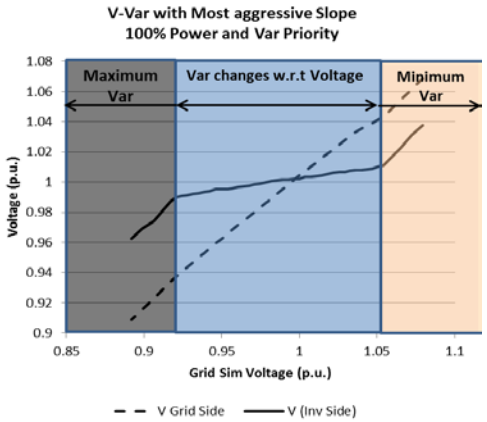

Figure 8: Voltage change across the transformer during volt-var test. The shaded regions indicate what region of the volt-var curve corresponds to the voltage at the inverter terminals.

- The voltage and reactive power measured by the *internal* sensors of the inverter match the programmed volt-var curve with high accuracy. The same cannot be said for external measurement as can be seen in Figure 9. The voltage and reactive power measured by the sensors *external* to the inverter do not match with the programmed volt-var curve with high accuracy. Also note that the error bound, which is a function of the MSA of voltage, is so wide that almost any volt-var behavior would pass the test. IEEE 1547-2018 puts upper limits on DER measurement accuracy for voltage and other parameters, which should partially mitigate this. In addition, the very steep volt-var curve shown in Figure 9 is likely steeper than would be applied in the field.

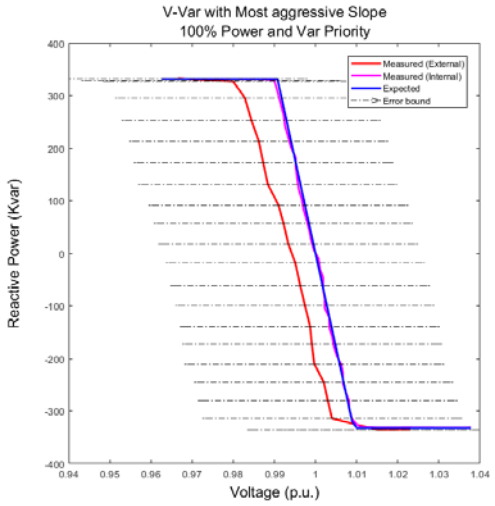

Figure 9: Performance evaluation of the test for volt-var function

- Settling time for the volt-var function is to be supplied by the manufacturer. As this information was not available for the inverter under test, it was measured through experiment. Figure 10 shows the test result for settling time.

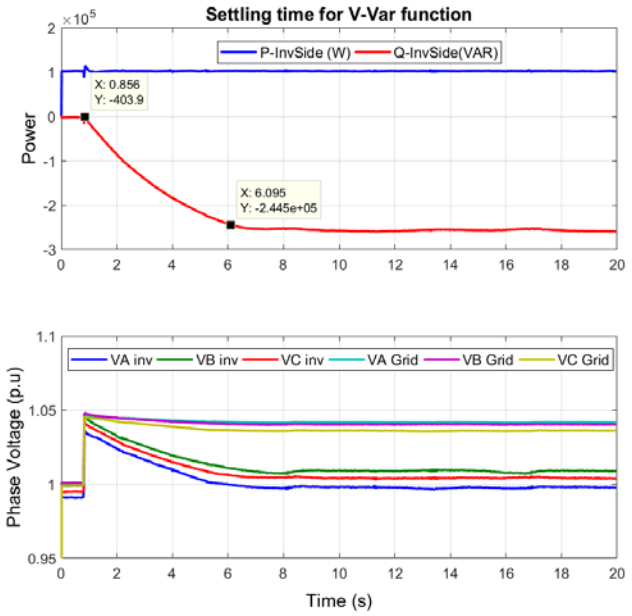

Figure 10: Settling time measurement for V-Var function

F. F-W test procedure from UL 1741 SA

The testing procedure of F-W function specified in UL 1741SA was followed. The testing procedure requires some information from manufacturer to define the F-W slope and minimum step size for frequency change to accommodate frequency and active power measurement errors. Tests were performed on the inverter to find some of these parameters as not all the information was available for the inverter under test.

Lessons learned from UL 1741 SA F-W tests

- F-W settling time is to be supplied by the manufacturer. As this information was not available for the inverter under test, it was measured through experiment.

G. F-W test procedure from IEEE P1547.1

The draft IEEE P1547.1 frequency-watt (aka frequency droop or frequency/power) test includes two procedures: one to confirm the time-domain response and one to confirm the steady-state response. Both were validated using the same 550 kVA inverter.

The draft test procedure for time response assumes an adjustable open loop F-W time response. The open loop F-W response time ($T_{response}$) of the inverter used in this test was not adjustable. The default value of $T_{response}$ was used to validate the test procedure. Figure 11 shows a result from the test as specified in Draft 3, which evaluates the time response only for power changes of less than 0.1 per unit. However, for DERs that can achieve larger changes, the test should evaluate those. Figure 12 shows the behavior of the inverter for a jump in output power from 100% to 10% due to frequency change. For this inverter, the response time varies significantly with the size of the power step.

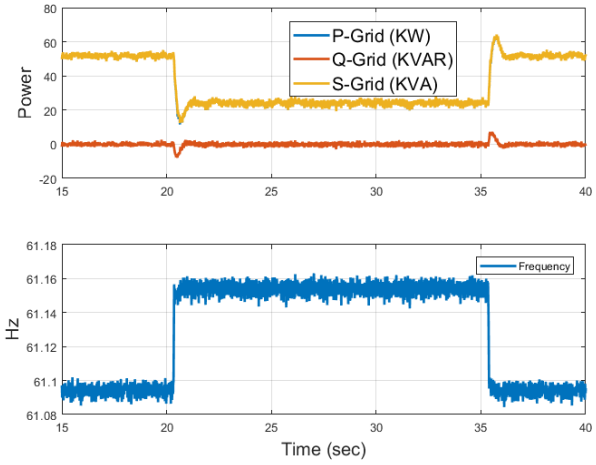

Figure 11: Test result for frequency droop time response test

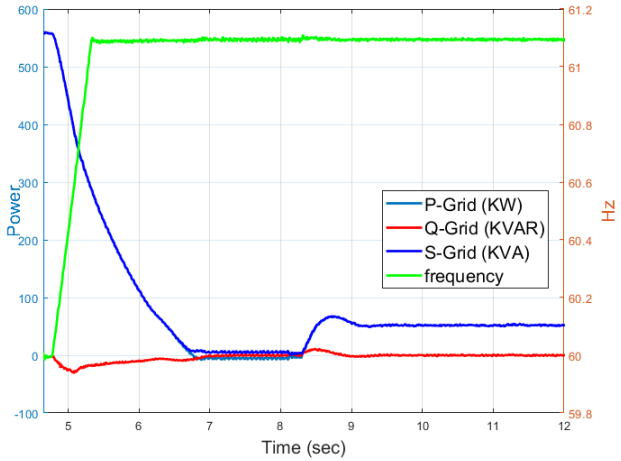

Figure 12: 100% to 10% power jump due to change in frequency

The draft P1547.1 test procedure for steady-state frequency droop was also evaluated. Figure 13 and Figure 14 show sample results:

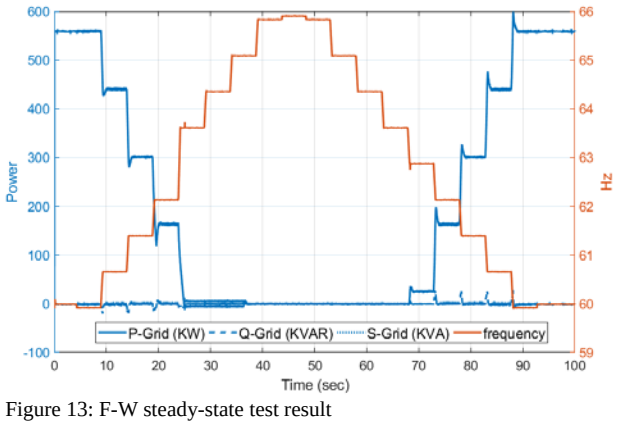

Figure 13: F-W steady-state test result

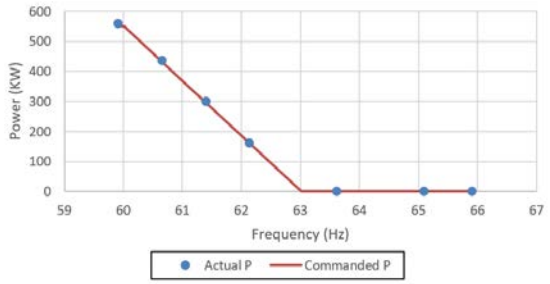

Figure 14: Performance evaluation of test for F-W function

Lessons learned from F-W test ollowing IEEE P1547.1

- Overall the draft F-W tests appear reasonable.

H. Lessons learned from overall experiments

- The testing procedures prescribed by UL 1741 SA require a large number of manufacturer-provided inverter parameters. 20 parameters are required for the V-Var test alone. IEEE P1547.1 will likely require a still larger number of parameters.
- When a transformer is to be installed with the inverter, it should be clearly specified in the test procedure which side of the transformer (grid side or inverter side) should be taken as point of contact for test voltage application as well as voltage and power measurements.
- For a Δ-Y transformer, there will be always some induced voltage in delta side of the transformer if zero voltage is applied in one of the phases of the other side. As can be seen in the following figure, though zero voltage was applied to phase A of the grid side of the transformer, the voltage on the inverter side was not zero.

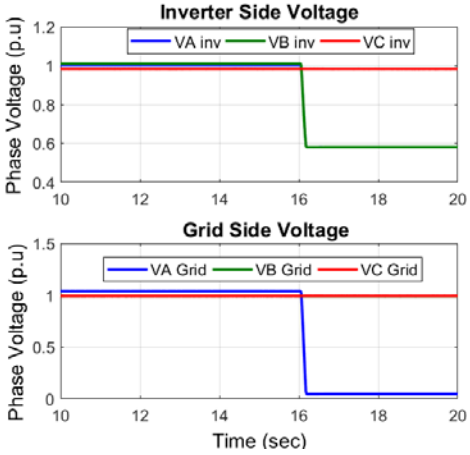

Figure 15: Induced voltage for a wye-delta transformer

- Instability was observed when running the inverter in maximum power point tracking (MPPT) mode and the DC supply as PV simulator. This results from an interaction between the PV simulator controls and the inverter's MPPT controls. At higher power levels, especially at the 100% inverter output power level, the instability condition becomes severe. To circumvent this issue, the DC power supply was put in constant voltage mode while the inverter was set to run in MPPT mode. The NREL team has discussed this issue with members of the IEEE P1547.1 Working Group. Discussions are ongoing as to whether some P1547.1 tests should impose requirements on the input source to the DER under test.

Conclusion

Test procedures from UL 1741 SA and from the draft IEEE P1547.1 were tested in the laboratory with a 550 kVA inverter to find any weak points or issues in the test procedures that need to be addressed as the standards develop. Selected laboratory test results, problems identified, and areas of concern are discussed in this paper. Knowledge gained from these tests has been shared with the IEEE P1547.1 Working Group for consideration in the upcoming standard. At the time of this writing, IEEE P1547.1 requires more analysis through laboratory testing before being published. The research team of this paper will continue to investigate draft test procedures as they become available.

Acknowledgement

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