Mechanically Stacked Dual-Junction and Triple-Junction III-V/Si-IBC Cells with Efficiencies Exceeding 31.5% and 35.4%

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MECHANICALLY STACKED DUAL-JUNCTION AND TRIPLE-JUNCTION III-V/SI-IBC CELLS WITH EFFICIENCIES OF 31.5 % AND 35.4 %

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ABSTRACT: The theoretical efficiency limit of 29.4 % for single-junction crystalline Silicon (c-Si) solar cells is an insurmountable barrier that is being steadily approached within the last decades. Combining the Si cell with a second absorber material on top in a dual junction tandem or triple junction solar cell is an attractive option to surpass this limit significantly. We demonstrate a mechanically stacked GaInP//Si dual-junction cell with an in-house measured efficiency of 31.5 % and a GaInP/GaAs//Si triple-junction cell with a certified efficiency of 35.4±0.5 %

Keywords:

1 Introduction

Steady improvements over decades have led to exceptional success of market-dominating silicon-based photovoltaics, which recently demonstrated an outstanding record efficiency of 26.7 % for an interdigitated back contact solar cell [12].Stacking of multiple junctions has proven to be a viable route to increase the cell efficiency further beyond the theoretical limit of 29.4% for silicon single-junction solar cells[6, 2]. Increasing research interest is currently dedicated to tandem concepts based on Si bottom cells for terrestrial, non-concentrated applications [2 and Ref. therein, 5, 10 and Ref. therein]. Here we prepared a mechanically stacked GaInP//Si dual-junction cell and a GaInP/GaAs//Si triple-junction cell, achieving energy conversion efficiencies of 31.5 % and 35.4 %, respectively. With this result, we demonstrate the potential of silicon based multi-junction solar cells for high efficiencies.

2 Experimental

2.1 Fabrication of POLO-IBC bottom cell

We prepare ion-implanted and inkjet-patterned interdigitated back contacted solar cells with **POL**y-Si on **O**xide (POLO) junctions for both polarities (POLO-IBC cells) [7, 8] with an active area of 7.6 mm × 15 mm (to match the top cell area) on saw-damage etched 156 mm × 156 mm *n*-type Czochralski silicon wafers with a base resistivity of 4 Ωcm and a final thickness of 155 µm.

After growing a thin thermal silicon dioxide layer in a tube furnace, undoped amorphous silicon (*a*-Si) is deposited on both sides by using LPCVD (E2000 from Centrotherm). Hereafter, the front side of the wafer receives a blanket phosphorus implantation, followed by masked phosphorus and blanket boron implantation on the rear side. For the latter, the phosphorus locally overcompensates the boron, and an interdigitated pattern with a pitch of 952 µm is formed. For the masking of the implantations, we use a sputtered dielectric layer, which is patterned by inkjet-printed hotmelt wax (Pixdro LP50 from Meyer Burger) and subsequent wet-chemical etching.

After the removal of dielectric implant masks, a high temperature treatment for the formation of the POLO junctions with an annealing duration of 60 minutes at 1050°C is performed. The junction formation annealing leads to recrystallization of the a-Si, redistribution and activation of dopants and a pinhole creation within the interfacial SiO_2 layer [11] for efficient carrier transport between c-Si and poly-Si [7]. Furthermore gettering of the bulk material with n^+ POLO is achieved [4].
During the junction formation step, a thick silicon dioxide layer is grown on top of the poly-Si by wet thermal oxidation.

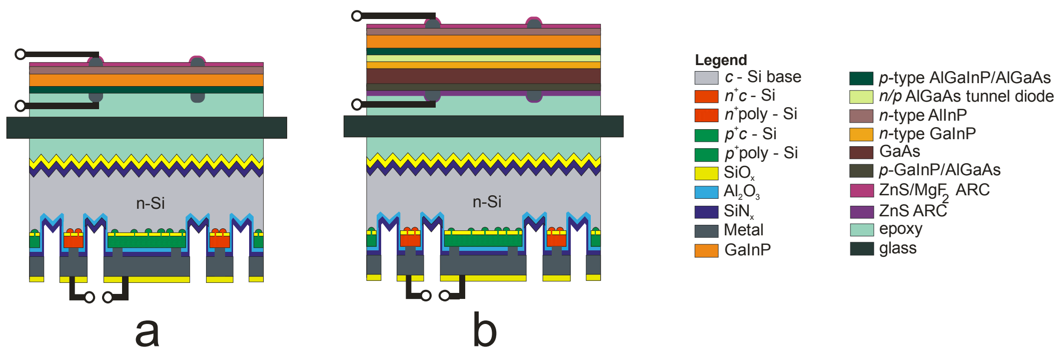

Figure 1: Schematic of GaInP//Si-IBC cell (a) and GaInP/GaAs//Si-IBC cell (b)

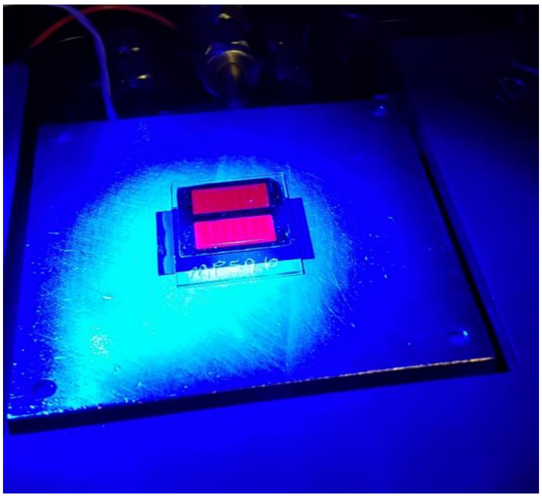

Figure 2: Photograph of GaInP/GaAs//Si-IBC cell with an efficiency of 35.4% illuminated with blue LED light

After the oxidation and junction formation process, the grown silicon dioxide layer is again patterned via inkjet printing and wet-chemical etching on the rear, and at the same time removed on full area from the front side of the wafer. The remaining SiO_2 on the rear acts as an etching barrier for a subsequent texturization process, which yields a textured front side and a separation of n^+ POLO BSF and p^+ POLO emitter regions by a textured trench of a width of 100 µm. The trench isolation significantly improves the overall recombination behaviour of the cells [8] and furthermore facilitates contact separation via the RISE process [1]. After removing the SiO_2 by HF etching from the rear side, the cell precursors are passivated with an aluminum oxide/silicon nitride stack on the rear side and a silicon nitride on the front side.
An additional SiO_2 layer is deposited by PECVD on the front side in order to improve the optics for one sun application rather than tandem cells. This leads to non-ideal optical coupling between silicon and III-V cells and represents an area for future improvements.

We use a picosecond UV laser to locally ablate the dielectric layers and realize via contact openings with an opening fraction of about 4.5% with respect to the total cell area.

The solar cell precursors are metalized by vacuum evaporation of a 10 µm thick aluminum layer on the rear side in a high-throughput tool from Applied Materials and the contact separation is performed via the RISE process [1]. Finally, the POLO-IBC bottom cells, as shown in Fig. 1, are laser-scribed and cleaved from the wafer.

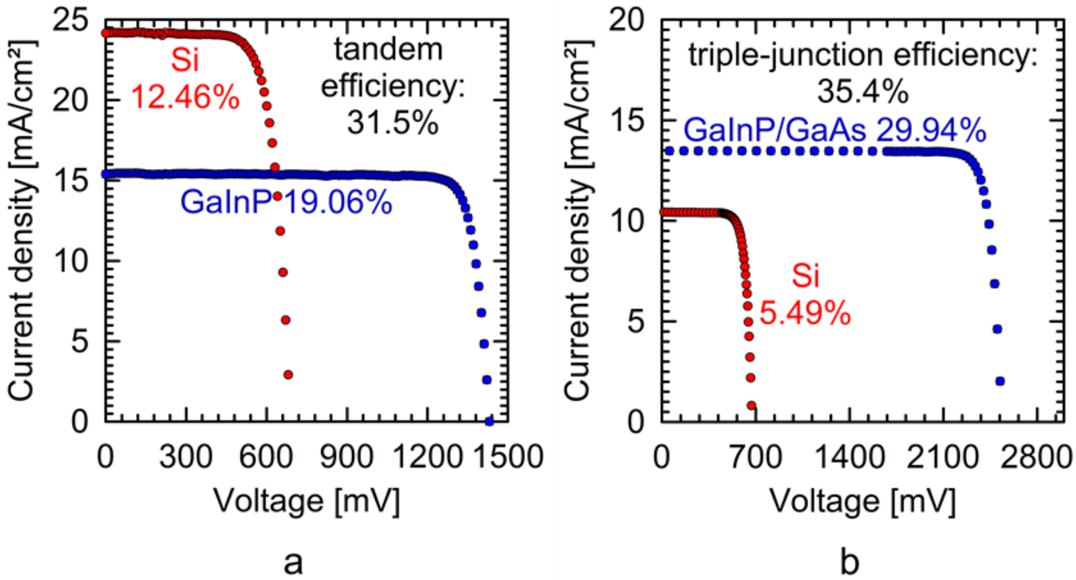

Figure 3: IV data of GaInP/Si-IBC cell (a) and GaInP/GaAs/Si-IBC cell

2.2 Fabrication of GaInP single junction cell

The GaInP cell was grown inverted, with a rear heterojunction, on a GaAs substrate with a 2° miscut towards <111> by metalorganic chemical vapor deposition (MOCVD), using the reactor, precursors, and process window described in Ref.[3]. Cell processing of the MOCVD-grown stack begins with a rear-side Au grid prepared by photolithographically patterned Au electroplating, followed by evaporation of ZnS as a rear-side antireflection coating. The cell is then bonded to glass using epoxy, and the GaAs substrate removed by etching. Finally, the front side is processed: a front grid is prepared by photolithographically-patterned Ni/Au electroplating, a photolithographically-patterned mesa etch is performed to define the cell area, and a MgF_2 / ZnS double-layer antireflection coating is evaporated.

2.3 Fabrication of GaInP/GaAs dual-junction cell

The process sequence for the GaInP/GaAs dual-junction cell is the same as for the single junction GaInP cell, except that both cells are grown in sequence during the MOCVD step. The GaInP cell is the same, and is grown first, followed by a $Al_{0.3}Ga_{0.7}As$/GaAs tunnel junction and then the GaAs cell, as described in ref. [3].

2.4 Stacking of the III-V cell on the Si cell

The III-V cell on glass is bonded to the front side of the

Si cell using epoxy. Stacking and bonding is done under an infrared camera in order to align the top cell area with the IBC grid fingers of the bottom cell. The final four-terminal triple-junction cell is shown in Fig. 2.

2.5 *IV* measurement

For the GaInP/Si IBC cell, the quantum efficiency and specular reflectance of both cells were measured on a custom-built instrument. The *IV* measurement of the GaInP/Si IBC cell was taken on a class A adjustable solar simulator with a primary calibration reference cell used to set the intensity. The two cells were contacted separately and measured sequentially. For each cell, the the illumination was set such that each cell was at an illumination level, which is the equivalent of AM1.5G and the filtered equivalent for the bottom cell. A shadow mask was used to ensure no photocarrier generation outside the 1 cm^2 active cell area. The GaInP cell was measured first, and during measurement of the Si cell, a resistor was used to hold the GaInP at its maximum power point (mpp). This is necessary because under open circuit conditions, GaInP luminescence coupling to the Si cell is higher than at mpp, artificially inflating its performance [2]. Luminescent coupling from Si to GaInP is negligible because Si luminescence is weak and not absorbed by the GaInP cell.

The GaInP/GaAs//Si-IBC cell was measured using the a calibrated measurement with same procedure at NREL's certified device performance laboratory.

3 Results and discussion

3.1 GaInP//Si dual-junction solar cell

The resulting in-house measured *IV* data is show in Fig. 3 a. After stacking, the GaInP top solar cell has a single junction efficiency of 19.1 % (V_{OC}=1430 mV, J_{SC}= 15.4 mA/cm², *FF*=86.6 %) and the Si bottom cell yields an efficiency of 12.5 % (V_{OC}=687 mV, J_{SC}= 24.2 mA/cm², *FF*=75.1 %, GaInP cell at mpp). A cumulative efficiency of 31.5 % is obtained, which exhibits, compared to the recently published III-V/Si record efficiency of 32.5 % [2], an 1 $\%_{abs}$ lower efficiency. This is attributed to the about 1 $\%_{abs}$ lower efficiency of the GaInP top cell. The Si bottom cell has nearly the same performance, but the V_{OC} of our POLO-IBC cell is 7 mV lower, which can be mainly explained by degradation during the stacking procedure as well as lower passivation quality of the SiN_x passivation at the front side and degraded passivation quality of the trench passivation at the rear side compared to excellent passivation by amorphous Si used in Ref. [2].

Further optimization of the back-end processing and minimizing perimeter recombination will lead to an increase in V_{OC} above 700 mV.

The low *FF* of the silicon cell is tentatively attributed to non-ideal heat-sinking during the measurement.
The absence of a metal grid, the high transparency of the front side and decent reflectivity of the rear side of our POLO-IBC bottom cell is responsible for the high short circuit current of 24.2 mA/cm² (1.1 mA/cm^2 higher than for the Si bottom cell in Ref [2]).Since the antireflection coating applied is optimized for the non-filtered solar spectrum, further improvements are anticipated by tuning the antireflection coating on the Si cell to the relevant infrared wavelength range.

Taking possible improvements into account and using a 20 % efficient GaInP cell and a filtered efficiency for our POLO-IBC cell above 13 %, a GaInP/Si tandem efficiency above 33 % is within reach.

3.2 GaInP/GaAs//Si triple-junction solar cell

For the GaInP/GaAs//Si triple-junction cell a calibrated *IV* measurement was performed at NREL's certified device performance laboratory.

The current-matched GaInP/GaAs dual-junction achieved an efficiency of 29.94±0.42 % (V_{OC} = 2535 mV, J_{SC} = 13.43 mA/cm², *FF* = 87.9 %) and the POLO-IBC bottom cell added another 5.49±0.08 % (V_{OC} = 670 mV, J_{SC}= 10.4 mA/cm², *FF*=78.8 %, GaInP/GaAs cell at mpp) filtered efficiency to achieve an overall four-terminal, triple-junction efficiency of 35.43±0.5 %. As with the GaInP/Si cell, improvements in Si J_{SC} are anticipated with optimized antireflection coatings.

This excellent efficiency is the second-highest after and close to the current world record of 35.9 % for III-V/Si triple-junction cells [2].

On its own, the efficiency of this type of Si wafer cell with POLO junctions reaches 25 %. Thus, the addition of the GaInP/GaAs top cell yields a total efficiency improvement of about 10 $\%_{abs.}$ The efficiency of the four-terminal GaInP/GaAs//Si cell is even close to the current world record of a series-connected 37.9 % for a non-Si triple-junction cell [9].

4. Conclusion

We have demonstrated lab scale dual-junction and triple-junction four-terminal III-V//Si solar cells using POLO junctions on the Si IBC cells for both polarities with efficiencies of 31.5 % and 35.4 %, respectively. The latter result is very close to the world record for III-V//Si and all-III-V triple-junction solar cells and therefore shows that silicon wafer cells, which provide the mature and cheap basis for over 90 % of today's photovoltaic (PV) devices, are well suited for tandem applications.

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