Advanced PHIL Interface for Multi-MW Scale Inverter Testing

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Overview

- Controllable Grid Interface (CGI) at the National Wind Technology Site
- CGI recent upgrades
- Communication links
- RTDS-CGI power-hardware-in-the-loop (PHIL) interface
- Delay compensation techniques
- PHIL test results
  - Fault testing (L-L, L-G)
  - Generator trip test and frequency response support from wind turbine
  - Capacitor bank switching
NWTC 7-MVA Controllable Grid Interface

Image from NREL
CGI Main Technical Characteristics

Power rating
- 7-MW continuous
- 39-MVA short circuit capacity (for 2 sec)
- 4-wire, 13.2-kV

Possible test articles
- Types 1, 2, 3 and 4 wind turbines
- Capable of fault testing of world’s largest 6.15-MW Type 3 wind turbine
- Photovoltaic (PV) inverters, energy storage systems
- Conventional generators
- Combinations of technologies

Voltage control (no load THD <3%)
- Balanced and unbalanced voltage fault conditions (ZVRT and 130% HVRT) – independent voltage control for each phase on 13.2-kV terminals
- Response time – 1 ms (from full voltage to zero, or from zero back to full voltage)
- Long-term symmetrical voltage variations (+/- 10%) and voltage magnitude modulations (0-10 Hz) – SSR conditions
- Programmable impedance (strong and weak grids)
- Programmable distortions (lower harmonics 3, 5, 7)

Frequency control
- Fast output frequency control (3 Hz/sec) within 45-65-Hz range
- 50/60-Hz operation
- Can simulate frequency conditions for any type of power system

• RTDS – PHIL capability
Recent upgrades in CGI

CGI 2.0 – commissioned in January 2016
- **Faster dynamic response**
- Various transformer saturation protection algorithms to allow ride-through of any reference command

Coming soon:
- High frequency LR filter to improve power quality with minor impact on dynamics
- Decreasing processing delays

Figure from ABB
Site Overview

- Unique infrastructure for multi-MW grid integration testing
- Typically devices are tested against arbitrary voltage and frequency patterns in open loop
- PHIL for testing of device operation in relatively weak grids where distributed energy resources (DERs) also impact the grid
Communication Architecture

- Distances between RTDS-point of connection (POI) and CGI ca. 300ft
- Preferred digital optical communication

- 2Gb/s RTDS optical link – glass optical fiber
- 10Mb/s CGI-ABB proprietary link – plastic optical fiber
- Up to 40x16bit variables exchanged between RTDS and CGI every 25us (40kHz)
RTDS Grid Model

- RTDS 9-bus model
  - 130-kV transmission
  - 4x synchronous generators with total capacity of 617 MW
  - AGC implemented
  - Loads during test at 400 MW
  - Various test scenarios
    - Dropping of G4 – 12.5% generation
    - Line to ground (LG) & line to line (LL) faults emulation
    - Cap bank switching

PHIL Point of Interconnection (POI)

- Configurable multiplier - “m” – allows for multiplying the impact of real devices connected to CGI to simulated grid
CGI-RTDS PHIL Interface

- Instantaneous voltage measured in model and commanded to CGI
  - Very fast tracking achieved thanks to instantaneous to phasor (I2P) algorithm
  - Controllable phase delay
- Active and reactive power measured at CGI terminals is fed back to model
  - Active (P) and reactive (Q) power is filtered to avoid PHIL experiment instability
  - Current is injected back to model and synchronized using PLL
RTDS -> CGI Voltage Tracking Capabilities

Output from RTDS simulation is 3x instantaneous voltages $u_{Mdl}$

CGI voltage is controlled by:

1) Frequency setpoint – $\omega_{ref}$
2) 3xPhasor magnitude – $M_{ref}$
3) 3xPhasor angle – $\Phi_{ref}$
4) CGI precise integrator (<0.001Hz accuracy) - actual angle ($\theta_{Cgi}$) is sent back to RTDS for synchronization

Real time algorithm I2P (Instantaneous to phasor) developed to allow:

1) Instantaneous synchronization of $u_{ref}$ & $u_{Mdl}$
2) Smooth phasor ($M_{ref}/\phi_{ref}$) reconstruction – to avoid dynamic limitations in CGI
3) Allow asymmetrical voltages (zero, pos, neg sequence)
4) Minimize delay for PHIL operation
5) Allow constant group delay – don’t distort waveform
6) Don’t depend on phase locked loop (PLL) for frequency control (transients, etc.)
 Assumption for lossless instantaneous conversion
\[ u[n] = \text{Re}\{M[n]e^{i(\Phi[n]+\theta[n])}\} \]
\[ \overline{u[n]} = M[n]e^{i(\Phi[n]+\theta[n])} \]
\[ u[n] = \text{Re}\{\overline{u[n]}\} \]

[n] point approximation based on [n-1] filtered phasor
\[ \overline{u'[n]} = U_{\text{filt}}[n-1]e^{i\theta[n]} \]
\[ \overline{u[n]} = u[n] + i\text{Im}\{u'[n]\} \]

Convert back to stationary frame – phasor reference
\[ \overline{U[n]} = u[n]e^{-i\theta[n]} \]
\[ \theta'[n] = \Phi[n] + \theta[n] \]
Frequency Step Test – CGI Voltage Tracking
Bode Plot

- Algorithm optimized for very low delay at nominal converter frequency: 45-65 Hz
- Leading phase delay at low frequencies/lagging at higher frequencies – causes distortion to wide spectrum voltages (e.g. transients)
Delay Compensation Technique

- Delay can be compensated to allow distortion less transfer function
- Group delay must be constant
- Comm delays ~ 25us
- Actual CGI delay mostly due to processing – Td
Delay Compensation: Bode Plot

- Transfer function optimized towards distortion less voltage transfer
- Group delay is close to constant
Line Fault Testing

- More real life example
- Line to line and line to ground faults simulated in RTDS – within certain electrical distance from POI
- Transient with rich harmonic content
- Zero, positive and negative sequence
- Highly asymmetrical events
1 Phase Line to Line Fault
1 Phase Line to Line Fault: No Delay Compensation
1 Phase Line to Line: With Delay Compensation
1 Phase Line to Line Fault
1 Phase Line to Line Fault
2 Phase Line to Line Fault
2 Phase Line to Line Fault
3 Phase Line to Line Fault
3 Phase Line to Line
3 Phase Line to Line
3 Phase Line to Line
1 Phase Line to Ground Fault
1 Phase Line to Ground Fault
2 Phase Line to Ground Fault
2 Phase Line to Ground Fault
3 Phase Line to Ground Fault
3 Phase Line to Ground Fault
PHIL Tests – GE 1.5 MW - 12% Generation Drop Case

- G4 generating 50 MW before the event
- G4 CB opens
- GE 1.5-MW wind energy controller (WEC) reacts with inertial response & droop
- Frequency recovers faster with higher $m$
- Frequency dip was slightly limited

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<th>$m$</th>
<th>$f_{\text{min}}$ [Hz]</th>
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PHIL Test – GE 1.5 MW – Capacitor Bank Enabling

- Wind Plant Controller (WPC) is configured to control voltage at POI with Volt/VAR droop
- Cap bank is disabled at t=0.9s

- With m=0 there is no impact of reactive power on POI voltage
- With m=100 voltage is being controlled by WPC
- PHIL helps in testing droop/load sharing techniques
Publications


Thank you!