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Solar cell efficiency and high temperature processing of *n*-type silicon grown by the noncontact crucible method

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Abstract

The capital expense (capex) of conventional crystal growth methods is a barrier to sustainable growth of the photovoltaic industry. It is challenging for innovative techniques to displace conventional growth methods due the low dislocation density and high lifetime required for high efficiency devices. One promising innovation in crystal growth is the noncontact crucible method (NOC-Si), which combines aspects of Czochralski (Cz) and conventional casting. This material has the potential to satisfy the dual requirements, with capex likely between that of Cz (high capex) and multicrystalline silicon (mc-Si, low capex). In this contribution, we observe a strong dependence of solar cell efficiency on ingot height, correlated with the evolution of swirl-like defects, for single crystalline *n*-type silicon grown by the NOC-Si method. We posit that these defects are similar to those observed in Cz, and we explore the response of NOC-Si to high temperature treatments including phosphorous diffusion gettering (PDG) and Tabula Rasa (TR). The highest lifetimes (2033 μs for the top of the ingot and 342 μs for the bottom of the ingot) are achieved for TR followed by a PDG process comprising a standard plateau and a low temperature anneal. Further improvements can be gained by tailoring the time-temperature profiles of each process. Lifetime analysis after the PDG process indicates the presence of a getterable impurity in the as-grown material, while analysis after TR points to the presence of oxide precipitates especially at the bottom of the ingot. Uniform lifetime degradation is observed after TR which we assign to a presently unknown defect. Future work includes additional TR processing to uncover the nature of this defect, microstructural characterization of suspected oxide precipitates, and optimization of the TR process to achieve the dual goals of high lifetime and spatial homogenization.

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1. Introduction

To meet the near-term challenge of increasing global solar electricity production, the silicon PV industry must scale current manufacturing capacities to meet growing demand without sacrificing either efficiency or cost to the consumer. A recent survey of the PV industry suggests that capital expense (capex, *.e.g.* equipment purchase), which is ~22% of the module price, is a barrier to sustainable growth of PV companies [1]. Capex related to wafer growth accounts for 16% of the cost to build a Czochralski (Cz) silicon-based solar cell factory, while the same number for a mc-Si silicon factory is 4% assuming identical upstream and downstream processes. To meet the goals of high efficiency and sustainable growth, innovations in wafer growth technologies that can offer compromises between cost and performance are necessary.

New wafer growth techniques must compete with incumbent technologies, including cast ingot methods to produce mc-Si silicon and Cz methods to produce single crystalline silicon. To displace these dominant technologies, dislocation densities as low as 10^4 cm^{-2} and minority carrier lifetimes as high as 1 millisecond are required to support high efficiency *p*-type base devices. [2]. The lifetime requirement is even higher for *n*-type base devices due to the lower minority carrier mobility. One of the most promising emerging growth technologies is the noncontact crucible (NOC-Si) growth method, which combines aspects of the incumbent methods to produce single crystalline silicon with low dislocation density ($<10^3$ cm^{-2} [3]) at growth rates exceeding those of conventional casting [3]–[5]. Both *n*- and *p*-type silicon can be produced by the NOC method; in this study, we focus on *n*-type material.

Previous studies of NOC-Si have shown that swirl-like defects evolve as a function of ingot height and depress minority carrier lifetime [3], [4]. Non-uniform resistivity and oxygen distributions suggest the formation of recombination-active oxide precipitates associated with these swirl defects [4]. Similar defects can be found in Cz-grown silicon, which has previously been observed to respond favorably to high temperature Tabula Rasa-like processes [6], [7].

In this contribution, we study the response of *n*-type NOC-Si to phosphorous diffusion gettering (PDG) and Tabula Rasa (TR) processes with the goal of designing a process which homogenizes ingot performance to produce lower capex material with performance comparable to Cz. We compare the order in which TR and PDG are applied to the wafer, and we evaluate two different PDG time-temperature profiles. We find that, when TR is applied prior to PDG, the lifetime in the bottom of the ingot improves and the relative recombination strength of the swirl region is maintained and/or improved. With further optimization of the TR process parameters, we hypothesize that this process can enable even higher lifetime, swirl-free wafers throughout the ingot.

2. Experimental details

An *n*-type single crystalline silicon cylindrical ingot with a diameter of 33 cm was grown by the noncontact crucible method [4], [5] with a (100) crystal orientation at a cooling rate of 0.4 K/min. The phosphorous-doped *n*-type resistivity was measured by four-point probe to be 1.7 Ω-cm near the top of the ingot (first to solidify, Fig. 1(a)) and 1.2 Ω-cm near the bottom of the ingot (last to solidify). The etch pit densities, measured according to the method described in Ref. [4], were $2.7\text{-}7.0\times10^4$ cm^{-2} (top) and $1.0\times10^2\text{-}2.4\times10^4$ cm^{-2} (bottom). Interstitial oxygen concentrations were measured by the method described in Ref. [8], with oxygen increasing from top to bottom ingot height and values between 1.2×10^{18} cm^{-3} and 1.45×10^{18} cm^{-3}.

Wafers selected from 21 different ingot heights were processed into *n*-type Passivated Emitter Rear Totally diffused (PERT) solar cells at the Institute for Solar Energy, located in Chambéry, France [9]. Reference Cz wafers were processed alongside the NOC-Si wafers to monitor the cell fabrication process. To investigate wafer performance variation along the length of the ingot, directly adjacent wafers (same bulk quality) were selected from approximately 14% (top) and 92% (bottom) ingot heights. 4×5 cm^2 samples were laser-cut from each larger wafer, symmetric about the centerline. After saw-damage removal of approximately 20 µm by CP4, adjacent samples were processed to allow for direct comparison of four different processes: PDG, TR, PDG+TR, and TR+PDG. In

addition, two different PDG time-temperature profiles are compared. PDG was performed at the Massachusetts Institute of Technology in a $POCl_3$ tube furnace (Tystar Titan 2800), with standard (STD) and extended (EXT) processes identical to those described in Ref. [3]. TR was performed at the National Renewable Energy Laboratory, reported in Ref. [6]. The TR process consists of a timed anneal at 1090°C in a clean tube furnace, with a rapid cooling rate above 100°C/min.

Lifetime measurements were performed on samples after each process with QSSPC (Sinton Instruments WCT-120) and photoconductance-calibrated photoluminescence [10]. Photoluminescence counts were converted to lifetime values according to calibration curves measured for each sample. Prior to lifetime measurements, Al_2O_3 was deposited as a passivating layer by atomic layer deposition followed by annealing. For samples in the as-grown, PDG, and TR+PDG states, a 20 nm layer was deposited and annealed at 350°C for 12 minutes in N_2. For samples after TR, a 15 nm layer was deposited and annealed at 400°C for 10 minutes. For each passivation step, an *n*-type float-zone wafer (280 µm, 2.5 Ω-cm) was used as a control to quantify surface recombination velocity. Surface recombination velocities below 6 cm/s were achieved for all passivation runs, ensuring that the measured lifetimes reported herein are minimally affected by surface recombination.

3. Results

Solar cell efficiency decreases from the top to bottom of the ingot, as shown in Fig. 1. Near the top of the ingot, the efficiency reaches a maximum value of 19.6%. Efficiency decreases to a minimum value of 18.0% at the bottom of the ingot. The reference Cz wafers demonstrate a maximum efficiency of 20.0%. This decrease in solar cell efficiency is correlated with the development and increasing recombination strength of swirl-like defects from the top to the bottom of the ingot as observed by photoluminescence.

The results for the high temperature processing experiment are summarized in Table 1. The spatially resolved lifetime maps and minority carrier lifetimes from two representative samples shown in Fig. 2. The lifetime maps were taken at the same generation rate. The first sample set (containing two adjacent wafers from each ingot height) was selected from the left side of the wafer (Fig. 2(a), (b)). One adjacent wafer was subjected to the STD and STD+TR processes; the other adjacent wafer was measured as-grown and then subjected to the TR and TR+STD processes. Similarly, the second sample set was selected from the right side of the wafer (Fig. 2(a), (c)) and subjected in the same manner to the EXT, EXT+TR, TR, and TR+EXT processes. The average lifetime results in each state are indicated in Fig. 2(d).

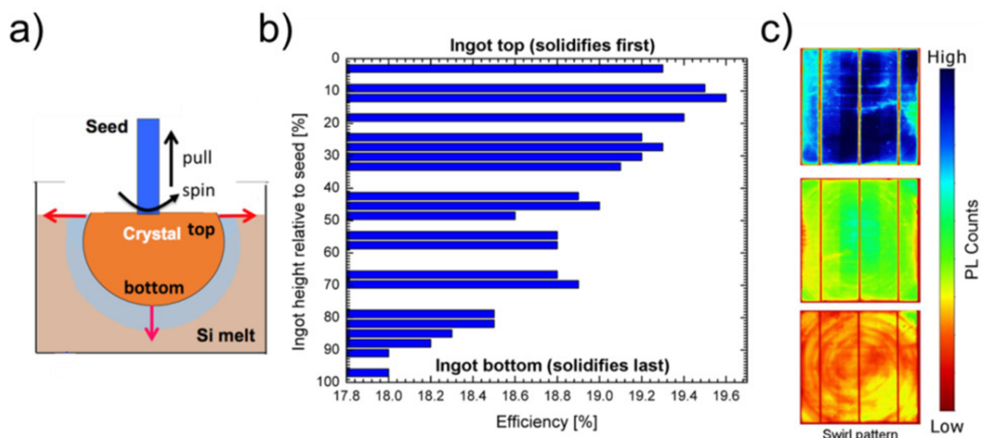

Fig. 1: (a) NOC-Si crystal growth orientation, in which 0% is the wafer closest to the seed (first to solidify, *i.e.* the NOC-Si ingot top), while 100% is the wafer furthest from the seed (last to solidify, *i.e.* the NOC-Si ingot bottom). (b) Solar cell efficiency is plotted as a function of ingot height. (c) Photoluminescence images are shown for each part of the ingot.

Table 1: Summary of key results from high temperature experiment. Lifetimes are reported at 10^{15} cm^{-3}.

		As-grown	**STD**	**TR**	**TR+ STD**	**As-grown**	**EXT**	**TR**	**TR+ EXT**	**Max estimated η**
Top	τ [µs]	998	1050	70	956	1053	1879	90	2033	19.7%
	Spatial	uniform	uniform	uniform	uniform	uniform	uniform	uniform	uniform	TR+EXT
Bottom	τ [µs]	62	207	23	215	86	269	32	342	19.1%
	Spatial	swirls	swirls, enhanced	uniform	swirls (light contrast)	swirls	swirls, enhanced	uniform	swirls	TR+EXT

3.1. Top of the ingot

As-grown lifetimes of wafers from the top of the ingot are approximately 1 ms, exceeding those from the bottom of the ingot by three orders of magnitude. Wafer lifetimes increase compared to as-grown by 5% and 78% for the STD and EXT processes, respectively. After TR, EXT+TR, and STD+TR, lifetime degrades to values below 100 µs. When TR is applied first and PDG is applied second, lifetimes are decreased compared to as-grown by 4% for the STD process and increased by 93% for the EXT process. The spatial homogeneity of the top ingot wafers observed in the as-grown state is not disrupted by any of the high temperature processes examined herein and will not be discussed further.

3.2. Bottom of the ingot

As-grown lifetimes from the bottom of the ingot are below 100 µs, and corresponding swirl defects are observed in the photoluminescence images. After the STD and EXT processes, the bottom ingot wafer lifetimes increase compared to as-grown by 234% and 211%, respectively. Similar to the top ingot wafers, lifetime degrades to values below 50 µs after TR, STD+TR, and EXT+TR. When TR is applied first and PDG is applied second, the lifetime is increased by 247% and 296% for the STD and EXT processes, respectively.

The spatially resolved lifetimes after each state offer further information about the different processes. After PDG, the relative recombination strength (inverse of swirl lifetime divided by inverse of lifetime in non-swirl region) increases in some regions. Photoluminescence images in the post-TR states (not shown due to the low lifetime) demonstrate qualitatively that the lifetime is spatially homogeneous for bottom ingot wafers that have not been subjected to PDG prior to TR. For wafers that have been subjected to PDG prior to TR, the swirl patterns observed in Fig. 2(b),(c) persist. When PDG follows TR, the spatially-resolved results demonstrate that the swirl pattern is not eliminated by TR. The relative recombination strength of the swirl region is decreased after TR+STD

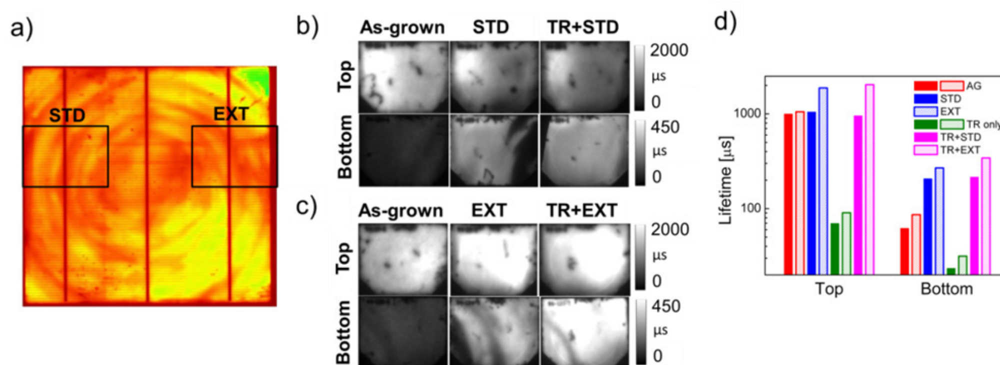

Fig. 2: PL image indicating where smaller samples were taken from within the original wafer (a) and smaller samples after each process, STD (b) and EXT (c). Images after TR and PDG+TR are not shown due to the low lifetime observed. (d) Lifetime measurements taken with QSSPC at 10^{15} cm^{-3} for wafers after STD (top) and EXT (bottom) processes.

compared to STD. The relative recombination strength remains approximately unchanged by TR+EXT compared to EXT.

To further elucidate the evolution of the spatially-resolved lifetime after each process, horizontal line scans after each process are shown in Fig. 3. Due to slight differences in alignment during wafer cutting, the line scans have been adjusted horizontally to compare lifetime magnitudes in the same wafer regions. Note that, especially in samples which have been subjected to PDG, WCT-120 markings can be seen in the photoluminescence images. This results in small, localized peaks in the line scans. Comparing STD and TR+STD (Fig. 3(a)), the lifetime is significantly improved by TR in the swirl region (the rightmost edge of the purple line before it drops to zero, indicating the edge of the sample). The shape of the curve is preserved from as-grown to TR+STD and from STD to STD+TR. However, lifetime is uniformly degraded after TR only. This trend is consistent with Fig. 3(b), with the added observation that the shapes of the EXT and TR+EXT are similar.

4. Discussion

Performance of NOC-Si solar cells is degraded by the presence of swirl defects especially in the bottom of the ingot. In this contribution, we evaluate the potential for high temperature processing to produce an ingot with uniformly high performance. The highest lifetimes for both the bottom and top of the ingot are achieved with the TR+EXT process. To determine the potential efficiency gain from this process, we plot experimental results for the measured efficiency versus measured minority carrier lifetime for the same NOC-Si ingot and cell process. To obtain solar cell efficiency values for the wafers measured in the lifetime experiment, we use a linear fit for solar cell efficiency as a function of ingot height (Fig. 1). Fig. 4 demonstrates the estimated solar cell efficiency as a function of lifetime (10^{15} cm^{-3}) measured for the PERT architecture on NOC-Si. We note that 10^{15} cm^{-3} does not necessarily correspond to the injection level during operation for PERT solar cells. Three vertical lines denote the measured lifetime for the bottom ingot sample in the as-grown, EXT, and TR+EXT states, where the efficiency gain is most impactful. These results demonstrate that the application of TR prior to PDG has the potential to produce solar cells with efficiencies comparable to those near the top of the ingot.

The change in lifetime after each process can be interpreted to gain insight into the dominant defects in NOC-Si. First, the bottom ingot material responds much more strongly to both PDG processes compared to the top ingot material. In top ingot material which is unaffected by swirl defects, the EXT process is more effective than the STD process for improving lifetime. Since the only difference is a low-temperature anneal at 650°C, these results suggest the presence of a getterable impurity (e.g. Cu, Ni, Fe, Cr) which segregates during growth and is sufficiently mobile at the annealing temperature [3]. The same trend is not observed in the bottom ingot material, likely due to the presence of oxide precipitates. In this part of the ingot, the TR process is unable to fully homogenize the performance after PDG. If the swirl patterns are presumed to coincide with oxygen-rich precipitates, these results

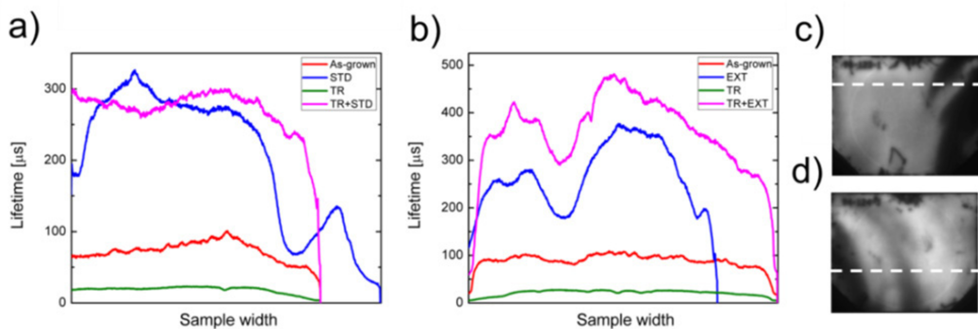

Fig. 3: Horizontal line scans of lifetime maps in each processing state are plotted with lifetime in microseconds on the y-axis and sample width on the x-axis. Due to inaccuracies during wafer cutting, the line scans are adjusted along the x-axis to compare the same wafer regions. (a) Line scans for the wafers subjected to STD gettering, taken from the region indicated in (c). (b) Line scans for the wafers subjected to EXT gettering, taken from the region indicated in (d).

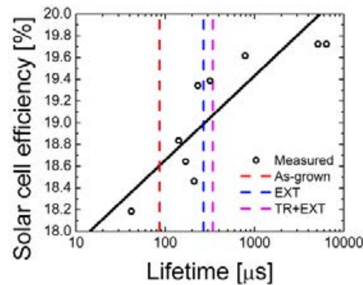

Fig. 4: Estimated correlation between PERT solar cell efficiency and minority carrier lifetime. Minority carrier lifetimes (10^{15} cm^{-3}) were measured for wafers at different heights from the same ingot. Solar cell efficiency was estimated as a function of ingot height with the data shown in Fig. 1. The estimated efficiencies for wafers as-grown and treated with the EXT and TR+EXT processes are delineated by the vertical dotted lines.

suggest that existing precipitates may be ripened by the gettering process and/or decorated with metals [11].

In contrast, the TR process applied before PDG results in spatially uniform lifetime in the bottom part of the ingot, with the as-grown patterns re-appearing after PDG. The average lifetime is higher after TR+PDG in these wafers. We conclude from these results that TR, when applied prior to PDG, serves to dissolve or reduce the size of existing oxide precipitates. When precipitates are not completely dissolved by TR, as we hypothesize is the case in our experiment, the precipitates are again ripened by PDG. This effect is enhanced by the EXT low temperature anneal. Further experiments and analysis should be conducted to determine the optimal TR temperature to eliminate the swirl pattern. Microstructural characterization techniques including selective etching and atom probe tomography will be employed to further investigate the nature of defects within the swirl regions.

Independent of the initial state of the material, lifetime degrades significantly after the current TR process. These data suggest a ubiquitously distributed recombination center. One explanation for this degradation is furnace contamination: lifetime is mostly uniform, lifetime is recovered when PDG is applied after TR, and lifetime degradation after high temperature processes has previously been observed [12], [13]. The TR process may allow fast-diffusing impurities into the sample, and the relatively fast cool traps these dissolved impurities within the sample. If this is the case, further improvements to the TR treatment may include slow cooling [14], annealing with a chlorinated gas to avoid metal ingress [7], and/or re-annealing at a low temperature to enhance metal out-diffusion while maintaining low oxygen diffusivity. An alternative explanation for the lifetime degradation is the formation of a different, presently unknown defect or defect complex within the wafer during the TR process. This hypothesis is supported by separate experiments in which lifetime degradation has been observed in similar wafers subjected to TR before and after furnace cleaning. Experiments comparing TR for float-zone and Cz in terms lifetime and/or resistivity changes may help discern between these two hypotheses.

5. Conclusion

In this contribution, we present the response of NOC-Si, a material which promises performance sufficient to support high-efficiency devices and reduced capex requirements compared to Cz, to high temperature processing, including phosphorous diffusion gettering and Tabula Rasa. We relate our results to PERT solar cell efficiency as a function of ingot height. The PDG processes indicate the presence of a getterable impurity in the as-grown material, while the spatially-resolved lifetime responses suggest the existence of oxide precipitates especially at the bottom of the ingot. Uniform lifetime degradation is observed after TR which we assign to a presently unknown defect. When TR is applied prior to PDG, lifetimes improve in the bottom of the ingot and the relative recombination strength of swirl regions is maintained and/or reduced. Future work includes optimization of the TR process to achieve the dual goals of high lifetime and spatial homogenization, microstructural characterization (e.g. atom probe tomography) of suspected oxide precipitates within the swirl defect patterns, and experiments to deduce the nature of the dominant defect after TR.

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