



## Power Electronics Thermal Management

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USDOE Vehicle Technologies Office Annual

Merit Review and Peer Evaluation,

Washington, D. C., June 6, 2017

EDT078

NREL/PR-5400-68077

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## Timeline

- Project start date: 2017
- Project end date: 2019
- Percent complete: 30%

## Budget

- Total project funding
  - DOE share: \$493K
- Funding for FY 2017: \$493K

## Barriers

- Size and Weight
- Performance and Lifetime
- Cost

## Partners

- John Deere
- Kyocera
- Oak Ridge National Laboratory (ORNL)
- Project Lead – National Renewable Energy Laboratory (NREL)

## Why is thermal management essential?

- ✓ Manage and dissipate heat
- ✓ Limit failure, increase reliability
- ✓ Increase power density

**Transition to wide-bandgap (WBG) devices changes, but does not reduce, need for thermal management**

## WBG devices

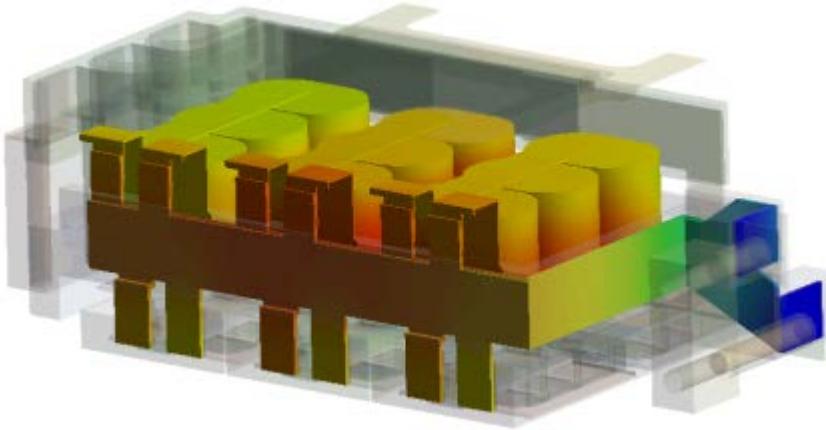
- More efficient → Less heat
- Yield and cost issues → Smaller die sizes/Reduced area
- Reduced area → Increased heat flux
- Higher junction temperature → Larger temperature gradients, impacts other components that may not tolerate higher temperatures:
  - At the module level: bonded interface materials, thermal greases
  - At the inverter level: DC-link capacitors, electrical boards

**Objective:** Develop thermal management techniques to enable high-temperature WBG devices in automotive power electronics

- Estimate component temperatures (e.g., capacitor, electrical board, solders) under elevated device temperature conditions
- Evaluate the effect of different under-hood (all-electric, hybrid electric) temperature environments on component temperatures
- Evaluate thermal management strategies for novel, compact inverter designs

## Power Electronics Thermal Management

WBG Power Electronics Thermal Management



Advanced Cooling Technologies for John Deere Inverter (cooperative research and development agreement [CRADA])

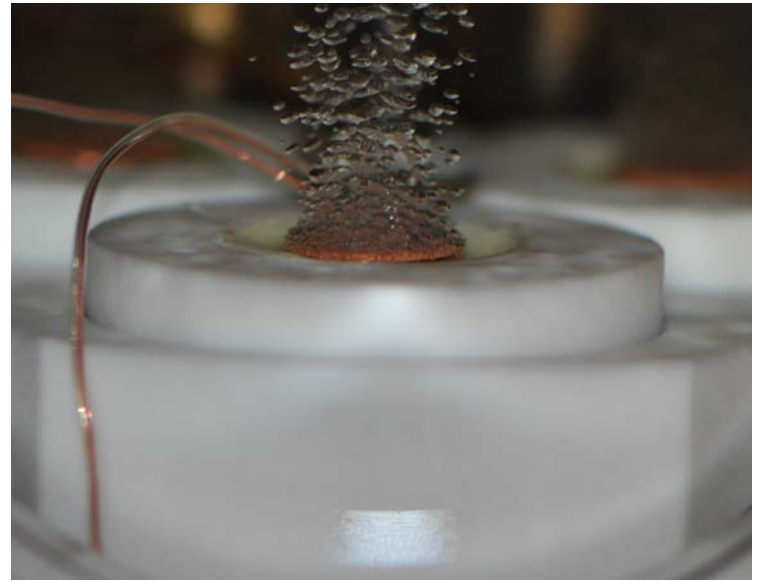
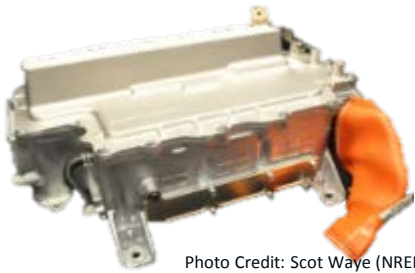


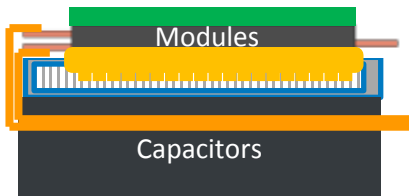
Photo Credit: Gilbert Moreno (NREL)

## WBG Power Electronics Thermal Management

Create thermal models of an automotive inverter

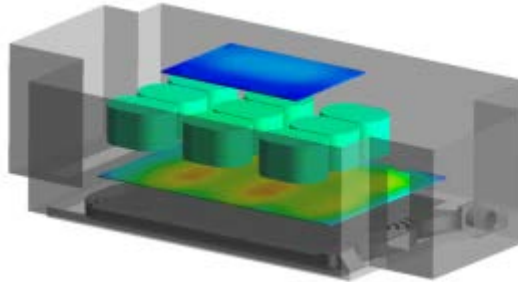


Validate the thermal models



Advanced compact inverter designs

Simulate WBG operation using the inverter model



Simulate elevated junction temperature conditions (up to 250°C)

Evaluate effect of different under-hood temperature environments (hybrid and all-electric)

Identify the components (e.g., capacitor) that are not expected to survive WBG conditions

Develop thermal management strategies for WBG-based inverters

Cooling strategies

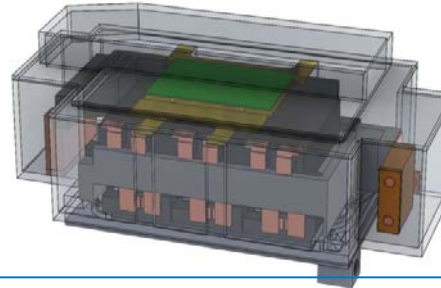
- Capacitor cooling
- Bus bar cooling
- Aggressive thermal management solutions



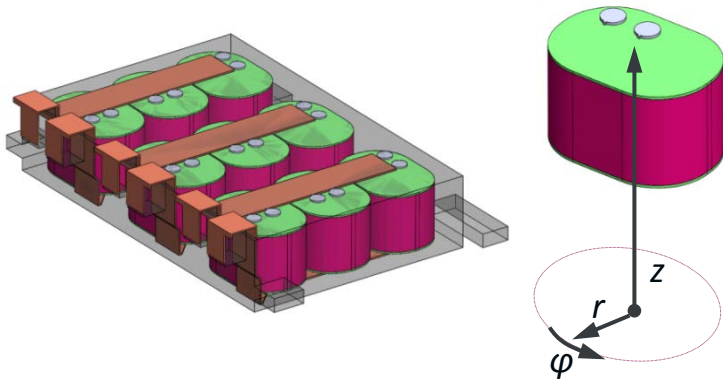
Experimentally validate some key thermal management concepts

# Inverter Model Description

## 2012 Nissan LEAF inverter



### Capacitors: Metalized film



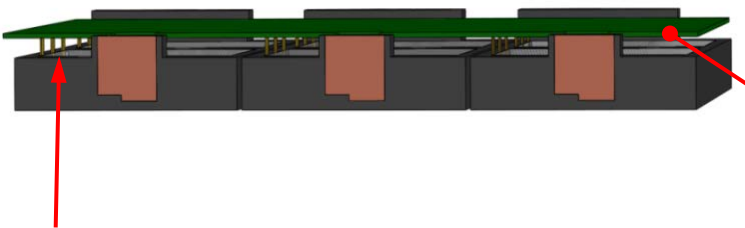
Capacitor winding thermal conductivity ( $k$ )

$$k_z = k_\phi = 0.46 \text{ W/m-K}$$

$$k_r = 0.16 \text{ W/m-K}$$

**Model-predicted capacitor temperature within  $\pm 1^\circ\text{C}$  of experimental data**

### Power modules and gate driver board



Electrical board thermal conductivity ( $k$ )

$$k_x = k_y = 0.81 \text{ W/m-K}$$

$$k_z = 0.29 \text{ W/m-K}$$

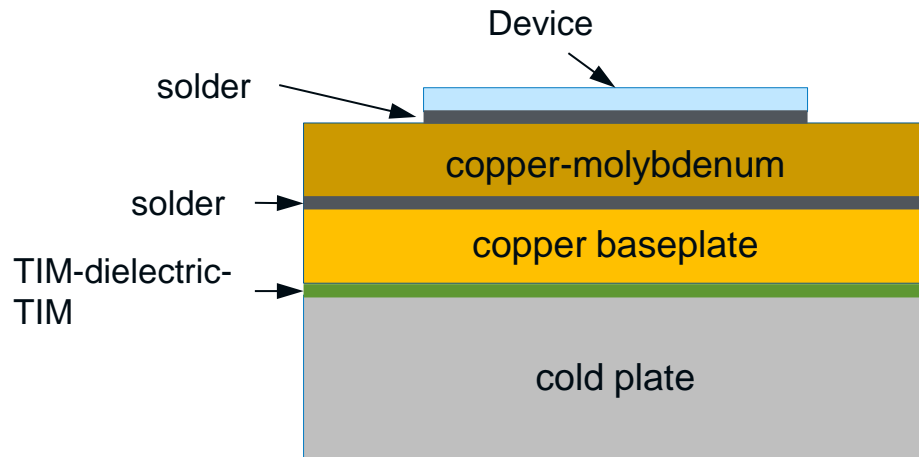
**Model-predicted junction-to-coolant resistance within  $\pm 6\%$  of experimental data**

Electrical pins included to account for the thermal path from the devices to the gate driver board



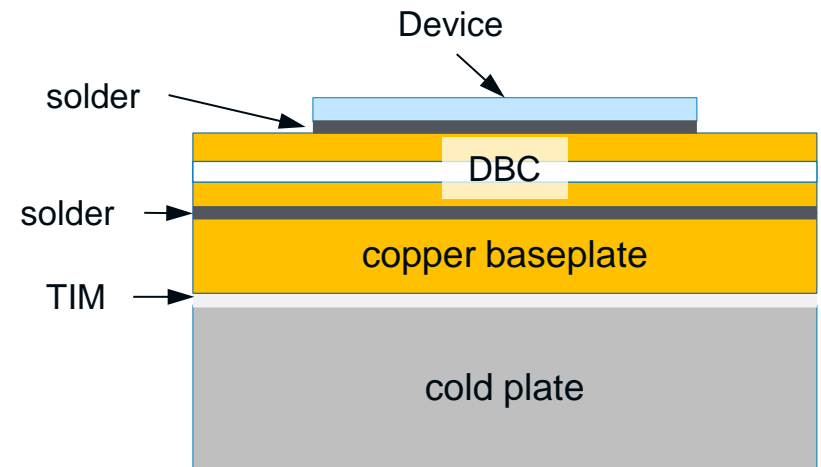
# Inverter Model Description

**Created two models – Attempt to account for the effect of different inverter designs on component temperatures**



**LEAF**

- Uses flexible film as the dielectric
- Uses two thermal interface material (TIM) layers



**LEAF (DBC)**

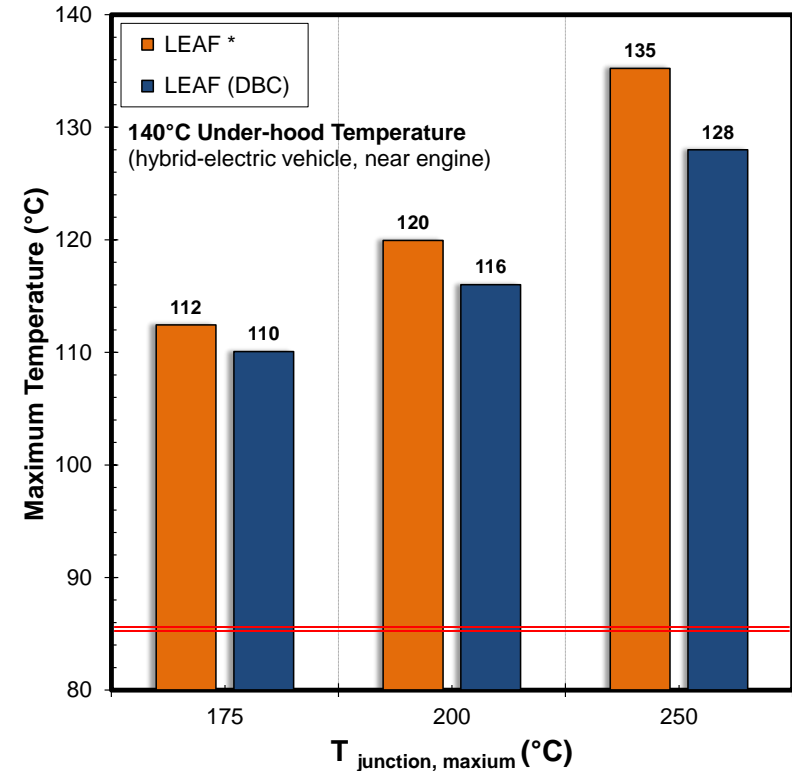
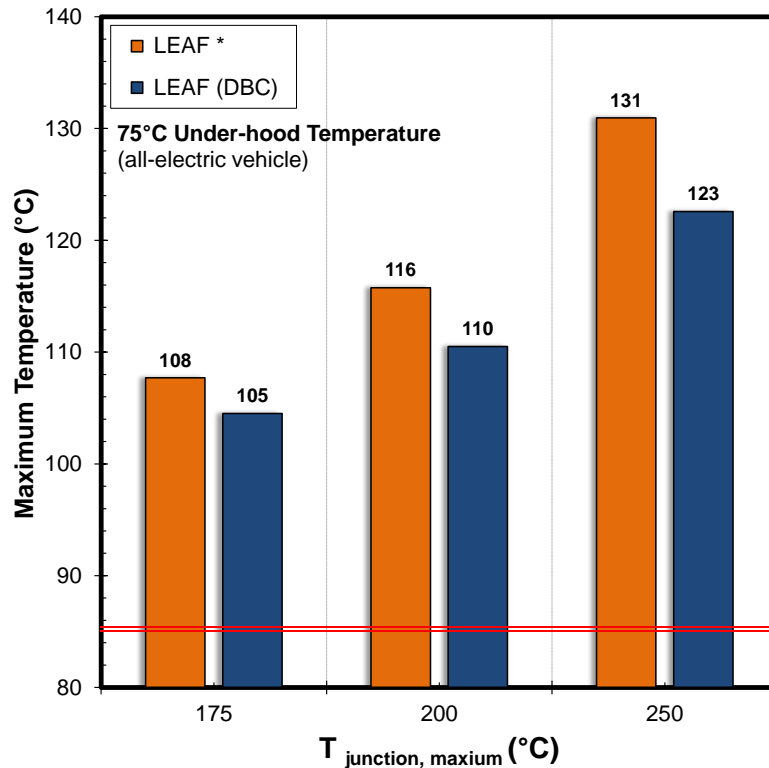
- Uses direct-bond copper (DBC) substrate as the dielectric
- Has 28% lower thermal resistance compared with flexible-film design
- Typical of most inverter designs



# Milestones / Approach

Date	Description of Milestone or Go/No-Go Decision
December 2016 (complete)	<b>Go/No-Go:</b> Model the thermal performance of various inverter designs and evaluate the effect of the thermal management concepts developed on each type of inverter.
March 2017 (complete)	<b>Milestone:</b> Model the effects of degrading material thermal properties (e.g., increasing heat generation rates and thermal resistance)
June 2017 (in-progress)	<b>Milestone:</b> Model heating-related effects associated with integrating the inverter close to the electric motor.
September 2017 (in-progress)	<b>Milestone:</b> Summarize the cooling concepts developed and down select one or two concepts for experimental validation.

# Accomplishments: Computed Capacitor Temperatures

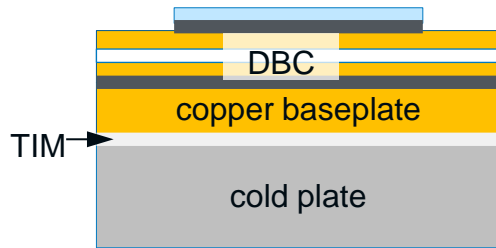


- Increasing under-hood temperature does not have a significant effect on capacitor temperatures
- For all cases, capacitors exceed 85°C (typical limit of polypropylene film capacitors)
- Lower junction-to-coolant resistance of DBC-based design provides lower capacitor temperatures
- Power module's heat is the primary reason for excessive capacitor temperatures

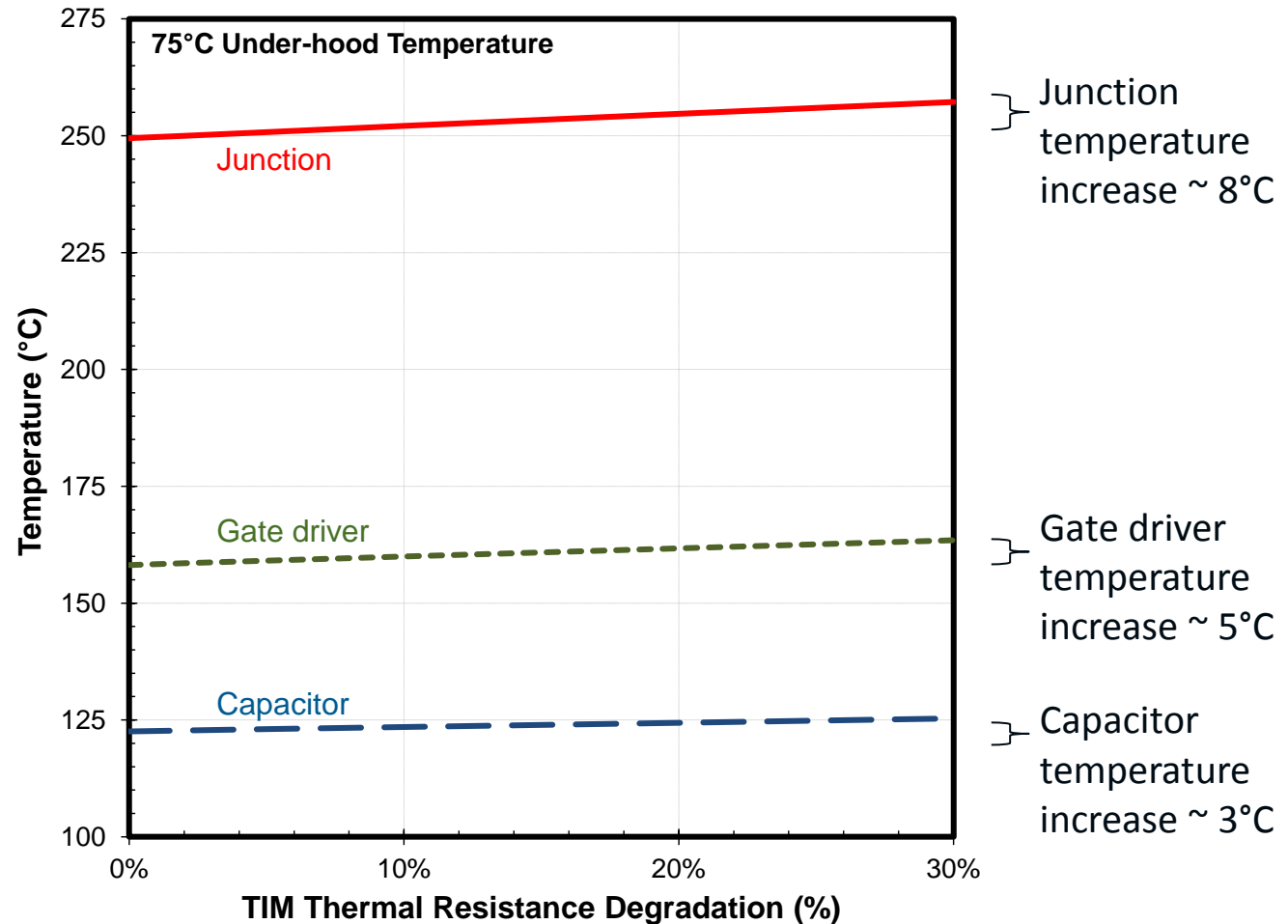
\* Results reported last year

# Accomplishments: TIM Degradation Effects

## DBC Design

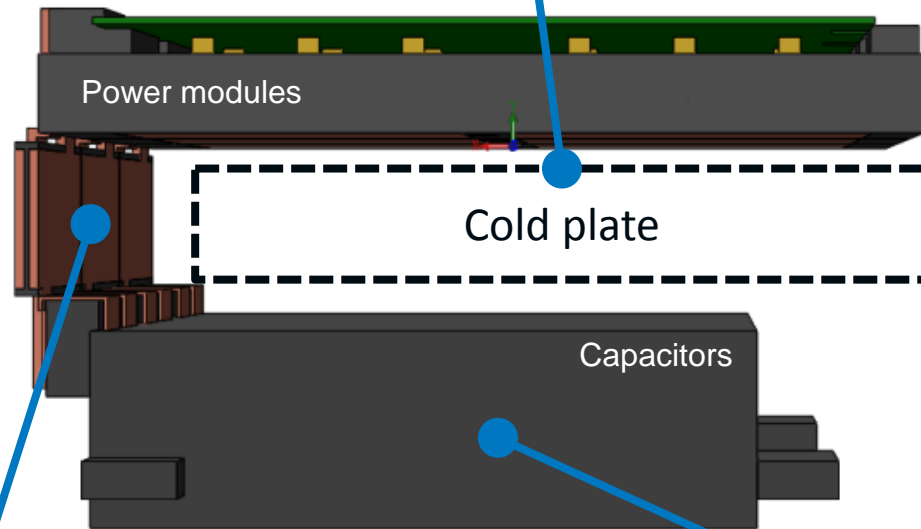


Initial TIM thermal resistance =  $55 \text{ mm}^2\text{-K/W}$



# Accomplishments: Capacitor Cooling Strategies

1. Improved power module cooling

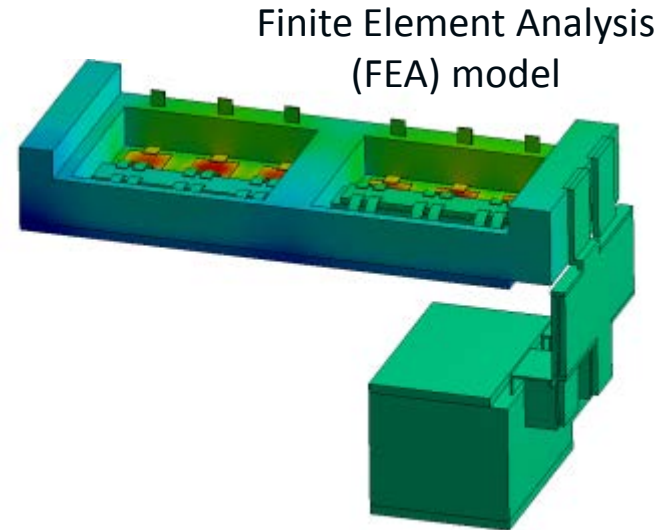
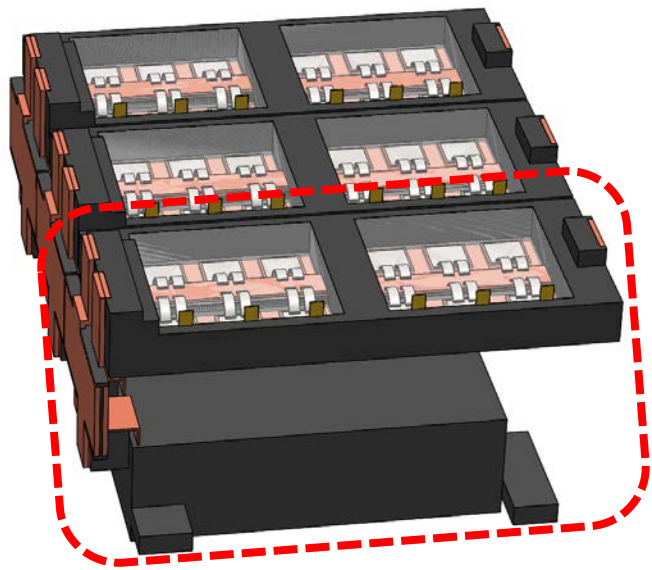


3. Cooling the DC bus bars using cold plates (one or two sides)

2. Cooling the capacitors using cold plates (one or two sides)

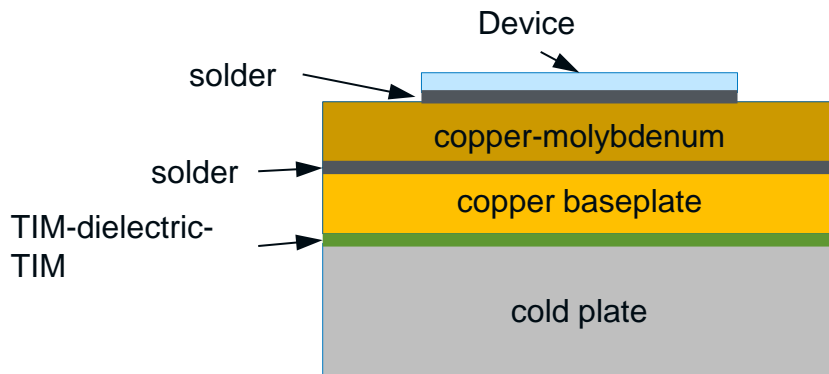
- Used a coolant temperature of 65°C
- These three capacitor-cooling strategies were evaluated on four inverter configurations

# Accomplishments: Inverter Configurations Evaluated

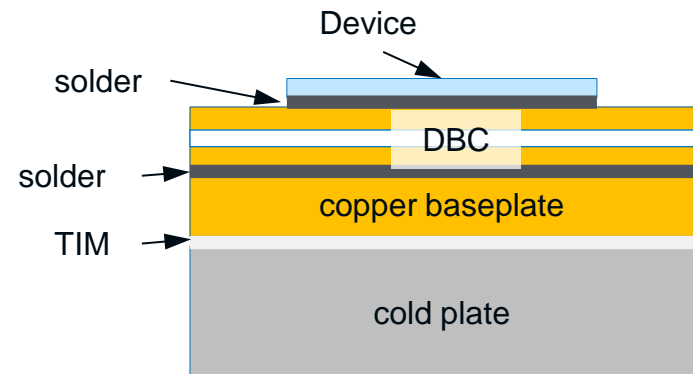


Two module configurations evaluated

## I. Flexible dielectric (LEAF) configuration



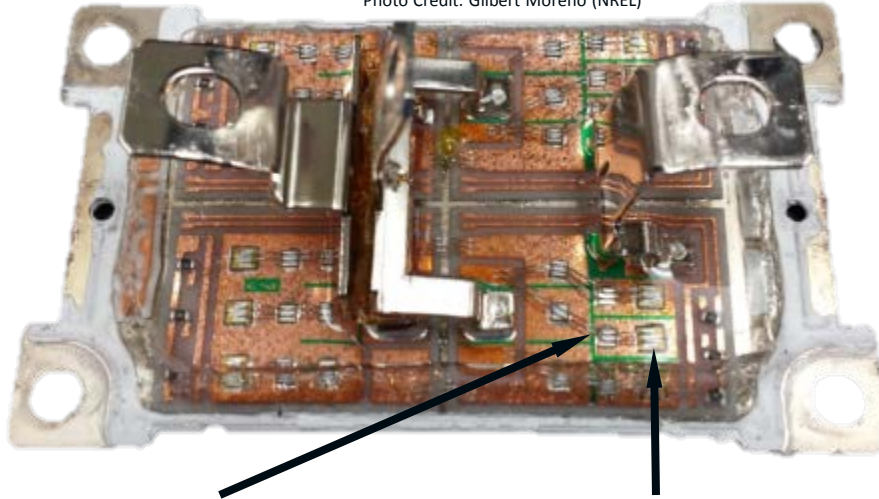
## II. DBC module [LEAF (DBC)] configuration



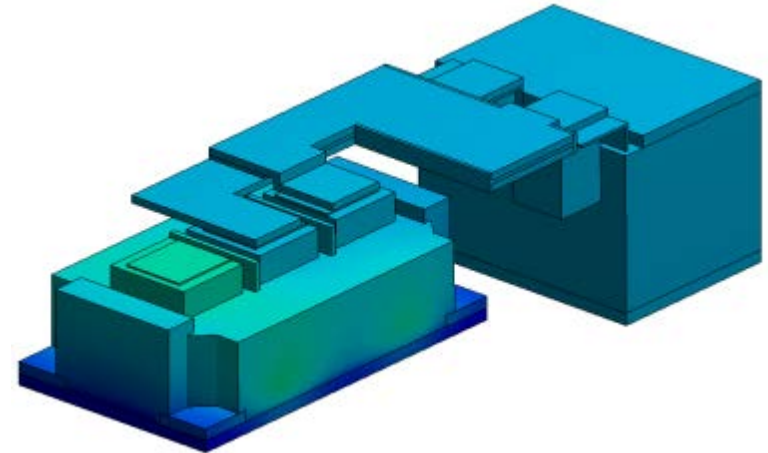
# Accomplishments: Inverter Configurations Evaluated

## Cree Silicon Carbide Module (DBC substrate, aluminum-nitride ceramic)

Photo Credit: Gilbert Moreno (NREL)



Diodes ( $2.3 \times 2.3$  mm) MOSFETs ( $3.1 \times 3.4$  mm)



FEA model

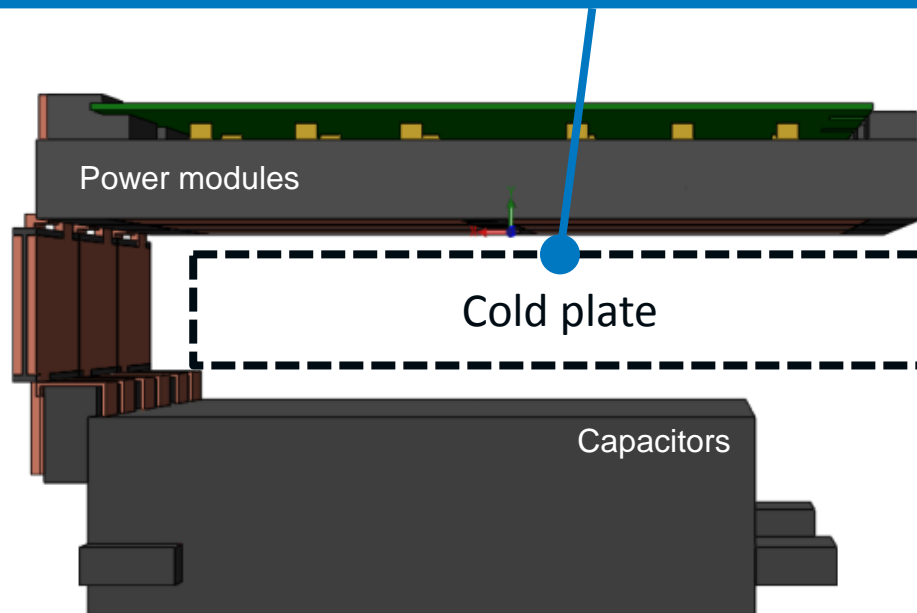
## Two module configurations evaluated:

- III. Cold plate (CP) cooled with TIM layer between module and cold plate
- IV. Baseplate (BP) cooled, no TIM layer

MOSFET: metal-oxide-semiconductor field-effect transistor

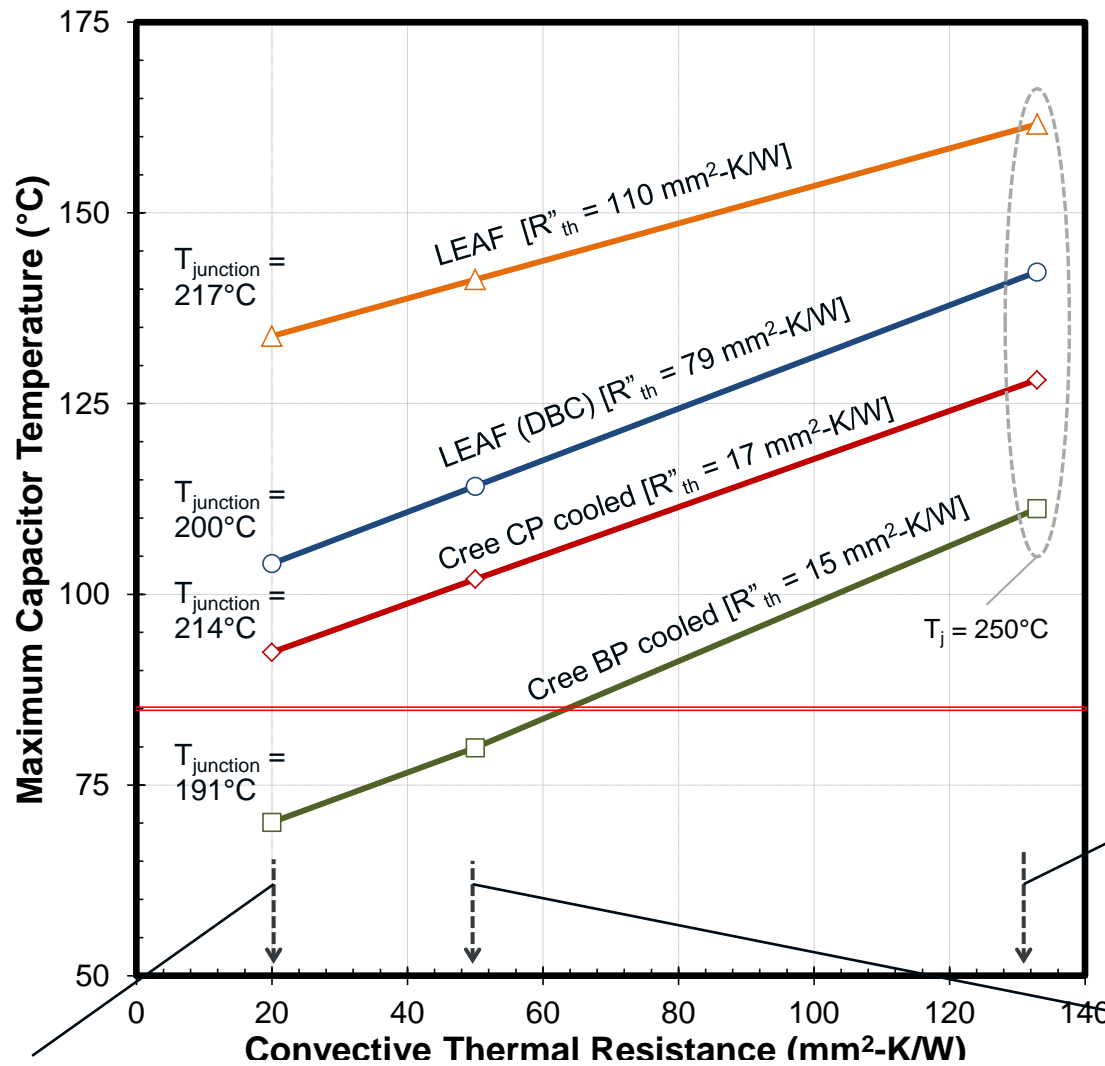
# Accomplishments: Capacitor Cooling Strategies

1. Improved power module cooling
  - Conventional cold plate (*lowest performance*)
  - High-performance, commercially available cold plate
  - Jet impingement-microchannel cold plate (*highest performance*)





# Accomplishments: Improved Module Cooling



Reduced capacitor temperatures by as much as ~40°C using a very-high performance cold plate

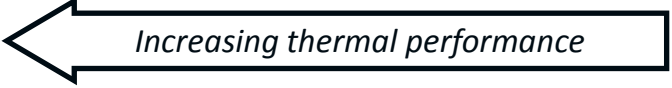
Photo Credit: Gilbert Moreno (NREL)



Conventional cold plate

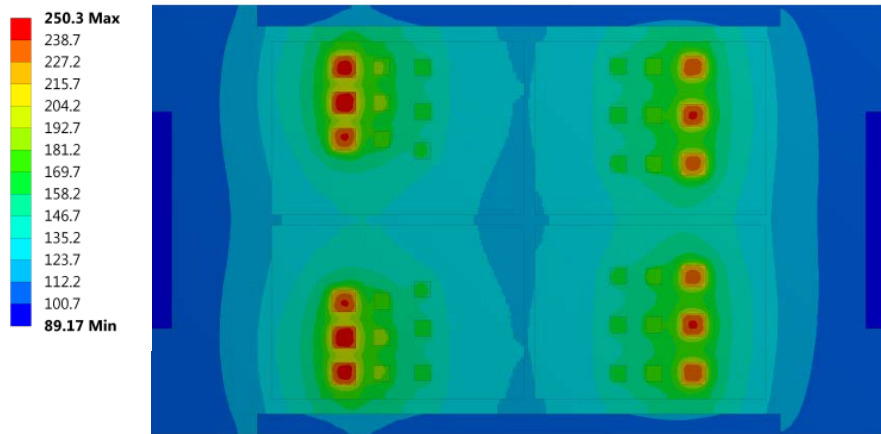
High-performance, commercially available cold plate

Jet impingement-microchannel cold plate



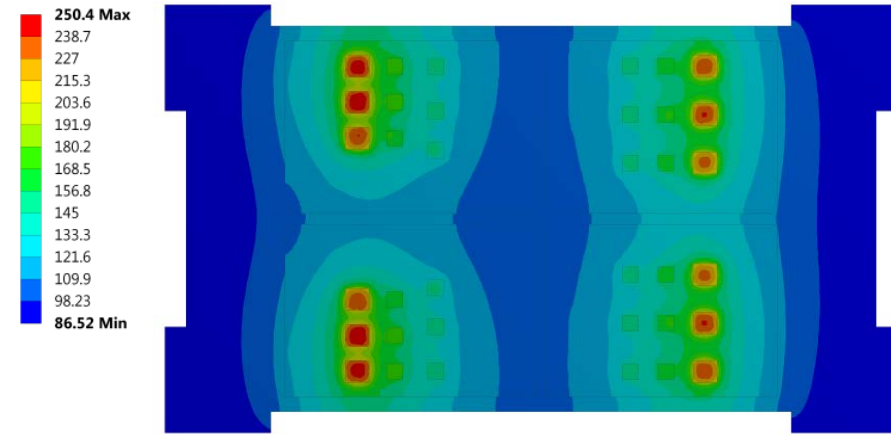
# Accomplishments: Improved Module Cooling

Cree CP cooled



$$R''_{thj-c} = 17 \text{ mm}^2/\text{K}/\text{W}$$

Cree BP cooled



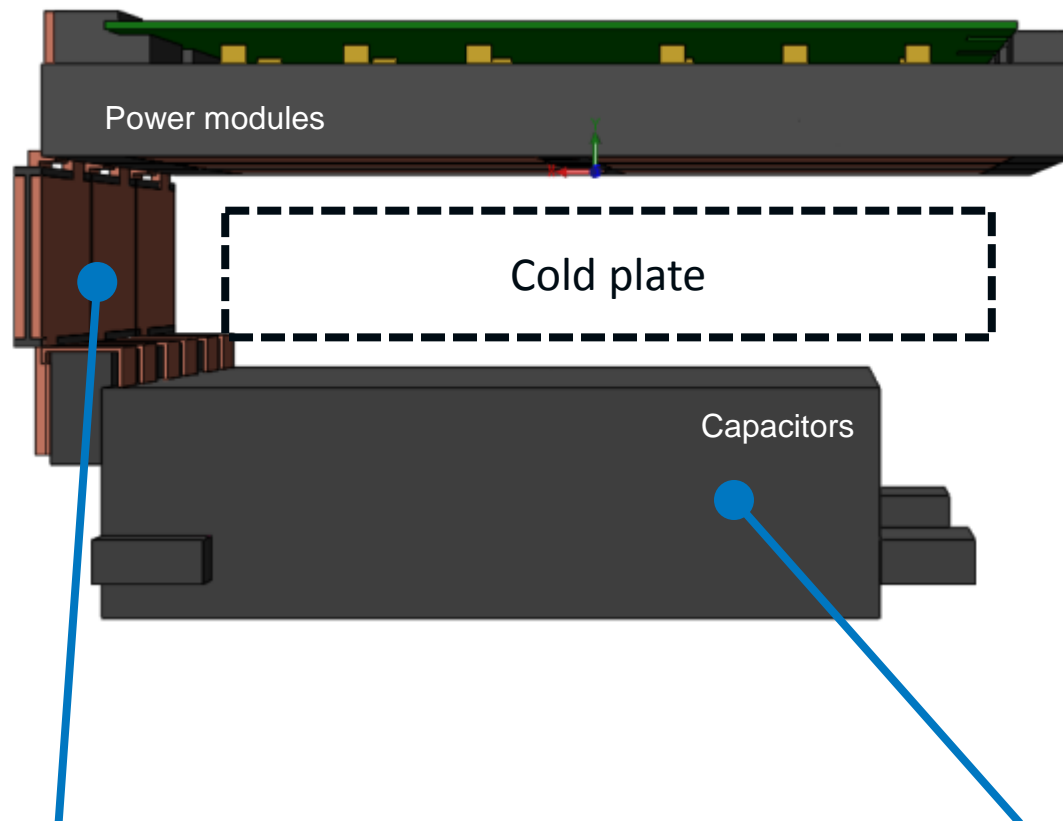
$$R''_{thj-c} = 15 \text{ mm}^2/\text{K}/\text{W}$$

(11% lower than CP-cooled case)

## Reducing the junction-to-coolant thermal resistance

- Enables higher heat dissipation
- Reduces heat spreading on module, which **lowers capacitor and gate driver temperatures**
- Enables compact packaging (**increases power density**)

# Accomplishments: Capacitor Cooling Strategies



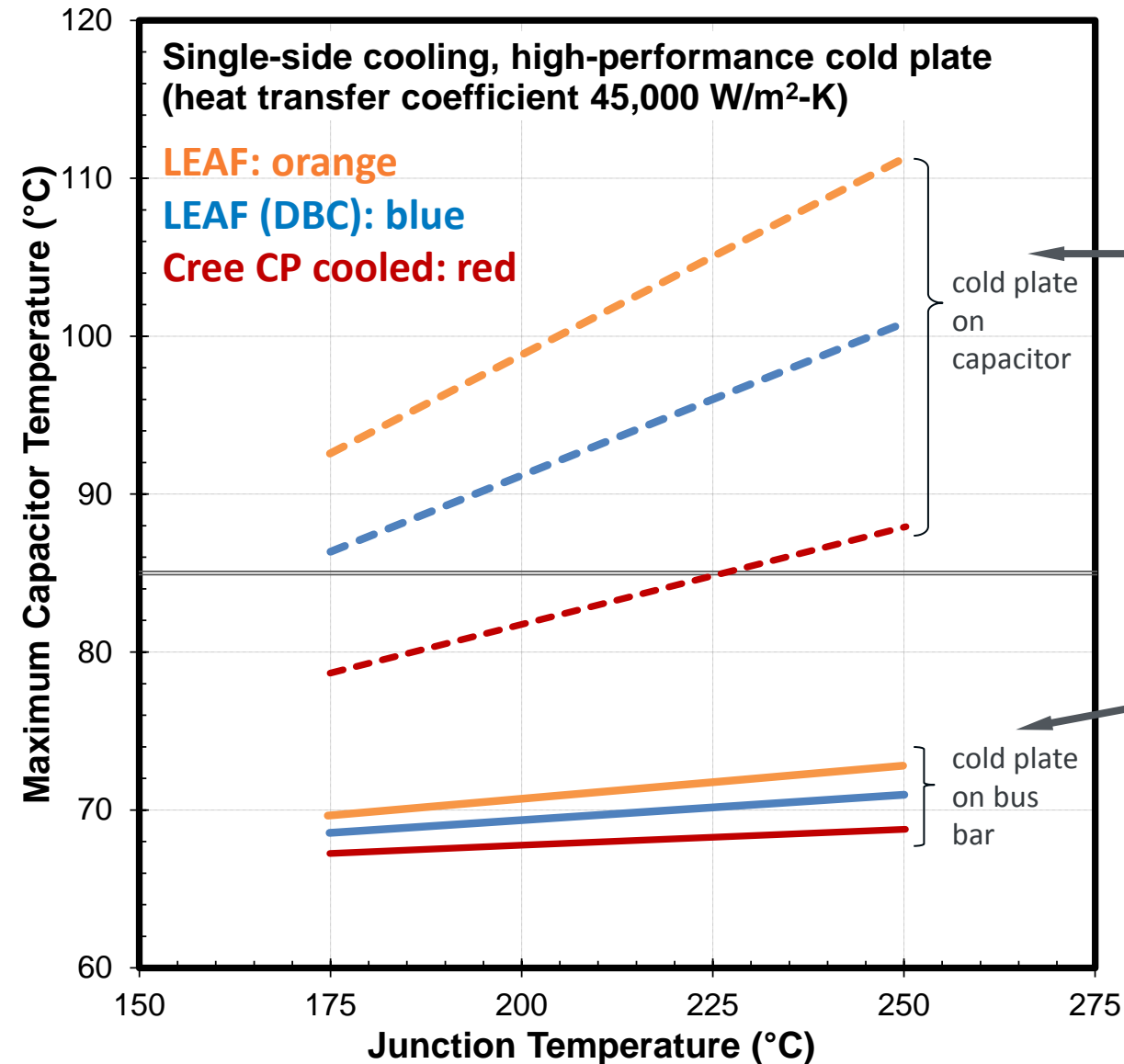
### 3. Cooling the DC bus bars using cold plates (one or two sides)

- Used a 3-mm-thick aluminum cold plate
- Included effect of dielectric pad layer (contact resistance =  $180 \text{ mm}^2\text{-K/W}$ )

### 2. Cooling the capacitors using cold plates (one or two sides)

- Used a 3-mm-thick aluminum cold plate
- Included effect of TIM layer (contact resistance =  $55 \text{ mm}^2\text{-K/W}$ )

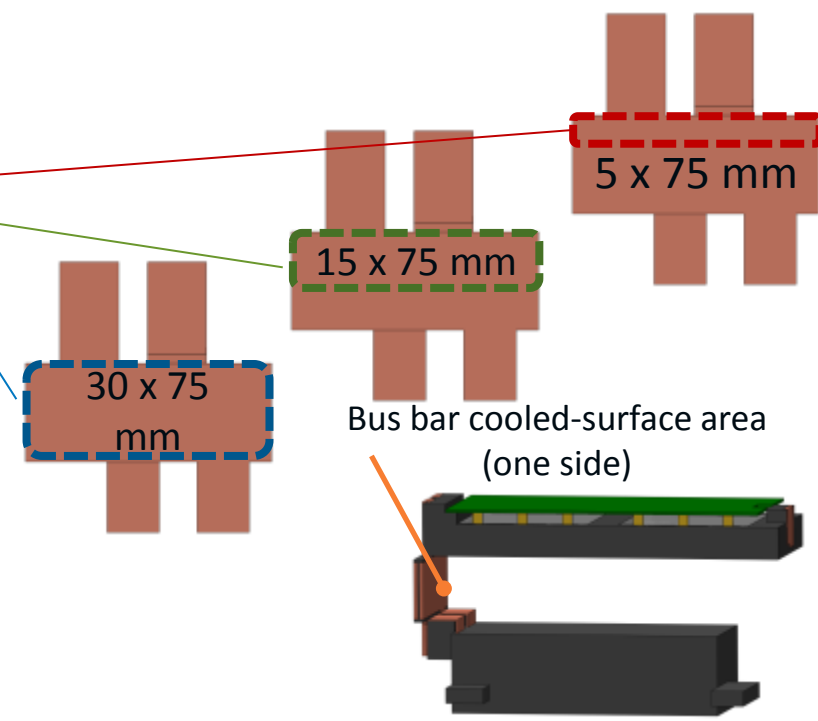
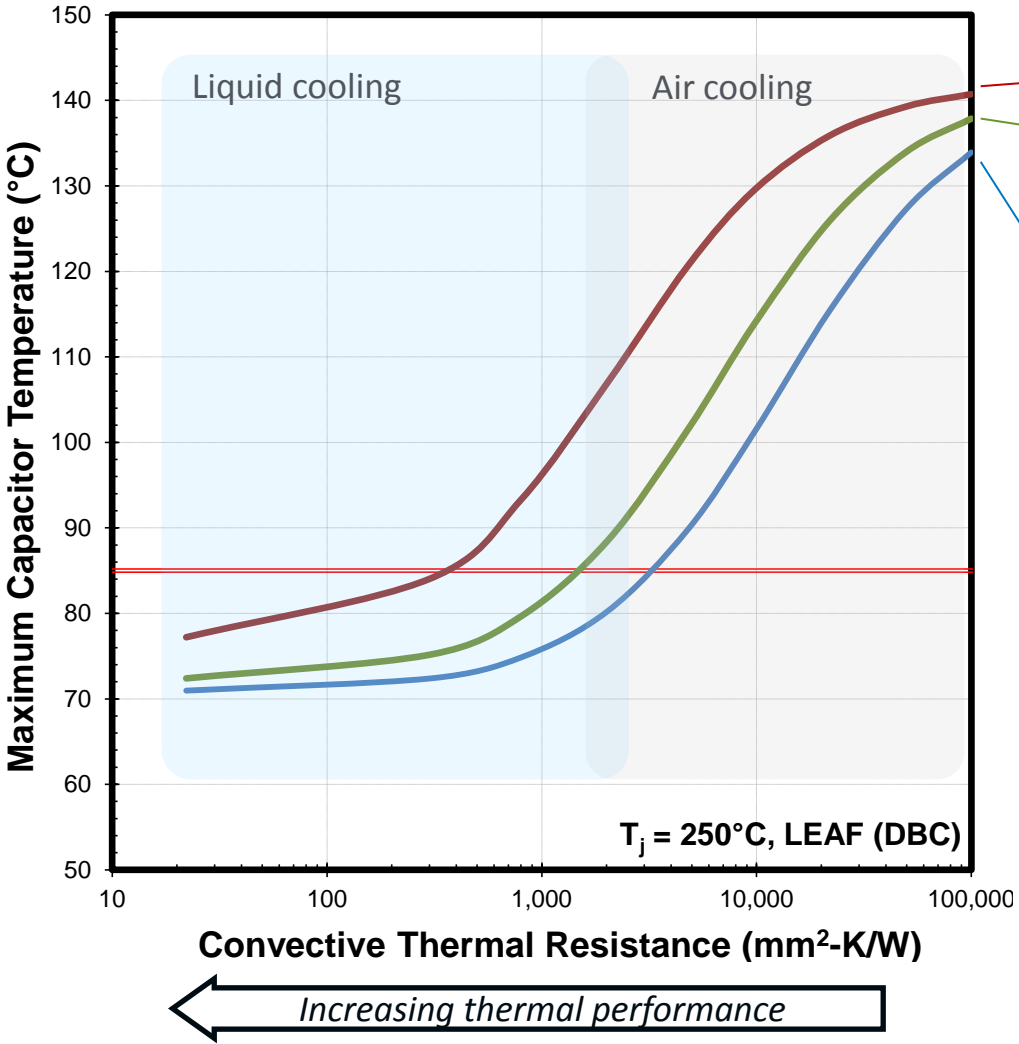
# Accomplishments: Comparing Capacitor Cooling Strategies



Poor capacitor thermal conductivity limits effect of using cold plates on capacitors

Cooling the bus bars is more effective at reducing capacitor temperatures

# Accomplishments: Capacitor Cooling Strategies-Bus Bar Cooling



Achieve capacitor temperatures < 85°C at 250°C junction temperatures using

- Small bus bar cooled area
- Relatively high convective thermal resistance (inexpensive cold plate)

Similar trends observed for other inverter configurations

# Response to Previous Year Reviewers' Comments

**This project is new for FY2017 as a partner with the power electronics activities at ORNL, but reviewer comments are provided below for the prior work.**

- The reviewer commented that the 140°C capacitor temperatures were consistent with what others have observed and questioned if there is a proposed solution.
  - *Model results indicated that a bus bar cooling strategy using cold plates enables capacitor temperatures below 85°C at junction temperatures up to 250°C.*
- Reviewers commented that the applications of the thermal management techniques need to be better defined.
  - *The capacitor cooling strategies evaluated were conducted in such a way as to be applicable across a wide range of designs. For example, bus bar cooling can be designed into an inverter system using a custom-designed cold plate.*



*Bus bar surfaces potentially available for cooling (2015 BMW i3)*

Photo Credit: Xuhui Feng (NREL)

# Collaboration and Coordination with Other Institutions

- John Deere (industry): CRADA project to develop a power-dense, two-phase-cooled inverter
- Kyocera (industry): Evaluated substrate cooling configurations
- ORNL (national laboratory): Interactions related to ORNL's benchmarking work
- Interactions with other industry contacts

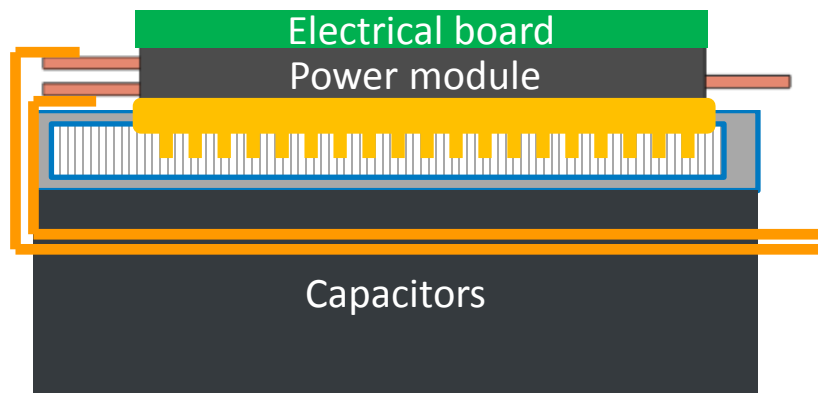


# Remaining Challenges and Barriers

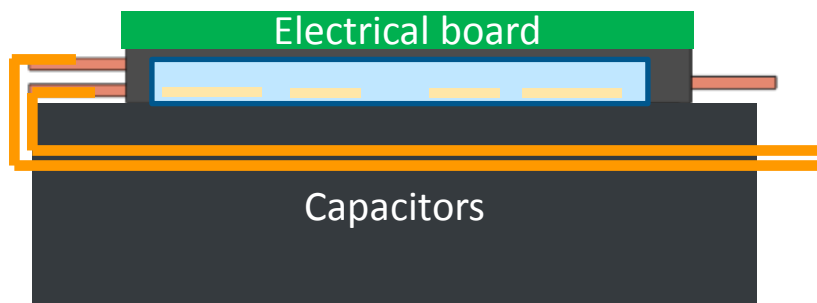
- Every inverter is unique, which makes it difficult to develop cooling strategies that are applicable to all inverters. We are working to develop thermal management concepts that are applicable to a wide range of inverter designs.

# Proposed Future Research

**Collaborate with ORNL to develop thermal management strategies for novel, compact inverter concepts**



- Develop small and modular cold plate designs for increased power density
- Develop device cooling strategies using dielectric fluids to reduce junction-to-coolant thermal resistance and reduce heat spreading



*Any proposed future work is subject to change based on funding levels*

# Summary

## Relevance

- Supports transition to high-efficiency WBG devices in automotive power electronics.
- Enables increased power density and use of lower cost components.

## Approach/Strategy

- Collaborate with ORNL to validate inverter-scale thermal models.
- Use validated models to simulate WBG conditions and to develop thermal management strategies to enable WBG-based power electronics systems.
- Collaborate with John Deere to develop and implement a power-dense two-phase cooled inverter.

## Technical Accomplishments

- Created inverter-scale thermal models and computed inverter component (e.g., capacitor, gate driver board) temperatures under high-temperature WBG conditions.
- Conducted over 2,000 simulations to evaluate various capacitor cooling strategies.
- Identified bus bar cooling as the most effective capacitor cooling strategy. This cooling approach enables capacitors to operate at temperatures below 85°C at junction temperatures up to 250°C.
- Collaborating with John Deere to develop a two-phase cooling strategy for their inverter.

## Collaborations

- John Deere
- Oak Ridge National Laboratory
- Kyocera

## **Acknowledgments**

Susan Rogers, U.S. Department of Energy

## **Team Members**

Kevin Bennion (NREL)  
Xuhui Feng (NREL)

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## **EDT Task Leader**

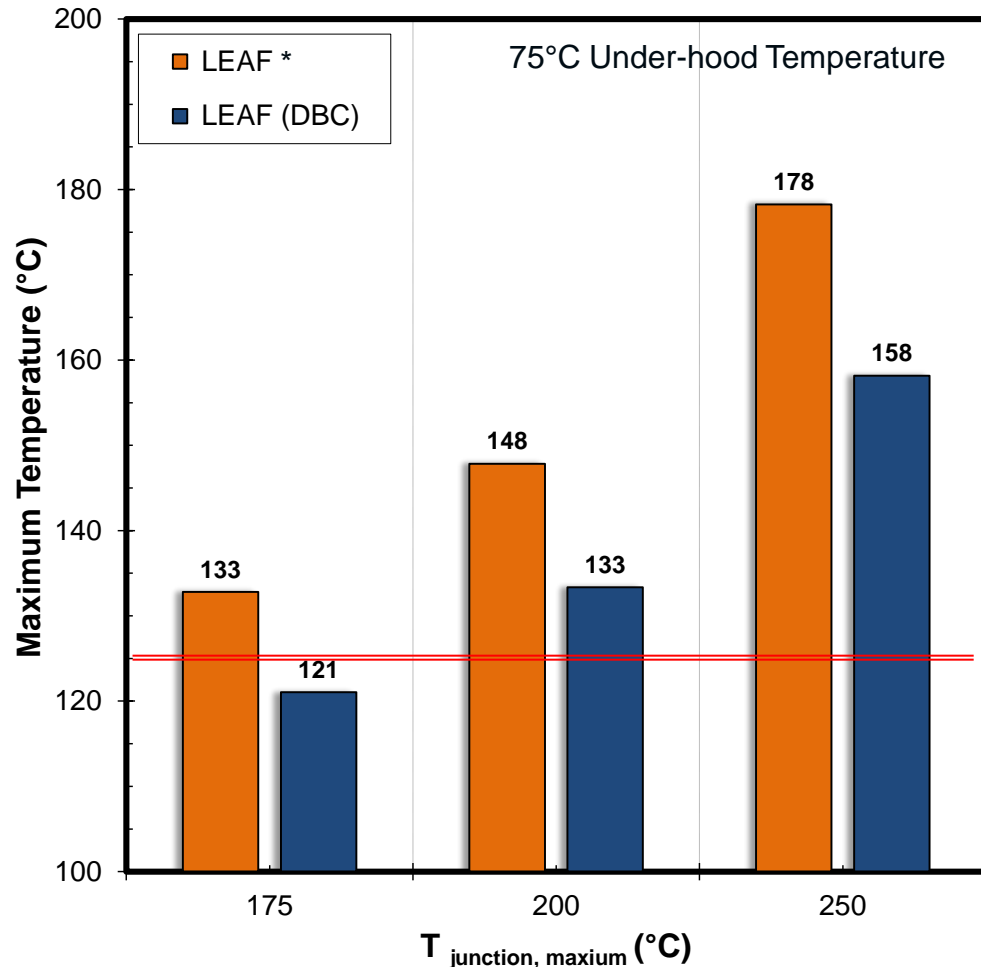
Sreekant Narumanchi  
Sreekant.Narumanchi@nrel.gov  
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# Technical Back-Up Slides

# Computed Gate Driver Board Temperatures

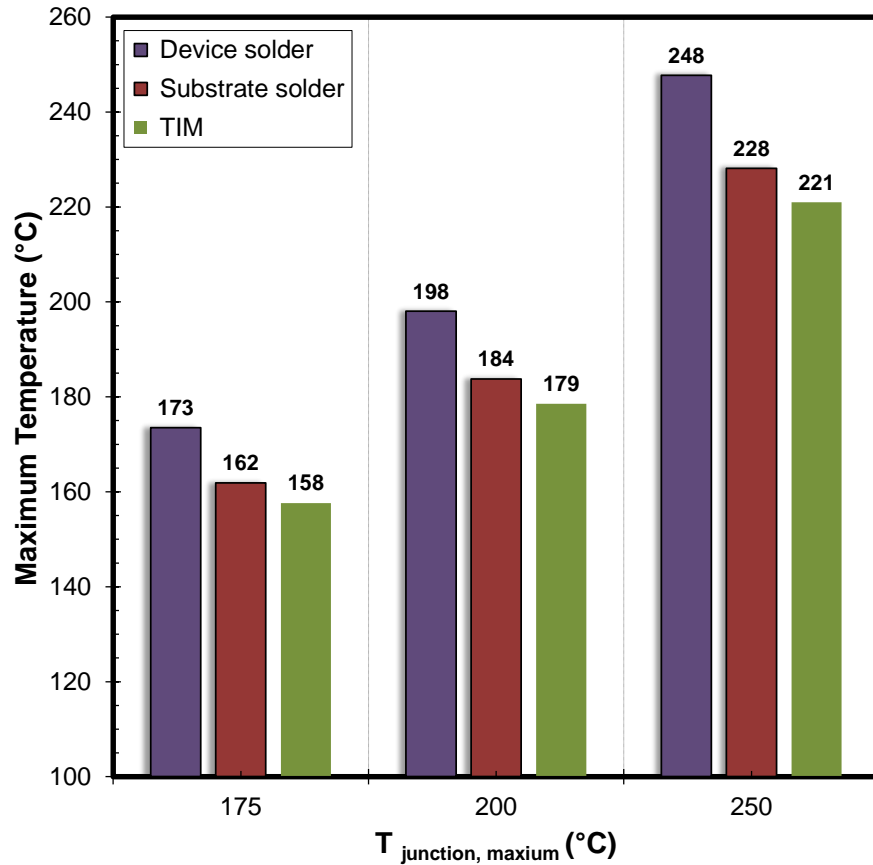
- Changing under-hood temperature has no effect on this component
- For almost all cases, gate driver board exceeds 125°C (typical temperature limit for electrical boards)
- Lower junction-to-coolant resistance of DBC-based design provides lower gate driver temperatures



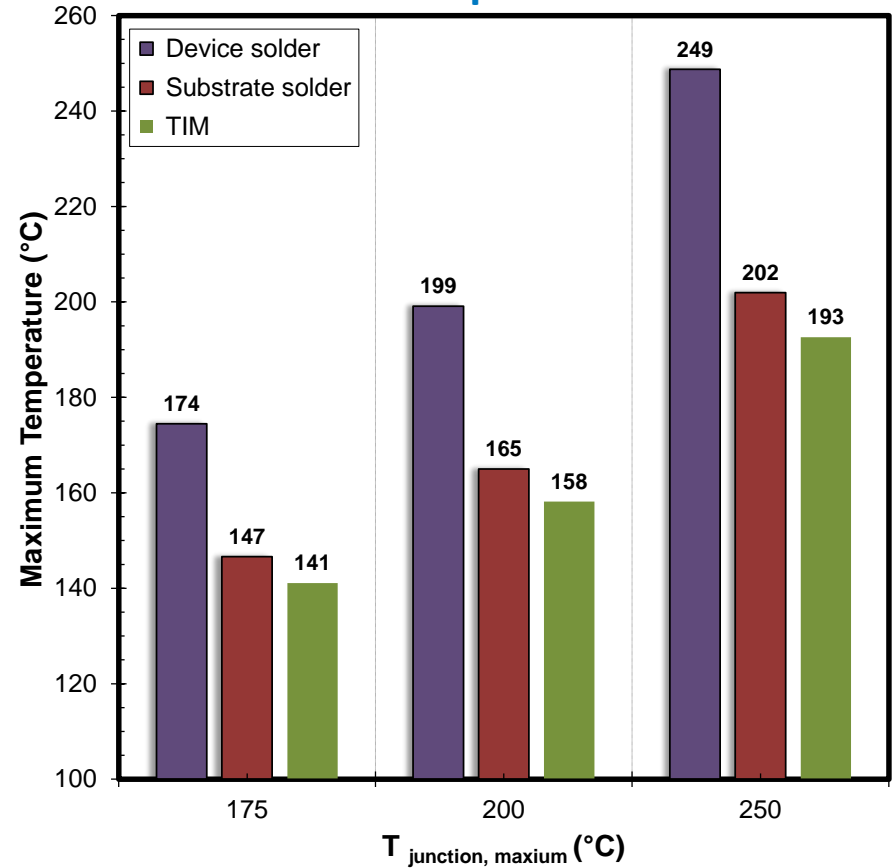
\* Results reported last year

# Computed Solder and TIM Temperatures

LEAF \*: 125°C under-hood temperature



LEAF (DBC): 125°C under-hood temperature

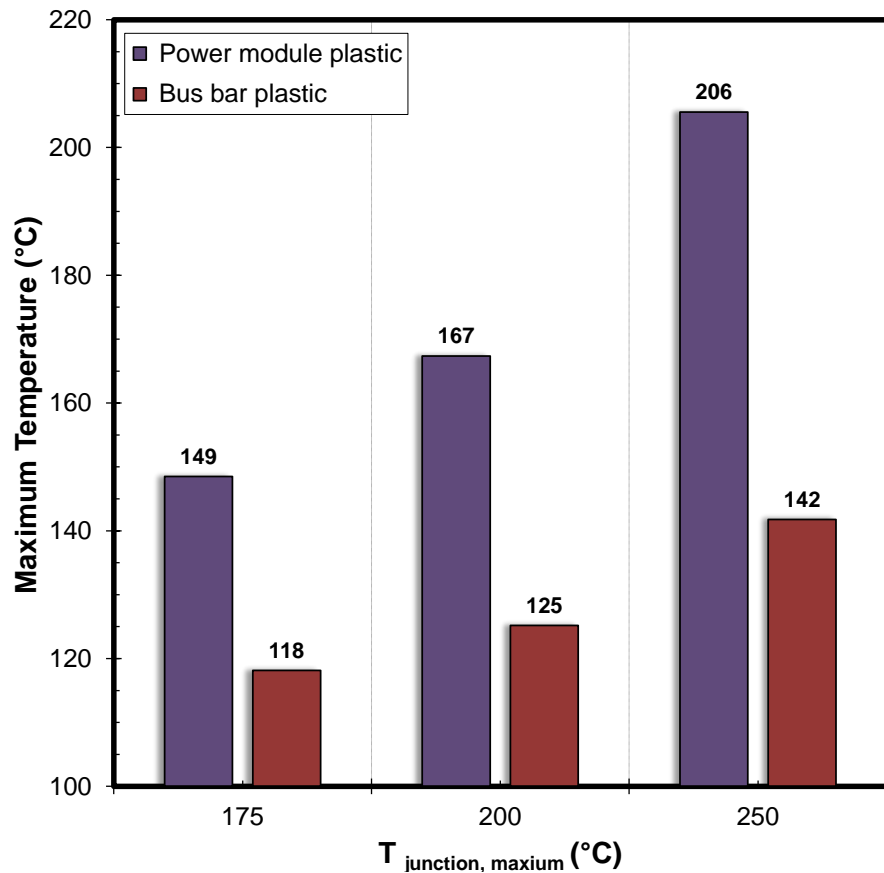


\* Results reported last year, but shown here for comparison

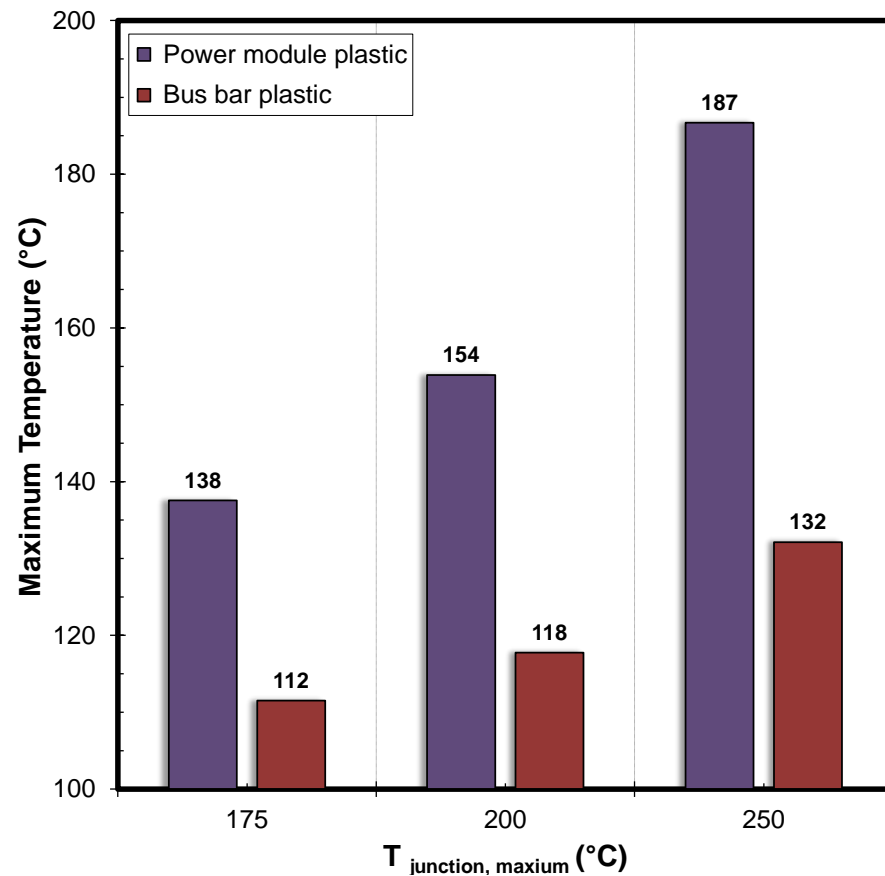


# Computed Molding Plastic Temperatures

LEAF \*: 125°C under-hood temperature

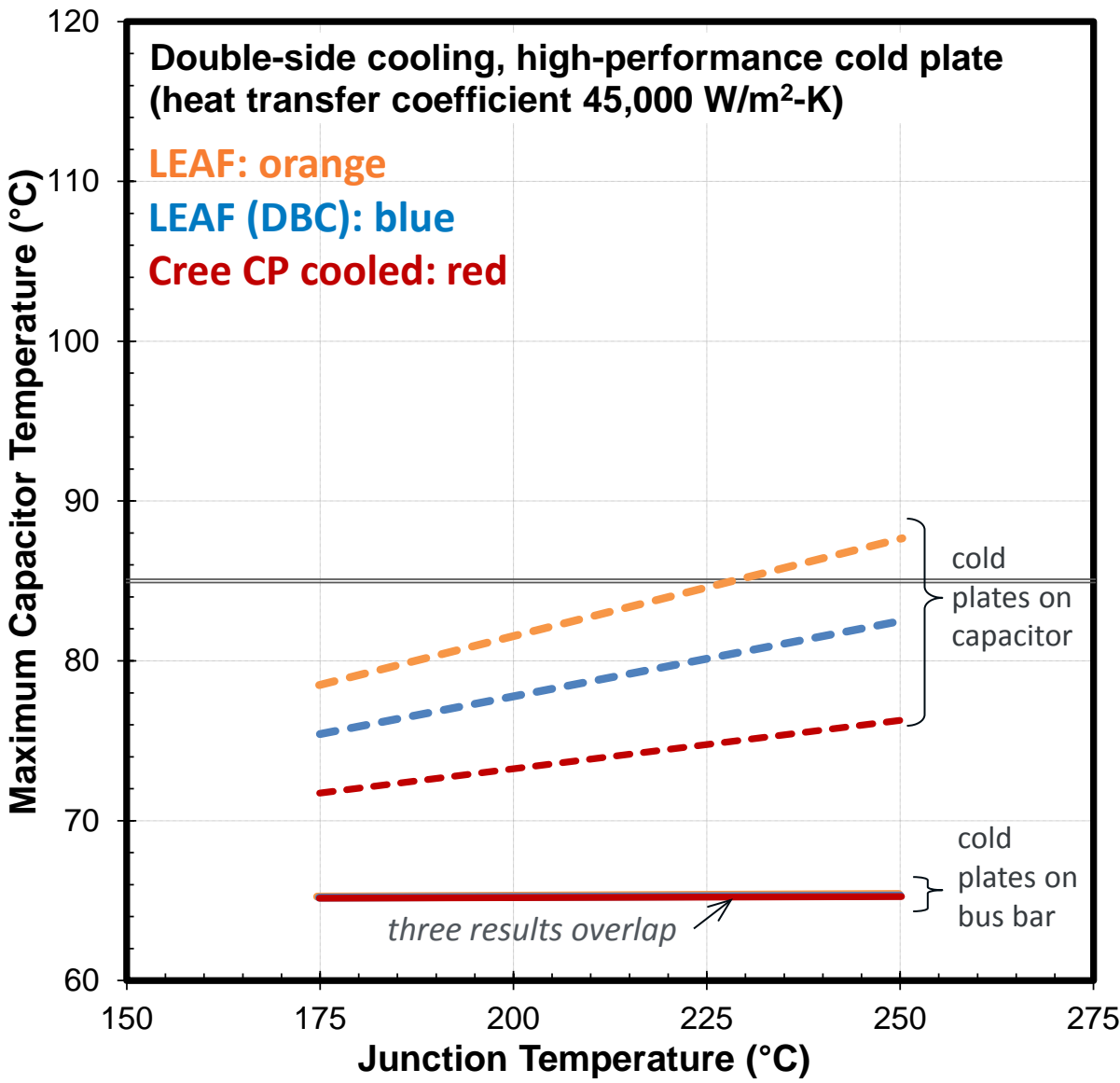


LEAF (DBC): 125°C under-hood temperature



\* Results reported last year, but shown here for comparison

# Comparing Capacitor Cooling Strategies



Use of two cold plates reduces temperatures – provides temperatures below 85°C for most cases