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Michelle Vaisman
Yale University

Qiang Li and Kei May Lau
Hong Kong University of Science and Technology

Nikhil Jain, Adele Tamboli, and Emily Warren
National Renewable Energy Laboratory

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GaAs Solar Cells on V-Grooved Silicon via Selective Area Growth

Michelle Vaisman, Nikhil Jain, Qiang Li, Kei May Lau, Adele C. Tamboli, and Emily L. Warren

National Renewable Energy Laboratory, Golden, CO 80401 USA; Yale University, New Haven, CT 06520; Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

***Abstract* — Interest in integrating III-Vs onto Si has recently resurged as a promising pathway towards high-efficiency, low-cost tandem photovoltaics. Here, we present single-junction GaAs solar cells grown monolithically on on-axis Si (001) substrates using V-grooves, selective area growth, and aspect ratio trapping to mitigate defect formation without the use of expensive, thick graded buffers, along with homoepitaxially grown GaAs solar cell test structures. The GaAs buffer grown directly on Si is free of antiphase domains and exhibits a relatively low TDD of 4×10^7 cm^{-2}, despite the lack of a graded buffer. These demonstration solar cells show promise for further improvements to III-V/Si tandems to enable cost-competitive photovoltaics.**

***Index Terms* – III-V on Si, GaAs, selective area growth, photovoltaic cell, solar energy, III-V semiconductor materials**

I. Introduction

In order to achieve high efficiency photovoltaics at a low cost, research on III-V integration onto Si has resurged in recent years [1]. Currently, bonding approaches lack the benefit of low-cost, large-area Si substrates, while current epitaxial approaches are disadvantaged by the need for expensive, thick graded buffers to achieve good material quality, thus undermining their commercial viability. Current metamorphic approaches utilize $GaAs_yP_{1-y}$ or $Si_{1-x}Ge_x$ graded buffers as thick as 3.6-10 μm [2, 3]. Cost modeling has predicted that even thinner buffers, 3.0 μm in thickness, would constitute nearly 25% of total monolithic III-V/Si dual-junction manufacturing cost, as seen in Fig. 1. Recently, heteroepitaxy of III-Vs on nano-patterned Si via selective area growth (SAG) was proposed as a pathway to achieve low-cost monolithic tandem devices [4].

III-V growth on Si without the use of graded buffers faces challenges with material polarity, as well as large lattice mismatch, both of which can cause defects detrimental to device performance. As graded buffers help control strain relief to minimize threading dislocation density (TDD) [5], large TDD is expected to pose a challenge which predominantly hinders the device open-circuit voltage (V_{OC}) and can also reduce short-circuit current density (J_{SC}) and fill factor (FF) [6-8]. Another material challenge is crack formation induced by the large difference in thermal expansion coefficients between GaAs and Si, which can cause issues such as electrical shunting and additional in-plane electrical resistance [9]. Recently, a GaAs on Si solar cell exhibited controlled crack formation through the use of millimeter-scale notches, achieving a V_{OC} of 0.87 V and efficiency (η) of 18% [10].

While such millimeter-scale approaches have been investigated, nano-scale approaches still remain unexplored for III-V/Si solar cell defect mitigation. Nano-patterns with aspect ratios >1 have been shown to mitigate challenges with lattice mismatch by drastically reducing TDD by confining threads to annihilate on pattern sidewalls [11]. Furthermore, antiphase domains (APDs) can be suppressed by growth on V-grooved Si (111) surfaces [12]. In this work, we grow a monolithic single-junction GaAs solar cell on a GaAs/Si template formed via SAG on nano-patterned V-grooved Si, achieving 5.0% efficiency. The GaAs/Si templates used in this work exhibit a TDD of ~4×10^7 cm^{-2} and have been employed as a promising platform for high-performance laser diodes [13]. Our work demonstrates progress towards a commercially viable III-V/Si tandem for low-cost, high efficiency photovoltaics (PV).

II. Experimental

The high quality GaAs/Si template was prepared as previously described [14]. An on-axis n-Si (001) substrate was prepared by patterning SiO_2 stripes along the [110] direction, followed by RCA and dilute 1% HF wet chemical cleanings, and a 45% KOH etch at 70°C for the formation of V-grooves that exposed (111) facets. Initial GaAs nucleation and growth of a 1.5 μm GaAs buffer was conducted with a two-step growth process [14] in a low-pressure 0.1 atm metal-organic

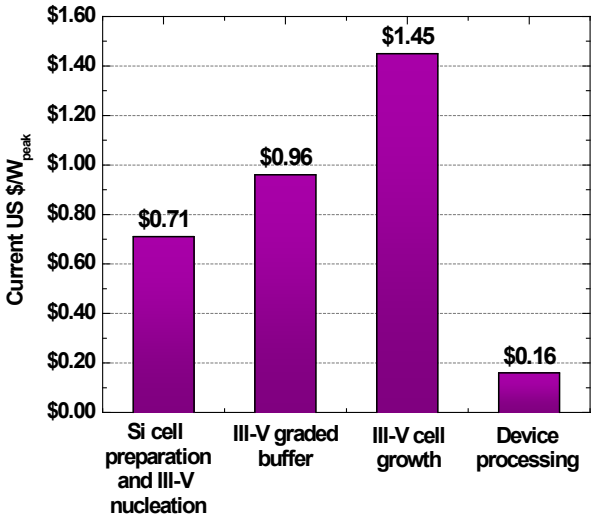

Figure 1. Techno-economic cost analysis conducted in 2013 predicts that the III-V graded buffer layer accounts for ~25% of the cost of a metamorphic III-V/Si tandem cell [15].

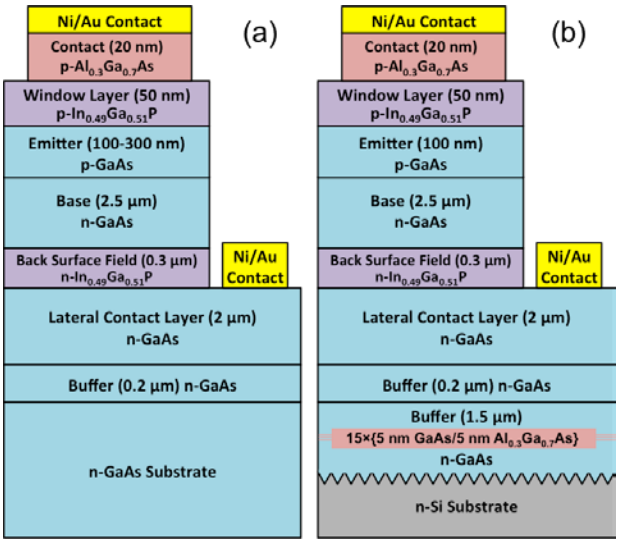

Figure 2. Schematic of (a) the homoepitaxially grown GaAs solar cells (MP423, MP425) and (b) the GaAs solar cell grown on a Si substrate (MP567).

chemical vapor deposition (MOCVD) system. An AlGaAs/GaAs superlattice was utilized to help control TDD [16]. The template was then shipped from Hong Kong to the National Renewable Energy Laboratory for growth in an atmospheric MOCVD chamber.

Device schematics for the individually grown GaAs solar cells can be seen in Fig. 2. The two initial GaAs solar cell test structures in Fig. 2(a) were compared to determine an appropriate cell design to grow on the GaAs/Si template. The first cell, MP423, was grown with a 300 nm emitter and lower Zn doping level compared to MP425's 100 nm emitter doping of p ~ 1×10^{19} cm^{-3}. A p-on-n structure was chosen in this work to account for the anticipated high defect density in the GaAs grown on Si, enabling slightly higher defect tolerance in the device due to the inherently lower hole mobilities, and thus diffusion lengths, of n-type GaAs [17]. Furthermore, a two top contact design was used to isolate the top cell performance from potential influence of the GaAs-Si interface, such as from high n-doping caused by Si diffusion into the GaAs. The GaAs cell grown on the GaAs/Si template (MP567) used the same structure as MP425 [Fig. 2(b)].

Solar cells were fabricated using conventional photolithography, metal electroplating, and solution-based mesa etching. No anti-reflection (AR) coatings were applied to our devices. Nomarski microscopy and atomic force microscopy were used to characterize surface morphology of our samples, while X-ray diffraction (XRD) and Ayer's model [18] was utilized for the determination of GaAs/Si template TDD. Lighted current-voltage (LIV) measurements were taken under 1-sun, AM1.5G illumination conditions with a custom-built Xe lamp solar simulator. External quantum efficiency (EQE) was characterized using a custom-built tool under chopped, monochromatic light.

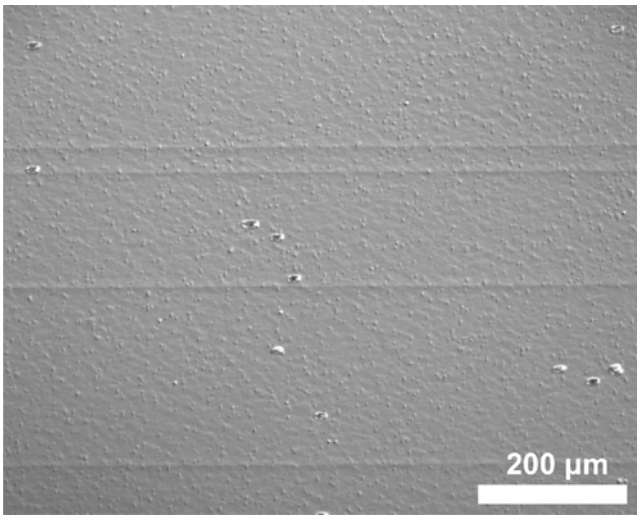

Figure 3. Nomarski microscopy image of our GaAs solar cell grown on a GaAs/Si template showing noticeable cracking.

III. Results and Discussion

The GaAs/Si template exhibited a smooth surface morphology with RMS roughness of 0.4-0.9 nm. Cracks were not found on the GaAs/Si templates, but crack formation was observed on the as-grown epitaxial material and GaAs solar cells on Si after processing (Fig. 3).

Our first cells grown homoepitaxially on GaAs substrates demonstrated high V_{OC} values of 1.03-1.04 V, indicative of good material quality (Table 1 and Fig. 4). The reduced emitter thickness in MP425 proved more optimal, enabling a larger J_{SC}. Despite the reduced emitter thickness, the increased emitter doping in MP425 was able to improved FF to 82.5% compared to MP423's FF of 79.7%. Given MP425's overall improved cell performance, the device on a GaAs/Si template (MP567) was grown with the same design.

The solar cell on a GaAs/Si template (MP567) exhibited a J_{SC} of 12.9 mA/cm^2 (Table 1), which is significantly lower than that of the corresponding homoepitaxially grown cell (MP425), which is also reflected in the EQE (Fig. 4). The V_{OC} and FF of the cell on Si were also lower than that on the GaAs substrate, contributing to a lower uncoated efficiency of 5.03% on Si compared to 17.9% on GaAs (Table 1 and Fig. 4). High TDD likely contributed to the reduced device V_{OC} and long wavelength EQE performance compared to the control device on GaAs. However, modeled efficiencies of GaAs cells on Si at this TDD can be as high as ~17% [8], suggesting other factors may be limiting cell performance, such as cracking. The low FF of the device on Si is suspected to be caused by a combination of shunting due to cracking, as well as processing issues.

While low compared with our homoepitaxially grown devices, the GaAs on Si cell exhibited an encouraging 5.03%

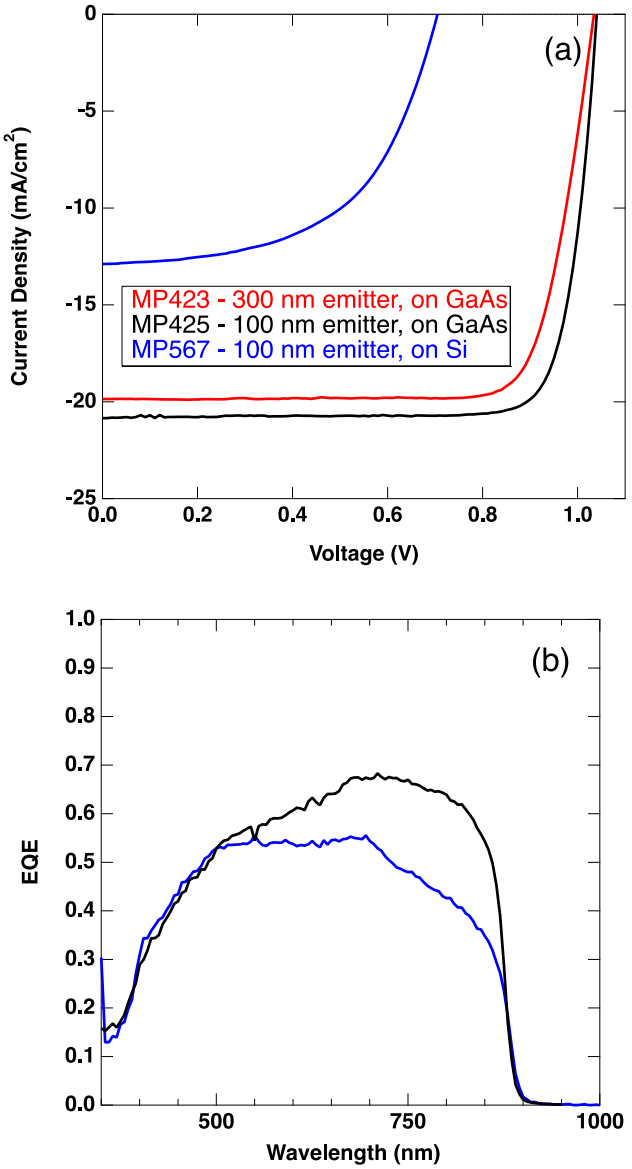

Figure 4. (a) LIV and (b) EQE of the uncoated GaAs solar cells grown homoepitaxially on GaAs with a thicker emitter (MP423, red) and a thinner emitter (MP425, black), and grown on Si with a thinner emitter (MP567, blue).

efficiency, demonstrating promise as a working device with numerous pathways available for future improvement. While the current best GaAs on Si single-junction solar cell achieved 20% efficiency with the use of thermal cycle annealing and an InGaAs/GaAs superlattice buffer [19], our approach in this work offers cost benefits over these previous approaches by minimizing reactor growth time (Fig. 1).

The initial GaAs cell on Si investigated here utilizes a 1.5 µm thick GaAs buffer to mitigate dislocations, less than half of the thickness of the $GaAs_yP_{1-y}$ metamorphic graded buffers used for $GaAs_{0.75}P_{0.25}$ cells [2] and significantly thinner than the ~10 µm $Si_{1-x}Ge_x$ buffers used for GaAs cells on Ge-SiGe-Si [3]. The additional 2 µm GaAs lateral conduction layer seen

TABLE I
GaAs SOLAR CELL PARAMETERS

Sample	Substrate	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	η (%)
MP423	GaAs	1.03	19.9	79.7	16.4
MP425	GaAs	1.04	20.8	82.5	17.9
MP567	Si	0.705	12.9	55.3	5.03

in our device design would not be present in an actual tandem structure, as instead a thin tunnel junction would interconnect the GaAs and Si subcells, and in a single-junction structure, this layer could likely be significantly thinned to reduce cost. We anticipate that thinner buffer layers may be used in the future to further cut costs, and potentially aid in mitigating crack formation.

Device and material improvements may help increase cell efficiency in future work. Using a high-performance AR coating will significantly improve cell J_{SC} with a concomitant boost to V_{OC}. Utilizing a p-i-n device design could help boost J_{SC} through field-assisted current collection. In addition, adjusting device polarity to a more standard n-on-p design could be an interesting option once TDD and cracking issues have been addressed; this design may cater to improved base diffusion lengths and thus improved long wavelength EQE and V_{OC} since electron mobilities are greater than that of holes in GaAs [17]. We further aim to improve upon cracking and TDD in future devices through exploration of the effect of growth parameters and fabrication techniques on material quality.

IV. CONCLUSIONS

We have demonstrated a GaAs solar cell grown epitaxially on nano-patterned Si, achieving 5.0% efficiency despite the large lattice-mismatch between these materials and lack of a graded buffer. The use of a two-step selective area growth process controlled TDD to 4×10^7 cm^{-2} on the GaAs/Si templates enabling a V_{OC} of 0.71 V. The results presented here show promise towards achieving the goal of commercially-viable III-V/Si multijunction devices for low-cost, high-efficiency PV.

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