Advanced Grid Support Functionality Testing for Florida Power and Light

Austin Nelson and Gregory Martin
National Renewable Energy Laboratory

James Hurtt
Florida Power and Light

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Strategic Partnership Project Report
NREL/TP-5D00-67577
January 2017

Contract No. DE-AC36-08GO28308

NREL
NATIONAL RENEWABLE ENERGY LABORATORY

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National Renewable Energy Laboratory
15013 Denver West Parkway
Golden, CO 80401
303-275-3000 • www.nrel.gov

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List of Acronyms

AC	Alternating current
DC	Direct current
FPF	Fixed power factor
FPL	Florida Power and Light Company
FRT	Frequency ride-through
FWC	Frequency-watt control
GSF	Grid support function
HF	High frequency
HF1	Overfrequency 1
HF2	Overfrequency 2
HV	High voltage
IEEE	Institute of Electrical and Electronics Engineers
I_{SC}	Short-circuit current
LF	Low frequency
LF1	Underfrequency 1
LF2	Underfrequency 2
LRO	Load rejection overvoltage
LV	Low voltage
MSA	Manufacturer's stated accuracy
NN	Near nominal
NREL	National Renewable Energy Laboratory
PV	Photovoltaic
ROT	Run on time
VA	Volt ampere
VAR	Volt ampere reactive
V_{DC}	DC voltage
V_{OC}	Open-circuit voltage
VRT	Voltage ride-through
VVC	Volt-VAR control

Executive Summary

This report describes the results of laboratory testing of advanced photovoltaic (PV) inverters undertaken by the National Renewable Energy Laboratory (NREL) on behalf of the Florida Power and Light Company (FPL). FPL recently commissioned a 1.1-MW AC PV installation on a solar carport at the Daytona International Speedway, in Daytona Beach, Florida. In addition to providing a source of clean energy production, the site serves as a live test bed with 36 different PV inverters from eight different manufacturers.

The inverter types have varied advanced grid support functions (GSFs), which are becoming increasingly common and are being required through revised interconnection standards such as UL 1741, Institute of Electrical and Electronics Engineers (IEEE) 1547, and California Rule 21. FPL is interested in evaluating the trade-offs among different GSFs, their compliance to emerging standards, and their effects on efficiency and reliability. NREL provided a controlled laboratory environment in which to undertake such a study.

This work covered nine different classes of tests to compare inverter capabilities and performance for four different inverters that were selected by FPL. The test inverters were all three-phase models rated between 24–36 kW, and they contained multiple PV input power point trackers. Advanced grid support functions were tested for functional behavior, including fixed power factor operation, voltage ride-through, frequency ride-through, volt-volt ampere reactive (VAR) control, and frequency-watt control. Response to abnormal grid conditions with GSFs enabled was studied through anti-islanding, fault, and load-rejection overvoltage tests. Finally, efficiency was evaluated among a range of operating conditions that included power factor, output power, and input voltage variations. Test procedures were derived from requirements of a draft revision of UL 741, California Rule 21, and/or previous studies at NREL.

This reports summarizes the results of each test case, providing a comparative performance analysis of the four test inverters. Inverters were mostly able to meet the requirements of their stated GSF capabilities, with deviations from expected results discussed throughout the report. There were mixed results among the range of abnormal tests, and results often depended on the capability of each test inverter to deploy the GSFs of interest. Detailed test data have been provided to FPL to support future decision-making with respect to inverter selection and GSF deployment in the field.

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1 Introduction

Florida Power and Light Company (FPL) collaborated with the National Renewable Energy Laboratory (NREL) to conduct testing of selected solar photovoltaic (PV) inverters at NREL's Energy Systems Integration Facility (ESIF). FPL recently commissioned a 1.1-MW AC PV solar site at the Daytona International Speedway, in Daytona Beach, Florida, creating a solar canopy shading a large number of parking spaces at the speedway. In addition to generating clean solar electricity within FPL's distribution network, the site serves as a test platform for a variety of solar inverters. A total of 36 grid-connected inverters are installed on the site from eight different inverter manufacturers. FPL is interested in understanding trade-offs among several of these products, including efficiency, grid support function performance, reliability, and cost.

FPL partnered with NREL to provide a performance evaluation of four of the inverter types installed at this site. The ESIF has the capability to test inverters under a wide range of operating conditions in a controlled laboratory environment which is typically not possible or desirable in the field. New requirements for GSFs have been introduced for inverter manufacturers, such as those required by California Rule 21 and the new requirements in the recently published revision of UL 1741 Supplement SA (CPUC, 2000; UL, 2016). Utilities have a vested interest in ensuring inverters are able to meet these new requirements. Additionally, there is interest in the validating the reliability performance of inverters under abnormal conditions with GSFs enabled, including events such as islanding, faults, or load rejection.

Nine types of tests were conducted in this study:

1. Voltage ride-through (VRT)
2. Frequency ride-through (FRT)
3. Fixed power factor operation (FPF)
4. Frequency-watt control (FWC)
5. Volt-volt ampere reactive (VAR) control (VVC)
6. Efficiency
7. Anti-islanding
8. Load rejection overvoltage (LRO)
9. Single- and three-phase faults.

Detailed test descriptions are provided in the following sections, and example test results are discussed. Any unexpected behavior is discussed in this report, and complete test data and summary plots have been provided to FPL for detailed review. The tests summarized in this report are not intended to substitute as certification tests; instead, they provide data for comparative purposes. Care was taken to program the proper settings for each inverter in each test case. In most tests, expected results were observed, but in cases where discrepancies were observed, efforts were made to work with the inverter manufacturers to reconcile the issue.

2 Test Equipment and Setup

All test procedures were based on a combination of requirements under California Rule 21 and a draft version of UL 1741 SA (the official publication of this standard occurred in the middle of the project, in September 2016). When necessary, the test procedures were modified to meet the time requirements and scope of the project and/or the capabilities of the inverters under test, with a goal of demonstrating a representative sample of each inverter's GSF capabilities. All test plans were agreed upon with FPL prior to execution. Details of each test procedure and results are provided in the respective sections below.

The four test inverters were selected by FPL, and several of each inverter type is installed at the Daytona International Speedway PV site. All inverters were 60-Hz, 277/480 AC voltage, three-phase models listed for use in North America. A summary of the basic operating parameters for the test inverters is shown in Table 1.

Table 1. Basic Specifications of Test Inverters

Inverter	Nominal Real Power (kW)	Nominal Reactive Power (kVA)	Nominal Current (A)	MPPT Range (V_{DC})[a]
1	24.0	24.0	28.9	450–800
2	36.0	39.8	47.9	480–850
3	36.0	36.0	43.3	540–800
4	30.0	33.0	39.7	560–850

[a] Direct current voltage

All inverters were connected to a bidirectional AC voltage source, which served as the grid simulator for all tests. The AC voltage source for this study was the AMETEK MX45, with three independently controllable phases, rated for a total power of 45 kVA. This AC source is also programmable for predefined voltage and frequency profiles, which were used for many of the test types.

Each inverter was powered with an appropriately sized PV simulator from the AMETEK TerraSAS family. These PV simulators can be programmed for specific PV panel characteristics (e.g., short-circuit current [I_{SC}] and open-circuit voltage [V_{OC}]), and they can also simulate programmable dynamic events such as changes in irradiance and temperature. The PV simulators have high slew-rate control to simulate PV response to rapidly changing conditions, such as maximum power point tracking perturbations. All inverters were powered with two sets of 1000-V /10-A modules, each configured with three parallel modules (1000 V/30 A per set); each set of modules was connected to one of the independent maximum power point tracking trackers on each inverter. The third available maximum power point tracking tracker on Inverter 4 was not used, but full power operation was still achievable with the dual inputs.

For the majority of the test cases, a solar current-voltage profile was selected such that the inverter would run at full power and be near the maximum power point of the curve at a DC voltage on the higher end of its stated power point tracking range. For tests below full power, the irradiance value of the curve was adjusted to attain the target AC output power. Efficiency tests

had stricter requirements on the DC input, and those are discussed in the efficiency test results section (Section 3.6.2).

Tests requiring a load bank included the Simplex Trident 100-kVA resistive-inductive-capacitive load bank. This load bank features independent loading on each of the phases, 100-W step sizes for resistive elements, and 75-VA step sizes for reactive elements.

All waveform data were captured using a Yokogawa DL850 oscilloscope at a sampling rate of 20 kHz (unless otherwise noted), and power measurements were recorded with a Yokogawa WT1800 power analyzer at an update rate of 100 ms (10 Hz). Depending on the type of test and its instrumentation requirements, different equipment was used; the instruments used for voltage and current measurements for each test type are summarized in Table 2.

Table 2. Voltage and Current Measurement Probe Types

Measure-ment Type	Manufact-urer	Model	Range/ Specifi-cations	Bandwidth	Accuracy	Tests
AC Current	AEMC	MN 261	10 mV/A, 200 A	10 kHz	2%	VRT, FRT, FPF, VVC, FWC, anti-islanding, LRO
AC Current	Yokogawa	701930	10 mV/A, 150 A	10 MHz	1%	Efficiency, fault
DC Current	AEMC	MR 561	10 mV/A 150 A	10 kHz	1.5%	VRT, FRT, FPF, VVC, FWC, anti-islanding, LRO, fault
DC Current	Murata	3020-01108-0	100 mV/ 100 V	Shunt	0.25%	Efficiency
DC Voltage	Yokogawa	700924	1 mV/V, 1400 V	100 MHz	2%	3

Tests requiring more equipment than a PV simulator input and grid simulator output connected to the inverter under test are described in the corresponding test section below.

3 Test Descriptions and Results

3.1 Voltage Ride-Through Tests

3.1.1 Voltage Ride-Through Procedures

All inverters were programmed to operate under the voltage trip limits specified in California Rule 21. Because a number of the trip times and magnitudes are adjustable under this standard, the example settings given in UL 1741 SA Table 9.1 were used for all inverters, which are summarized in Table 3. Inverters with a programmable country profile that deviated from these settings were manually adjusted, and inverters without such a profile were manually programmed. For inverters that were manually programmed, the trip time was set between the middle of the "Ride-Through Until" and the "Maximum Trip Time" values found in the table (e.g., the HV1 trip time was set to 12.5 seconds).

Table 3. Voltage Ride-Through Magnitude and Durations According to California Rule 21

Operating Region	Voltage Range (% Nominal)	Ride-Through Until	Maximum Trip Time
High-Voltage 2 (HV2)	V > 120	N/A	0.16 s
High-Voltage 1 (HV1)	120 ≥ V > 110	12 s	13 s
Near Nominal (NN)	110 ≥ V ≥ 88	Indefinite	N/A
Low-Voltage 1 (LV1)	88 > V ≥ 70	20 s	21 s
Low-Voltage 2 (LV2)	70 > V ≥ 50	10 s	11 s
Low-Voltage 3 (LV3)	V < 50	1 s	1.5 s

Each of the five ride-through regions was tested by programming a voltage magnitude profile with rise, fall, and hold times and magnitudes defined by UL 1741 SA. Successful ride-through was demonstrated in the HV1, LV1, LV2, and LV3 regions; trip times were tested in the HV2 and LV3 regions. In addition, steady-state tests were run near the 88% and 110% trip limits to demonstrate that the inverters could run within the given trip limit indefinitely. All tests were repeated at 100% and 20% inverter output power, creating 14 test cases per inverter.

The UL 1741 SA VRT test procedure intentionally creates a difficult test for the inverter to ride through by maximizing the size of the voltage transient. High-voltage ride-through tests are run by starting near the bottom of the normal operating region (i.e., slightly more than 88%) and quickly raising the voltage higher than the threshold of the test, with a rise time of "less than or equal to the larger of 1 cycle or 1% of the ride-through region duration". After the overvoltage window has passed, the voltage is then returned to slightly more than 88% with a fall time equal to the rise time. The low-voltage ride-through test is run in a similar manner, starting near the top of the normal operating region (slightly less than 110%). Thus, the VRT tests confirm the ability of the distributed energy resource to not only ride through the abnormal voltage condition for the programmed time but also tolerate very fast voltage slew rates.

Each test case depends on the manufacturer's stated accuracy (MSA) in voltage measurement. When testing a voltage limit either before or beyond a given voltage limit, the voltage was set to

a value equal to 1.5 times that of the MSA voltage measurement to create a buffer and eliminate possible nuisance trips due to measurement inaccuracies. All inverters were tested at an MSA of 1% for this study, resulting in the voltage test profiles summarized in Table 4. Any required modifications to these voltage profiles are discussed in the results section below (Section 3.1.2).

Some tests required an additional parallel resistive load in the circuit due to current limitations of the grid simulator. This was because low-voltage conditions during testing of the 36 kVA rated models caused larger currents than the maximum current rating of the grid simulator when programmed to its highest voltage range; it was assumed that these parallel load banks did not impact the ride-through behavior of each test inverter.

Table 4. Voltage Ride-Through Test Profiles

Test Case	Rise/Fall Time (s)	Hold Time[a] (s)	Start Voltage (% Nominal)	Hold Voltage (% Nominal)	Expected Result
HV1	0.016	11.968	89.5	118.5	Ride through
LV1	0.016	19.968	108.5	71.5	Ride through
LV2	0.016	9.968	108.5	51.5	Ride through
LV3	0.016	0.968*	108.5	48.5	Ride through
HV2	0.016	0.968*	108.5	121.5	Trip
LV3	0.016	1.968*	89.5	48.5	Trip
NN1	0.016	75.0*	100.0	108.5	Ride through
NN2	0.016	75.0*	100.0	89.5	Ride through

[a] The hold times are not critical in these tests, but they must exceed the trip time for the trip tests, and they must be longer than 60 seconds for the steady-state (NN) tests.

3.1.2 Voltage Ride-Through Results

The inverters passed the majority of the ride-through tests completed in this study, with some exceptions as discussed below.

Inverter 1 was not entirely programmable for the complete Rule 21 settings shown in Table 3; the maximum low-voltage trip time for this inverter was 10 seconds. For the LV1 and LV2 test cases, the trip time was set to 10 seconds, and the hold time in Table 4 was set to 9.868 seconds rather than 9.968 seconds. (Note that this aggressively tested the stated trip time by running the entire transient profile up to the total trip time rather than the minimum ride-through time.) Additionally, only two low-voltage trip settings could be programmed simultaneously, rather than three. The inverter was reprogrammed for successive low-voltage ride-through tests depending on the trip limit being tested.

A representative set of time-series plots is shown in Figure 1 for Inverter 1 at 100% output power for the HV1 and LV2 test cases. There was a small amount of power curtailment in all low-voltage conditions due to internal current limits. The amount of power limiting varied by inverter and depended on the maximum rated AC current and the AC voltage. Also, note that the LV2 test case shown is for a10 second ride-through time, as discussed.

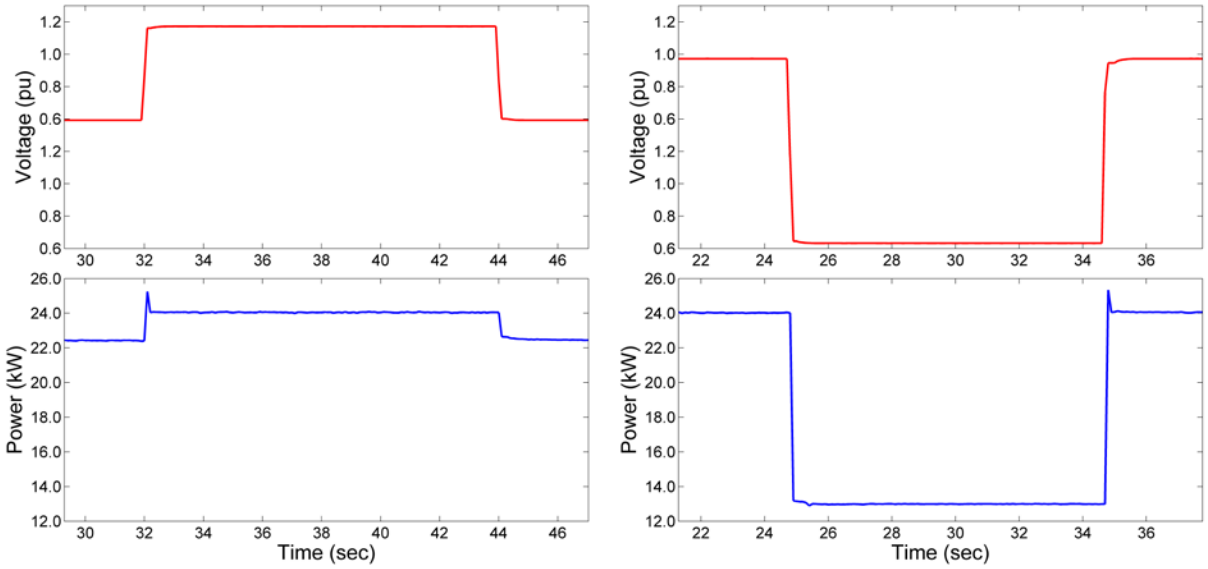

Figure 1. HV1 (left) and LV2 (right) test cases for Inverter 1 at 100% output power

Inverter 2 was not programmable to the California Rule 21 ride-through requirements, so a modified set of test cases was run. The maximum low-voltage ride-through time was 3 seconds at all of the voltage levels. As such, the LV1 and LV2 test profiles were run with a hold time of 2.968 seconds, and the inverter successfully passed these tests. The LV3 and LV4 profiles were unchanged, and this inverter passed the former but rode through the latter (the inverter was expected to trip within 1.5 seconds). An example of ride-through on the LV4 test case at 100% output power is shown in Figure 2 (left). Note that the output is mostly reactive power during the ride-through window.

On the high-voltage case, the stated ride-through time for Inverter 2 was up to 1 second for voltages beyond the 120% trip limit. This inverter tripped within 160 ms both for voltages outside of 120% (HV2) and within 120% (HV1). A successful ride-through was expected in the latter test, and an example waveform showing the trip is shown in Figure 2 (right). Ride-through settings were programmed per inverter documentation and manufacturer input. With the exception of the unexpected tests results shown in Figure 2, Inverter 2 otherwise passed all modified ride-through tests successfully, including the steady-state tests.

Inverter 3 was programmable to the California Rule 21 settings and successfully passed all test cases without modification. This inverter curtailed output current significantly for some low-voltage tests cases, but it always rode through the event. Note: this inverter tripped very rapidly (within one AC cycle) during the HV2 trip tests. The reason for this is not known but may have been the result of a fast control response due to the aggressive voltage ramp.

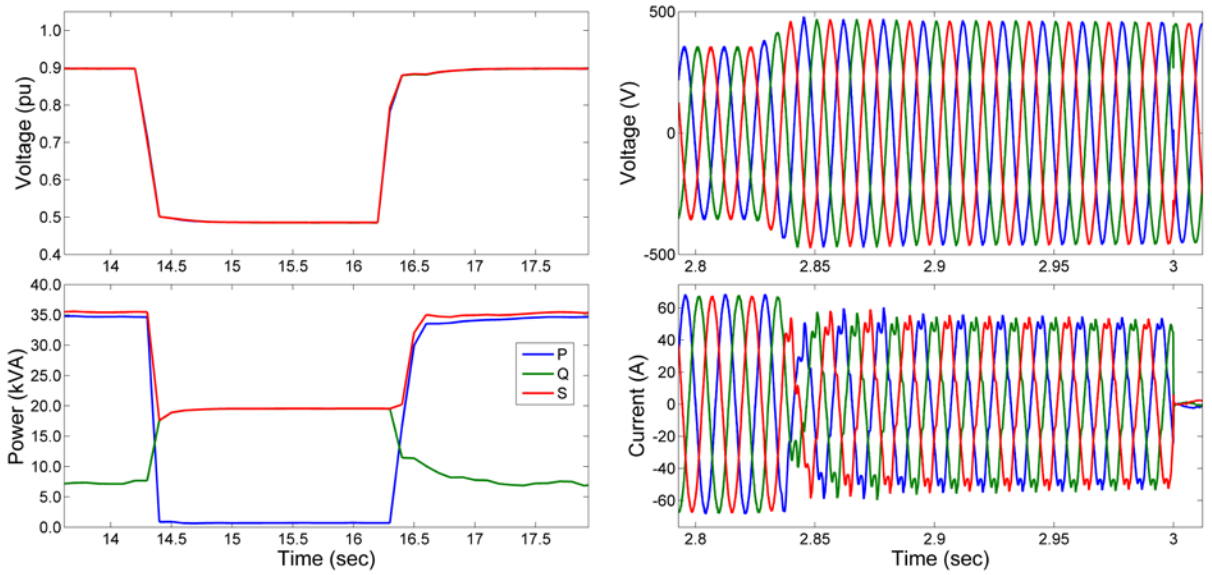

Figure 2. LV4 (left) and HV1 (right) test cases for Inverter 2 at 100% output power, showing two unexpected test cases

Inverter 4 likewise had a programmable profile and successfully passed all tests without modification; however, this inverter demonstrated unexpected behavior when the grid simulator was set to approximately 300 V (corresponding to approximately 108.0%–108.5% of nominal). This voltage level was the pre-ramp level for all low-voltage tests and also the level used for the high-voltage steady-state test. The inverter oscillated between full output power and zero output power in approximately 1 second periods. An example of this behavior is shown in Figure 3 (left), where power dropped to zero twice both before and after the low-voltage hold time. This behavior was observed only at full power and not at the power level of 20%.

Discussions with the manufacturer revealed that the programmable California Rule 21 profile in this inverter was made available for a specific customer, and this was not meant to cover the exact requirements used in this study. The problematic voltage level was near a cease-to-energize boundary, which likely caused the unexpected inverter response. An additional set of tests was run with the California Rule 21 limits manually programmed, and the problem at this voltage level was no longer observed. The identical LV1 test case in Figure 3 (right) shows a clean ride-through response, i.e., without the power fluctuations during the pre-ramp voltages (the momentary power dropout shown in this plot is due to the voltage transient). The inverter manufacturer subsequently provided FPL with updated firmware that addressed these issues and met the ride-through requirements shown in Table 3; the new firmware was not tested in this study.

A summary of all VRT test results is shown in Table 8. Test results that required a modification to the test procedures are marked with notes. The trip times are all shown in milliseconds, and all inverters met the trip time requirements. Also, all inverters successfully passed the steady-state tests for both low-voltage and high-voltage situations, which are not shown in this table.

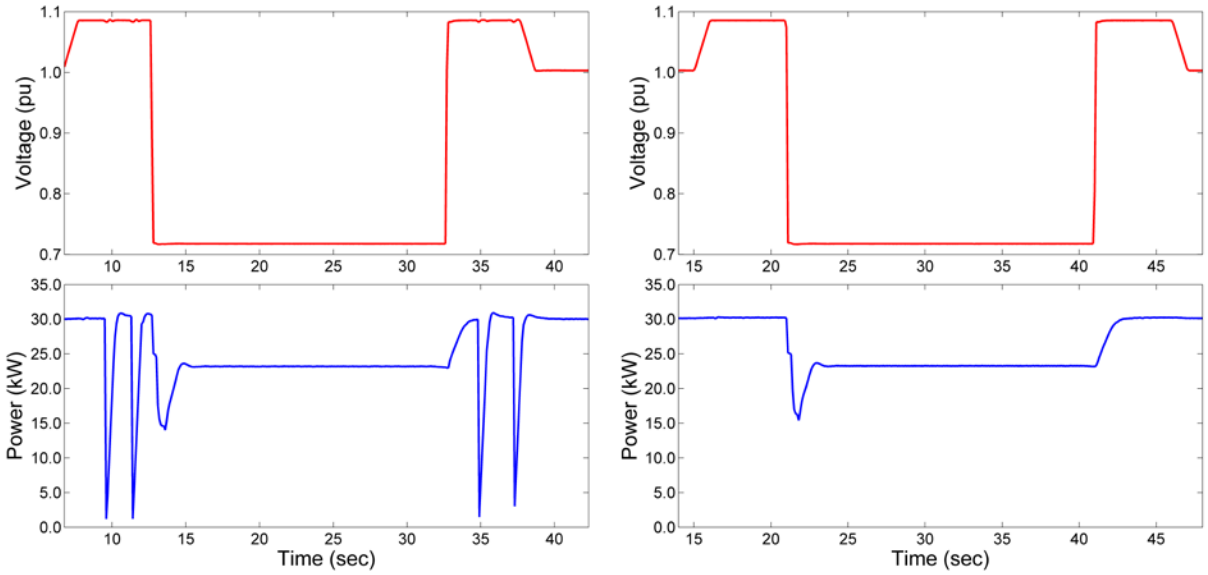

Figure 3. LV1 test case with default California Rule 21 profile (left) and manually programmed VRT trip limits (right) for Inverter 4 at 100% power

Table 5. Voltage Ride-Through Test Results Summary

VRT Test	Output Power (%)	Expected Result	Inverter Response (Trip Times in Milliseconds)			
			1	2	3	4
HV2	100	Trip ≤ 160 ms	141	134	8	138
HV2	20	Trip ≤ 160 ms	156	136	7	138
HV1	100	Ride-through	PASS	157[a]	PASS	PASS
HV1	20	Ride-through	PASS	151[a]	PASS	PASS
LV1	100	Ride-through	PASS[b]	PASS[b]	PASS	PASS[c]
LV1	20	Ride-through	PASS[b]	PASS[b]	PASS	PASS[c]
LV2	100	Ride-through	PASS[b]	PASS[b]	PASS	PASS[c]
LV2	20	Ride-through	PASS[b]	PASS[b]	PASS	PASS[c]
LV3	100	Ride-through	PASS	PASS[b]	PASS	PASS[c]
LV3	20	Ride-through	PASS	PASS[b]	PASS	PASS[c]
LV4	100	Trip ≤ 1500 ms	1466	FAIL	1185	1470
LV4	20	Trip ≤ 1500 ms	1469	FAIL	1184	1477

[a] Considered a failing test result; ride-through was expected
[b] Modified (shorter) ride-through time
[c] Required modified profile to obtain steady-state results

3.2 Frequency Ride-Through Tests

3.2.1 Frequency Ride-Through Procedures

Similar to VRT testing, all inverters were programmed to operate under the frequency trip limits specified in California Rule 21. Because a number of the trip times and magnitudes are adjustable under this standard, the example settings used in UL 1741 SA Table 10.1 were used for all inverters, which are summarized in Table 6. Inverters with a programmable country profile that deviated from these settings were manually adjusted when necessary, and inverters without such a profile were manually programmed. For inverters that were manually programmed, the trip time was set between the middle of the "Ride-Through Until" and the "Maximum Trip Time" values shown in the table (e.g., 299.5 seconds for HF1 and LF1).

Table 6. Frequency Ride-Through Magnitude and Durations According to California Rule 21

Operating Region	Voltage Range (Hz)	Ride-Through Until	Maximum Trip Time
Overfrequency 2 (HF2)	f > 62.0	No ride-through	0.16 s
Overfrequency 1 (HF1)	62.0 ≥ f > 60.5	299 s	300 s
Near Nominal (NN)	60.5 ≥ f ≥ 58.5	Indefinite	N/A
Underfrequency 1 (LF1)	58.5 > f ≥ 57.0	299 s	300 s
Underfrequency 2 (LF2)	57.0 > f	No ride-through	0.16 s

Each of the ride-through regions was tested by programming a frequency magnitude profile with rise, fall, and hold times as well as magnitudes defined by UL 1741 SA. Successful ride-through was demonstrated in the HF1 and LF1 regions, and trip times were tested in the HF2 and LF2 regions. In addition, steady-state tests were run near the 58.5 Hz and 60.5 Hz trip limits to demonstrate that the inverters could run indefinitely within the given trip limit. Steady-state tests were run for 600 seconds to demonstrate steady-state operation at twice the longest allowable ride-through time. All tests were repeated at 100% and 20% inverter output power, creating 10 test cases per inverter.

Similar to the VRT tests, the UL 1741 SA FRT test procedure intentionally creates a difficult test for the inverter to ride through by maximizing the frequency excursion. High-frequency ride-through tests were run by starting near the bottom of the normal operating region (i.e., slightly more than 58.5 Hz) and quickly raising the frequency above the threshold of the test, with a rise time of at least 1 Hz/s. After the overfrequency window has passed, the frequency is then returned to slightly more than 58.5 Hz with a fall time equal to the rise time. All tests in this study were run with a ramp time of 2 Hz/s to more aggressively exercise tolerance to frequency changes. The low-frequency ride-through test was run in a similar manner, starting near the upper range of the normal operating region (slightly less than 60.5 Hz). Thus, the FRT tests confirm the ability of the distributed energy resource to both ride through the abnormal frequency condition and to tolerate very fast changes in frequency, as may be experienced in the field during remote fault events.

Each test case depends on the manufacturer's stated accuracy (MSA in the frequency measurement. When testing a frequency limit either before or beyond a given frequency limit, the frequency was set to a value equal to 1.5 times the MSA in the frequency measurement to create a buffer to eliminate possible nuisance trips due to measurement inaccuracies. Three of the inverters had an MSA of ±0.10 Hz in frequency, and one of them claimed an MSA of ±0.01 Hz. To create fair test cases, all inverters were tested at an MSA of 0.10 Hz for this study, creating the frequency profiles summarized in Table 7. Any required modifications to these frequency profiles are discussed in the results section below.

Table 7. Frequency Ride-Through Test Profiles

Test Case	Rise/Fall Time (s)	Hold Time (s)	Start Frequency (Hz)	Hold Frequency (Hz)	Expected Result
HF1	1.6	295.8	58.65	61.85	Ride through
LF1	1.6	295.8	60.35	57.15	Ride through
HF2	0.9	1.0[a]	60.35	62.15	Trip
LF2	0.9	1.0[a]	58.65	56.85	Trip
NN1	0.175	600[a]	60.00	60.35	Ride through
NN2	0.675	600[a]	60.00	58.65	Ride through

[a] The hold times are not critical in these tests, but they must exceed the trip time for the trip tests, and they must be longer than or equal to 600 seconds for the steady-state (NN) tests.

3.2.2 Frequency Ride-Through Results

All inverters passed the described FRT tests, with a few exceptions noted below.

Inverter 1 was manually programmed for the frequency limits, and had a maximum high-frequency trip limit of 90 seconds. As such, this inverter was tested with a modified profile with a hold time of 85.8 seconds rather than the full 295.8 seconds to exercise this ride-through time. Test results for the modified HF1 profile (left) as well as the LF1 profile are shown in Figure 4. This inverter produced some reactive power following the large frequency excursions, but it settled back to unity power factor after several seconds.

Inverter 2 had options to program all required frequency trip parameters manually; however, this inverter tripped within 160 ms for frequencies greater than 60.5 Hz and was therefore able to pass the low-frequency ride-through tests but not the test case HF1. Figure 5 shows Inverter 1 tripping after 65 ms for the HF1 test (left) at 20% output power as well as the expected result for LF2 (right), which tripped in 28 ms for a low-frequency event at 100% output power. This inverter successfully passed all tests in this group except for the HF1 tests at both power levels.

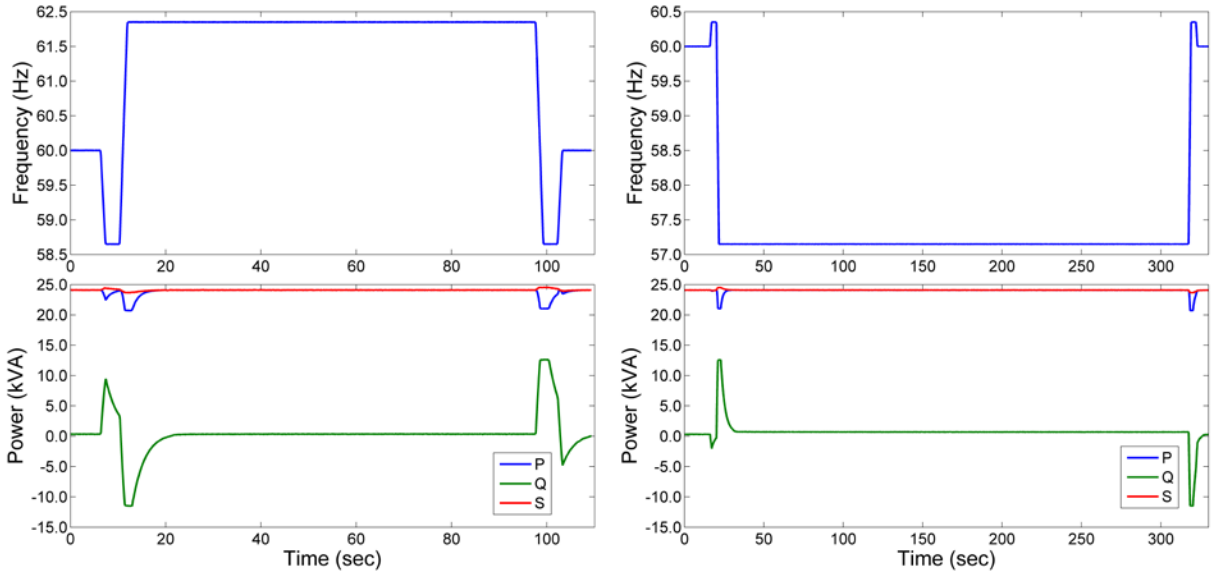

Figure 4. HF1 (left) and modified LF1 (right) test results for Inverter 1 at 100% output power

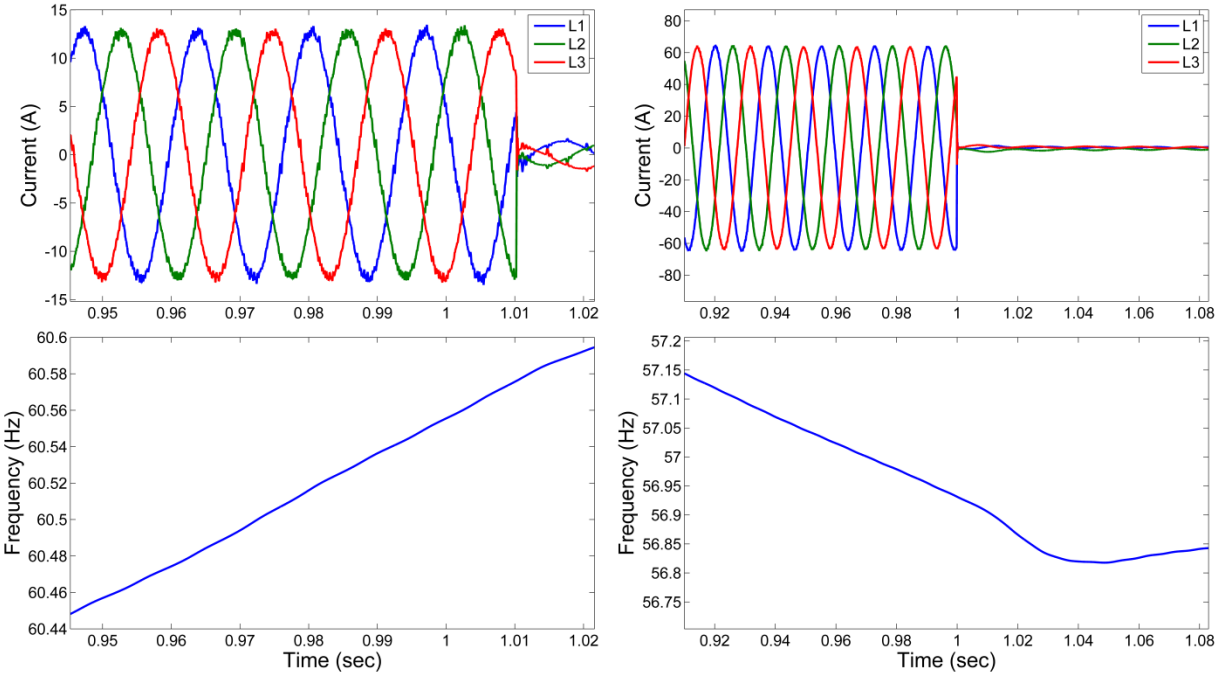

Figure 5. HF1 (left) and LF2 (right) test results for Inverter 2 at 20% and 100% output power, respectively

Inverters 3 and 4 were both programmed with preloaded California Rule 21 profiles and successfully passed all frequency tests in this group, including ride-through tests, trip tests, and steady-state tests. Inverter 3 demonstrated momentary transients during the frequency ramps, but settled back to the expected output within several seconds, as shown in Figure 6 (left). The Inverter 4 response demonstrated unexpected behavior; it reduced its power output during high-frequency events and then slowly ramped back to full power after returning to the nominal frequency, as shown in Figure 6 (right). This behavior occurred for tests at 20% and 100% output power.

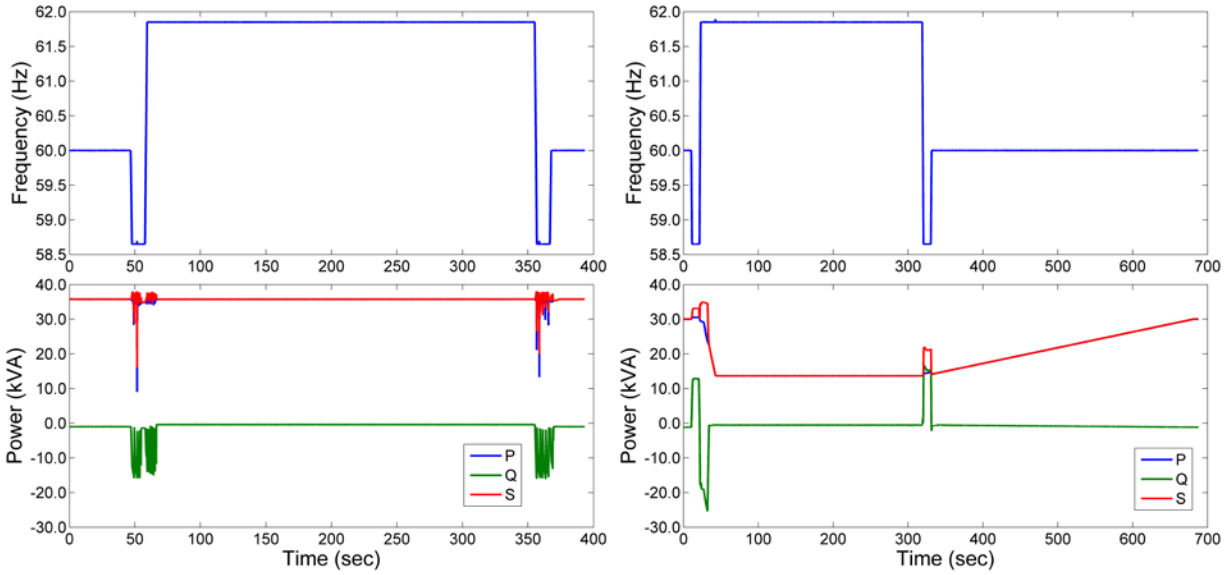

Figure 6. HF1 at 100% output for Inverter 3 (left) and Inverter 4 (right)

For the trip tests—HF2 and LF2—all test inverters successfully tripped within the required trip time of 160 ms. Because of bandwidth limitations on the power analyzer used in this testing, measured frequency was computed on a cycle-by-cycle basis from measured waveforms using MATLAB/Simulink.

A summary of all FRT test results is shown in Table 8. All test cases wherein the test inverter successfully rode through are marked as "PASS," and the trip times are given for the tests.

Table 8. Frequency Ride-Through Test Result Summary

FRT Test	Output Power (%)	Expected Result	Inverter (Trip Times in Milliseconds)			
			1	2	3	4
HF2	100	Trip ≤ 160 ms	117	70	120	107
HF2	20	Trip ≤ 160 ms	115	60	121	104
HF1	100	Ride through	PASS[a]	65[b]	PASS	PASS
HF1	20	Ride through	PASS[a]	40[b]	PASS	PASS
LF1	100	Ride through	PASS	PASS	PASS	PASS
LF1	20	Ride through	PASS	PASS	PASS	PASS
LF2	100	Trip ≤ 160 ms	78	28	84	104
LF2	20	Trip ≤ 160 ms	78	14	78	127
NN1	100	Run continuous	PASS	PASS	PASS	PASS
NN2	100	Run continuous	PASS	PASS	PASS	PASS

[a] Modified frequency hold time
[b] Considered a failing test result; ride-through was expected.

3.3 Fixed Power Factor Tests

Steady-state fixed power factor was tested on each inverter at two different output power levels (20% and 100%) and at five different power factor values (±0.80, ±0.90, and 1.00), creating a total of 10 test cases for each inverter. Steady-state data were logged for at least 60 seconds at each test level, and the measured power factor was taken to be an average throughout this time window. The power factor was calculated directly using the WT1800 power analyzer, and the values reported are of the fundamental (60 Hz) component only (i.e., the displacement power factor).

Negative power factors were considered absorbing VARs, with current leading voltage (reduces voltage at the point of interconnection) according to the common generator sign convention, and vice versa. Each inverter was programmed manually for each power factor level.

"Full power" operation often resulted in less than nameplate real power output, depending on the inverter and power factor setting. Inverters 1 and 3 had no margin between nameplate real power and nameplate apparent power, so any non-unity power factor operation resulted in a reduction in real power output. Inverters 2 and 4 had some margin in apparent power and could produce rated real power at power factors more than ±0.90; operation at ±0.80 power factor resulted in reduced real power output.

The results of the fixed power factor tests are summarized in Table 9. These data are also represented graphically in Figure 7. (Note that the graph shows the magnitude of the power factor.) For unity power factor, errors between the expected and actual power factor were very small (≤ 0.2%). However, the size of the error increased for decreasing power factor magnitude and at lower power output, reaching maximum errors up to 4–5% of the target value. The test setup introduced a small amount of error due to line impedances between the inverter terminals and points of measurement, but it was assumed that the effect of this impedance on the test results was minimal.

Table 9. Fixed Power Factor Test Result Summary

Power Factor	Output Power (%)	Inverter Number and Power Factor			
		1	2	3	4
0.80	100	0.792	0.805	0.832	0.821
0.80	20	0.785	0.785	0.842	0.825
0.90	100	0.895	0.905	0.920	0.915
0.90	20	0.889	0.890	0.928	0.917
1.00	100	0.999	0.999	0.999	0.999
1.00	20	0.999	0.999	0.998	0.999
-0.90	100	-0.906	-0.898	-0.878	-0.881
-0.90	20	-0.913	-0.898	-0.870	-0.876
-0.80	100	-0.808	-0.795	-0.764	-0.774
-0.80	20	-0.819	-0.797	-0.756	-0.768

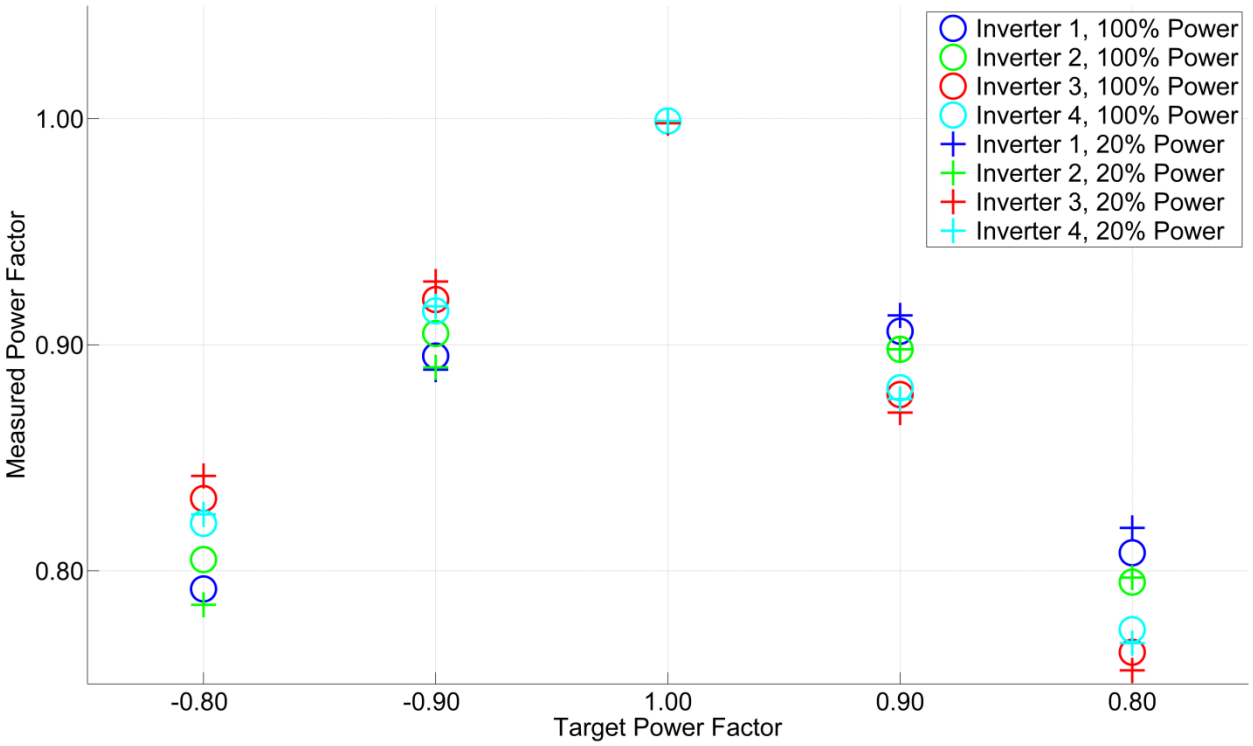

Figure 7. Fixed power factor test summary showing the magnitude of the measured power factor compared to expected power factor at power levels of 100% and 20%

Several example tests results are shown in Figure 8 and Figure 9. Figure 8 shows steady-state operation of Inverter 1 at +0.8 power factor (left) and Inverter 2 at -0.8 power factor (right), both at 100% output power. Similarly, Figure 9 shows +0.9 power factor operation for Inverter 3 (left) and -0.9 power factor operation for Inverter 4 (right) at full power. Note that although the scales are different on these plots, the range in the y-axis is equal, showing the relative amount of ripple in power factor measurement. The larger fluctuations in steady-state power factor on Inverter 2 are possibly due to differences in power point tracking algorithm, anti-islanding detection method, or other control factors.

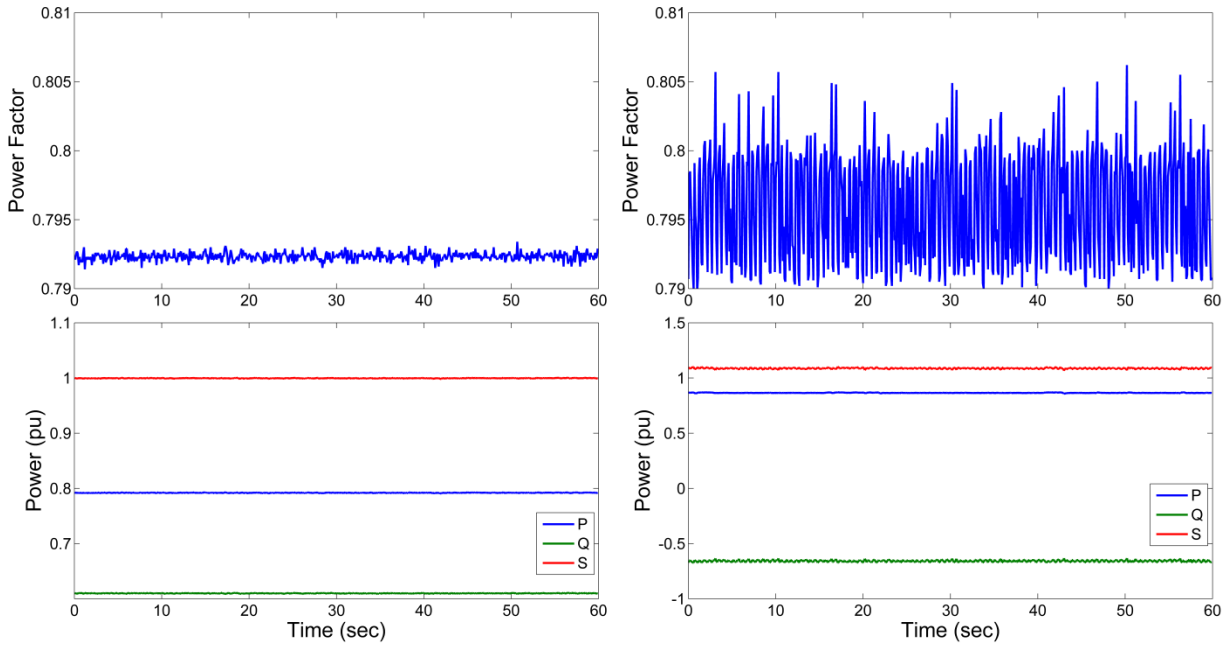

Figure 8. Fixed power factor steady-state tests at 100% output power and +0.8 power factor on Inverter 1 (left) and -0.8 power factor on Inverter 2 (right)

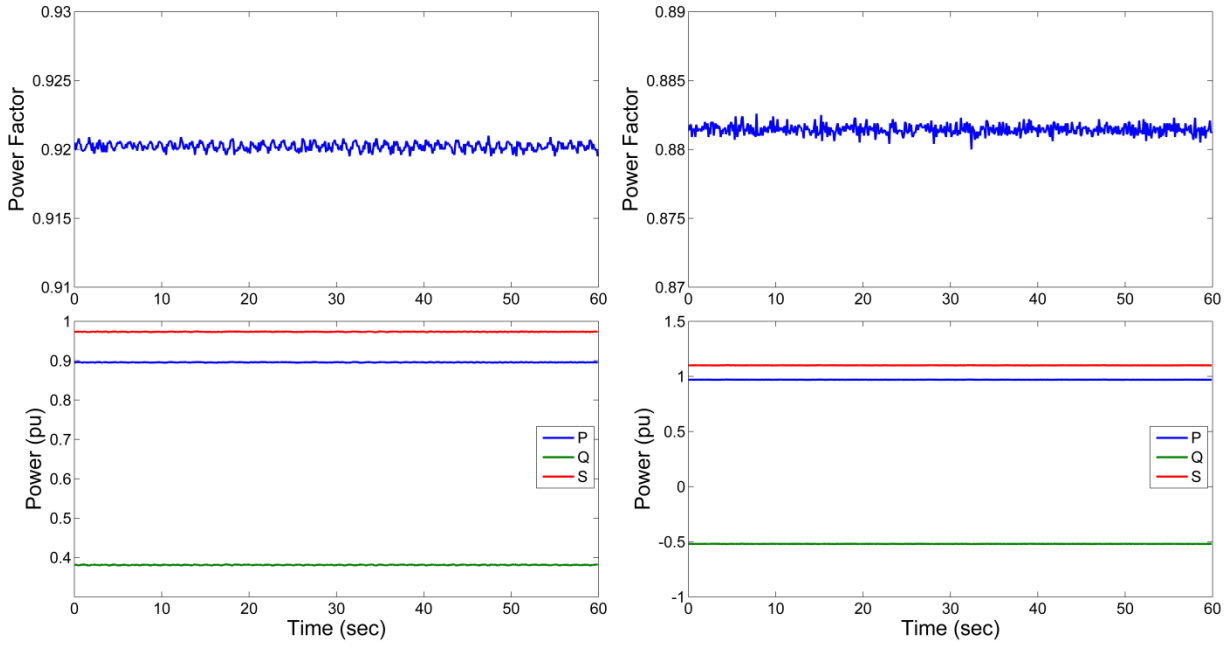

Figure 9. Fixed power factor steady-state tests at 100% output power and +0.9 power factor on Inverter 3 (left) and -0.9 power factor on Inverter 4 (right)

3.4 Frequency-Watt Tests

3.4.1 Frequency-Watt Test Procedures

Inverters with FWC can help regulate grid frequency in the event of a large loss of load on the network, mimicking the droop curve of a synchronous generator. For PV inverters, the FWC characteristic curve is typically limited to overfrequency events, linearly curtailing power between full power output up until a start frequency and curtailing to zero power output at a final stop frequency. A series of FWC tests were derived from the UL 1741 SA standard for this portion of the testing. A series of three FWC characteristic curves were defined in conjunction with FPL for this portion of the testing, referred to as "mild," "moderate," and "aggressive" based on their slopes, as shown in Figure 10. Each curve was characterized by its start frequency and stop frequency, with a linear real power curtailment portion connecting the two; details of these curves are also summarized in Table 10.

A series of frequency profiles were run on the grid simulator, wherein the frequency was stepped up to different magnitudes along each curve, ensuring that at least three data points were captured on each portion of the curve, as required in UL 1741 SA. Each frequency step was held for at least twice the manufacturer's settling time so that the inverter stabilized at a steady-state output power operating point. After reaching the maximum frequency, the frequency was stepped down, repeating each of the frequency set points. When necessary, frequency trip times and/or limits were adjusted to execute the test without having the inverter trip offline.

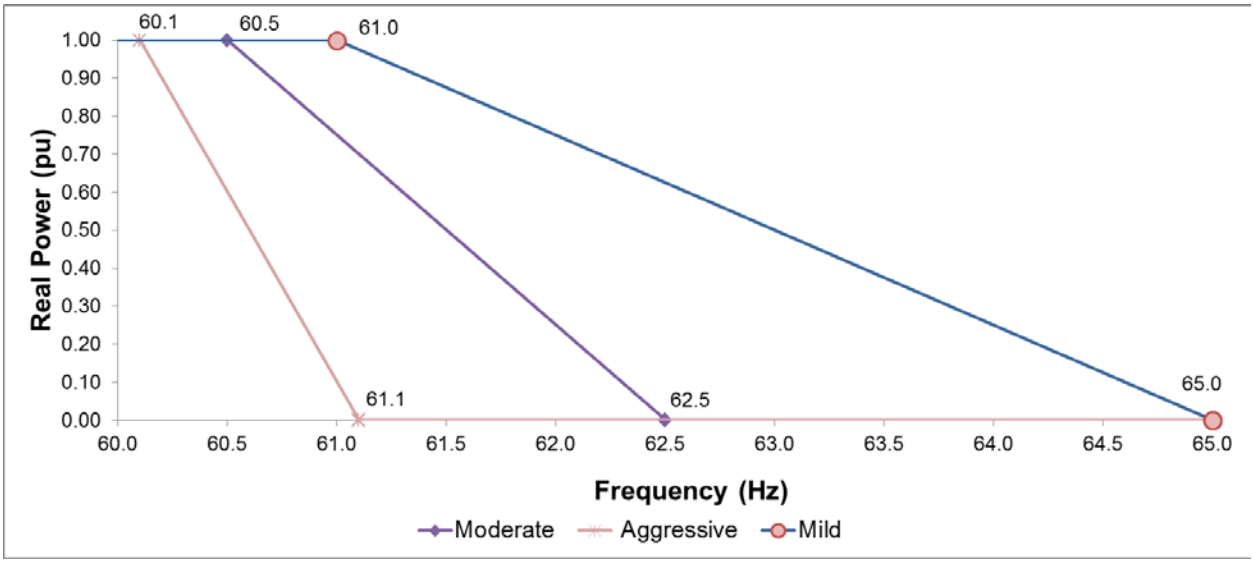

Figure 10. Mild, moderate, and aggressive FWC curves

Each of the curve types was tested with the inverter set to 100%, 67%, and 33% of nominal output power at unity power factor. Output power was controlled by adjusting the irradiance settings at the PV simulators. Additionally, a representative test was run to demonstrate the effect of hysteresis settings, when available. With hysteresis enabled, the inverter was expected to maintain curtailed output power until the grid frequency dropped below the specified hysteresis limit. Also, one of the test inverters was programmable to compare snapshot and nameplate power modes. In nameplate power mode, the characteristic FWC control curve shown in Figure

10 assumes that 1.0 p.u. power is set at the nameplate rating of the inverter. In snapshot mode, 1.0 p.u. power is set at what the output power of the inverter was at the moment it entered the linear region of the FWC curve, when the function was first activated.

Table 10. FWC Test Case Summary

Test Case	Curve Type	Start Frequency (Hz)	Stop Frequency (Hz)	Input Power (%)	Hysteresis On?	Mode
1	Aggressive	60.1	61.1	100	No	Snapshot
2	Aggressive	60.1	61.1	67	No	Snapshot
3	Aggressive	60.1	61.1	33	No	Snapshot
4	Moderate	60.5	62.5	100	No	Snapshot
5	Moderate	60.5	62.5	67	No	Snapshot
6	Moderate	60.5	62.5	33	No	Snapshot
7	Mild	61.0	65.0	100	No	Snapshot
8	Mild	61.0	65.0	67	No	Snapshot
9	Mild	61.0	65.0	33	No	Snapshot
10	Moderate	60.5	62.5	100	Yes	Snapshot
11	Moderate	60.5	62.5	67	No	Nameplate

3.4.2 Frequency-Watt Test Results

Only Inverter 1 and Inverter 3 were capable of running the FWC function, so the tests were limited to these two inverters. Inverter 3 always ran in snapshot mode, so Case 11 shown in Table 10 was not run. In general, both inverters performed as expected among all test cases, with any deviations described below. Representative time series and summary plots are shown below for each inverter, but they do not represent comprehensive test data. Appendix A includes a comprehensive set of tables showing the grid frequency, expected output power, measured output power, and percent error in power for every step of every test case.

A typical set of time series plots in Figure 11 shows the effect of changing the output power from 100% (left) to 67% (right) using the aggressive curve. Several small steps in frequency occurred to start and finish the test to demonstrate no change in output power when the frequency was less than the start frequency at 60.1 Hz. The inverter then curtailed power in proportional steps through the linear region of the curve, demonstrating the inverter operating in snapshot mode. The inverter then held at zero output power until the frequency was reduced below the stop frequency, demonstrating that no hysteresis was used in this test. Some overshoot in real power occurred and a small amount of reactive power was generated during the rapid changes in frequency, but the inverter quickly recovered to its target operating point at each step.

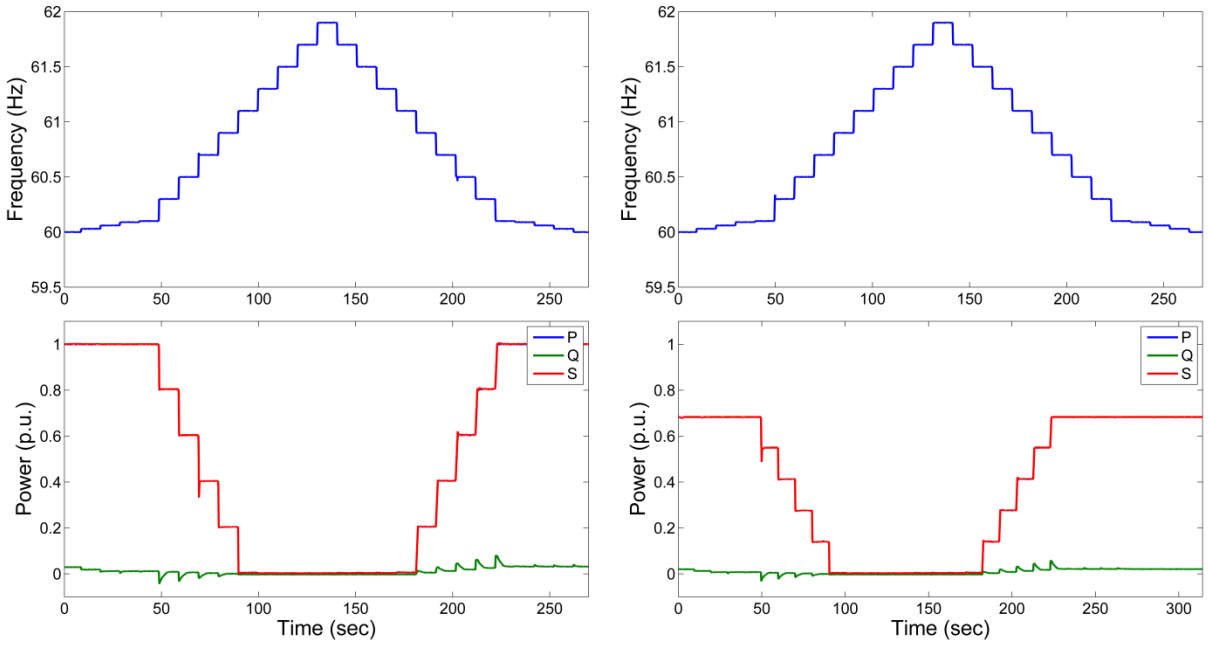

Figure 11. Inverter 1 FWC time series for the aggressive curve at 100% output power (left) and 67% output power (right)

Figure 12 shows a pair of summary curves demonstrating the differences between the moderate and mild curves at 100% power output. For both cases, the power output followed the expected values very closely, with a very small error between the expected and actual output power. Note that the zero power portion of the mild curve was not tested because the inverter could not be programmed to ride through frequencies ≥ 65 Hz for a significant period of time.

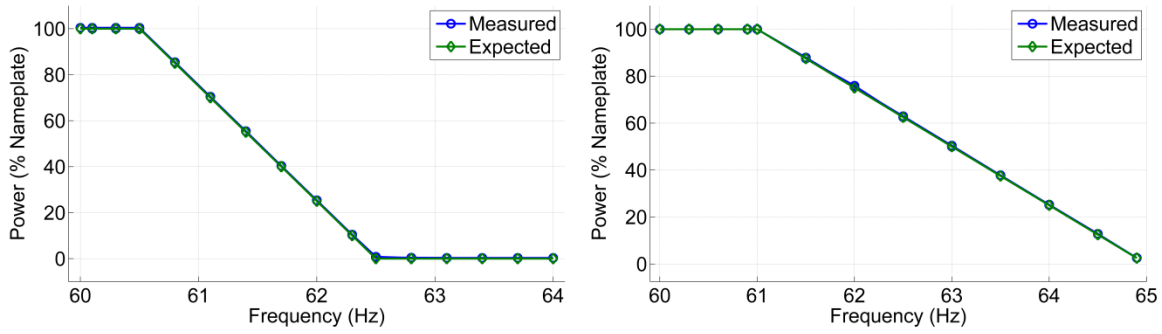

Figure 12. Inverter 1 FWC summary curves for the moderate curve (left) and mild curve (right) at 100% output power

Figure 13 demonstrates the effect of adding hysteresis functionality using the moderate curve at 100% output power. Without hysteresis (left), the inverter output the power specified along the linear portion of the characteristic curve during decreases in frequency (latter portion of the test). With hysteresis enabled, the output power remained at zero during decreases in grid frequency, and it did not reach full power until the restoration frequency (60.1 Hz) was met. Note that the

time series plot in the left portion of Figure 13 represents the same data that are summarized in the left portion of Figure 12.

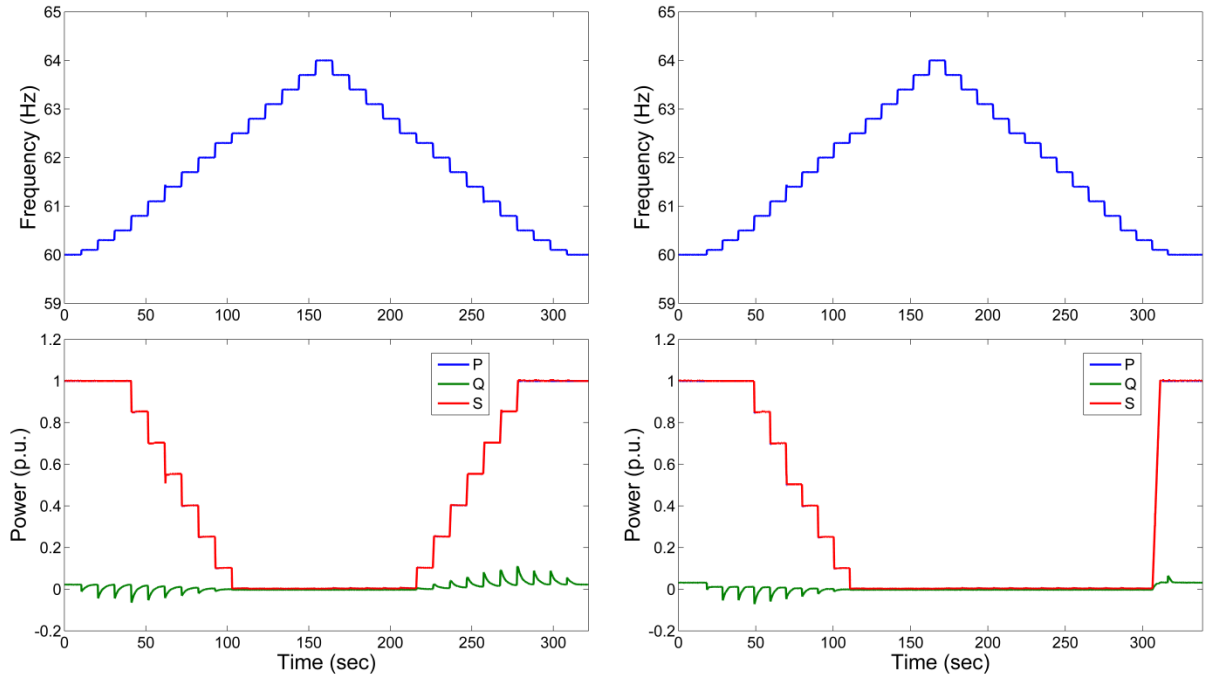

Figure 13. Inverter 1 FWC time series for the moderate curve at 100% output power showing the effects of no hysteresis (left) compared to adding hysteresis functionality (right)

Finally, Figure 14 shows summary plots demonstrating the effect of switching between the nameplate (right) and snapshot (left) modes for Inverter 1 using the moderate curve and 67% output power. (These modes are identical at 100% output power.) As expected, power curtailment began right at the start frequency in snapshot mode, but it started later in nameplate mode, which effectively changed the slope of the characteristic curve.

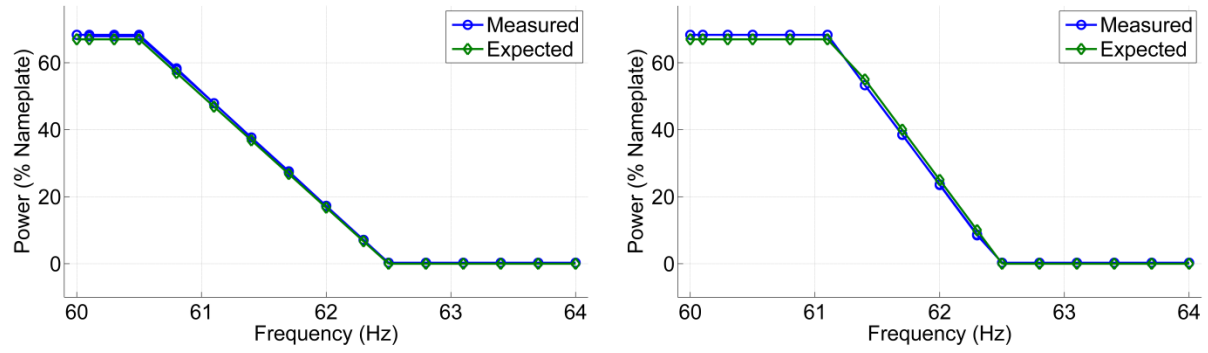

Figure 14. Inverter 1 FWC summary curves demonstrating snapshot mode (left) compared to nameplate mode (right), moderate curve at 67% output power

The maximum error in output power for any test point was 4.6% for one frequency step on Case 10 for Inverter 1. Other than that, all errors were ≤ 1.7%; it is unknown what caused the single

larger error in output power for this test case. A summary of errors for every frequency step is found in Appendix A.

Inverter 3 was likewise tested for cases 1–10 in Table 10, and it generally performed as expected. One distinct difference from Inverter 1 was that Inverter 3 always required hysteresis mode to be enabled, with the recovery frequency always set to less than or equal that of the start frequency. The example set of time series data in Figure 15 shows the difference between the aggressive curve and the mild curve at 100% output power. Much larger frequency excursions were required to force power curtailment with the mild curve, as expected. As shown, the power did not return to nominal until the frequency returned below the start frequency. This inverter also had a finite power ramp time when the mode was deactivated, which is demonstrated clearly in the mild curve's return to nominal, but it varied among tests. This inverter typically had some oscillations in reactive power (and thus apparent power) after a rapid frequency excursion, but it settled out after several seconds. The real power output remained relatively flat during these oscillations.

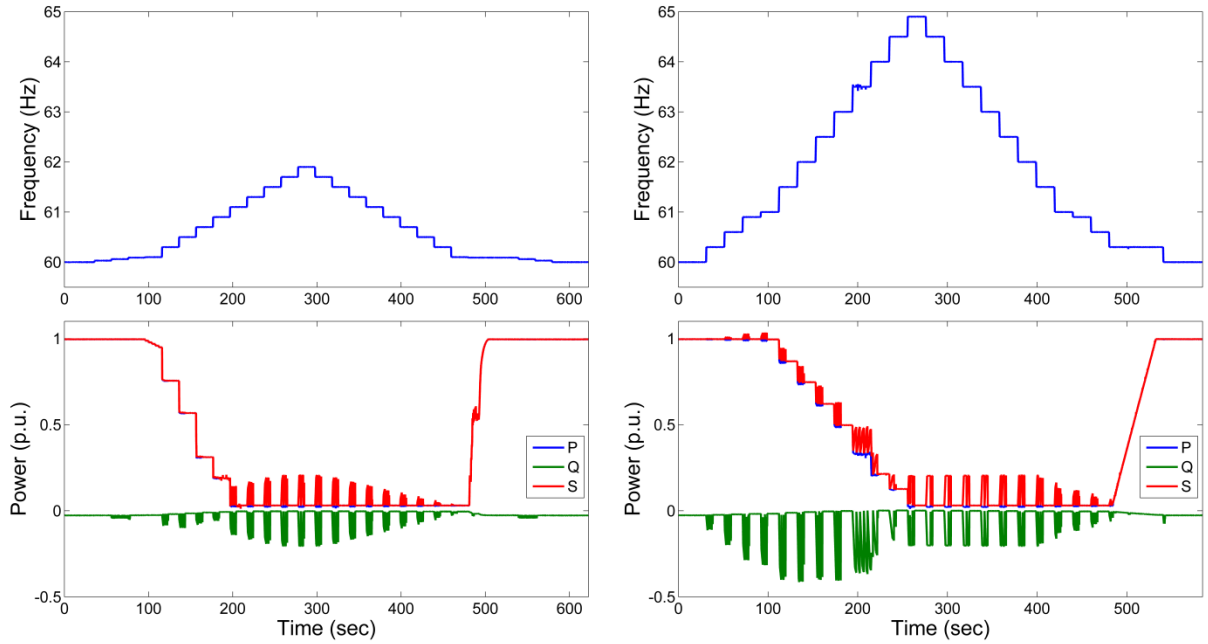

Figure 15. Inverter 3 FWC time series for the aggressive curve (left) and mild curve (right) at 100% output power

Figure 16 shows a pair of summary curves demonstrating the difference between 33% and 100% power output using the moderate curve. Power curtailment began at the same start frequency, which demonstrates that this inverter effectively operated in snapshot mode at all times. In the 100% power case, some power curtailment occurred right at the start frequency, which was the knee of the characteristic curve. Both tests show operation in hysteresis mode, as demonstrated by the zero output power regions in the linear portion of the curve (which occurred when the frequency returned to nominal). Also, a small power offset occurred in the zero power region, showing that the inverter did not curtail to zero power, but instead it remained near approximately 3% of nominal.

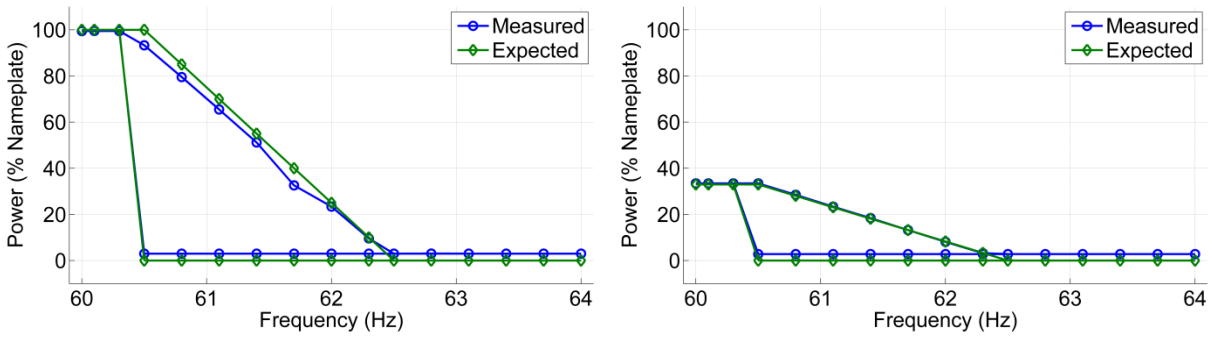

Figure 16. Inverter 3 FWC summary curves using the moderate curve at 100% output power (left) and 33% output power (right)

Finally, Figure 17 shows summary curves demonstrating the effect of changing the restoration frequency. In the left plot, power was restored when the frequency dropped to 60.30 Hz; whereas in the right plot, power was not restored until the frequency dropped to 60.05 Hz.

Overall, Inverter 3 had slightly higher errors between expected and actual output power, with a maximum error of 8.9%. Typically, errors were < 3% of the target power level. Tables showing errors for every frequency step for each test are shown in Appendix A.

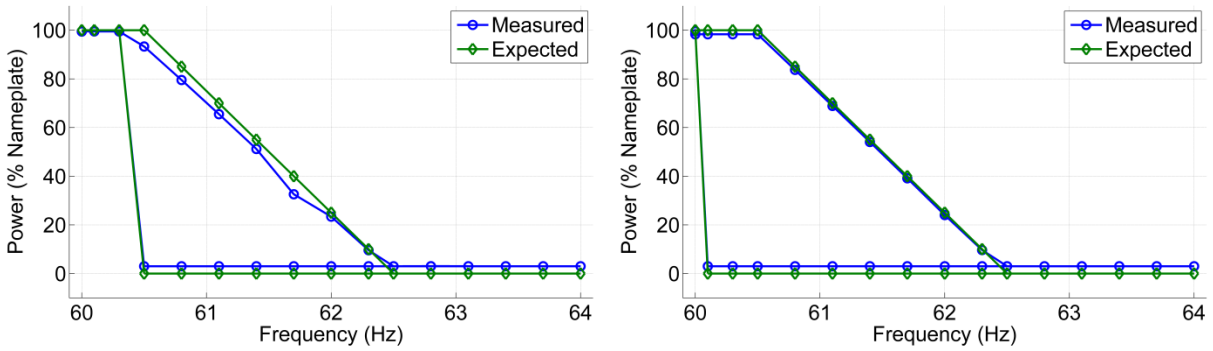

Figure 17. Inverter 3 FWC time series showing the effect of changing the restoration frequency from 60.5 Hz (left) to 60.1 Hz (right)

3.5 Volt-VAR Tests

3.5.1 Volt-VAR Test Procedures

Inverters with VVC help regulate grid voltage while minimizing real power reduction, as might occur in the volt-watt control function. A series of VVC tests were derived from the UL 1741 SA standard for this portion of the testing. Three different VVC curves were defined in conjunction with FPL for this portion of the testing, referred to as mild, moderate, and aggressive, based on their slopes; they are shown in Figure 18. Each curve is symmetrical, and it is characterized by a dead band around nominal voltage, a linear region for increasing/decreasing reactive power, and maximum reactive power limits. The peak reactive power for these curves depended on the inverter manufacturer, and it was scaled accordingly to each test inverter. The aggressive curve represents a very extreme implementation of this function, because no dead band exists, and

excursions from maximum positive to maximum negative reactive power occurred for voltage changes of only ±1%.

For each test, AC voltage was stepped through each segment of the VVC curve, capturing at least three data points within each segment, as required by UL 1741 SA. Each voltage step was held for at least two times the manufacturer's settling time so that the inverter stabilized at a steady-state output power operating point. Voltage was first stepped down to a minimum value, was ramped back to nominal, and was then stepped up incrementally to a maximum value; the voltage profiles depended on the curve type. Each voltage step was set for a ramp time of 16 ms (within one AC cycle).

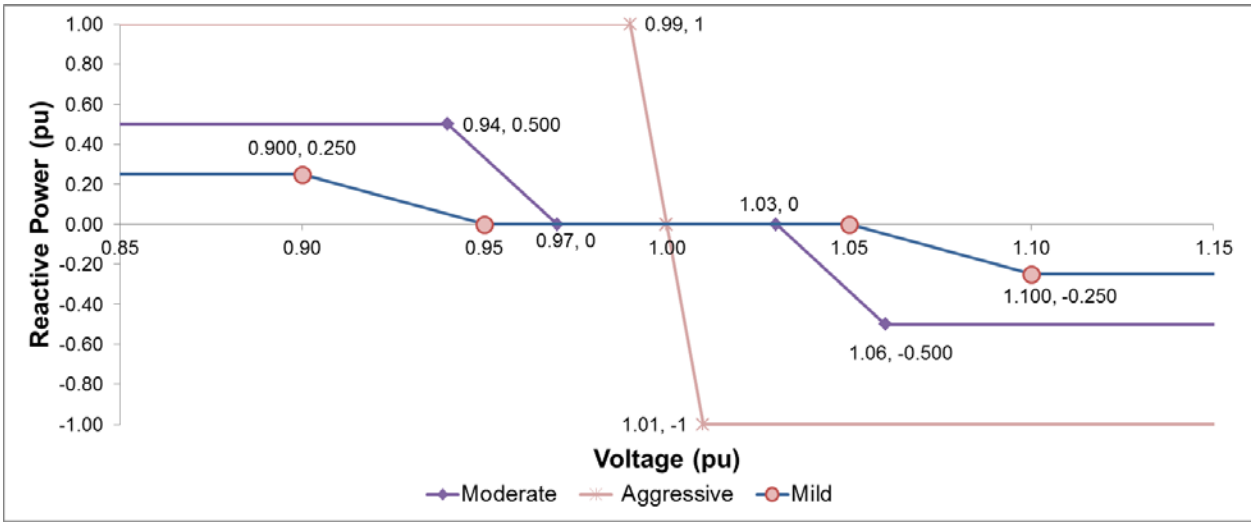

Figure 18. Mild, moderate, and aggressive volt-VAR control curves

Each of the curve types was tested with the inverter set to 100%, 67%, and 20% of nominal output power, which was controlled with the irradiance value at the PV simulators. In addition to the characteristic curves shown in Figure 18, inverters were tested with absorption and production offsets in the dead band region, with a magnitude of 5% of maximum reactive power, as required in UL 1741 SA. This created five different curves at three different power levels, for a total of 15 tests for each inverter, as summarized in Table 11. When necessary, voltage trip limits and/or trip times were manually adjusted to ensure that the inverter did not trip during the test.

Table 11. VVC Test Case Summary

Test Case	Curve Type	Offset	Max Reactive Power	Dead Band	Output Power (%)
1	Aggressive	None	Qmax	None	100
2	Aggressive	None	Qmax	None	67
3	Aggressive	None	Qmax	None	20
4	Moderate	None	Qmax/2	±3%	100
5	Moderate	None	Qmax/2	±3%	67
6	Moderate	None	Qmax/2	±3%	20
7	Mild	None	Qmax/4	±5%	100
8	Mild	None	Qmax/4	±5%	67
9	Mild	None	Qmax/4	±5%	20
10	Moderate	Production	Qmax/2	±3%	100
11	Moderate	Production	Qmax/2	±3%	67
12	Moderate	Production	Qmax/2	±3%	20
13	Moderate	Absorption	Qmax/2	±3%	100
14	Moderate	Absorption	Qmax/2	±3%	67
15	Moderate	Absorption	Qmax/2	±3%	20

3.5.2 Volt-VAR Test Results

Only inverters 1, 3, and 4 were capable of running the VVC function, so the tests were not run on Inverter 2. In general, all inverters performed as expected among all test cases, with any deviations described below. Representative time series and summary plots are shown below for each inverter, but they do not represent comprehensive test data. Appendix B includes a comprehensive set of tables showing the grid voltage, expected reactive power, measured reactive power, and percent error in power for every step of every test case.

Inverter 1 was capable of sourcing 100% of nameplate power with reactive power, and it was programmed for this setting. Figure 19 demonstrates Inverter 1 producing fully rated reactive power using the aggressive curve for 100% output power (left) and 67% output power (right). These plots show the standard test sequence, whereby voltage was stepped down in discrete steps, returned to nominal, and then stepped up in discrete steps. The voltage step magnitudes were selected to cover both the linear and flat regions of the characteristic curve of interest.

As shown, at the extreme low and high voltage levels real power was curtailed to zero, whereas reactive power reached the full nameplate rating of this product. Each voltage step led to an exponential time response in power output, and the output settled to a steady-state value before the next voltage step was executed. Some overshoots in power measurement occurred immediately following a step change in voltage, but these recovered very quickly.

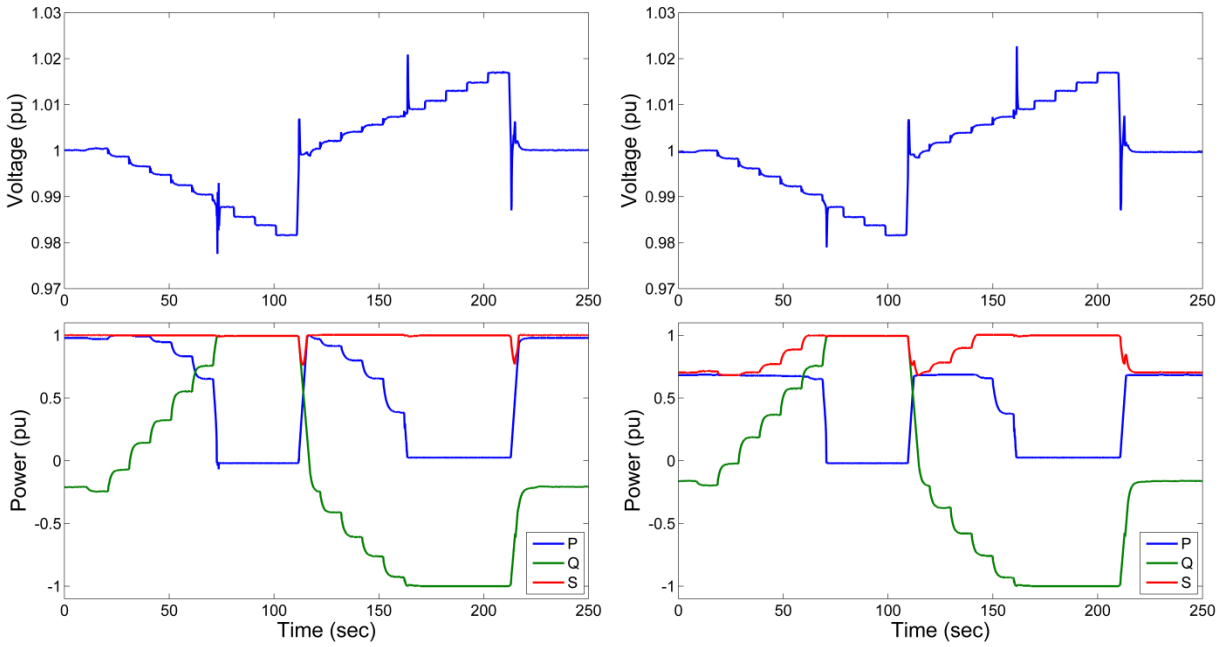

Figure 19. Inverter 1 VVC time series for the aggressive curve at 100% output power (left) and 67% output power (right)

Figure 20 shows summary curves for Inverter 1 operating at 100% output power, but it contrasts the difference between the moderate (left) and mild (right) curves. Both curves show very good agreement between expected and actual behavior. As expected, larger voltage excursions were required to force the maximum reactive power output for the mild curve, but the magnitude of the maximum value was one-half that of the moderate curve.

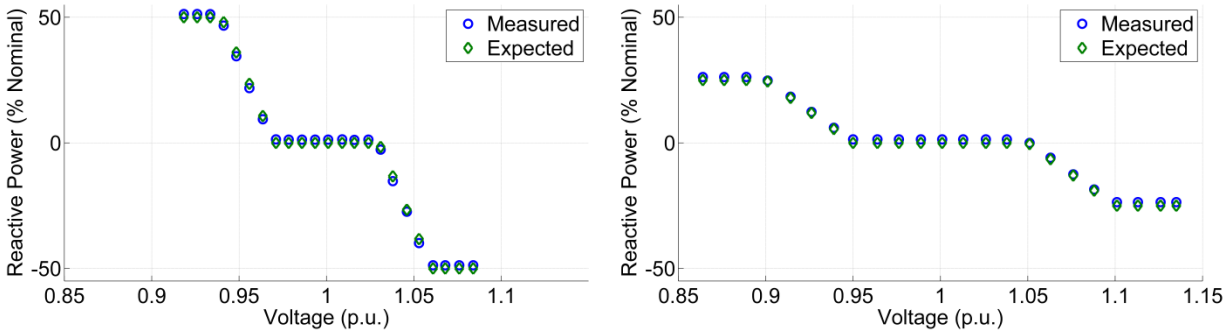

Figure 20. Inverter 1 VVC summary curves for the moderate curve (left) and mild curve (right) at 100% output power

Figure 21 demonstrates the difference between the production (left) and absorption (right) offset modes for Inverter 1 at 67% output power using the moderate curve. The output was mostly the same for each test case, except there was a small positive/negative offset in reactive power in the dead band for the production/absorption modes, which occurred at the beginning, middle, and end of these time series plots. The offset is equal to approximately 5% of the rated output power, as expected. Real power output was flat; it was near 67% of rated through all excursions in reactive power.

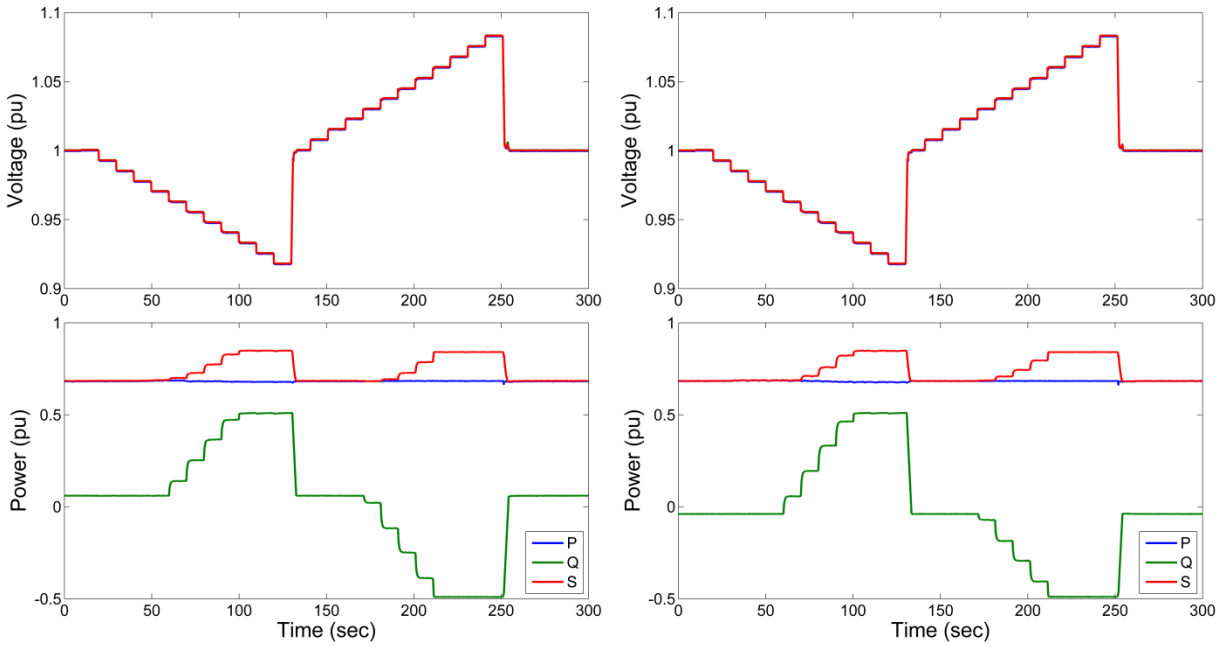

Figure 21. Inverter 1 VVC time series showing production offset (left) and absorption offset (right) at 67% output power

Inverter 3 had a stated maximum reactive power output of 60% of nameplate rating, and it was programmed for this setting. Figure 22 shows the difference between the aggressive and moderate curves for Inverter 3 at 100% output power. As expected, larger voltage excursions were required to obtain maximum reactive power output for the moderate curve, and the magnitude of the maximum reactive power output was one-half as large for this curve compared to the aggressive curve. Additionally, the dead band is shown for the moderate curve, but it was absent in the aggressive curve. A visible offset occurred between the measured and expected results, which was particularly prominent in the case of the aggressive curve. In fact, the nominal starting voltage led to a significant negative reactive power output. A discussion on the sources of error in the aggressive curve is found at the end of this section.

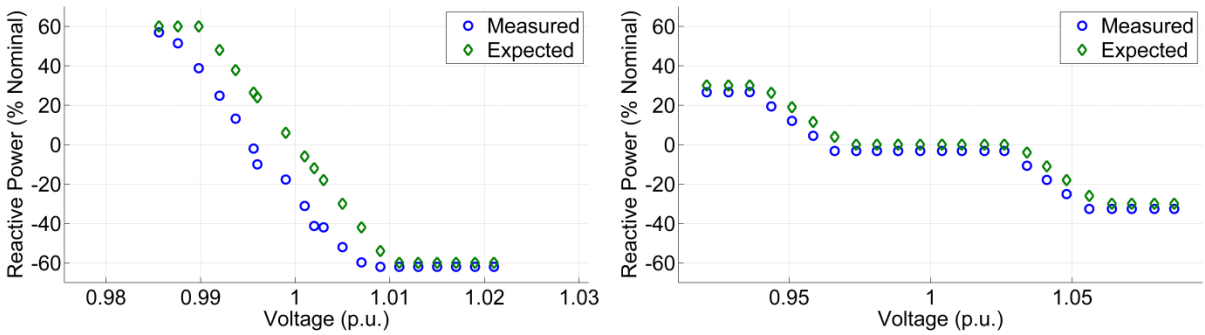

Figure 22. Inverter 3 VVC summary for the aggressive curve (left) and moderate curve (right) at 100% output power

Figure 23 shows example time series data for Inverter 3 operating with the mild curve at 100% (left) and 20% (right) output power. The reactive power profile was the same for both test cases, but real power needed to be curtailed for the 100% test case to produce the required reactive power, whereas real power was relatively flat for the 20% test case. There were some oscillations in real power output for one high-voltage step in the 100% test case, but those occurred at the knee of the curve. (This was not observed in the case of 67% output power.)

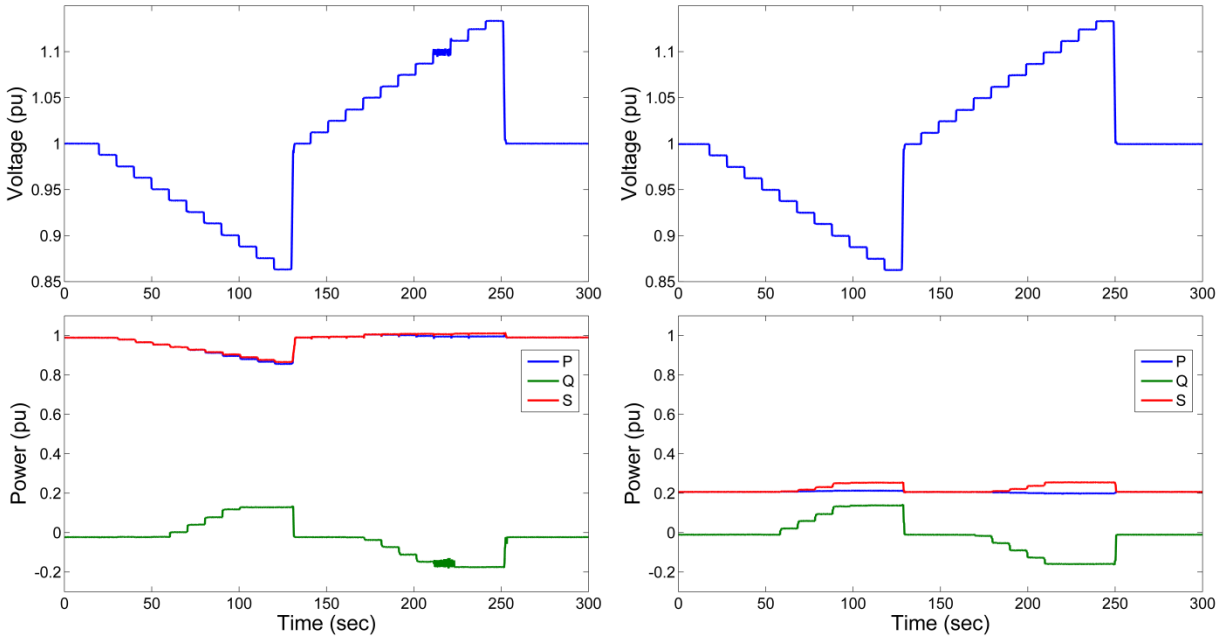

Figure 23. Inverter 3 VVC time series at 100% output power (left) and 20% output power (right) with the mild curve

Figure 24 demonstrates the differences between the production offset (left) and absorption offset (right) modes for Inverter 3 at 100% output power. As shown, the production offset mode did not produce the expected reactive power throughout the dead band; this behavior was consistent for the tests at 20% and 67% output power as well. The absorption offset test appeared to produce the expected result, with a small negative offset in reactive power in the dead band, although a similar offset was observed for tests without an offset programmed, suggesting that the offset feature did not perform as expected for this inverter.

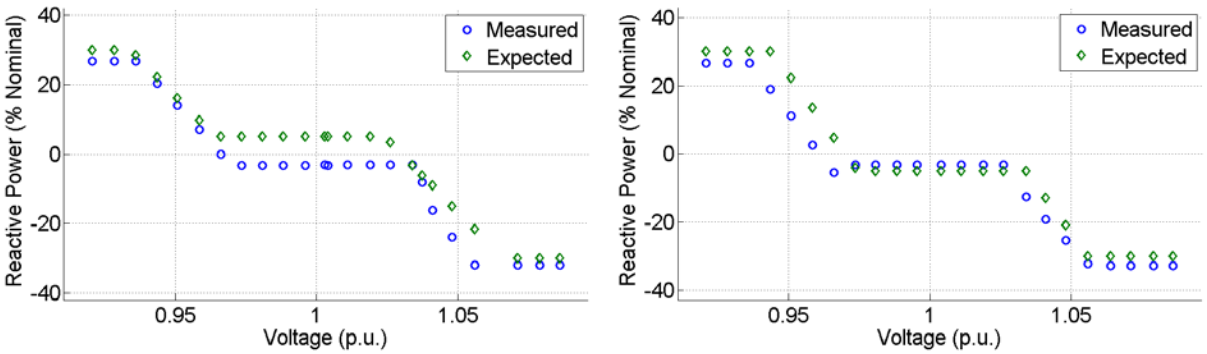

Figure 24. Inverter 3 VVC summary curves for production offset (left) and absorption offset (right) at 100% output power

Inverter 4 was rated for maximum reactive power of 50% of nameplate real power, and it was programmed accordingly. Figure 25 shows the different behaviors for the moderate curve (left) and mild curve (right) at 67% output power. As expected, larger voltage excursions were required to obtain maximum reactive power output for the mild curve, and the maximum reactive power was one-half that of the moderate curve. In both tests, as shown, the reactive power did not settle into a steady-state value in the linear region of the curve, but the flat regions of the curve behaved as expected. This behavior in the linear region was typical among all tests for this inverter. Also, the one dropout in power measurement for the case of the mild curve was not a typical response for this inverter.

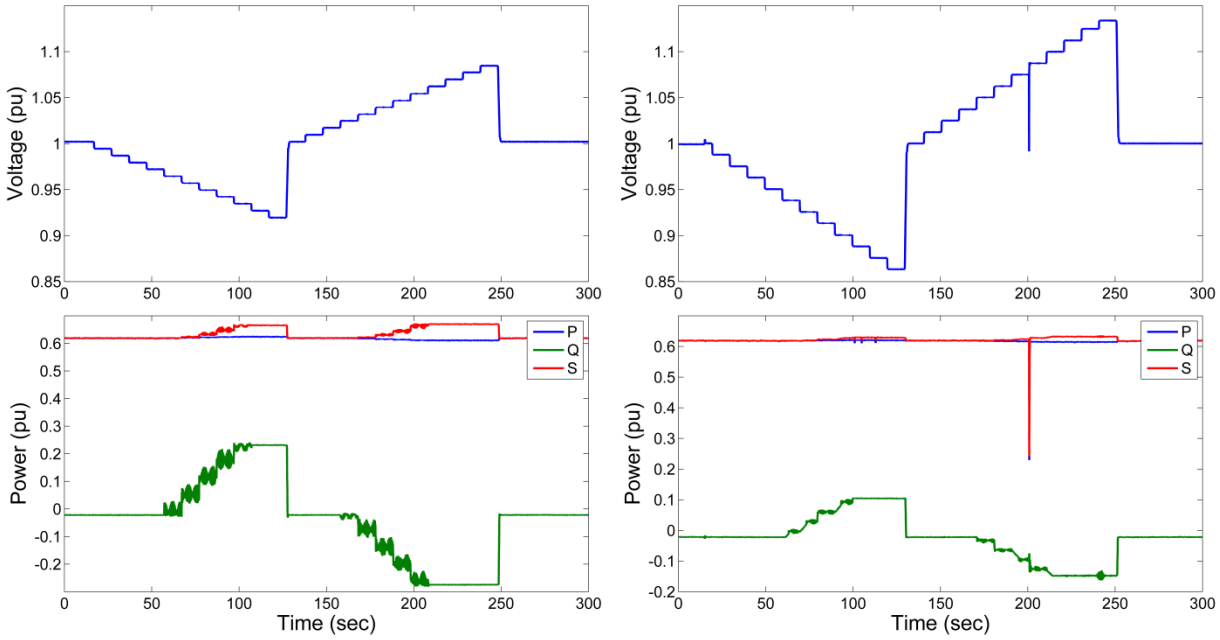

Figure 25. Inverter 4 VVC time series with the moderate curve (left) and mild curve (right) at 67% output power

Figure 26 shows the summary curves for Inverter 4 using the aggressive curve at 67% (left) and 20% (right) output power. In both cases, the inverter was able to output maximum reactive

power regardless of real power output level; however, there was a sizable offset between the expected and actual output, similar to that observed for Inverter 3. A similar offset was present at 100% output power using the aggressive curve. A discussion of possible sources of error in the aggressive curves is found at the end of this section. The steady-state reactive power reported for the summary plots in the linear regions were subject to judgment, given that it never settled to a constant value for this inverter.

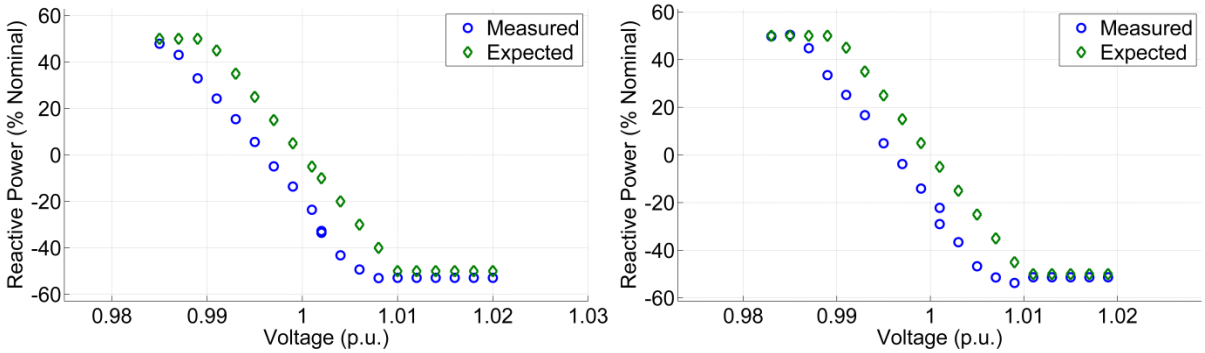

Figure 26. Inverter 4 VVC summary curves at 67% output power (left) and 20% output power (right) for the aggressive curve

Figure 27 shows time series data demonstrating the difference between the production offset mode (left) and absorption offset mode (right) for Inverter 4 at 100% output power. As expected, the inverter was able to produce the maximum reactive power in the flat regions of the characteristic curve, and there was a small positive/negative offset for the production/absorption offset cases in the dead band, which occurred at the beginning, middle, and end of these time series; however, these data also show the issues with reaching a steady-state reactive power output in the sloping region. Additionally, the production offset was approximately +2% of nameplate power, whereas the absorption offset was approximately -8% of nameplate. This is consistent with the approximate 2–3% offset in expected power factor that was observed in fixed power factor tests.

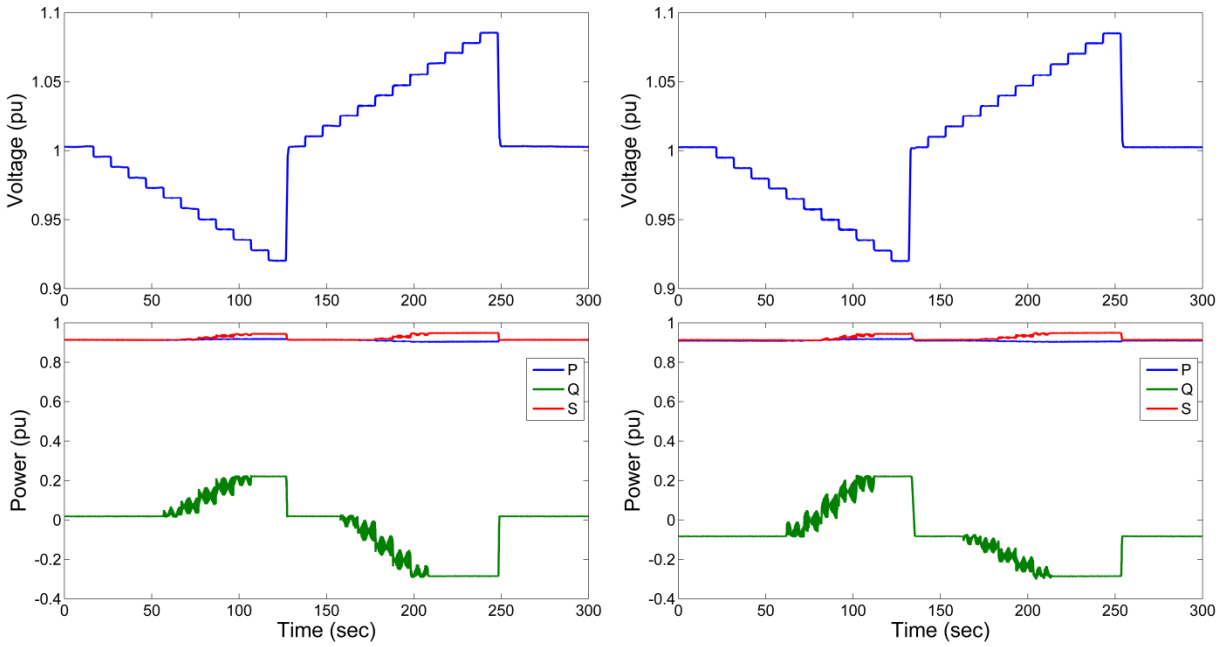

Figure 27. Inverter 4 VVC time series with the production offset (left) and absorption offset (right) at 100% output power

Several sources of error existed in these tests, which particularly affected results for the aggressive curve tests. The MSA in voltage was 2% for Inverter 1 and 1% for Inverter 3 and Inverter 4. The aggressive curve required an excursion between zero and maximum reactive power output for a 1% change in terminal voltage, with no dead band around nominal. Such a steep curve created a very challenging situation because a wide difference in reactive power was required for voltage changes within the manufacturers' stated ability to measure voltage. Additionally, there was a finite cable length between the inverter terminals and the probe points for the instrumentation, so even small voltage drops could create discrepancies between the expected and actual reactive power outputs. Both of these factors compounded to create noticeable offsets between the actual and expected output behaviors for each inverter, affecting all tests but particularly the aggressive curve.

3.6 Efficiency Tests

3.6.1 Efficiency Test Procedures

Given that typical inverter efficiency ratings fail to evaluate inverter performance at non-unity power factor, several variables of interest were tested to provide comparative analyses of inverter performance among a range of operating conditions. The primary variables of interest for the efficiency study were input power, DC input voltage, and fixed power factor. Similar to the FPF tests, each inverter was run at steady state for 60 seconds at a given set of operating conditions, and the reported efficiencies are an average of sampled efficiencies during this time window (at a sampling rate of 10 Hz at power analyzer). AC currents were measured using Yokogawa 701930 current probes with 1% accuracy, maximum range of 150 A, and output of 10 mV/A. The power analyzer was set at the range of 500 mV for these probes. DC currents were measured using a 1 mΩ shunt resistor with 0.25% tolerance and a ratio of 100 mV/100 A. The 50 mV range was

used on DC current inputs at the power analyzer. AC and DC voltages were directly input to high-voltage modules on the power analyzer, and all signals were filtered at 100 kHz.

Each inverter was tested at several DC input voltages from the PV simulator, DC input power ratings, and output power factors. The power factors of interest included ±0.80, ±0.90, and 1.00; the power levels of interest were 25%, 50%, 75%, and 100% of rated power; the DC input voltages of interest were 580, 680, and 780 V_{DC}. These variables were combined in different ways to create 22 tests cases, which are summarized in the test results in Table 12. Variable DC voltages were tested only at the 50% output power levels due to current limits on the PV simulator at lower voltages; all other tests were completed at the 780 V_{DC} level. The DC voltage levels were selected to be within each inverter's rated power point tracking voltages, with some buffer given to avoid the extremes of any individual range. Operating points were selected by adjusting the open-circuit voltage, short-circuit current, and irradiance level at the PV simulator to attain the desired output power at the target DC voltage for each test at unity power factor. For tests below full power, the primary variable used to adjust the power level was the irradiance level, with fine adjustments in voltage and current used to obtain the desired operating point. Each operating point was selected such that the inverter operated within ±5 V_{DC} of the target voltage; momentary excursions outside of this range were permissible due to power point tracking perturbations, but the average voltage was required to reside within this range. The output power was required to be within +1% of the target value at unity power factor.

For non-unity power factor operation, output power was curtailed by varying amounts depending on the inverter. Inverters 1 and 3 had no margin between real and apparent power ratings, and thus they reduced real power output at any non-unity power factor setting. Inverters 2 and 4 had slightly higher rated apparent power ratings than real power ratings, and they could support full real power operation to ±0.90 power factor. As such, the input power was the fixed variable in these tests. Due to this power curtailment, tests that were operated in the 100% output power rating at non-unity power factors occurred at slightly different DC input voltages due to required excursions in power point tracking.

3.6.2 Efficiency Test Results

Figure 28 shows a summary of efficiency test results as a function of output power (x-axis) and power factor (marker type) for each inverter (color). As shown, Inverter 1 tended to have the highest efficiencies among all operating conditions, with Inverter 3 generally the next highest and Inverter 2 and Inverter 4 with very similar results. As expected, unity power factor operation led to the highest efficiencies for all inverters, except for some cases at the 25% output power level. Operation at -0.80 power factor led to the lowest efficiencies for each inverter, often 1.0–1.5% lower than unity power factor. Maximum efficiencies occurred at 75% output power at unity power factor, with small drops at full power output. Maximum efficiencies tended to occur at 50% output power for operation at +0.80 power factor, and they were in the power range of 50–75% for operation at -0.80 power factor. Finally, the relative amount of power curtailment required to support operation ±0.80 power factor can be observed for each inverter, and there tended to be sharper reductions in efficiency for these tests at full power.

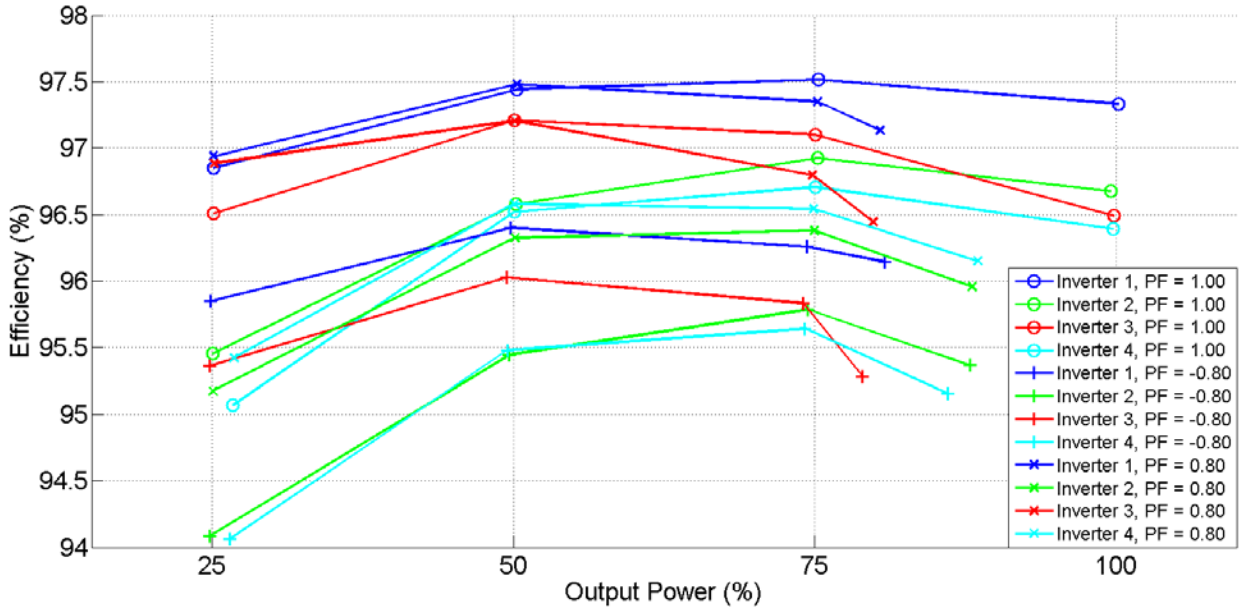

Figure 28. Efficiency comparisons for each inverter as a function of power factor and output power (all tests at 780 V_{DC})

Figure 29 shows a summary of efficiencies as a function of power factor (x-axis) and output power (marker type) for each inverter (color). Note that this plot shows an additional power factor level (±0.90) but only for two different power levels (75% and 100%) relative to the previous plot. Inverter 1 again had the highest efficiencies for all operating conditions, with mixed results for the other inverter types. Slightly higher efficiencies occurred at the 75% power level than the 100% power level, maximum efficiencies occurred at unity power factor, and efficiency decreased with decreasing power factor magnitude. Interestingly, every inverter had lower efficiencies at absorbing (negative) power factors than at producing (positive) power factors of the same magnitude.

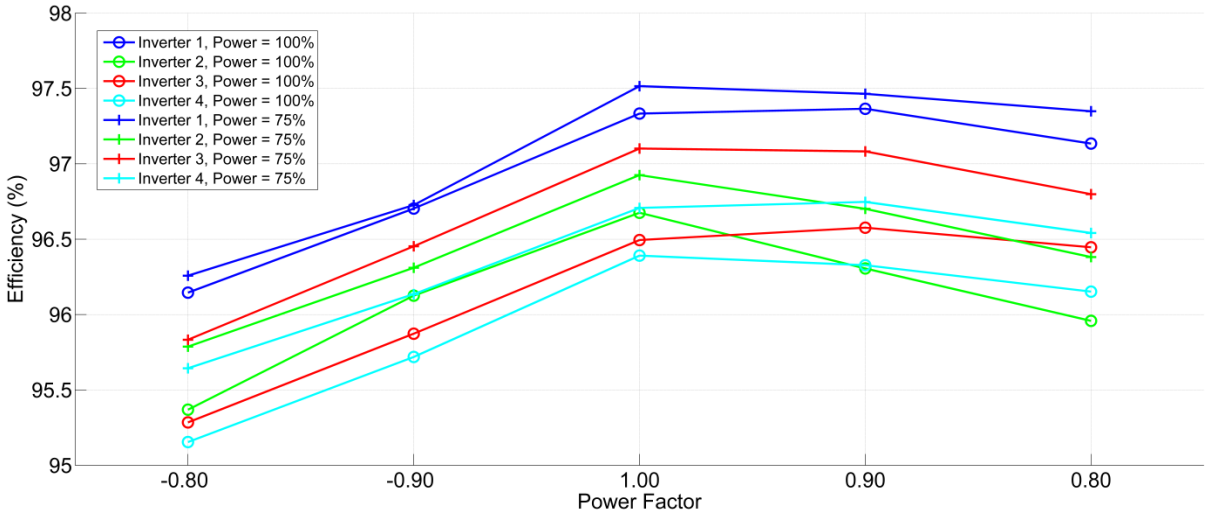

Figure 29. Efficiency comparisons for each inverter as a function of power factor and output power (all tests at 780 V_{DC}, 75%, and 100% output power only)

Figure 30 shows a summary of efficiencies for different DC input voltages (x-axis) and power factors (marker type) for each inverter (color). In this case, Inverter 3 achieved slightly higher efficiencies than Inverter 1 at lower voltages, although the results were very close. Every inverter tended to have very small differences in efficiency at the levels of 580 V_{DC} and 680 V_{DC}, but they either increased (Inverter 1 and Inverter 2) or decreased (Inverter 3 and Inverter 4) by a fractional percentage at the level of 780 V_{DC}. The lowest efficiencies for every inverter occurred at a power factor of -0.80.

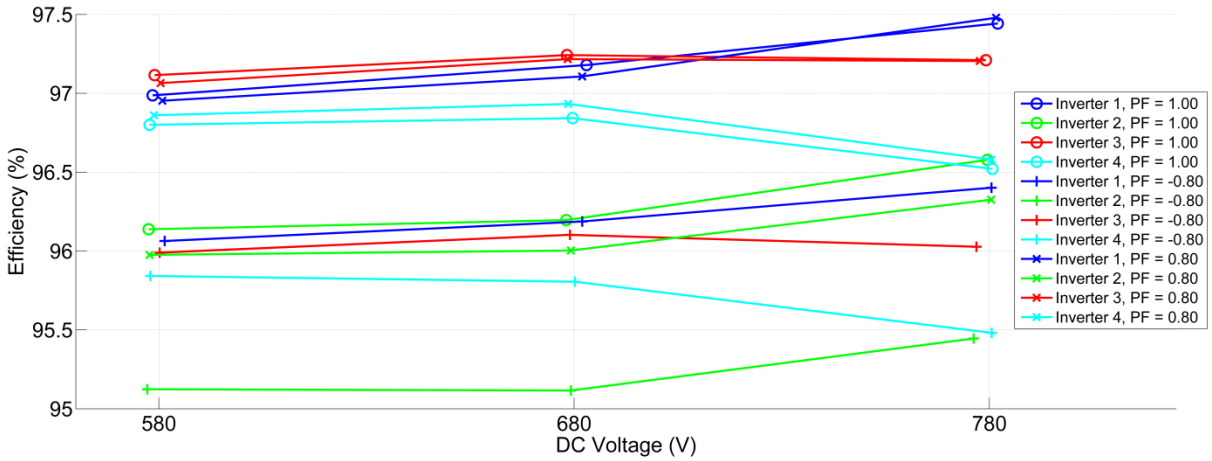

Figure 30. Efficiency comparisons for each inverter as a function of power factor and DC voltage (50% power only)

Table 12 shows a summary of all efficiency test results. Note that all data in this table is contained in the previous three figures in one form or another.

Table 12. Efficiency Test Result Summary

DC Voltage	Power Factor	Output Power (%)	Inverter Number and Efficiency (%)			
			1	2	3	4
580	1.00	50	97.0	96.1	97.1	96.8
580	-0.80	50	96.1	95.1	96.0	95.8
580	0.80	50	97.0	96.0	97.1	96.9
680	1.00	50	97.2	96.2	97.2	96.8
680	-0.80	50	96.2	95.1	96.1	95.8
680	0.80	50	97.1	96.0	97.2	96.9
780	1.00	50	97.4	96.6	97.2	96.5
780	-0.80	50	96.4	95.4	96.0	95.5
780	0.80	50	97.5	96.3	97.2	96.6
780	1.00	75	97.5	96.9	97.1	96.7
780	-0.90	75	96.7	96.3	96.5	96.1
780	-0.80	75	96.3	95.8	95.8	95.6
780	0.90	75	97.5	96.7	97.1	96.7
780	0.80	75	97.3	96.4	96.8	96.5
780	1.00	100	97.3	96.7	96.5	96.4
780	-0.90	100	96.7	96.1	95.9	95.7
780	-0.80	100	96.1	95.4	95.3	95.2
780	0.90	100	97.4	96.3	96.6	96.3
780	0.80	100	97.1	96.0	96.4	96.2
780	1.00	25	96.9	95.5	96.5	95.1
780	-0.80	25	95.8	94.1	95.4	94.1
780	0.80	25	96.9	95.2	96.9	95.4

Several important factors should be considered when interpreting the efficiency data, and the results should be considered on a comparative, rather than absolute, basis. In particular, several possible sources of errors in accuracy were present (probes, instrumentation, etc.), so the reported efficiencies may deviate from those stated by the manufacturer. Despite such sources of inaccuracy, all inverters were subjected to the same test setup for all test cases, and all probes were recalibrated (zeroed) at the power analyzer at the beginning of a new testing period; however, differences in efficiency on the order of several tenths of a percent were observed for the *same inverter under the same test conditions* from one day to the next, likely due to varying levels of component heating, ambient temperature conditions, etc.

One additional consideration is the effect of power point tracking algorithms on full power efficiency results. It was observed that some products switched between power point tracking mode and constant AC power mode for very slight changes in input, and such mode switching could also cause efficiency changes on the order of several tenths of a percent. Efforts were

made to seek a stable operating point for each inverter, but some products were more dynamic than others in terms of switching between modes. An example of such behavior for Inverter 1 is shown in Figure 31. Step changes in efficiency occurred throughout the unity power factor case (left), whereas there was a relatively flat efficiency measurement at -0.90 power factor (right); note that the range in y-axis scaling is the same to demonstrate the relative amount of excursion in measurement. The effect of averaging the perturbations in these tests did not cause a change of more than ±0.1% in reported efficiency, which is within the rounding tolerance of all efficiency data, which were reported to three significant digits.

Given these considerations, the data show relative differences in efficiency, but this test does not claim to show absolute efficiency data. Additionally, very small differences in efficiency among test cases and inverter type are likely within the margin of error for this test setup.

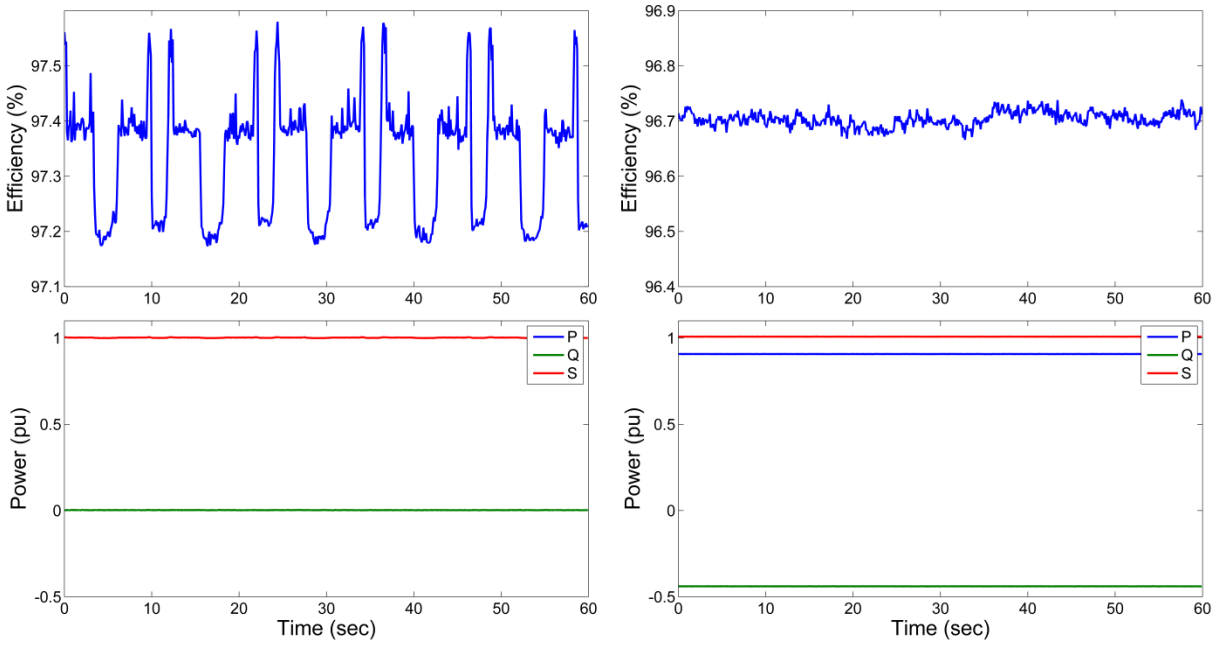

Figure 31. Efficiency tests at a power factor of 1.00 (left) and -0.90 (right) and full power output for Inverter 1

3.7 Anti-Islanding Tests

3.7.1 Anti-Islanding Test Procedures

Because many GSFs such as ride-through, FWC, and VVC have the objective of supporting the grid during voltage and frequency excursions, there is increasing concern that such functions could adversely impact anti-islanding detection. As such, anti-islanding tests were run on each inverter with different combinations of GSFs enabled to examine the impacts of these functions on island detection.

All anti-islanding tests were run under the test procedures required in IEEE 1547, which describes the use of a resonant resistive-inductive-capacitive load to create a difficult loading scenario for islanding detection (IEEE, 2003; IEEE, 2014). The basic test circuit is shown in Figure 32, where the Simulated Area EPS was realized using the MX-45 grid simulator, Switch

S1 was a shunt trip circuit breaker, and the resistive-inductive-capacitive load was the Simplex Trident 100-kVA resistive-inductive-capacitive load bank, which has 100-W resistive load steps and 75-VA capacitive and inductive load steps. All tests were run at 100% inverter power, and the resistive-inductive-capacitive load was tuned for unity quality factor, such that the fundamental component of the grid current was less than 2% of nominal. After the circuit was operating in steady state, S1 was opened, and the amount of time for the inverter to cease to energize the load was measured via the current waveform. Each test was run five times, with 1% changes in the inductive load for each successive test (two tests with increased load, two tests with decreased load).

Three different sets of GSFs were programmed on the test inverters for each set of tests, when available. California Rule 21 FRT and VRT settings were programmed for all tests, and they were the only GSFs enabled for the first set of five tests. For inverters with more limited programmability, as described in the previous section, the worst-case settings were used (widest limits, longest trip times). For the second set of tests, inverters capable of VVC functionality were programmed with the most aggressive curve used in previous testing along with the FRT/VRT settings. Note that in some cases, some reactive power was output from the test inverter at nominal voltage due to the aggressive characteristic curve, and the reactive load was adjusted accordingly to minimize grid current. Finally, inverters capable of FWC were programmed with the most aggressive curve from the previous testing (VVC disabled) along with the FRT/VRT settings. Each set of GSF settings was repeated at five different loading cases, creating a maximum of 15 tests per inverter.

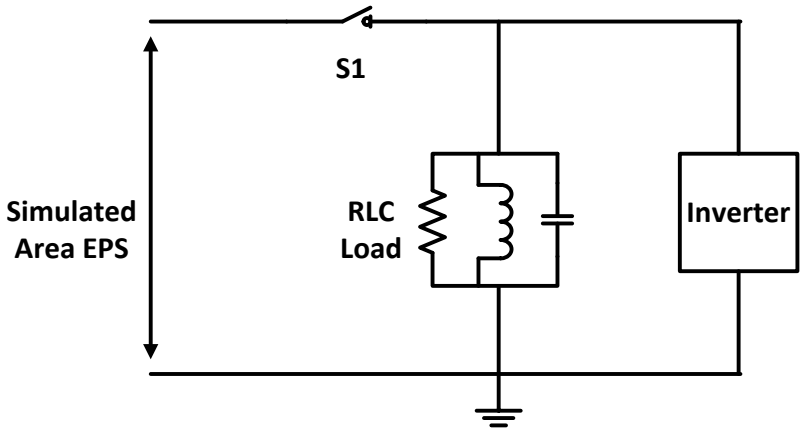

Figure 32. Anti-islanding test circuit

3.7.2 Anti-Islanding Test Results

All anti-islanding test results are summarized in Table 13 and Figure 33 for every test case. VVC was not programmable for Inverter 2, and FWC was not programmable for Inverter 2 or Inverter 4, so these tests cases were not run. Inverter 2 had increased run-on times (ROTs) at both the maximum and minimum inductive loads, so several additional tests were run with continually decreasing/increasing inductive load, creating a total of 11 test cases. The load was decreased by two increments of 1% and also increased by four successive increments of 1% to account for the six additional test cases. A summary of the mean and maximum ROTs for each set of test cases is summarized in Table 14.

As shown in the summary data, results were mixed depending on the test inverter and the GSFs enabled. Overall, Inverter 1 had the shortest and most repeatable ROTs, including the shortest overall ROT of all test cases. Inverter 3 tended to have the longest ROTs for each of the different GSF settings (again with the exception of one test case for Inverter 2). It should be emphasized that a longer ROT does *not* necessarily imply worse behavior from one inverter to the next. IEEE 1547 requires that inverters cease to energize within 2 seconds of island formation, and the time under which such detection occurs depends on the manufacturer's choice of detection strategy, and it may be purposely programmed to sustain longer ROTs.

The more important metric to consider is the effect of GSF combination on ROT for each inverter. For Inverter 1, the mean and maximum ROT decreased slightly with VVC enabled, and it decreased further with FWC enabled. Regardless, the ROTs were all much faster than the required trip time, and differences were on the order of several AC cycles. Similarly, the mean and maximum ROTs for Inverter 4 decreased slightly with VVC enabled, but the differences were also within several AC cycles. Inverter 3 demonstrated increased mean and maximum ROTs with VVC, and there were even higher ROTs with FWC enabled; however, even the peak ROT for all test case (1671 ms) was safely with the 2-second trip requirement.

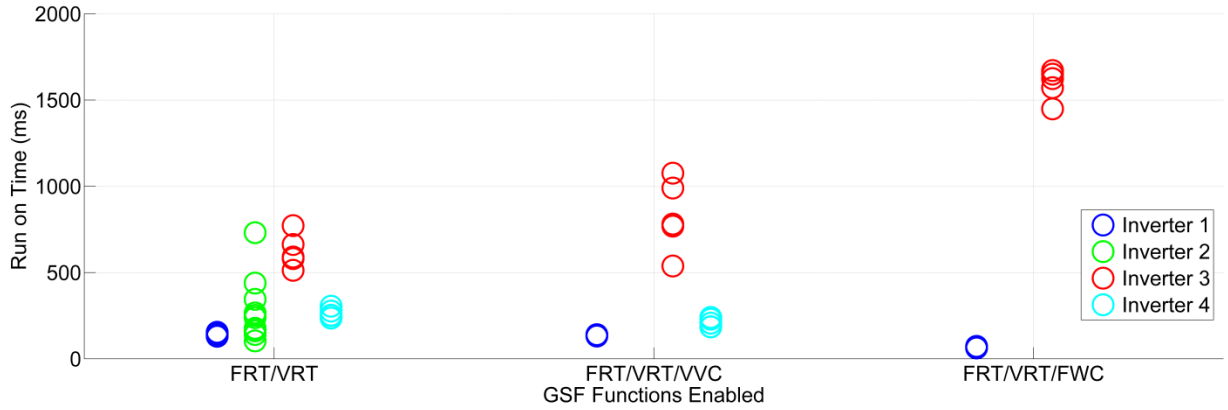

Figure 33. Anti-islanding test summary data showing trip time for every test case

Table 13. Anti-Islanding test result summary

Grid Support Functions Enabled	Reactive Load (%)	Inverter Number and Run on Time (ms)			
		1	2	3	4
VRT, FRT	98	142	439	513	236
VRT, FRT	99	148	345	772	277
VRT, FRT	100	154	252	663	305
VRT, FRT	101	137	104	590	253
VRT, FRT	102	131	162	581	250
VRT, FRT, VVC	98	140	239[a]	769	186
VRT, FRT, VVC	99	137	141[a]	990	240
VRT, FRT, VVC	100	132	731[a]	1076	207
VRT, FRT, VVC	101	132	166[a]	781	185
VRT, FRT, VVC	102	133	266[a]	538	230
VRT, FRT, FWC	98	69	177[a]	1624	N/A
VRT, FRT, FWC	99	72	N/A	1671	N/A
VRT, FRT, FWC	100	72	N/A	1650	N/A
VRT, FRT, FWC	101	68	N/A	1572	N/A
VRT, FRT, FWC	102	63	N/A	1449	N/A

[a] Additional tests run with VRT and FRT enabled, see discussion

Table 14. Anti-Islanding Test Result Mean and Maximum Run-On Times for Each Test Group

Grid Support Functions Enabled	Metric	Inverter Number and Run-On Time (ms)			
		1	2	3	4
VRT, FRT	Mean	142.4	274.7[a]	623.8	264.2
	Maximum	154	731[a]	772	305
VRT, FRT, VVC	Mean	134.8	N/A	830.8	209.6
	Maximum	140	N/A	1076	240
VRT, FRT, FWC	Mean	68.8	N/A	1593.2	N/A
	Maximum	72	N/A	1671	N/A

[a] Statistics based on 11 test cases rather than 5

A waveform plot for the worst-case ROT for each inverter is shown in the following figures, and a comprehensive set of waveform plots for this class of tests has been provided to FPL for analysis. Note that for each of these figures, the grid simulator was disconnected at approximately 0.11 second. Figure 34 shows the longest ROT of 154 ms for Inverter 1 (left), as well as the longest ROT of 731 ms for Inverter 2 (right). Figure 35 shows the longest ROT of 1671 ms for Inverter 3 (left) as well as the longest ROT of 305 ms for Inverter 4 (right). Of particular note in Figure 35 is that Inverter 3 significantly reduced output power around 400–500 ms after the island event was triggered, before disconnecting approximately 1.0–1.5 seconds

later. This behavior was consistent for all tests with FWC enabled, suggesting that the inverter still detected an island within several hundred milliseconds, but may have been intentionally programmed to disconnect from the grid much later when operating with FWC mode enabled.

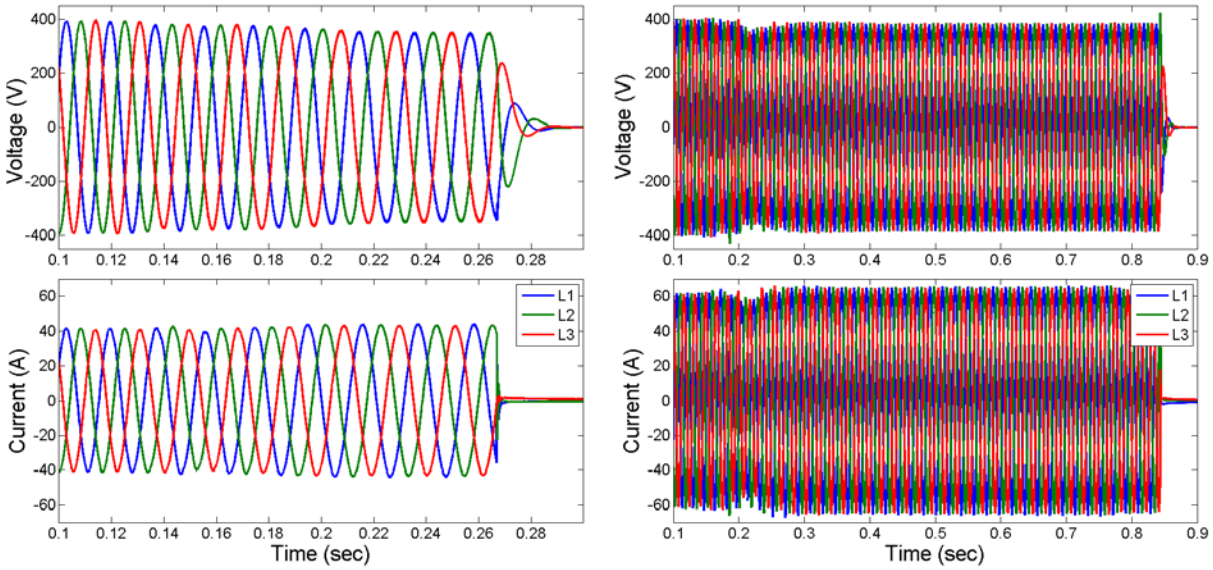

Figure 34. Longest ROTs for Inverter 1 (left) and Inverter 2 (right)

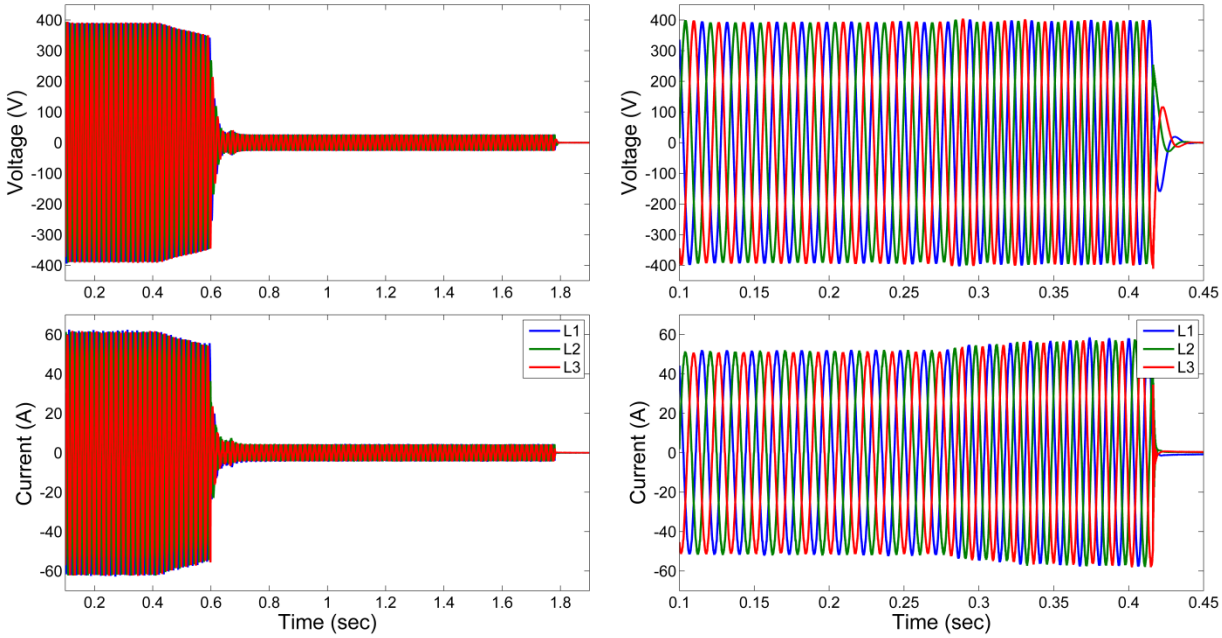

Figure 35. Longest ROTs for Inverter 3 (left) and Inverter 4 (right)

3.8 Load Rejection Overvoltage Tests

3.8.1 Load Rejection Overvoltage Test Procedures

LRO occurs when a portion of a distribution feeder becomes disconnected from the grid, resulting in a high ratio of PV generation to load. During the brief period before inverter controls detect the island situation, the current injected by the inverter into the load can cause transient overvoltages, particularly when the load power is much lower than the inverter output power. This phenomenon was previously studied by NREL for small residential inverters and a 12-kW commercial inverter (Nelson, *et al*., 2015), but it has not been examined in the output range of 24–36 kW as in this study.

A series of 11 LRO tests were run for each inverter at various ratios of inverter output power to load, following the same procedures are those described in the previous NREL LRO study. The basic test circuit is the same as those for the anti-islanding tests shown in Figure 32, except only purely resistive loads were used for these tests. Once the inverter was running at the target power level (adjusted by irradiance changes at the PV simulator), S1 was opened, forcing all inverter output current into the resistive load. These tests similarly used the MX-45 grid simulator as the Simulated Area EPS and the Simplex Trident load bank for resistive loads. The first 11 tests were run with California Rule 21 FRT and VRT settings programmed for all tests. For inverters with more limited programmability, as described in the previous section, the worst-case settings were used (widest limits, longest trip times). For inverters capable of VVC, a subsequent set of four tests was run for the test scenarios at the four highest inverter-to-load ratios. The peak voltage was measured using a sampling rate of 100 kHz at the oscilloscope and no filtering enabled.

3.8.2 Load Rejection Overvoltage Test Results

All LRO test results are summarized in Table 15 and Figure 36. VVC was not programmable for Inverter 4, so the additional four test cases were not run for this inverter.

As shown from the summary data, results were mixed depending on the test inverter and the inverter-to-load power ratio. The higher this ratio, the higher overvoltage magnitudes are expected, based on a simplified ideal current source model of the inverters. As shown in Figure 36, there is no clear correlation between the inverter-to-load ratio and the peak overvoltage magnitude, except perhaps for lower values of this ratio. In general, Inverter 3 had among the lowest overvoltage peaks. Almost no overvoltage was measured for Inverter 1 or Inverter 3 for unity inverter-to-load power ratios. Inverter 4 had several of the largest overvoltages of any of the tests, but the maximum for any test case was 152% of nominal, which is well below some overvoltages measured in the previous NREL LRO study. Finally, there was no clear evidence that enabling VVC caused any increase in peak voltage, and in several cases the peaks were lower than they were in cases without VVC enabled.

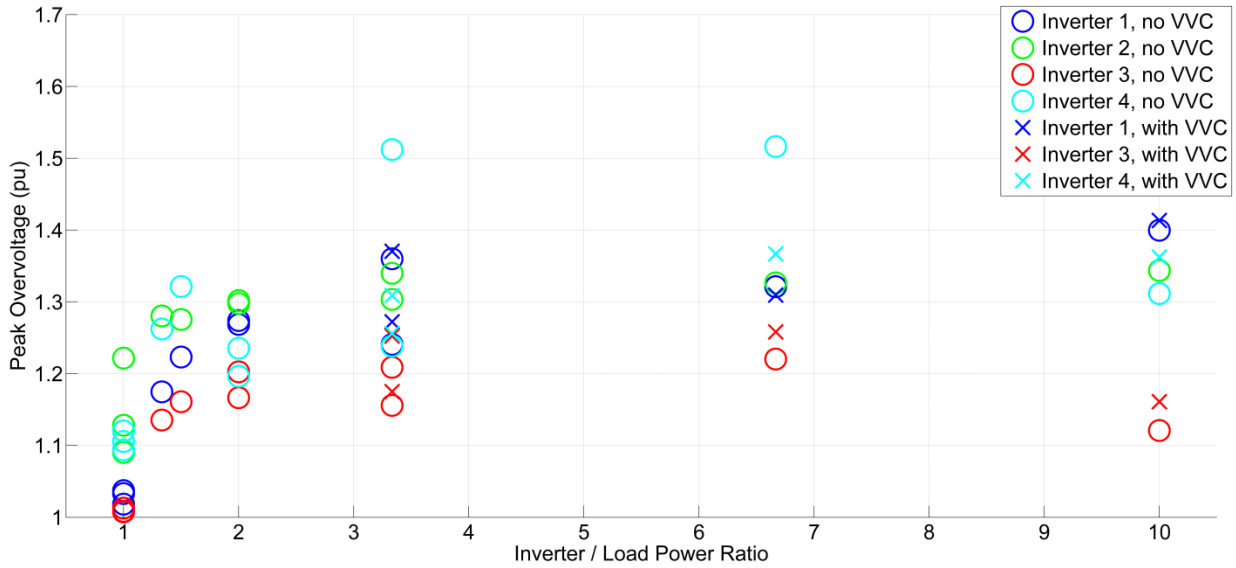

Figure 36. Load rejection overvoltage test summary data showing maximum peak voltage (as multiple of nominal peak voltage) for every test case

Table 15. Load Rejection Overvoltage Test Result Summary

Inverter Power (%)	Load Power (%)	VVC ON/OFF	Inverter Number and Peak Voltage (pu)[a]			
			1	2	3	4
100	100	OFF	1.04	1.09	1.01	1.11
100	67	OFF	1.22	1.28	1.16	1.32
100	50	OFF	1.27	1.30	1.17	1.24
100	33	OFF	1.36	1.34	1.16	1.24
100	10	OFF	1.40	1.34	1.12	1.31
67	67	OFF	1.03	1.13	1.01	1.09
67	50	OFF	1.17	1.28	1.14	1.26
67	33	OFF	1.27	1.30	1.20	1.20
67	10	OFF	1.32	1.33	1.22	1.52
33	33	OFF	1.02	1.22	1.01	1.12
33	10	OFF	1.24	1.30	1.21	1.51
100	33	ON	1.37	N/A	1.17	1.31
100	10	ON	1.41	N/A	1.16	1.36
67	10	ON	1.31	N/A	1.26	1.37
33	10	ON	1.27	N/A	1.25	1.26

[a] Voltages reported as a multiple of nominal L-N peak voltage

A waveform plot for the worst-case peak voltage for each inverter is shown in the following figures, and a comprehensive set of waveform plots for this class of tests has been provided to

FPL for analysis. Note that for each of these figures, the grid simulator was disconnected just after 0.01 second (a finite delay existed between the command and the opening of S1). Figure 37 shows the largest peak voltage of 141% of nominal for Inverter 1 (left) as well as the largest peak voltage of 134% of nominal for Inverter 2 (right), which occurred on two different tests. Figure 38 shows the largest peak voltage of 126% of nominal for Inverter 3 (left) as well as the largest peak voltage of 152% of nominal for Inverter 4 (right).

In addition to overvoltage magnitudes, the total duration of the overvoltage is important to understand the possibility of damaging equipment. At the time of this writing, a draft revision to IEEE 1547 proposes tiered limits on the total duration above different voltage levels. This draft specifies that the duration for more than 130% of nominal is less than 16 ms and the total duration for more than 140% of nominal is less than 3 ms. To date, this draft does not address test details such as inverter-to-load ratios nor whether the maximum duration limits are per phase or the sum of all three phases. Also, these duration limits were not required of inverters at the time the testing took place.

As shown in the example waveforms for inverters 1–3, the peak overvoltages were a single pulse (sometimes on several phases), lasting a very brief period of time, often on the order of tens of microseconds; however, Inverter 4 had several test cases similar to that shown in Figure 38, wherein the overvoltage increased during the course of approximately 7 AC cycles before the inverter tripped. The total durations above the nominal voltage threshold limits of 120%, 130%, and 140% was summed for all three phases and is shown in Table 16.

As shown, the total durations at each level are well below the proposed IEEE 1547 requirements for Inverters 1–3, but they are much longer for Inverter 4. The maximum duration for any of these inverters at more than 120% of nominal was 8.2 ms (Inverter 2); the maximum duration at more than 130% of nominal was 0.5 ms (Inverter 2); and the maximum duration at more than 140% of nominal was less than 0.1 ms (Inverter 1). Inverter 3 never exceeded the 130% threshold. In contrast, Inverter 4 had maximum durations of 100.5 ms, 55.4 ms, and 24.7 ms above the threshold levels, which all occurred on the test case shown in Figure 38.

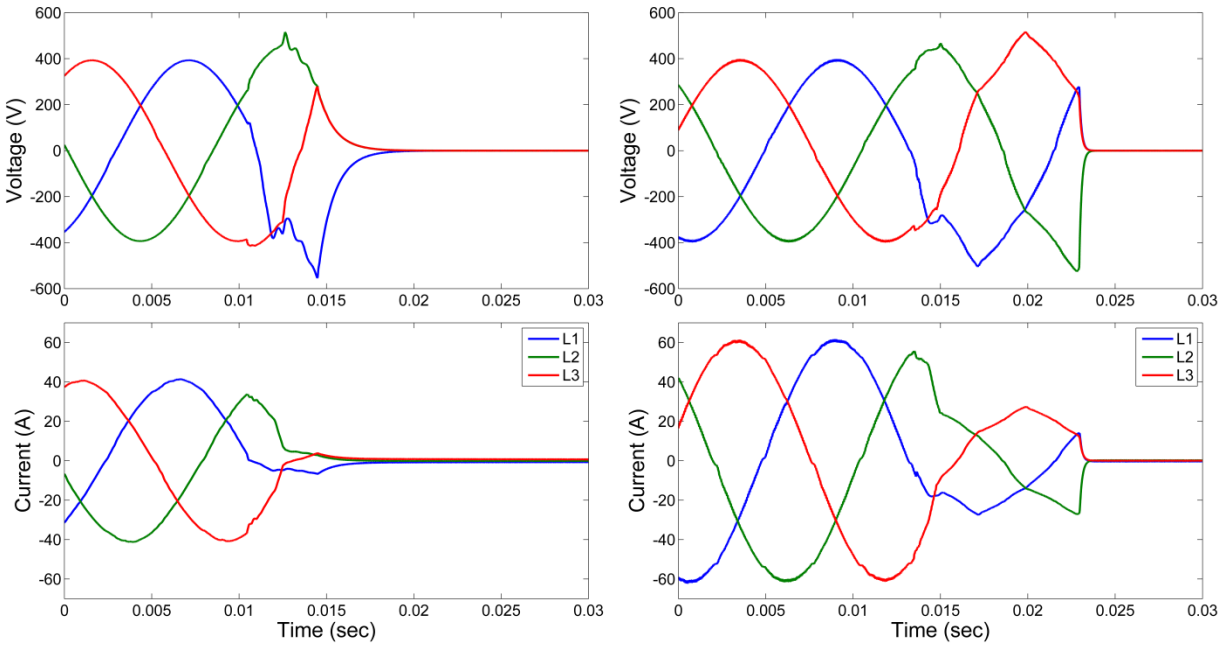

Figure 37. Largest peak voltage for Inverter 1 (left) and Inverter 2 (right)

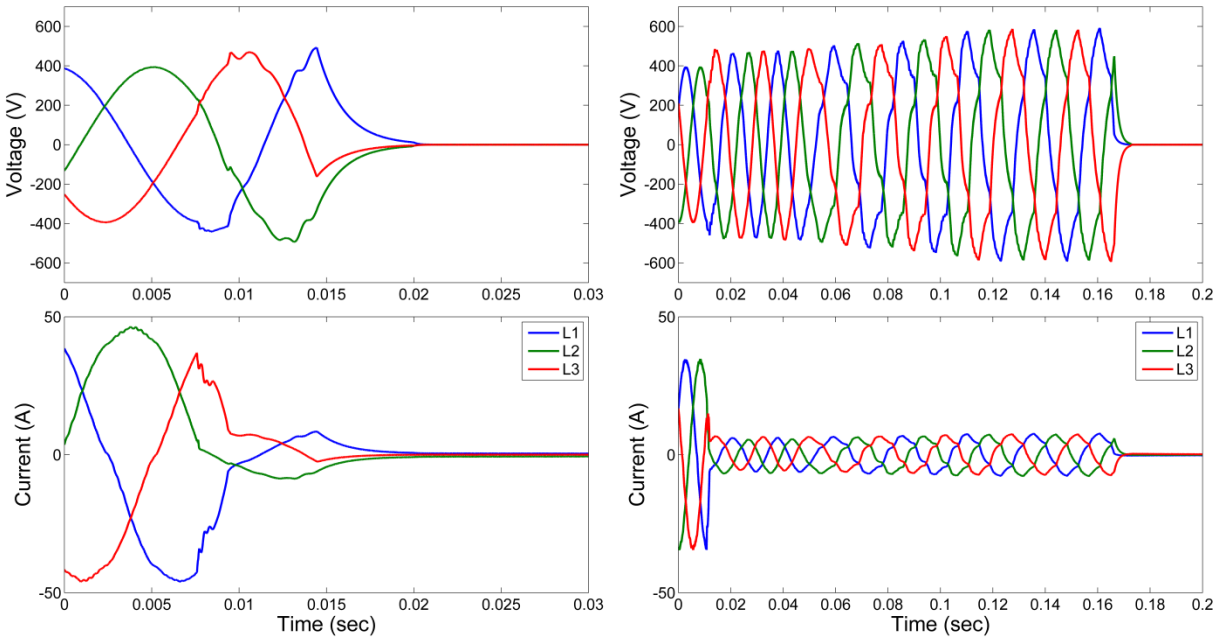

Figure 38. Largest peak voltages for Inverter 3 (left) and Inverter 4 (right)

Table 16. Overvoltage Durations Above 120%, 130%, and 140% Thresholds for Each Test Case

Inverter Power/ Load Power (%)	VVC ON/ OFF	Voltage Threshold (%) and Duration (ms)											
		Inverter 1			Inverter 2			Inverter 3			Inverter 4		
		120	130	140	120	130	140	120	130	140	120	130	140
100/100	OFF	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
100/67	OFF	1.0	0.0	0.0	8.2	0.0	0.0	0.0	0.0	0.0	17.0	0.3	0.0
100/50	OFF	1.1	0.0	0.0	2.4	0.0	0.0	0.0	0.0	0.0	1.1	0.0	0.0
100/33	OFF	0.7	0.3	0.0	2.7	0.5	0.0	0.0	0.0	0.0	1.8	0.0	0.0
100/10	OFF	1.1	0.5	0.0	1.6	0.3	0.0	0.0	0.0	0.0	13.9	0.5	0.0
67/67	OFF	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
67/50	OFF	0.0	0.0	0.0	6.7	0.0	0.0	0.0	0.0	0.0	3.0	0.0	0.0
67/33	OFF	1.3	0.0	0.0	3.3	0.0	0.0	0.1	0.0	0.0	0.0	0.0	0.0
67/10	OFF	0.9	0.2	0.0	2.1	0.3	0.0	1.0	0.0	0.0	100.5	55.4	24.7
33/33	OFF	0.0	0.0	0.0	1.1	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
33/10	OFF	0.6	0.0	0.0	7.1	0.1	0.0	0.1	0.0	0.0	70.1	41.9	20.7
100/33	ON	0.8	0.3	0.0	N/A	N/A	N/A	0.0	0.0	0.0	2.5	0.1	0.0
100/10	ON	1.0	0.4	0.1	N/A	N/A	N/A	0.0	0.0	0.0	16.1	1.0	0.0
67/10	ON	0.4	0.1	0.0	N/A	N/A	N/A	1.7	0.0	0.0	48.4	10.2	0.0
33/10	ON	0.9	0.0	0.0	N/A	N/A	N/A	3.7	0.0	0.0	2.8	0.0	0.0

An additional point of interest concerns run-on events for Inverter 2 when the load power matched the inverter power (three different test cases). Figure 39 shows the waveforms for this inverter for the unity inverter/load power tests at 67% and 33% power. As shown, the inverter continued to source current to the load for approximately 2.4 seconds and approximately 4.1 seconds, respectively (in the 100% power matched case, the run-on was approximately 640 ms). These ROTs would violate the 2-second requirement for disconnection for anti-islanding; however, LRO tests were run with resistive loads only, and this inverter successfully passed all anti-islanding tests described in the previous section.

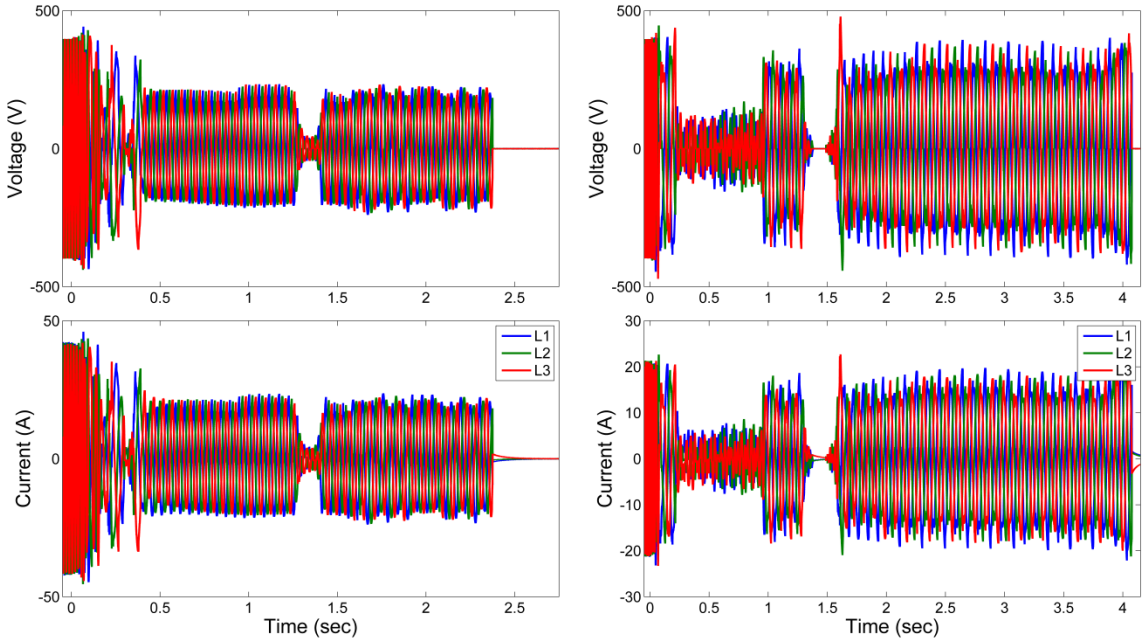

Figure 39. Run-on events for Inverter 2 at matched inverter-to-load ratios at 67% power (left) and 33% power (right)

3.9 Fault Tests

3.9.1 Fault Test Procedures

The final test in this study was to examine the effect of GSFs on fault current contribution. Each inverter was brought to full power and allowed to reach a steady state operating condition; then, both single-phase-to-ground and three-phase-to-ground faults were executed. Each of the four fault types was tested at unity power factor and ±0.80 power factors. Each test was repeated three times to randomize the phase angle on the AC cycle at which the fault occurred, leading to a total of 36 tests per inverter. Fixed power factor operation was tested because it was programmable for every inverter, and it also served as a proxy for inverter behavior when operating in VVC mode away from nominal voltage.

The basic test circuit was similar to the one used for anti-islanding and LRO testing, but it had an additional controlled switch (S2) to generate the fault, as shown in Figure 40. The inverter was run at full power, and the load was set to approximately match the inverter output to minimize grid current. The load was resistive only for unity power factor, and was a combination of resistive and inductive or capacitive for tests at ±0.80 power factors. The test was started with S1 closed and S2 opened. S1 was the output contactor of the grid simulator, which could be controlled with a command line prompt with the equipment software interface. S2 was a contactor, and only the phase(s) that was to be shorted was connected to this switch. Once running at steady state, a timing circuit was used to open S1 just before switch S2 was closed to create the fault; this timing was tuned such that S2 closed approximately one-half of one AC cycle after S1 was opened. A balanced load was added to the circuit so that the inverter would continue to operate at nominal condition for the small period of time after S1 was opened—effectively, islanded operation.

AC current was measured at each of the three phases at the inverter terminals to determine the fault current contributions. Current was measured with a Yokogawa 701931 current probe, which has bandwidth from DC to 10 MHz, and measurements were sampled at a rate of 10 MHz at the oscilloscope to capture high-frequency content of the fault current. All tests were run at the same VRT and FRT limits used for the California Rule 21 ride-through tests previously discussed, and both VVC and FWC were disabled.

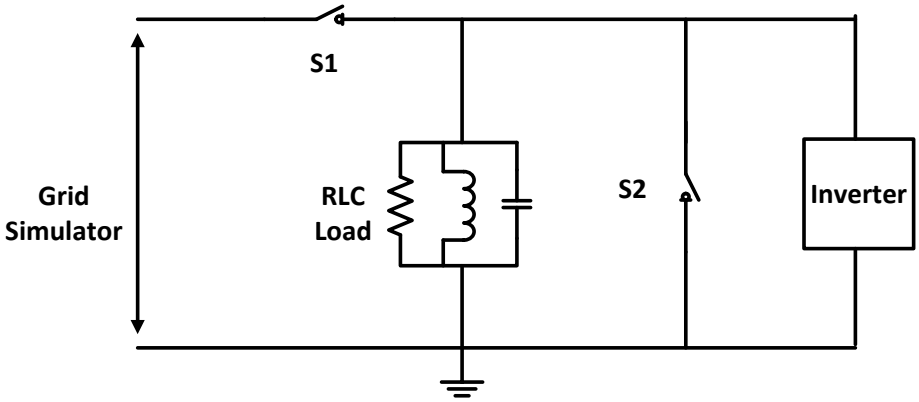

Figure 40. Fault test circuit

3.9.2 Fault Test Results

All single-phase-to-ground fault test results are summarized in Figure 41, Figure 42, and Table 17 for every test case. The magnitude of the peak fault current was independent of which phase was faulted, so a total of nine test cases (three tests for each of three phases) is summarized for each power factor value. Figure 41 shows the absolute magnitude of peak fault current, and the same data are normalized to the nominal current (from Table 1) for each inverter in Figure 42. Table 18 shows the mean and maximum normalized current peak for each set of nine fault cases at different power factors.

As shown in the summary data, there is no clear effect on peak fault currents as a function of power factor. Three of the four inverters had a slightly higher mean peak current at -0.80 power factor, but the range of peak values significantly overlapped for all inverters at all power factors. Inverter 1 consistently had the lowest peak currents and the smallest range of peak values. Inverters 3 and 4 had very similar behavior for absolute magnitudes, and Inverter 1 was also very similar when normalized to nominal current. Inverter 2 had both the largest peak current values and the widest range of responses. The maximum fault current peak was 202.7 A (2.99 p.u.) from Inverter 2. Note that reported fault maxima are the peak fault current of any of the three phases, and in some cases they occurred on a phase other than the one that was faulted.

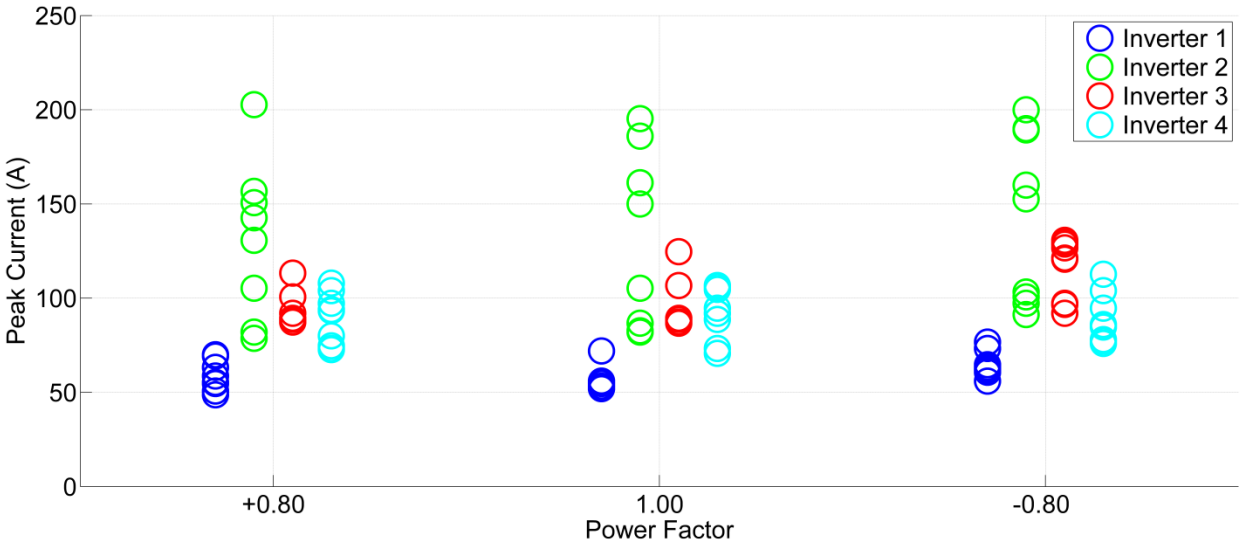

Figure 41. Peak fault current for all single-phase-to-ground fault test cases

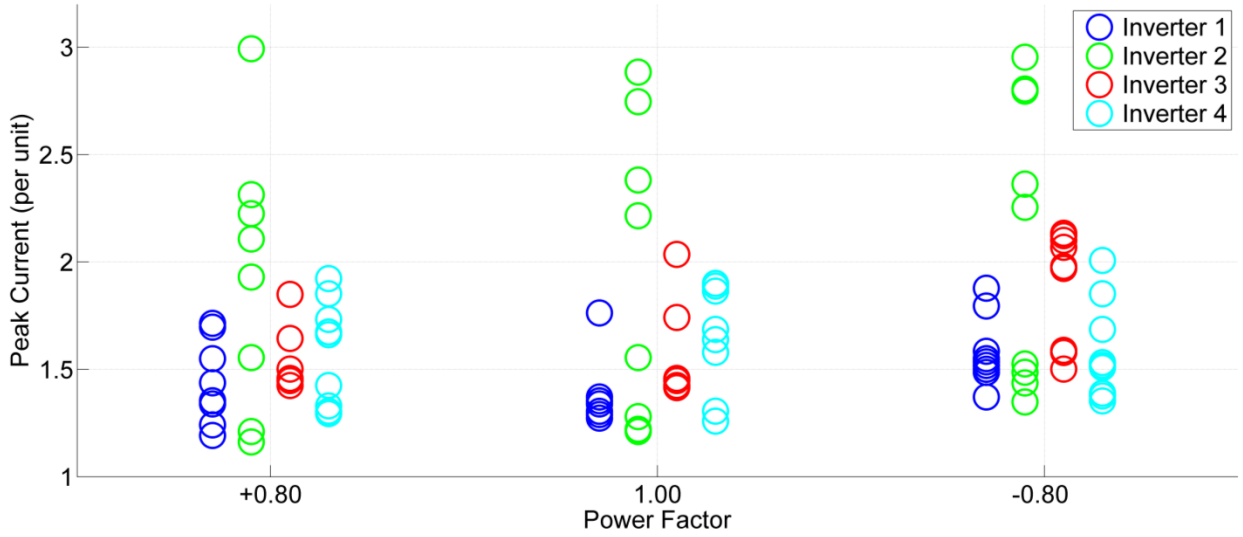

Figure 42. Normalized peak fault current for all single-phase-to-ground fault test cases

All three-phase-to-ground fault test results are summarized in Figure 45 and Table 19 for every test case. Table 20 shows the mean and maximum fault current peak for each set of three fault tests at different power factors.

As shown in the summary data, there is no clear effect on peak fault currents as a function of power factor. Inverter 1 once again had the most consistently low and repeatable peak fault current magnitudes, but it was similar to Inverter 2 for normalized peaks. Inverter 3 had the largest range and magnitude of fault current peaks for the three-phase case, with a maximum among all tests of 683.3 A (11.16 p.u.) at unity power factor. Note that for all three-phase fault data, the reported currents are the maximum of any of the in individual phases, and they are not additive among all phases.

Table 17. Single-Phase-to-Ground Fault Test Data

Fault Type	Power Factor	Inverter Number and Peak Fault Current (p.u.)			
		1	2	3	4
L1-G	+0.80	1.71	1.56	1.64	1.33
L1-G	+0.80	1.70	1.93	1.45	1.66
L1-G	+0.80	1.19	2.31	1.45	1.43
L2-G	+0.80	1.55	2.23	1.43	1.31
L2-G	+0.80	1.24	2.99	1.50	1.30
L2-G	+0.80	1.70	1.16	1.46	1.85
L3-G	+0.80	1.44	1.21	1.46	1.67
L3-G	+0.80	1.34	2.11	1.43	1.92
L3-G	+0.80	1.35	1.21	1.85	1.73
L1-G	1.00	1.29	2.38	1.74	1.69
L1-G	1.00	1.34	1.28	1.43	1.26
L1-G	1.00	1.35	2.22	1.43	1.31
L2-G	1.00	1.27	2.75	2.04	1.87
L2-G	1.00	1.37	2.88	1.45	1.64
L2-G	1.00	1.37	1.22	1.45	1.58
L3-G	1.00	1.37	1.56	1.46	1.90
L3-G	1.00	1.31	2.88	1.42	1.31
L3-G	1.00	1.76	1.21	1.43	1.89
L1-G	-0.80	1.58	2.95	1.59	1.53
L1-G	-0.80	1.52	2.80	1.50	2.01
L1-G	-0.80	1.88	1.44	2.12	1.52
L2-G	-0.80	1.50	1.35	1.58	1.85
L2-G	-0.80	1.80	2.26	1.97	1.69
L2-G	-0.80	1.37	1.53	1.98	1.35
L3-G	-0.80	1.55	1.49	2.07	1.38
L3-G	-0.80	1.54	2.81	2.10	1.39
L3-G	-0.80	1.49	2.36	2.13	1.51

Table 18. Single-Phase-to-Ground Fault Test Result Mean and Maximum Peak Currents

Power Factor	Metric	Inverter Number and Peak Fault Current (p.u.)[a]			
		1	2	3	4
+0.80	Mean	1.47	1.86	1.52	1.58
	Maximum	1.71	2.99	1.85	1.92
1.00	Mean	1.38	2.04	1.54	1.60
	Maximum	1.76	2.88	2.04	1.90
-0.80	Mean	1.58	2.11	1.89	1.58
	Maximum	1.88	2.95	2.13	2.01

[a] Statistics based on nine test cases

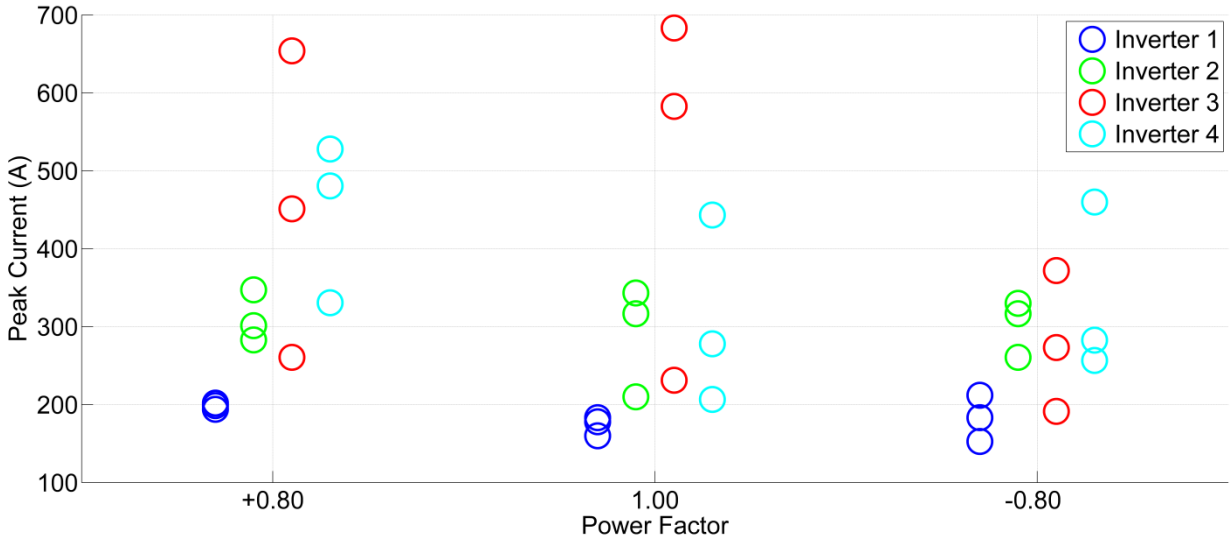

Figure 43. Peak fault current for all three-phase-to-ground fault test cases

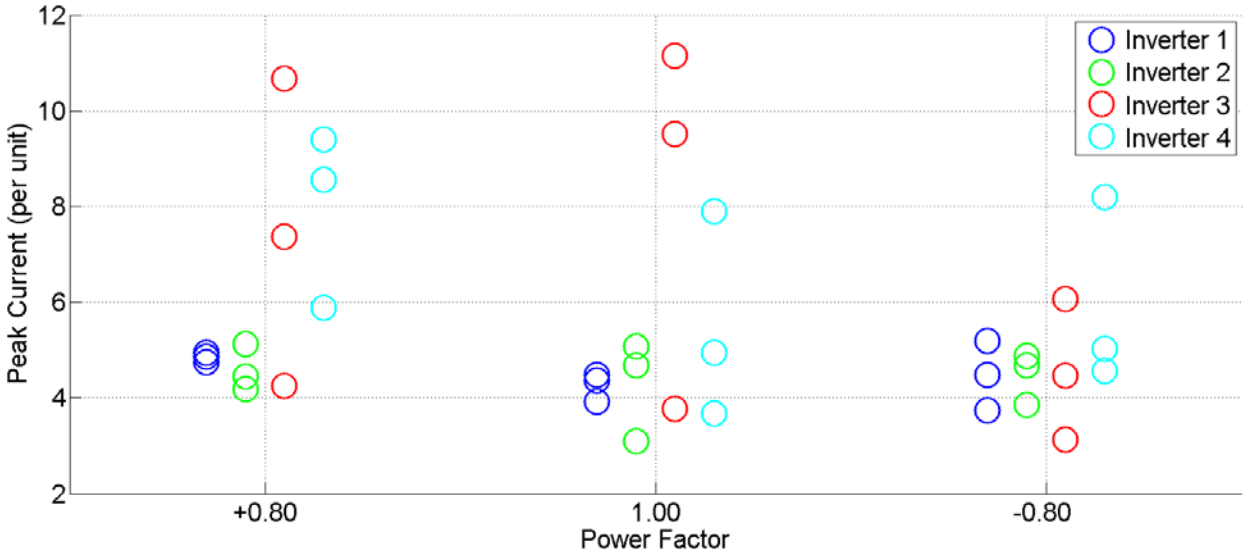

Figure 44. Normalized peak fault current for all three-phase-to-ground fault test cases

Table 19. Three-Phase-to-Ground Fault Test Data

Power Factor	Inverter Number and Peak Fault Current (A)			
	1	2	3	4
+0.80	4.75	4.45	7.37	8.56
+0.80	4.87	5.13	4.26	5.89
+0.80	4.95	4.18	10.68	9.41
1.00	4.36	3.10	11.16	3.68
1.00	3.92	4.68	9.52	4.95
1.00	4.49	5.07	3.78	7.90
-0.80	4.49	3.85	4.46	8.19
-0.80	5.19	4.87	6.07	4.57
-0.80	3.74	4.68	3.12	5.04

Table 20. Three-Phase-to-Ground Fault Test Result Mean and Maximum Peak Currents

Power Factor	Metric	Inverter Number and Peak Fault Current (A)[a]			
		1	2	3	4
+0.80	Mean	4.86	4.59	7.44	7.95
	Maximum	4.95	5.13	10.68	9.41
1.00	Mean	4.26	4.28	8.15	5.51
	Maximum	4.49	5.07	11.16	7.90
-0.80	Mean	4.47	4.47	4.55	5.93
	Maximum	5.19	4.87	6.07	8.19

[a] Statistics based on three test cases

A waveform plot for the worst-case peak fault current for each inverter is shown in the following figures for both the single-phase and three-phase fault test scenarios, and a comprehensive set of waveform plots for this class of tests has been provided to FPL for analysis. Note that for each of these figures, the grid simulator was disconnected at approximately 0 second. Figure 45 shows the maximum single-phase fault current of 76.7 A (1.88 p.u.) for Inverter 1 (left) and 202.7 A (2.99 p.u.) for Inverter 2 (right). The 202.7 A fault peak was very brief, with a duration of approximately 36 µs. Figure 46 shows the maximum three-phase fault current peaks of 212.0 A (5.19 p.u.) for Inverter 1 (left) and 347.3 A (5.13 p.u.) for Inverter 2 (right).

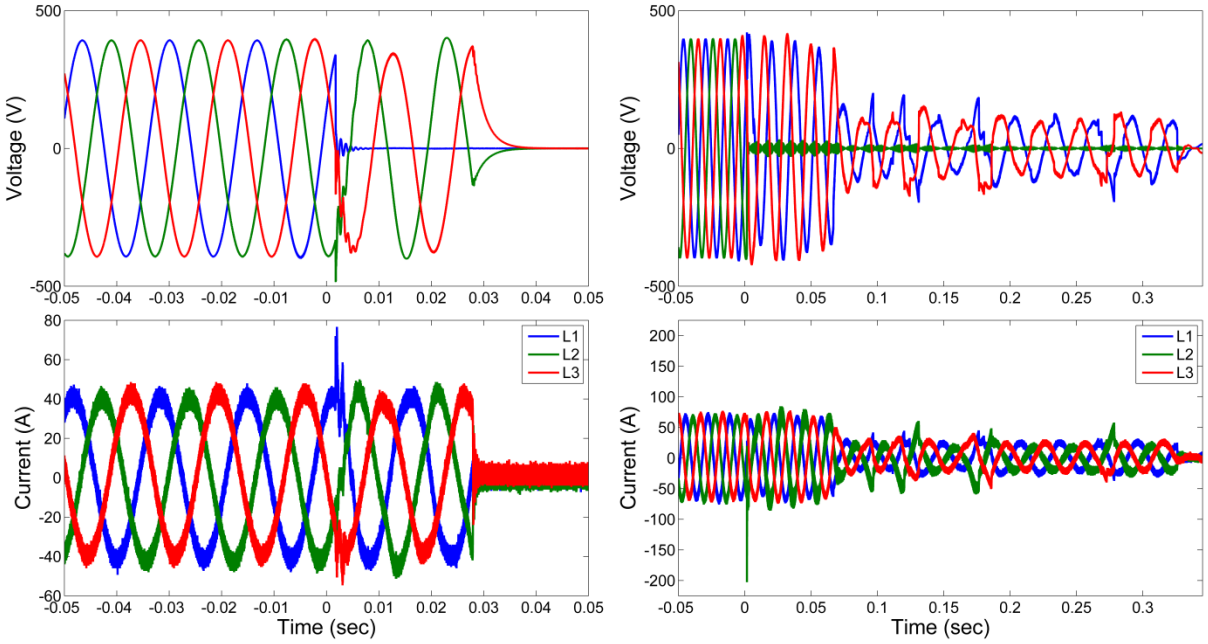

Figure 45. Largest peak single-phase fault currents for Inverter 1 (left) and Inverter 2 (right)

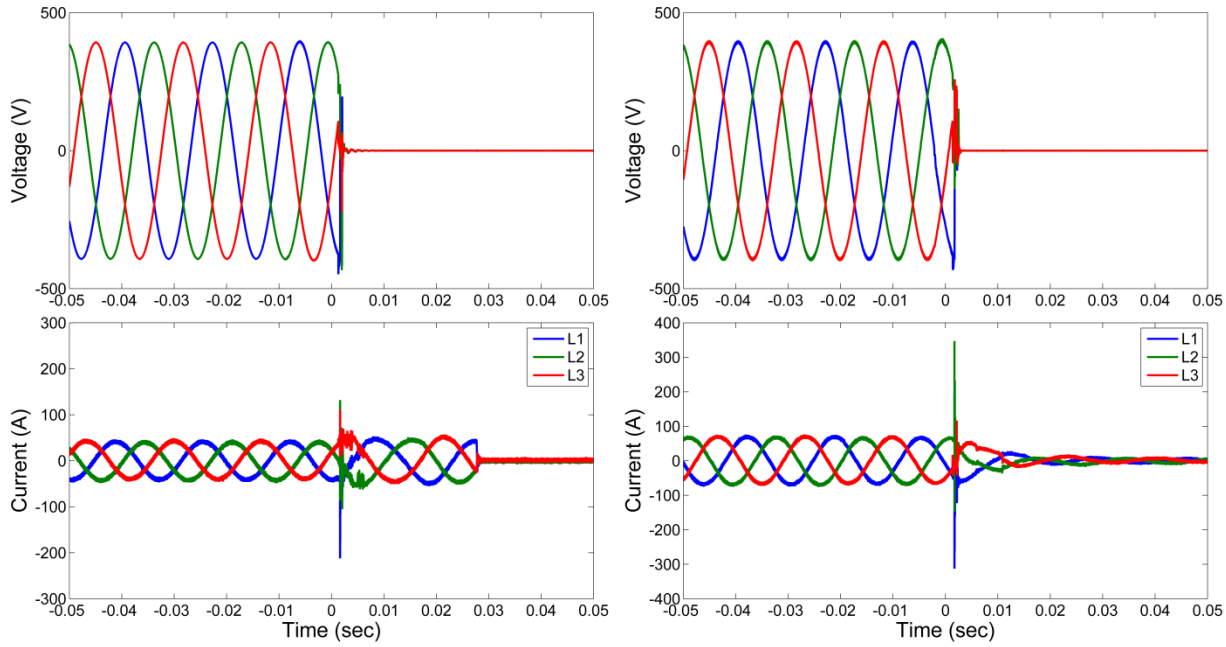

Figure 46. Largest peak three-phase fault currents for Inverter 1 (left) and Inverter 2 (right)

Figure 47 shows the maximum single-phase fault current of 130.7 A (2.13 p.u.) for Inverter 3 (left) and 112.7 A (2.01 p.u.) for Inverter 4 (right). Figure 48 shows the maximum three-phase fault current peaks of 683.3 A (11.16 p.u.) for Inverter 3 (left) and 528.0 A (9.41 p.u.) for Inverter 4 (right). The 683.3 A fault peak was the largest for all test cases but was very brief, with a duration of approximately 39 µs. In no test cases did the fault current cause the 60 A, Type J time delay fuses to open.

Several of the fault test waveforms show that the inverters were able to run on after the peak fault currents had occurred. In most tests, the inverters tripped immediately; in other tests, run-on times on the order of tens to hundreds of milliseconds occurred. Figure 49 shows two notable run-on cases. The left plot shows Inverter 4 running on for approximately 645 ms on a L2-G fault case (+0.80 power factor) before disconnecting, and the right plot shows Inverter 4 running on for approximately 1790 ms on a L1-G fault case (a power factor of 1.00) before disconnecting. This type of response was considered atypical, but it did occur on several test cases, and it never exceeded the 2-second anti-islanding trip time requirement.

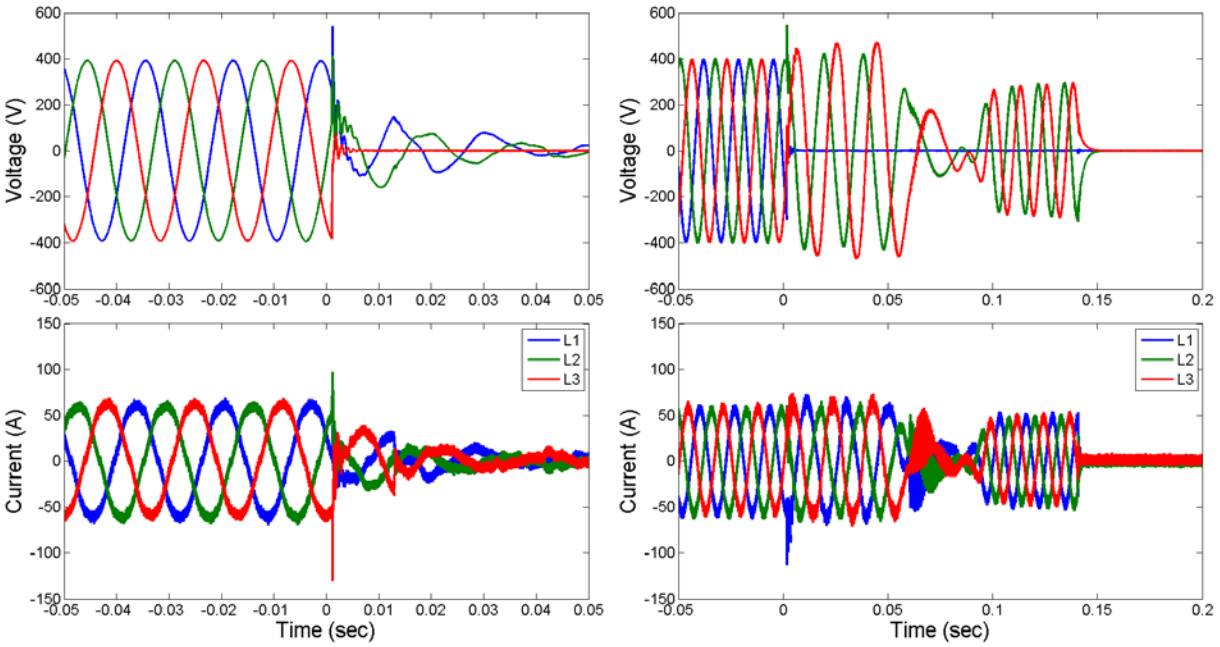

Figure 47. Largest peak single-phase fault currents for Inverter 3 (left) and Inverter 4 (right)

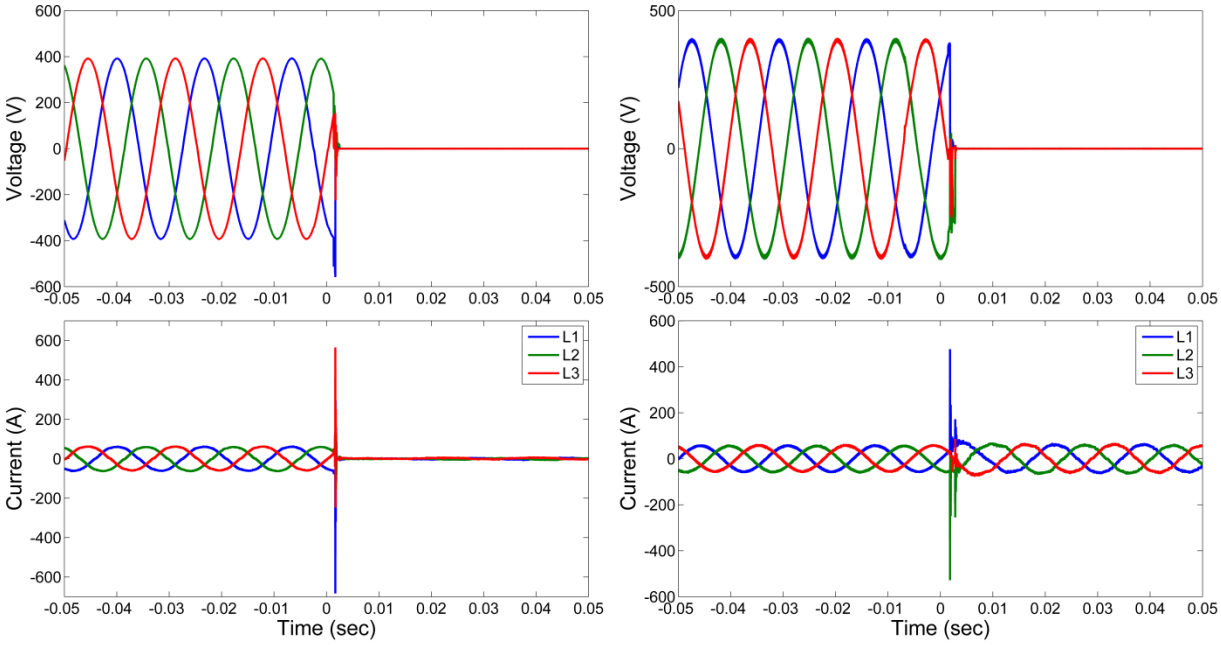

Figure 48. Largest peak three-phase fault currents for Inverter 3 (left) and Inverter 4 (right)

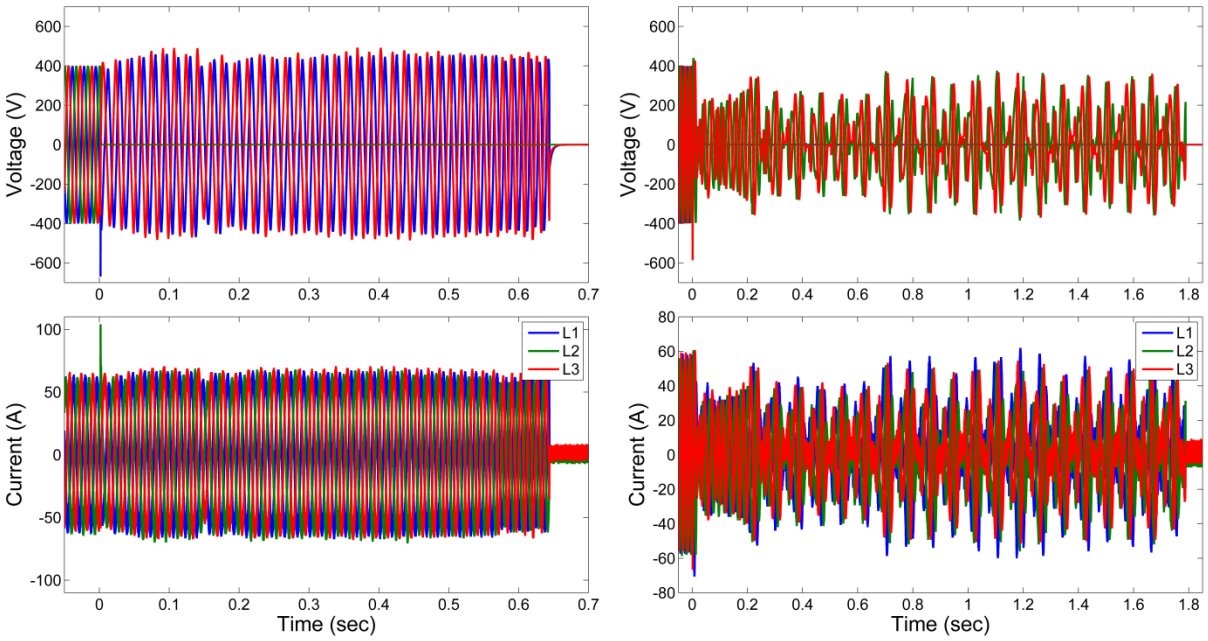

Figure 49. Example extended run-on times for Inverter 4

4 Conclusions

The tests described in this report examined the performance of various PV inverter-based grid support functions as well as their impacts on efficiency and their behavior during abnormal grid conditions. These tests were designed to be comparative in nature; they are not a substitute for full certification testing by a Nationally Recognized Testing Laboratory. At the time these tests were conducted, many of the grid support functions were not yet required by IEEE 1547, UL 1741, California Rule 21 or any other major standard in the United States, although they were expected to be required in California in the near future. The test inverters were not yet certified for many of the functions tested, so some tests results that were noncompliant to draft standards were expected.

All inverters were programmable for variable power factor, and they were able to run in steady state for both absorbing and producing modes down to a power factor of ±0.8 at different output power levels. The errors in target power factor were nearly negligible at unity power factor, but they tended to increase with decreasing power factor. Additionally, the errors in power factor tended to increase with decreasing output power, as the effects of line impedances and inverter controls became more pronounced. Maximum errors were on the order of several percentage points at the lowest output power levels and lowest power factor magnitudes.

Most inverters were found to be compliant with California Rule 21 guidelines for voltage and frequency ride-through requirements. Inverter 1 had some limitations on maximum ride-through times and the number of low voltage settings. Inverter 2 was not compliant with California Rule 21 for FRT and VRT, and a modified set of tests were run to exercise its ride-through settings. All inverters that were compliant with California Rule 21 settings were able to pass a series of ride-through, trip time, and steady-state tests as expected. The tests were derived from UL 1741 SA, which requires very rapid excursions in voltage and frequency magnitudes.

Inverters 1 and 3 were programmable for FWC, although some differences existed in how the function was implemented. Inverter 1 could be programmed for operation in both nameplate and snapshot mode, and hysteresis could be enabled or disabled. Inverter 3 always operated in snapshot mode, and it always required a hysteresis frequency set less than or equal to the start frequency. Both inverters were able to follow the three different FWC characteristic curves of interest at several power levels with relatively small errors in expected power output. Inverter 1 had relatively smaller errors in expected output power than Inverter 3, particularly on curves with higher slopes ramp rates.

Inverters 1, 3, and 4 were capable of VVC operation and implemented the function as expected. Inverter 1 was capable of outputting nameplate ratings in reactive power and thus demonstrated the widest range of reactive power capacity. Errors between expected and actual reactive power were low for this inverter, even for the most aggressive VVC characteristic curve. Inverter 3 had relatively small errors in many test cases, but it had some offsets between actual and expected reactive power, particularly for the most aggressive curve. The production and absorption offset functions test did not appear to behave as expected in the dead band for this inverter. Inverter 4 was able to meet the requirements for this mode in the flat regions of the VVC characteristics curves, but it consistently failed to settle into a consistent steady state reactive power operating point. It likewise had a noticeable offset for the aggressive curve, and there was frequently a 2–3 p.u. offset between the expected and actual reactive power output.

Several sources of error were present in these tests that made the aggressive VVC curve particularly challenging. The inverters were expected to change from zero to maximum reactive power for a 1% change in grid voltage, which was within the MSA of voltage measurement stated by the manufacturers. Additionally, there were voltage drops across the cables between the inverter terminals and instrumentation probe points, which further exacerbated differences between the expected values and actual inverter outputs.

Efficiency tests were run on each inverter for different combinations of output power, power factor, and DC input voltages. All inverters had the highest efficiencies for unity power factor, and they decreased for decreasing power factor magnitude. Absorbing power factor operation tended to have lower efficiency than producing power factor of the same magnitude. Maximum efficiencies occurred at 75% output power in most test cases, with slight reductions at full power output. Varying DC input voltage had mixed results for each inverter. Inverter 1 had the highest efficiencies among the majority of the test cases, and other inverters were mixed for the suite of test cases. All efficiency results in this report should be considered comparative in nature rather than absolute because several sources of the inaccuracies were inherent in the test setup.

Anti-islanding tests were run following the IEEE 1547 test standards, but with different combinations for FRT, VRT, VVC, and FWC grid support functions enabled. Two of the three inverters that were VVC-capable demonstrated lower mean and maximum ROTs with VVC enabled. Inverter 1 had shorter run-on times with FWC enabled, whereas Inverter 3 had longer run-on times with FWC enabled. Although Inverter 3 had ROTs that were more than 1.5 seconds with FWC enabled, it entered a low power output mode within several hundred milliseconds, suggesting that inverter controls detected the island condition much more quickly than the ROT data suggest. In summary, all inverters passed all anti-islanding tests with different GSF modes enabled.

Similarly, load rejection overvoltage tests were run on each inverter following a similar test plan used in previous NREL studies. Inverters were operated at different output power to resistive load power ratios, and the transient overvoltage peaks were measured after the grid was abruptly disconnected from the inverter and load. These tests were run with only FRT and VRT enabled, and also with these function and VVC enabled. There was no clear correlation between peak overvoltage magnitude and inverter-to-load ratio, nor was there a clear positive or negative impact to enabling VVC. The maximum overvoltage was 152% of nominal, and in most cases for inverters 1–3 the overvoltage peaks persisted for a very short period of time (microseconds). Inverter 4 did have several test cases with longer overvoltage durations, exceeding 130% and 140% of nominal for tens of milliseconds.

Single-phase-to-ground and three-phase-to-ground faults were executed on each inverter at different power factors to examine the effects of GSFs on peak fault current contribution. There was no clear correlation between the inverter output power factor and the peak current magnitude for any test inverter. Inverter 1 had the lowest peak fault current magnitudes and the most repeatable results, and results were mixed for the other test inverters. Fault current peaks were typically very short in duration—on the order of tens of microseconds. Some inverters were capable of continuing operation at near-nominal current for several hundred milliseconds after the peak current event occurred.

References

1. California Public Utilities Commission, "Cal. Pub. Util. Code, Rule 21 Generating Facility Interconnections," 2000.

2. UL, "UL 1741 Supplement SA: Grid Support Utility Interactive Inverters and Converters," 2016.

3. IEEE, "IEEE Standard 1547: Standard for Interconnecting Distributed Resources with Electric Power Systems," 2003.

4. IEEE, "IEEE Standard 1547a: Standard for Interconnecting Distributed Resources with Electric Power Systems—Amendment 1," 2014.

5. Nelson, A., A. Hoke, S. Chakraborty, J. Chebatah, T. Wang, and B. Zimmerly, *Inverter Load Rejection Over-Voltage Testing* (Technical Report NREL/TP-5D00-63510) (Golden, CO: National Renewable Energy Laboratory, 2015).

Appendix A: Frequency-Watt Test Data

Test case (column 2) can be cross-referenced with Table 10.

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
1	1	60.00	60.00	100.0	100.4	0.4
1	1	60.03	60.03	100.0	100.4	0.4
1	1	60.06	60.06	100.0	100.0	0.0
1	1	60.09	60.09	100.0	100.0	0.0
1	1	60.10	60.10	100.0	100.0	0.0
1	1	60.30	60.30	80.0	80.4	0.4
1	1	60.50	60.50	60.0	60.4	0.4
1	1	60.70	60.70	40.0	40.3	0.3
1	1	60.90	60.90	20.0	20.6	0.6
1	1	61.10	61.10	0.0	0.6	0.6
1	1	61.30	61.30	0.0	0.3	0.3
1	1	61.50	61.50	0.0	0.4	0.4
1	1	61.70	61.70	0.0	0.3	0.3
1	1	61.90	61.90	0.0	0.4	0.4
1	1	61.70	61.70	0.0	0.4	0.4
1	1	61.50	61.50	0.0	0.4	0.4
1	1	61.30	61.30	0.0	0.3	0.3
1	1	61.10	61.10	0.0	0.6	0.6
1	1	60.90	60.90	20.0	20.7	0.7
1	1	60.70	60.70	40.0	40.7	0.7
1	1	60.50	60.50	60.0	60.4	0.4
1	1	60.30	60.30	80.0	80.8	0.8
1	1	60.10	60.10	100.0	100.4	0.4
1	1	60.09	60.09	100.0	100.0	0.0
1	1	60.06	60.06	100.0	100.4	0.4
1	1	60.03	60.03	100.0	100.4	0.4
1	1	60.00	60.00	100.0	100.4	0.4
1	2	60.00	60.00	67.0	68.3	1.3
1	2	60.03	60.03	67.0	68.3	1.3
1	2	60.06	60.06	67.0	68.3	1.3
1	2	60.09	60.09	67.0	68.3	1.3
1	2	60.10	60.10	67.0	68.3	1.3
1	2	60.30	60.30	53.6	55.0	1.4
1	2	60.50	60.50	40.2	41.3	1.1
1	2	60.70	60.70	26.8	27.4	0.6
1	2	60.90	60.90	13.4	14.3	0.8
1	2	61.10	61.10	0.0	0.5	0.5
1	2	61.30	61.30	0.0	0.3	0.3

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
1	2	61.50	61.50	0.0	0.2	0.2
1	2	61.70	61.70	0.0	0.2	0.2
1	2	61.90	61.90	0.0	0.3	0.3
1	2	61.70	61.70	0.0	0.3	0.3
1	2	61.50	61.50	0.0	0.3	0.3
1	2	61.30	61.30	0.0	0.3	0.3
1	2	61.10	61.10	0.0	0.5	0.5
1	2	60.90	60.90	13.4	13.8	0.3
1	2	60.70	60.70	26.8	27.6	0.8
1	2	60.50	60.50	40.2	41.2	1.0
1	2	60.30	60.30	53.6	55.0	1.4
1	2	60.10	60.10	67.0	68.3	1.3
1	2	60.09	60.09	67.0	68.3	1.3
1	2	60.06	60.06	67.0	68.3	1.3
1	2	60.03	60.03	67.0	68.3	1.3
1	2	60.00	60.00	67.0	68.3	1.3
1	3	60.00	60.00	33.0	34.0	1.0
1	3	60.03	60.03	33.0	34.1	1.1
1	3	60.06	60.06	33.0	34.1	1.1
1	3	60.09	60.09	33.0	33.9	0.9
1	3	60.10	60.10	33.0	34.1	1.1
1	3	60.30	60.30	26.4	27.3	0.9
1	3	60.50	60.50	19.8	20.7	0.9
1	3	60.70	60.70	13.2	14.1	0.9
1	3	60.90	60.90	6.6	6.8	0.1
1	3	61.10	61.10	0.0	0.4	0.4
1	3	61.30	61.30	0.0	0.2	0.2
1	3	61.50	61.50	0.0	0.2	0.2
1	3	61.70	61.70	0.0	0.2	0.2
1	3	61.90	61.90	0.0	0.2	0.2
1	3	61.70	61.70	0.0	0.2	0.2
1	3	61.50	61.50	0.0	0.2	0.2
1	3	61.30	61.30	0.0	0.2	0.2
1	3	61.10	61.10	0.0	0.3	0.3
1	3	60.90	60.90	6.6	7.2	0.6
1	3	60.70	60.70	13.2	14.2	1.0
1	3	60.50	60.50	19.8	20.7	0.9
1	3	60.30	60.30	26.4	27.5	1.1
1	3	60.10	60.10	33.0	34.1	1.1
1	3	60.09	60.09	33.0	34.1	1.1
1	3	60.06	60.06	33.0	34.1	1.1

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
1	3	60.03	60.03	33.0	34.1	1.1
1	3	60.00	60.00	33.0	34.1	1.1
1	4	60.00	60.00	100.0	100.4	0.4
1	4	60.10	60.10	100.0	100.0	0.0
1	4	60.30	60.30	100.0	100.0	0.0
1	4	60.50	60.50	100.0	100.0	0.0
1	4	60.80	60.80	85.0	85.4	0.4
1	4	61.10	61.10	70.0	70.4	0.4
1	4	61.40	61.40	55.0	55.4	0.4
1	4	61.70	61.70	40.0	40.3	0.3
1	4	62.00	62.00	25.0	25.3	0.3
1	4	62.30	62.30	10.0	10.3	0.2
1	4	62.50	62.50	0.0	0.5	0.5
1	4	62.80	62.80	0.0	0.4	0.4
1	4	63.10	63.10	0.0	0.3	0.3
1	4	63.40	63.40	0.0	0.3	0.3
1	4	63.70	63.70	0.0	0.3	0.3
1	4	64.00	64.00	0.0	0.3	0.3
1	4	63.70	63.70	0.0	0.3	0.3
1	4	63.40	63.40	0.0	0.3	0.3
1	4	63.10	63.10	0.0	0.3	0.3
1	4	62.80	62.80	0.0	0.3	0.3
1	4	62.50	62.50	0.0	0.8	0.8
1	4	62.30	62.30	10.0	10.4	0.4
1	4	62.00	62.00	25.0	25.4	0.4
1	4	61.70	61.70	40.0	40.3	0.3
1	4	61.40	61.40	55.0	55.4	0.4
1	4	61.10	61.10	70.0	70.4	0.4
1	4	60.80	60.80	85.0	85.4	0.4
1	4	60.50	60.50	100.0	100.4	0.4
1	4	60.30	60.30	100.0	100.4	0.4
1	4	60.10	60.10	100.0	100.4	0.4
1	4	60.00	60.00	100.0	100.4	0.4
1	5	60.00	60.00	67.0	68.3	1.3
1	5	60.10	60.10	67.0	68.3	1.3
1	5	60.30	60.30	67.0	68.3	1.3
1	5	60.50	60.50	67.0	68.3	1.3
1	5	60.80	60.80	57.0	58.3	1.4
1	5	61.10	61.10	46.9	47.9	1.0
1	5	61.40	61.40	36.9	37.7	0.8
1	5	61.70	61.70	26.8	27.6	0.8

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
1	5	62.00	62.00	16.8	17.3	0.5
1	5	62.30	62.30	6.7	7.1	0.4
1	5	62.50	62.50	0.0	0.3	0.3
1	5	62.80	62.80	0.0	0.3	0.3
1	5	63.10	63.10	0.0	0.3	0.3
1	5	63.40	63.40	0.0	0.3	0.3
1	5	63.70	63.70	0.0	0.3	0.3
1	5	64.00	64.00	0.0	0.3	0.3
1	5	63.70	63.70	0.0	0.3	0.3
1	5	63.40	63.40	0.0	0.3	0.3
1	5	63.10	63.10	0.0	0.3	0.3
1	5	62.80	62.80	0.0	0.3	0.3
1	5	62.50	62.50	0.0	0.3	0.3
1	5	62.30	62.30	6.7	7.1	0.4
1	5	62.00	62.00	16.8	17.3	0.5
1	5	61.70	61.70	26.8	27.4	0.6
1	5	61.40	61.40	36.9	37.7	0.8
1	5	61.10	61.10	46.9	47.9	1.0
1	5	60.80	60.80	57.0	57.9	1.0
1	5	60.50	60.50	67.0	67.9	0.9
1	5	60.30	60.30	67.0	67.9	0.9
1	5	60.10	60.10	67.0	67.9	0.9
1	5	60.00	60.10	67.0	67.9	0.9
1	6	60.00	60.00	33.0	34.0	1.0
1	6	60.10	60.10	33.0	34.0	1.0
1	6	60.30	60.30	33.0	34.0	1.0
1	6	60.50	60.50	33.0	34.0	1.0
1	6	60.80	60.80	28.1	29.0	0.9
1	6	61.10	61.10	23.1	24.0	0.9
1	6	61.40	61.40	18.2	18.8	0.6
1	6	61.70	61.70	13.2	13.7	0.5
1	6	62.00	62.00	8.3	8.7	0.4
1	6	62.30	62.30	3.3	3.6	0.3
1	6	62.50	62.50	0.0	0.3	0.3
1	6	62.80	62.80	0.0	0.3	0.3
1	6	63.10	63.10	0.0	0.3	0.3
1	6	63.40	63.40	0.0	0.3	0.3
1	6	63.70	63.70	0.0	0.3	0.3
1	6	64.00	64.00	0.0	0.3	0.3
1	6	63.70	63.70	0.0	0.3	0.3
1	6	63.40	63.40	0.0	0.3	0.3

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
1	6	63.10	63.10	0.0	0.3	0.3
1	6	62.80	62.80	0.0	0.3	0.3
1	6	62.50	62.50	0.0	0.3	0.3
1	6	62.30	62.30	3.3	3.5	0.2
1	6	62.00	62.00	8.3	8.7	0.4
1	6	61.70	61.70	13.2	13.8	0.6
1	6	61.40	61.40	18.2	18.9	0.8
1	6	61.10	61.10	23.1	24.0	0.9
1	6	60.80	60.80	28.1	29.4	1.3
1	6	60.50	60.50	33.0	34.4	1.4
1	6	60.30	60.30	33.0	34.4	1.4
1	6	60.10	60.10	33.0	34.4	1.4
1	6	60.00	60.00	33.0	34.4	1.4
1	7	60.00	60.00	100.0	100.0	0.0
1	7	60.30	60.30	100.0	100.0	0.0
1	7	60.60	60.60	100.0	100.0	0.0
1	7	60.90	60.90	100.0	100.0	0.0
1	7	61.00	61.00	100.0	100.0	0.0
1	7	61.50	61.50	87.5	87.5	0.0
1	7	62.00	62.00	75.0	75.9	0.9
1	7	62.50	62.50	62.5	62.5	0.0
1	7	63.00	63.00	50.0	50.0	0.0
1	7	63.50	63.50	37.5	37.7	0.2
1	7	64.00	64.00	25.0	25.1	0.1
1	7	64.50	64.50	12.5	12.7	0.2
1	7	64.90	64.90	2.5	2.6	0.1
1	7	64.50	64.50	12.5	12.8	0.3
1	7	64.00	64.00	25.0	25.3	0.3
1	7	63.50	63.50	37.5	37.8	0.3
1	7	63.00	63.00	50.0	50.4	0.4
1	7	62.50	62.50	62.5	62.9	0.4
1	7	62.00	62.00	75.0	75.4	0.4
1	7	61.50	61.50	87.5	87.9	0.4
1	7	61.00	61.00	100.0	100.0	0.0
1	7	60.90	60.90	100.0	100.0	0.0
1	7	60.60	60.60	100.0	100.0	0.0
1	7	60.30	60.30	100.0	100.0	0.0
1	7	60.00	60.00	100.0	100.0	0.0
1	8	60.00	60.00	67.0	67.1	0.1
1	8	60.30	60.30	67.0	67.1	0.1
1	8	60.60	60.60	67.0	67.1	0.1

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
1	8	60.90	60.90	67.0	67.1	0.1
1	8	61.00	61.00	67.0	67.1	0.1
1	8	61.50	61.50	58.6	60.0	1.4
1	8	62.00	62.00	50.3	51.3	1.0
1	8	62.50	62.50	41.9	42.9	1.0
1	8	63.00	63.00	33.5	34.3	0.8
1	8	63.50	63.50	25.1	25.8	0.6
1	8	64.00	64.00	16.8	17.2	0.4
1	8	64.50	64.50	8.4	8.6	0.2
1	8	64.90	64.90	1.7	1.8	0.1
1	8	64.50	64.50	8.4	8.8	0.4
1	8	64.00	64.00	16.8	17.3	0.5
1	8	63.50	63.50	25.1	25.9	0.8
1	8	63.00	63.00	33.5	34.4	0.9
1	8	62.50	62.50	41.9	42.9	1.0
1	8	62.00	62.00	50.3	51.3	1.0
1	8	61.50	61.50	58.6	60.0	1.4
1	8	61.00	61.00	67.0	68.3	1.3
1	8	60.90	60.90	67.0	68.3	1.3
1	8	60.60	60.60	67.0	68.3	1.3
1	8	60.30	60.30	67.0	68.3	1.3
1	8	60.00	60.00	67.0	68.3	1.3
1	9	60.00	60.00	33.0	34.1	1.1
1	9	60.30	60.30	33.0	34.1	1.1
1	9	60.60	60.60	33.0	34.1	1.1
1	9	60.90	60.90	33.0	34.1	1.1
1	9	61.00	61.00	33.0	34.1	1.1
1	9	61.50	61.50	28.9	29.8	0.9
1	9	62.00	62.00	24.8	25.6	0.8
1	9	62.50	62.50	20.6	21.4	0.7
1	9	63.00	63.00	16.5	17.0	0.5
1	9	63.50	63.50	12.4	12.9	0.5
1	9	64.00	64.00	8.3	8.6	0.4
1	9	64.50	64.50	4.1	4.2	0.1
1	9	64.90	64.90	0.8	1.0	0.2
1	9	64.50	64.50	4.1	4.5	0.4
1	9	64.00	64.00	8.3	8.7	0.4
1	9	63.50	63.50	12.4	12.9	0.6
1	9	63.00	63.00	16.5	17.2	0.7
1	9	62.50	62.50	20.6	21.5	0.8
1	9	62.00	62.00	24.8	25.6	0.8

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
1	9	61.50	61.50	28.9	30.0	1.1
1	9	61.00	61.00	33.0	34.4	1.4
1	9	60.90	60.90	33.0	34.1	1.1
1	9	60.60	60.60	33.0	34.1	1.1
1	9	60.30	60.30	33.0	34.1	1.1
1	9	60.00	60.00	33.0	34.1	1.1
1	10	60.00	60.00	100.0	100.0	0.0
1	10	60.10	60.10	100.0	100.0	0.0
1	10	60.30	60.30	100.0	100.0	0.0
1	10	60.50	60.50	100.0	100.0	0.0
1	10	60.80	60.80	85.0	85.4	0.4
1	10	61.10	61.10	70.0	70.4	0.4
1	10	61.40	61.40	55.0	50.4	-4.6
1	10	61.70	61.70	40.0	40.1	0.1
1	10	62.00	62.00	25.0	25.2	0.2
1	10	62.30	62.30	10.0	10.2	0.2
1	10	62.50	62.50	0.0	0.4	0.4
1	10	62.80	62.80	0.0	0.4	0.4
1	10	63.10	63.10	0.0	0.4	0.4
1	10	63.40	63.40	0.0	0.4	0.4
1	10	63.70	63.70	0.0	0.4	0.4
1	10	64.00	64.00	0.0	0.4	0.4
1	10	63.70	63.70	0.0	0.4	0.4
1	10	63.40	63.40	0.0	0.4	0.4
1	10	63.10	63.10	0.0	0.4	0.4
1	10	62.80	62.80	0.0	0.4	0.4
1	10	62.50	62.50	0.0	0.4	0.4
1	10	62.30	62.30	0.0	0.4	0.4
1	10	62.00	62.00	0.0	0.4	0.4
1	10	61.70	61.70	0.0	0.4	0.4
1	10	61.40	61.40	0.0	0.4	0.4
1	10	61.10	61.10	0.0	0.4	0.4
1	10	60.80	60.80	0.0	0.4	0.4
1	10	60.50	60.50	0.0	0.4	0.4
1	10	60.30	60.30	0.0	0.4	0.4
1	10	60.10	60.10	100.0	100.0	0.0
1	10	60.00	60.00	100.0	100.0	0.0
1	11	60.00	60.00	67.0	68.3	1.3
1	11	60.10	60.10	67.0	68.3	1.3
1	11	60.30	60.30	67.0	68.3	1.3
1	11	60.50	60.50	67.0	68.3	1.3

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
1	11	60.80	60.80	67.0	68.3	1.3
1	11	61.10	61.10	67.0	68.3	1.3
1	11	61.40	61.40	55.0	53.3	-1.7
1	11	61.70	61.70	40.0	38.5	-1.5
1	11	62.00	62.00	25.0	23.5	-1.5
1	11	62.30	62.30	10.0	8.5	-1.5
1	11	62.50	62.50	0.0	0.3	0.3
1	11	62.80	62.80	0.0	0.3	0.3
1	11	63.10	63.10	0.0	0.3	0.3
1	11	63.40	63.40	0.0	0.3	0.3
1	11	63.70	63.70	0.0	0.3	0.3
1	11	64.00	64.00	0.0	0.3	0.3
1	11	63.70	63.70	0.0	0.3	0.3
1	11	63.40	63.40	0.0	0.3	0.3
1	11	63.10	63.10	0.0	0.3	0.3
1	11	62.80	62.80	0.0	0.3	0.3
1	11	62.50	62.50	0.0	0.3	0.3
1	11	62.30	62.30	10.0	8.7	-1.3
1	11	62.00	62.00	25.0	23.7	-1.3
1	11	61.70	61.70	40.0	38.5	-1.5
1	11	61.40	61.40	55.0	53.3	-1.7
1	11	61.10	61.10	67.0	68.3	1.3
1	11	60.80	60.80	67.0	68.3	1.3
1	11	60.50	60.50	67.0	68.3	1.3
1	11	60.30	60.30	67.0	68.3	1.3
1	11	60.10	60.10	67.0	68.3	1.3
1	11	60.00	60.00	67.0	68.3	1.3
3	1	60.00	60.00	100.0	100.0	0.0
3	1	60.03	60.03	100.0	100.0	0.0
3	1	60.06	60.06	100.0	100.0	0.0
3	1	60.09	60.09	100.0	100.0	0.0
3	1	60.10	60.10	100.0	94.9	-5.1
3	1	60.30	60.30	80.0	75.6	-4.4
3	1	60.50	60.50	60.0	56.7	-3.3
3	1	60.70	60.70	40.0	31.1	-8.9
3	1	60.90	60.90	20.0	18.9	-1.1
3	1	61.10	61.10	0.0	3.1	3.1
3	1	61.30	61.30	0.0	3.0	3.0
3	1	61.50	61.50	0.0	3.0	3.0
3	1	61.70	61.70	0.0	3.0	3.0
3	1	61.90	61.90	0.0	3.0	3.0

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
3	1	61.70	61.70	0.0	3.0	3.0
3	1	61.50	61.50	0.0	3.0	3.0
3	1	61.30	61.30	0.0	3.0	3.0
3	1	61.10	61.10	0.0	3.0	3.0
3	1	60.90	60.90	0.0	3.0	3.0
3	1	60.70	60.70	0.0	3.0	3.0
3	1	60.50	60.50	0.0	3.0	3.0
3	1	60.30	60.30	0.0	3.0	3.0
3	1	60.10	60.10	100.0	99.5	-0.5
3	1	60.09	60.09	100.0	99.5	-0.5
3	1	60.06	60.06	100.0	99.5	-0.5
3	1	60.03	60.03	100.0	99.5	-0.5
3	1	60.00	60.00	100.0	99.5	-0.5
3	2	60.00	60.00	67.0	68.0	1.0
3	2	60.03	60.03	67.0	68.0	1.0
3	2	60.06	60.06	67.0	68.0	1.0
3	2	60.09	60.09	67.0	68.0	1.0
3	2	60.10	60.10	67.0	66.2	-0.8
3	2	60.30	60.30	53.6	52.8	-0.8
3	2	60.50	60.50	40.2	39.3	-0.9
3	2	60.70	60.70	26.8	19.4	-7.4
3	2	60.90	60.90	13.4	13.0	-0.4
3	2	61.10	61.10	0.0	2.9	2.9
3	2	61.30	61.30	0.0	2.9	2.9
3	2	61.50	61.50	0.0	2.9	2.9
3	2	61.70	61.70	0.0	2.9	2.9
3	2	61.90	61.90	0.0	2.9	2.9
3	2	61.70	61.70	0.0	2.9	2.9
3	2	61.50	61.50	0.0	2.9	2.9
3	2	61.30	61.30	0.0	2.9	2.9
3	2	61.10	61.10	0.0	2.9	2.9
3	2	60.90	60.90	0.0	2.9	2.9
3	2	60.70	60.70	0.0	2.9	2.9
3	2	60.50	60.50	0.0	2.9	2.9
3	2	60.30	60.30	0.0	2.9	2.9
3	2	60.10	60.10	0.0	3.0	3.0
3	2	60.09	60.09	67.0	67.7	0.7
3	2	60.06	60.06	67.0	67.8	0.8
3	2	60.03	60.03	67.0	68.0	1.0
3	2	60.00	60.00	67.0	68.0	1.0
3	3	60.00	60.00	33.0	33.4	0.4

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
3	3	60.03	60.03	33.0	33.4	0.4
3	3	60.06	60.06	33.0	33.4	0.4
3	3	60.09	60.09	33.0	33.4	0.4
3	3	60.10	60.10	33.0	33.4	0.4
3	3	60.30	60.30	26.4	33.4	7.0
3	3	60.50	60.50	19.8	23.4	3.6
3	3	60.70	60.70	13.2	13.2	0.0
3	3	60.90	60.90	6.6	6.4	-0.2
3	3	61.10	61.10	0.0	2.9	2.9
3	3	61.30	61.30	0.0	2.9	2.9
3	3	61.50	61.50	0.0	2.9	2.9
3	3	61.70	61.70	0.0	2.9	2.9
3	3	61.90	61.90	0.0	2.9	2.9
3	3	61.70	61.70	0.0	2.9	2.9
3	3	61.50	61.50	0.0	2.9	2.9
3	3	61.30	61.30	0.0	2.9	2.9
3	3	61.10	61.10	0.0	2.9	2.9
3	3	60.90	60.90	0.0	2.9	2.9
3	3	60.70	60.70	0.0	2.9	2.9
3	3	60.50	60.50	0.0	2.9	2.9
3	3	60.30	60.30	0.0	2.9	2.9
3	3	60.10	60.10	0.0	2.9	2.9
3	3	60.09	60.09	33.0	33.1	0.1
3	3	60.06	60.06	33.0	33.1	0.1
3	3	60.03	60.03	33.0	33.1	0.1
3	3	60.00	60.00	33.0	33.1	0.1
3	4	60.00	60.00	100.0	99.5	-0.5
3	4	60.10	60.10	100.0	99.7	-0.3
3	4	60.30	60.30	100.0	99.5	-0.5
3	4	60.50	60.50	100.0	93.3	-6.7
3	4	60.80	60.80	85.0	79.5	-5.5
3	4	61.10	61.10	70.0	65.5	-4.5
3	4	61.40	61.40	55.0	51.2	-3.8
3	4	61.70	61.70	40.0	32.6	-7.4
3	4	62.00	62.00	25.0	23.4	-1.6
3	4	62.30	62.30	10.0	9.6	-0.4
3	4	62.50	62.50	0.0	3.0	3.0
3	4	62.80	62.80	0.0	3.0	3.0
3	4	63.10	63.10	0.0	3.0	3.0
3	4	63.40	63.40	0.0	3.0	3.0
3	4	63.70	63.70	0.0	3.0	3.0

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
3	4	64.00	64.00	0.0	3.0	3.0
3	4	63.70	63.70	0.0	3.0	3.0
3	4	63.40	63.40	0.0	3.0	3.0
3	4	63.10	63.10	0.0	3.0	3.0
3	4	62.80	62.80	0.0	3.0	3.0
3	4	62.50	62.50	0.0	3.0	3.0
3	4	62.30	62.30	0.0	3.0	3.0
3	4	62.00	62.00	0.0	3.0	3.0
3	4	61.70	61.70	0.0	3.0	3.0
3	4	61.40	61.40	0.0	3.0	3.0
3	4	61.10	61.10	0.0	3.0	3.0
3	4	60.80	60.80	0.0	3.0	3.0
3	4	60.50	60.50	0.0	3.0	3.0
3	4	60.30	60.30	100.0	99.5	-0.5
3	4	60.10	60.10	100.0	99.5	-0.5
3	4	60.00	60.00	100.0	99.5	-0.5
3	5	60.00	60.00	67.0	68.1	1.1
3	5	60.10	60.10	67.0	68.1	1.1
3	5	60.30	60.30	67.0	68.0	1.0
3	5	60.50	60.50	67.0	67.3	0.3
3	5	60.80	60.80	57.0	55.8	-1.1
3	5	61.10	61.10	46.9	46.0	-0.9
3	5	61.40	61.40	36.9	32.6	-4.2
3	5	61.70	61.70	26.8	26.4	-0.4
3	5	62.00	62.00	16.8	16.5	-0.3
3	5	62.30	62.30	6.7	6.7	0.0
3	5	62.50	62.50	0.0	2.8	2.8
3	5	62.80	62.80	0.0	2.8	2.8
3	5	63.10	63.10	0.0	2.8	2.8
3	5	63.40	63.40	0.0	2.8	2.8
3	5	63.70	63.70	0.0	2.8	2.8
3	5	64.00	64.00	0.0	2.8	2.8
3	5	63.70	63.70	0.0	2.8	2.8
3	5	63.40	63.40	0.0	2.8	2.8
3	5	63.10	63.10	0.0	2.8	2.8
3	5	62.80	62.80	0.0	2.8	2.8
3	5	62.50	62.50	0.0	2.8	2.8
3	5	62.30	62.30	0.0	2.8	2.8
3	5	62.00	62.00	0.0	2.8	2.8
3	5	61.70	61.70	0.0	2.8	2.8
3	5	61.40	61.40	0.0	2.8	2.8

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
3	5	61.10	61.10	0.0	2.8	2.8
3	5	60.80	60.80	0.0	2.8	2.8
3	5	60.50	60.50	0.0	2.8	2.8
3	5	60.30	60.30	67.0	67.5	0.5
3	5	60.10	60.10	67.0	68.0	1.0
3	5	60.00	60.00	67.0	68.0	1.0
3	6	60.00	60.00	33.0	33.5	0.5
3	6	60.10	60.10	33.0	33.5	0.5
3	6	60.30	60.30	33.0	33.5	0.5
3	6	60.50	60.50	33.0	33.5	0.5
3	6	60.80	60.80	28.1	28.5	0.4
3	6	61.10	61.10	23.1	23.3	0.2
3	6	61.40	61.40	18.2	18.4	0.2
3	6	61.70	61.70	13.2	13.2	0.0
3	6	62.00	62.00	8.3	8.1	-0.2
3	6	62.30	62.30	3.3	3.2	-0.1
3	6	62.50	62.50	0.0	2.8	2.8
3	6	62.80	62.80	0.0	2.8	2.8
3	6	63.10	63.10	0.0	2.8	2.8
3	6	63.40	63.40	0.0	2.8	2.8
3	6	63.70	63.70	0.0	2.8	2.8
3	6	64.00	64.00	0.0	2.8	2.8
3	6	63.70	63.70	0.0	2.8	2.8
3	6	63.40	63.40	0.0	2.8	2.8
3	6	63.10	63.10	0.0	2.8	2.8
3	6	62.80	62.80	0.0	2.8	2.8
3	6	62.50	62.50	0.0	2.8	2.8
3	6	62.30	62.30	0.0	2.8	2.8
3	6	62.00	62.00	0.0	2.8	2.8
3	6	61.70	61.70	0.0	2.8	2.8
3	6	61.40	61.40	0.0	2.8	2.8
3	6	61.10	61.10	0.0	2.8	2.8
3	6	60.80	60.80	0.0	2.8	2.8
3	6	60.50	60.50	0.0	2.8	2.8
3	6	60.30	60.30	33.0	33.4	0.4
3	6	60.10	60.10	33.0	33.4	0.4
3	6	60.00	60.00	33.0	33.4	0.4
3	7	60.00	60.00	100.0	99.9	-0.1
3	7	60.30	60.30	100.0	99.9	-0.1
3	7	60.60	60.60	100.0	99.9	-0.1
3	7	60.90	60.90	100.0	99.9	-0.1

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
3	7	61.00	61.00	100.0	99.9	-0.1
3	7	61.50	61.50	87.5	86.8	-0.7
3	7	62.00	62.00	75.0	74.6	-0.4
3	7	62.50	62.50	62.5	62.2	-0.3
3	7	63.00	63.00	50.0	49.7	-0.3
3	7	63.50	63.50	37.5	33.8	-3.7
3	7	64.00	64.00	25.0	21.5	-3.5
3	7	64.50	64.50	12.5	12.6	0.1
3	7	64.90	64.90	2.5	3.0	0.5
3	7	64.50	64.50	0.0	3.0	3.0
3	7	64.00	64.00	0.0	3.0	3.0
3	7	63.50	63.50	0.0	3.0	3.0
3	7	63.00	63.00	0.0	3.0	3.0
3	7	62.50	62.50	0.0	3.0	3.0
3	7	62.00	62.00	0.0	3.0	3.0
3	7	61.50	61.50	0.0	3.0	3.0
3	7	61.00	61.00	0.0	3.0	3.0
3	7	60.90	60.90	0.0	3.0	3.0
3	7	60.60	60.60	0.0	3.0	3.0
3	7	60.30	60.30	100.0	99.7	-0.3
3	7	60.00	60.00	100.0	99.7	-0.3
3	8	60.00	60.00	67.0	67.8	0.8
3	8	60.30	60.30	67.0	67.8	0.8
3	8	60.60	60.60	67.0	67.8	0.8
3	8	60.90	60.90	67.0	67.8	0.8
3	8	61.00	61.00	67.0	67.8	0.8
3	8	61.50	61.50	58.6	59.0	0.4
3	8	62.00	62.00	50.3	50.5	0.3
3	8	62.50	62.50	41.9	42.1	0.2
3	8	63.00	63.00	33.5	31.4	-2.1
3	8	63.50	63.50	25.1	25.2	0.1
3	8	64.00	64.00	16.8	17.0	0.3
3	8	64.50	64.50	8.4	8.4	0.0
3	8	64.90	64.90	1.7	3.1	1.4
3	8	64.50	64.50	0.0	3.1	3.1
3	8	64.00	64.00	0.0	3.1	3.1
3	8	63.50	63.50	0.0	3.1	3.1
3	8	63.00	63.00	0.0	3.1	3.1
3	8	62.50	62.50	0.0	3.1	3.1
3	8	62.00	62.00	0.0	3.1	3.1
3	8	61.50	61.50	0.0	3.1	3.1

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
3	8	61.00	61.00	0.0	3.1	3.1
3	8	60.90	60.90	0.0	3.1	3.1
3	8	60.60	60.60	0.0	3.1	3.1
3	8	60.30	60.30	67.0	68.1	1.1
3	8	60.00	60.00	67.0	68.1	1.1
3	9	60.00	60.00	33.0	33.5	0.5
3	9	60.30	60.30	33.0	33.5	0.5
3	9	60.60	60.60	33.0	33.5	0.5
3	9	60.90	60.90	33.0	33.5	0.5
3	9	61.00	61.00	33.0	33.5	0.5
3	9	61.50	61.50	28.9	29.7	0.8
3	9	62.00	62.00	24.8	24.9	0.2
3	9	62.50	62.50	20.6	20.8	0.2
3	9	63.00	63.00	16.5	16.6	0.1
3	9	63.50	63.50	12.4	12.5	0.1
3	9	64.00	64.00	8.3	8.2	-0.1
3	9	64.50	64.50	4.1	4.1	0.0
3	9	64.90	64.90	0.8	3.0	2.2
3	9	64.50	64.50	0.0	3.0	3.0
3	9	64.00	64.00	0.0	3.0	3.0
3	9	63.50	63.50	0.0	3.0	3.0
3	9	63.00	63.00	0.0	3.0	3.0
3	9	62.50	62.50	0.0	3.0	3.0
3	9	62.00	62.00	0.0	3.0	3.0
3	9	61.50	61.50	0.0	3.0	3.0
3	9	61.00	61.00	0.0	3.0	3.0
3	9	60.90	60.90	0.0	3.0	3.0
3	9	60.60	60.60	0.0	3.0	3.0
3	9	60.30	60.30	33.0	33.3	0.3
3	9	60.00	60.00	33.0	33.3	0.3
3	10	60.00	60.00	100.0	98.3	-1.7
3	10	60.10	60.10	100.0	98.3	-1.7
3	10	60.30	60.30	100.0	98.3	-1.7
3	10	60.50	60.50	100.0	98.3	-1.7
3	10	60.80	60.80	85.0	83.7	-1.3
3	10	61.10	61.10	70.0	68.9	-1.1
3	10	61.40	61.40	55.0	54.1	-0.9
3	10	61.70	61.70	40.0	39.1	-0.9
3	10	62.00	62.00	25.0	24.0	-1.0
3	10	62.30	62.30	10.0	9.7	-0.4
3	10	62.50	62.50	0.0	3.0	3.0

Test Inverter	Test Case	Commanded Frequency (Hz)	Measured Frequency (Hz)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
3	10	62.80	62.80	0.0	3.0	3.0
3	10	63.10	63.10	0.0	3.0	3.0
3	10	63.40	63.40	0.0	3.0	3.0
3	10	63.70	63.70	0.0	3.0	3.0
3	10	64.00	64.00	0.0	3.0	3.0
3	10	63.70	63.70	0.0	3.0	3.0
3	10	63.40	63.40	0.0	3.0	3.0
3	10	63.10	63.10	0.0	3.0	3.0
3	10	62.80	62.80	0.0	3.0	3.0
3	10	62.50	62.50	0.0	3.0	3.0
3	10	62.30	62.30	0.0	3.0	3.0
3	10	62.00	62.00	0.0	3.0	3.0
3	10	61.70	61.70	0.0	3.0	3.0
3	10	61.40	61.40	0.0	3.0	3.0
3	10	61.10	61.10	0.0	3.0	3.0
3	10	60.80	60.80	0.0	3.0	3.0
3	10	60.50	60.50	0.0	3.0	3.0
3	10	60.30	60.30	0.0	3.0	3.0
3	10	60.10	60.10	0.0	3.0	3.0
3	10	60.00	60.00	100.0	99.5	-0.5

Appendix B: Volt-VAR Test Data

Test case (column 2) can be cross-referenced with Table 11.

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
1	1	277.1	277.4	0.0	-20.7	-20.7
1	1	276.6	276.9	8.0	-7.1	-15.1
1	1	276.0	276.4	28.0	14.3	-13.7
1	1	275.5	275.9	46.0	32.3	-13.7
1	1	274.9	275.2	70.0	55.4	-14.6
1	1	274.4	274.6	90.0	75.8	-14.2
1	1	273.9	273.9	100.0	99.6	-0.4
1	1	273.3	273.3	100.0	99.6	-0.4
1	1	272.8	272.7	100.0	99.6	-0.4
1	1	272.2	272.2	100.0	99.6	-0.4
1	1	277.1	277.4	-10.0	-21.9	-11.9
1	1	277.6	278.0	-30.0	-41.1	-11.1
1	1	278.2	278.5	-50.0	-60.8	-10.8
1	1	278.7	278.8	-60.0	-75.8	-15.8
1	1	279.3	279.3	-80.0	-92.9	-12.9
1	1	279.9	279.6	-90.0	-99.2	-9.2
1	1	280.4	280.2	-100.0	-100.0	0.0
1	1	281.0	280.7	-100.0	-100.0	0.0
1	1	281.5	281.3	-100.0	-100.0	0.0
1	1	282.1	281.8	-100.0	-100.0	0.0
1	2	277.1	277.1	0.0	-16.0	-16.0
1	2	276.6	276.8	11.0	-2.2	-13.2
1	2	276.0	276.2	33.0	18.8	-14.2
1	2	275.5	275.7	51.0	36.8	-14.2
1	2	274.9	275.2	71.0	57.5	-13.5
1	2	274.4	274.6	90.0	75.8	-14.2
1	2	273.9	273.9	100.0	99.6	-0.4
1	2	273.3	273.3	100.0	99.6	-0.4
1	2	272.8	272.8	100.0	99.6	-0.4
1	2	272.2	272.2	100.0	99.6	-0.4
1	2	277.1	277.1	0.0	-18.5	-18.5
1	2	277.6	277.7	-20.0	-37.6	-17.6
1	2	278.2	278.2	-40.0	-57.9	-17.9
1	2	278.7	278.8	-60.0	-75.8	-15.8
1	2	279.3	279.3	-80.0	-92.9	-12.9
1	2	279.9	279.6	-90.0	-99.6	-9.6
1	2	280.4	280.2	-100.0	-100.0	0.0

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
1	2	281.0	280.7	-100.0	-100.0	0.0
1	2	281.5	281.3	-100.0	-100.0	0.0
1	2	282.1	281.8	-100.0	-100.0	0.0
1	3	277.1	277.0	5.0	-8.5	-13.5
1	3	276.6	276.6	19.0	5.0	-14.0
1	3	276.0	276.0	40.0	26.3	-13.8
1	3	275.5	275.5	60.0	47.9	-12.1
1	3	274.9	274.9	80.0	67.5	-12.5
1	3	274.4	274.5	96.0	84.6	-11.4
1	3	273.9	273.9	100.0	99.6	-0.4
1	3	273.3	273.3	100.0	99.6	-0.4
1	3	272.8	272.8	100.0	99.6	-0.4
1	3	272.2	272.2	100.0	99.6	-0.4
1	3	277.1	277.1	0.0	-11.6	-11.6
1	3	277.6	277.7	-20.0	-29.6	-9.6
1	3	278.2	278.2	-40.0	-49.6	-9.6
1	3	278.7	278.8	-60.0	-66.3	-6.3
1	3	279.3	279.3	-80.0	-87.9	-7.9
1	3	279.9	279.6	-90.0	-99.6	-9.6
1	3	280.4	280.2	-100.0	-100.0	0.0
1	3	281.0	280.7	-100.0	-100.0	0.0
1	3	281.5	281.3	-100.0	-100.0	0.0
1	3	282.1	281.8	-100.0	-100.0	0.0
1	4	277.1	277.4	0.0	1.3	1.3
1	4	275.0	275.3	0.0	1.3	1.3
1	4	272.9	273.2	0.0	1.3	1.3
1	4	270.8	271.1	0.0	1.3	1.3
1	4	268.8	269.1	0.0	1.4	1.4
1	4	266.7	267.0	10.7	9.4	-1.3
1	4	264.6	264.9	23.5	21.8	-1.7
1	4	262.5	262.8	36.0	34.5	-1.5
1	4	260.5	260.8	48.0	46.7	-1.3
1	4	258.4	258.7	50.0	51.3	1.3
1	4	256.3	256.6	50.0	51.3	1.3
1	4	254.2	254.5	50.0	51.3	1.3
1	4	277.1	277.4	0.0	1.3	1.3
1	4	279.2	279.6	0.0	1.4	1.4
1	4	281.3	281.6	0.0	1.2	1.2
1	4	283.4	283.8	0.0	1.3	1.3
1	4	285.4	285.7	-1.7	-2.7	-1.0
1	4	287.5	287.7	-13.3	-15.3	-1.9

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
1	4	289.5	289.9	-26.7	-27.4	-0.8
1	4	291.6	291.8	-38.3	-39.9	-1.6
1	4	293.8	294.0	-50.0	-48.8	1.3
1	4	295.9	296.0	-50.0	-48.8	1.3
1	4	298.0	298.2	-50.0	-48.8	1.3
1	4	300.1	300.4	-50.0	-48.8	1.3
1	5	277.1	277.4	0.0	0.9	0.9
1	5	275.0	275.2	0.0	0.9	0.9
1	5	272.9	273.1	0.0	0.9	0.9
1	5	270.8	271.0	0.0	0.9	0.9
1	5	268.8	269.0	0.0	0.9	0.9
1	5	266.7	266.9	11.5	10.0	-1.5
1	5	264.6	264.8	24.0	22.5	-1.5
1	5	262.5	262.7	36.5	35.1	-1.4
1	5	260.5	260.7	48.5	47.1	-1.4
1	5	258.4	258.6	50.0	50.8	0.8
1	5	256.3	256.5	50.0	50.8	0.8
1	5	254.2	254.5	50.0	50.8	0.8
1	5	277.1	277.4	0.0	0.9	0.9
1	5	279.2	279.3	0.0	0.9	0.9
1	5	281.3	281.6	0.0	0.9	0.9
1	5	283.4	283.5	0.0	0.9	0.9
1	5	285.4	285.4	0.0	-2.5	-2.5
1	5	287.5	287.7	-13.3	-15.0	-1.7
1	5	289.5	289.6	-25.0	-27.3	-2.3
1	5	291.6	291.8	-38.3	-39.8	-1.5
1	5	293.8	294.0	-50.0	-49.2	0.8
1	5	295.9	296.0	-50.0	-49.2	0.8
1	5	298.0	298.2	-50.0	-49.2	0.8
1	5	300.1	300.1	-50.0	-49.2	0.8
1	6	277.1	277.1	0.0	0.0	0.0
1	6	275.0	275.0	0.0	0.0	0.0
1	6	272.9	272.9	0.0	0.0	0.0
1	6	270.8	270.8	0.0	0.0	0.0
1	6	268.8	268.8	0.1	0.0	-0.1
1	6	266.7	266.7	12.7	10.5	-12.7
1	6	264.6	264.6	25.3	22.9	-25.3
1	6	262.5	262.6	38.0	35.3	-38.0
1	6	260.5	260.6	50.0	47.1	-50.0
1	6	258.4	258.4	50.0	50.0	-50.0
1	6	256.3	256.3	50.0	50.0	-50.0

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
1	6	254.2	254.2	50.0	50.0	-50.0
1	6	277.1	277.1	0.0	0.0	0.0
1	6	279.2	279.3	0.0	0.0	0.0
1	6	281.3	281.3	0.0	0.0	0.0
1	6	283.4	283.5	0.0	0.0	0.0
1	6	285.4	285.4	0.0	0.0	0.0
1	6	287.5	287.4	-12.4	-14.4	12.4
1	6	289.5	289.6	-24.4	-26.4	24.4
1	6	291.6	291.5	-37.0	-39.0	37.0
1	6	293.8	293.8	-50.0	-49.6	50.0
1	6	295.9	296.0	-50.0	-49.6	50.0
1	6	298.0	297.9	-50.0	-49.6	50.0
1	6	300.1	300.1	-50.0	-49.6	50.0
1	7	277.1	277.4	0.0	1.4	1.4
1	7	273.7	274.0	0.0	1.4	1.4
1	7	270.2	270.5	0.0	1.4	1.4
1	7	266.8	267.1	0.0	1.4	1.4
1	7	263.3	263.3	0.0	1.4	1.4
1	7	259.9	260.2	5.5	6.0	0.5
1	7	256.4	256.7	11.9	12.3	0.4
1	7	253.0	253.4	17.9	18.4	0.5
1	7	249.4	249.7	24.5	24.8	0.4
1	7	246.0	246.3	25.0	26.2	1.2
1	7	242.5	242.8	25.0	26.2	1.2
1	7	239.1	239.4	25.0	26.2	1.2
1	7	277.1	277.4	0.0	1.4	1.4
1	7	280.5	280.7	0.0	1.4	1.4
1	7	284.0	284.3	0.0	1.4	1.4
1	7	287.4	287.7	0.0	1.4	1.4
1	7	291.0	291.3	-0.5	0.0	0.5
1	7	294.4	294.6	-6.5	-5.9	0.6
1	7	297.9	298.2	-13.0	-12.5	0.5
1	7	301.3	301.5	-19.0	-18.6	0.4
1	7	304.8	305.1	-25.0	-23.6	1.4
1	7	308.2	308.4	-25.0	-23.6	1.4
1	7	311.7	312.0	-25.0	-23.6	1.4
1	7	314.2	314.5	-25.0	-23.6	1.4
1	8	277.1	277.1	0.0	0.0	0.0
1	8	273.7	273.9	0.0	0.0	0.0
1	8	270.2	270.4	0.0	0.0	0.0
1	8	266.8	267.0	0.0	0.0	0.0

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
1	8	263.3	263.5	0.0	0.0	0.0
1	8	259.9	260.2	5.6	5.9	0.3
1	8	256.4	256.6	12.0	12.2	0.1
1	8	253.0	253.2	18.1	18.3	0.2
1	8	249.4	249.6	24.6	24.8	0.2
1	8	246.0	246.2	25.0	25.9	0.9
1	8	242.5	242.8	25.0	25.9	0.9
1	8	239.1	239.4	25.0	25.9	0.9
1	8	277.1	277.4	0.0	0.0	0.0
1	8	280.5	280.7	0.0	0.0	0.0
1	8	284.0	284.1	0.0	0.0	0.0
1	8	287.4	287.7	0.0	0.0	0.0
1	8	291.0	291.3	-0.5	0.0	0.5
1	8	294.4	294.6	-6.5	-6.3	0.2
1	8	297.9	298.2	-13.0	-12.6	0.4
1	8	301.3	301.5	-19.0	-18.7	0.3
1	8	304.8	304.8	-25.0	-24.1	0.9
1	8	308.2	308.2	-25.0	-24.1	0.9
1	8	311.7	311.8	-25.0	-24.1	0.9
1	8	314.2	314.3	-25.0	-24.1	0.9
1	9	277.1	277.1	0.0	0.0	0.0
1	9	273.7	273.7	0.0	0.0	0.0
1	9	270.2	270.2	0.0	0.0	0.0
1	9	266.8	266.8	0.0	0.0	0.0
1	9	263.3	263.3	0.0	0.0	0.0
1	9	259.9	259.9	6.0	5.4	-0.6
1	9	256.4	256.4	12.4	11.8	-0.6
1	9	253.0	253.0	18.5	17.9	-0.6
1	9	249.4	249.4	25.0	24.3	-0.7
1	9	246.0	246.0	25.0	24.9	-0.1
1	9	242.5	242.5	25.0	24.9	-0.1
1	9	239.1	239.2	25.0	24.9	-0.1
1	9	277.1	277.1	0.0	0.0	0.0
1	9	280.5	280.5	0.0	0.0	0.0
1	9	284.0	284.1	0.0	0.0	0.0
1	9	287.4	287.4	0.0	0.0	0.0
1	9	291.0	291.0	0.0	0.0	0.0
1	9	294.4	294.3	-6.0	-6.6	-0.6
1	9	297.9	297.9	-12.5	-12.9	-0.4
1	9	301.3	301.2	-18.5	-19.0	-0.5
1	9	304.8	304.8	-25.0	-24.8	0.2

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
1	9	308.2	308.2	-25.0	-24.8	0.2
1	9	311.7	311.8	-25.0	-24.8	0.2
1	9	314.2	314.3	-25.0	-24.8	0.2
1	10	277.1	277.4	5.0	6.4	1.4
1	10	275.0	275.3	5.0	6.5	1.5
1	10	272.9	273.2	5.0	6.5	1.5
1	10	270.8	271.1	5.0	6.5	1.5
1	10	268.8	269.1	5.0	6.5	1.5
1	10	266.7	267.0	9.6	13.5	3.9
1	10	264.6	265.0	20.7	24.9	4.2
1	10	262.5	262.8	32.4	36.3	3.9
1	10	260.5	260.8	43.2	46.9	3.7
1	10	258.4	258.7	50.0	51.2	1.2
1	10	256.3	256.6	50.0	51.2	1.2
1	10	254.2	254.5	50.0	51.2	1.2
1	10	277.1	277.4	5.0	6.5	1.5
1	10	279.2	279.6	5.0	6.5	1.5
1	10	281.3	281.6	5.0	6.5	1.5
1	10	283.4	283.8	5.0	6.5	1.5
1	10	285.4	285.7	-1.5	1.8	3.3
1	10	287.5	287.7	-12.0	-12.1	-0.1
1	10	289.5	289.9	-24.0	-25.3	-1.3
1	10	291.6	291.8	-34.5	-39.2	-4.7
1	10	293.8	294.0	-46.5	-48.8	-2.3
1	10	295.9	296.0	-50.0	-48.8	1.2
1	10	298.0	298.2	-50.0	-48.8	1.2
1	10	300.1	300.4	-50.0	-48.8	1.2
1	11	277.1	277.1	5.0	6.0	1.0
1	11	275.0	275.2	5.0	6.0	1.0
1	11	272.9	273.1	5.0	6.0	1.0
1	11	270.8	271.0	5.0	6.0	1.0
1	11	268.8	269.0	5.0	6.0	1.0
1	11	266.7	266.9	10.2	14.0	3.8
1	11	264.6	264.8	21.6	25.4	3.8
1	11	262.5	262.7	32.8	36.5	3.7
1	11	260.5	260.7	43.8	47.3	3.5
1	11	258.4	258.6	50.0	50.9	0.9
1	11	256.3	256.5	50.0	50.9	0.9
1	11	254.2	254.5	50.0	50.9	0.9
1	11	277.1	277.4	5.0	6.0	1.0
1	11	279.2	279.3	5.0	6.0	1.0

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
1	11	281.3	281.6	5.0	6.0	1.0
1	11	283.4	283.5	5.0	6.0	1.0
1	11	285.4	285.4	0.0	2.2	2.2
1	11	287.5	287.7	-12.0	-11.7	0.3
1	11	289.5	289.6	-22.5	-24.8	-2.3
1	11	291.6	291.8	-34.5	-38.8	-4.3
1	11	293.8	294.0	-46.5	-48.9	-2.4
1	11	295.9	296.0	-50.0	-48.9	1.1
1	11	298.0	298.2	-50.0	-48.9	1.1
1	11	300.1	300.1	-50.0	-48.9	1.1
1	12	277.1	277.1	5.0	5.1	0.0
1	12	275.0	275.0	5.0	5.1	0.0
1	12	272.9	272.9	5.0	5.1	0.0
1	12	270.8	270.8	5.0	5.1	0.0
1	12	268.8	268.8	5.0	5.1	-0.1
1	12	266.7	266.7	11.2	14.3	-12.7
1	12	264.6	264.6	22.7	25.5	-25.3
1	12	262.5	262.6	33.9	36.8	-38.0
1	12	260.5	260.6	44.7	47.6	-50.0
1	12	258.4	258.4	50.0	50.0	-50.0
1	12	256.3	256.3	50.0	50.0	-50.0
1	12	254.2	254.3	50.0	50.0	-50.0
1	12	277.1	277.1	5.0	5.0	0.0
1	12	279.2	279.1	5.0	5.0	0.0
1	12	281.3	281.3	5.0	5.0	0.0
1	12	283.4	283.5	5.0	5.0	0.0
1	12	285.4	285.4	0.0	2.6	0.0
1	12	287.5	287.4	-10.5	-11.1	12.4
1	12	289.5	289.6	-22.5	-24.0	24.4
1	12	291.6	291.5	-33.0	-38.0	37.0
1	12	293.8	293.8	-45.0	-49.7	50.0
1	12	295.9	296.0	-50.0	-49.7	50.0
1	12	298.0	297.9	-50.0	-49.7	50.0
1	12	300.1	300.1	-50.0	-49.7	50.0
1	13	277.1	277.4	-5.0	-3.4	1.6
1	13	275.0	275.3	-5.0	-3.4	1.6
1	13	272.9	273.2	-5.0	-3.4	1.6
1	13	270.8	271.1	-5.0	-3.4	1.6
1	13	268.8	269.1	-2.0	-3.4	-1.4
1	13	266.7	267.0	11.7	5.3	-6.5
1	13	264.6	264.9	25.7	18.9	-6.8

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
1	13	262.5	262.8	39.6	32.8	-6.8
1	13	260.5	260.8	50.0	46.0	-4.0
1	13	258.4	258.7	50.0	51.3	1.3
1	13	256.3	256.6	50.0	51.2	1.2
1	13	254.2	254.5	50.0	51.2	1.2
1	13	277.1	277.4	-5.0	-3.3	1.7
1	13	279.2	279.3	-5.0	-3.3	1.7
1	13	281.3	281.6	-5.0	-3.3	1.7
1	13	283.4	283.8	-5.0	-3.3	1.7
1	13	285.4	285.7	-5.0	-7.5	-2.5
1	13	287.5	287.7	-14.7	-18.7	-4.0
1	13	289.5	289.9	-29.3	-29.6	-0.2
1	13	291.6	291.8	-42.2	-40.8	1.4
1	13	293.8	294.0	-50.0	-48.6	1.4
1	13	295.9	296.0	-50.0	-48.6	1.4
1	13	298.0	298.2	-50.0	-48.6	1.4
1	13	300.1	300.4	-50.0	-48.6	1.4
1	14	277.1	277.1	-5.0	-3.8	1.2
1	14	275.0	275.2	-5.0	-3.8	1.2
1	14	272.9	273.1	-5.0	-3.8	1.2
1	14	270.8	271.0	-5.0	-3.8	1.2
1	14	268.8	269.0	-1.1	-3.8	-2.7
1	14	266.7	266.9	12.6	5.6	-7.0
1	14	264.6	264.8	26.6	19.5	-7.1
1	14	262.5	262.7	40.3	33.5	-6.9
1	14	260.5	260.7	50.0	46.4	-3.7
1	14	258.4	258.5	50.0	50.9	0.9
1	14	256.3	256.6	50.0	50.9	0.9
1	14	254.2	254.4	50.0	50.9	0.9
1	14	277.1	277.1	-5.0	-3.8	1.2
1	14	279.2	279.3	-5.0	-3.8	1.2
1	14	281.3	281.6	-5.0	-3.8	1.2
1	14	283.4	283.5	-5.0	-3.8	1.2
1	14	285.4	285.4	-5.0	-7.0	-2.0
1	14	287.5	287.7	-14.7	-18.6	-3.9
1	14	289.5	289.6	-27.5	-29.3	-1.8
1	14	291.6	291.8	-42.2	-40.6	1.6
1	14	293.8	294.0	-50.0	-48.9	1.1
1	14	295.9	296.0	-50.0	-48.9	1.1
1	14	298.0	298.2	-50.0	-48.9	1.1
1	14	300.1	300.1	-50.0	-48.9	1.1

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
1	15	277.1	277.1	-5.0	-4.7	0.3
1	15	275.0	275.0	-5.0	-4.7	0.3
1	15	272.9	272.9	-5.0	-4.7	0.3
1	15	270.8	270.8	-5.0	-4.7	0.3
1	15	268.8	268.8	0.2	-4.7	-4.9
1	15	266.7	266.7	13.9	6.3	-7.6
1	15	264.6	264.6	27.7	20.1	-7.6
1	15	262.5	262.6	41.4	33.9	-7.5
1	15	260.5	260.6	50.0	47.0	-3.0
1	15	258.4	258.4	50.0	49.9	-0.1
1	15	256.3	256.5	50.0	49.9	-0.1
1	15	254.2	254.2	50.0	49.9	-0.1
1	15	277.1	277.1	-5.0	-4.7	0.3
1	15	279.2	279.1	-5.0	-4.7	0.3
1	15	281.3	281.3	-5.0	-4.7	0.3
1	15	283.4	283.5	-5.0	-4.7	0.3
1	15	285.4	285.4	-5.0	-6.7	-1.7
1	15	287.5	287.4	-12.8	-18.0	-5.2
1	15	289.5	289.6	-27.5	-28.7	-1.2
1	15	291.6	291.5	-40.3	-40.1	0.3
1	15	293.8	293.8	-50.0	-49.8	0.2
1	15	295.9	296.0	-50.0	-49.8	0.2
1	15	298.0	297.9	-50.0	-49.8	0.2
1	15	300.1	300.1	-50.0	-49.8	0.2
3	1	277.1	277.1	-12.0	-41.3	-29.3
3	1	276.6	276.6	-6.0	-31.1	-25.1
3	1	276.0	276.0	6.0	-17.7	-23.7
3	1	275.5	275.5	24.0	-10.0	-34.0
3	1	274.9	274.9	26.4	-2.0	-28.4
3	1	274.4	274.4	37.8	13.2	-24.6
3	1	273.9	273.9	48.0	24.8	-23.2
3	1	273.3	273.3	60.0	38.8	-21.2
3	1	272.8	272.8	60.0	51.4	-8.6
3	1	272.2	272.2	60.0	56.9	-3.1
3	1	277.1	277.1	-18.0	-42.0	-24.0
3	1	277.6	277.6	-30.0	-52.0	-22.0
3	1	278.2	278.2	-42.0	-59.8	-17.8
3	1	278.7	278.7	-54.0	-62.0	-8.0
3	1	279.3	279.3	-60.0	-62.0	-2.0
3	1	279.9	279.9	-60.0	-62.0	-2.0
3	1	280.4	280.4	-60.0	-62.0	-2.0

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
3	1	281.0	281.0	-60.0	-62.0	-2.0
3	1	281.5	281.5	-60.0	-62.0	-2.0
3	1	282.1	282.1	-60.0	-62.0	-2.0
3	2	277.1	277.1	-18.0	-34.4	-16.4
3	2	276.6	276.6	-6.0	-22.5	-16.5
3	2	276.0	276.0	6.0	-9.4	-15.4
3	2	275.5	275.5	18.0	-2.1	-20.1
3	2	274.9	274.9	31.2	12.4	-18.8
3	2	274.4	274.4	40.8	22.4	-18.4
3	2	273.9	273.9	52.8	32.4	-20.4
3	2	273.3	273.3	60.0	44.8	-15.2
3	2	272.8	272.8	60.0	55.6	-4.4
3	2	272.2	272.2	60.0	57.2	-2.8
3	2	277.1	277.1	-6.0	-34.3	-28.3
3	2	277.6	277.6	-24.0	-43.7	-19.7
3	2	278.2	278.2	-42.0	-54.5	-12.5
3	2	278.7	278.7	-48.0	-61.6	-13.6
3	2	279.3	279.3	-60.0	-61.6	-1.6
3	2	279.9	279.9	-60.0	-61.6	-1.6
3	2	280.4	280.4	-60.0	-61.6	-1.6
3	2	281.0	281.0	-60.0	-61.6	-1.6
3	2	281.5	281.5	-60.0	-61.6	-1.6
3	2	282.1	282.1	-60.0	-61.6	-1.6
3	3	277.1	277.1	-12.0	-17.4	-5.4
3	3	276.6	276.6	0.6	-7.3	-7.9
3	3	276.0	276.0	13.8	0.0	-13.8
3	3	275.5	275.5	23.4	14.9	-8.5
3	3	274.9	274.9	36.6	27.5	-9.1
3	3	274.4	274.4	49.2	42.6	-6.6
3	3	273.9	273.9	58.8	47.9	-10.9
3	3	273.3	273.3	60.0	58.3	-1.7
3	3	272.8	272.8	60.0	58.6	-1.4
3	3	272.2	272.2	60.0	58.6	-1.4
3	3	277.1	277.1	-12.0	-16.7	-4.7
3	3	277.6	277.6	-18.0	-27.7	-9.7
3	3	278.2	278.2	-30.0	-40.2	-10.2
3	3	278.7	278.7	-42.0	-50.3	-8.3
3	3	279.3	279.3	-60.0	-60.6	-0.6
3	3	279.9	279.9	-60.0	-60.6	-0.6
3	3	280.4	280.4	-60.0	-60.6	-0.6
3	3	281.0	281.0	-60.0	-60.6	-0.6

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
3	3	281.5	281.5	-60.0	-60.6	-0.6
3	3	282.1	282.1	-60.0	-60.6	-0.6
3	4	277.1	277.1	0.0	-3.2	-3.2
3	4	275.0	275.0	0.0	-3.2	-3.2
3	4	272.9	272.9	0.0	-3.2	-3.2
3	4	270.8	270.8	0.0	-3.2	-3.2
3	4	268.8	268.8	0.0	-3.2	-3.2
3	4	266.7	266.7	3.9	-3.2	-7.1
3	4	264.6	264.6	11.5	4.5	-7.0
3	4	262.5	262.5	19.0	12.0	-7.0
3	4	260.5	260.5	26.3	19.4	-6.9
3	4	258.4	258.4	30.0	26.6	-3.4
3	4	256.3	256.3	30.0	26.6	-3.4
3	4	254.2	254.2	30.0	26.6	-3.4
3	4	277.1	277.1	0.0	-3.2	-3.2
3	4	279.2	279.2	0.0	-3.2	-3.2
3	4	281.3	281.3	0.0	-3.2	-3.2
3	4	283.4	283.4	0.0	-3.2	-3.2
3	4	285.4	285.4	-4.0	-10.7	-6.7
3	4	287.5	287.5	-11.0	-17.9	-6.9
3	4	289.5	289.5	-18.0	-25.1	-7.1
3	4	291.6	291.6	-26.0	-32.6	-6.6
3	4	293.8	293.8	-30.0	-32.6	-2.6
3	4	295.9	295.9	-30.0	-32.6	-2.6
3	4	298.0	298.0	-30.0	-32.6	-2.6
3	4	300.1	300.1	-30.0	-32.6	-2.6
3	5	277.1	277.1	0.0	-2.3	-2.3
3	5	275.0	275.0	0.0	-2.3	-2.3
3	5	272.9	272.9	0.0	-2.3	-2.3
3	5	270.8	270.8	0.0	-2.3	-2.3
3	5	268.8	268.8	0.0	-2.3	-2.3
3	5	266.7	266.7	4.5	0.0	-4.5
3	5	264.6	264.6	12.0	6.7	-5.3
3	5	262.5	262.5	19.7	14.1	-5.6
3	5	260.5	260.5	26.8	21.3	-5.5
3	5	258.4	258.4	30.0	27.4	-2.6
3	5	256.3	256.3	30.0	27.6	-2.4
3	5	254.2	254.2	30.0	27.2	-2.8
3	5	277.1	277.1	0.0	-2.4	-2.4
3	5	279.2	279.2	0.0	-2.4	-2.4
3	5	281.3	281.3	0.0	-2.4	-2.4

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
3	5	283.4	283.4	0.0	-2.4	-2.4
3	5	285.4	285.4	-3.0	-8.2	-5.2
3	5	287.5	287.5	-10.0	-15.7	-5.7
3	5	289.5	289.5	-18.0	-22.6	-4.6
3	5	291.6	291.6	-25.0	-30.1	-5.1
3	5	293.8	293.8	-30.0	-32.2	-2.2
3	5	295.9	295.9	-30.0	-32.2	-2.2
3	5	298.0	298.0	-30.0	-32.2	-2.2
3	5	300.1	300.1	-30.0	-32.2	-2.2
3	6	277.1	277.1	0.0	-1.1	-1.1
3	6	275.0	275.0	0.0	-1.1	-1.1
3	6	272.9	272.9	0.0	-1.1	-1.1
3	6	270.8	270.8	0.0	-1.1	-1.1
3	6	268.8	268.8	0.0	-1.1	-1.1
3	6	266.7	266.7	5.7	3.1	-2.6
3	6	264.6	264.6	13.3	10.7	-2.6
3	6	262.5	262.5	20.8	18.1	-2.7
3	6	260.5	260.5	28.1	25.3	-2.8
3	6	258.4	258.4	30.0	27.5	-2.5
3	6	256.3	256.3	30.0	27.7	-2.3
3	6	254.2	254.2	30.0	28.6	-1.4
3	6	277.1	277.1	0.0	-1.0	-1.0
3	6	279.2	279.2	0.0	-1.0	-1.0
3	6	281.3	281.3	0.0	-1.0	-1.0
3	6	283.4	283.4	0.0	-1.0	-1.0
3	6	285.4	285.4	-2.0	-4.5	-2.5
3	6	287.5	287.5	-9.0	-11.8	-2.8
3	6	289.5	289.5	-17.0	-18.8	-1.8
3	6	291.6	291.6	-24.0	-26.5	-2.5
3	6	293.8	293.8	-30.0	-30.7	-0.7
3	6	295.9	295.9	-30.0	-30.7	-0.7
3	6	298.0	298.0	-30.0	-30.7	-0.7
3	6	300.1	300.1	-30.0	-30.7	-0.7
3	7	277.1	277.1	0.0	-2.2	-2.2
3	7	273.7	273.7	0.0	-2.2	-2.2
3	7	270.2	270.2	0.0	-2.2	-2.2
3	7	266.8	266.8	0.0	-2.2	-2.2
3	7	263.3	263.3	0.0	-2.2	-2.2
3	7	259.9	259.9	2.6	0.3	-2.3
3	7	256.4	256.4	6.4	4.2	-2.2
3	7	253.0	253.0	10.1	7.9	-2.2

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
3	7	249.4	249.4	14.0	11.8	-2.2
3	7	246.0	246.0	15.0	12.9	-2.1
3	7	242.5	242.5	15.0	12.9	-2.1
3	7	239.1	239.1	15.0	12.9	-2.1
3	7	277.1	277.1	0.0	-2.2	-2.2
3	7	280.5	280.5	0.0	-2.2	-2.2
3	7	284.0	284.0	0.0	-2.2	-2.2
3	7	287.4	287.4	0.0	-2.2	-2.2
3	7	291.0	291.0	-1.2	-3.8	-2.6
3	7	294.4	294.4	-4.8	-7.3	-2.5
3	7	297.9	297.9	-8.4	-11.1	-2.7
3	7	301.3	301.3	-11.7	-14.7	-3.0
3	7	304.8	304.8	-15.0	-17.5	-2.5
3	7	308.2	308.2	-15.0	-17.5	-2.5
3	7	311.7	311.7	-15.0	-17.5	-2.5
3	7	314.2	314.2	-15.0	-17.5	-2.5
3	8	277.1	277.1	0.0	-2.3	-2.3
3	8	273.7	273.7	0.0	-2.3	-2.3
3	8	270.2	270.2	0.0	-2.3	-2.3
3	8	266.8	266.8	0.0	-2.3	-2.3
3	8	263.3	263.3	0.0	-2.3	-2.3
3	8	259.9	259.9	3.2	0.0	-3.2
3	8	256.4	256.4	7.1	3.9	-3.2
3	8	253.0	253.0	10.7	7.5	-3.2
3	8	249.4	249.4	14.6	11.3	-3.3
3	8	246.0	246.0	15.0	12.5	-2.5
3	8	242.5	242.5	15.0	12.5	-2.5
3	8	239.1	239.1	15.0	12.5	-2.5
3	8	277.1	277.1	0.0	-2.3	-2.3
3	8	280.5	280.5	0.0	-2.3	-2.3
3	8	284.0	284.0	0.0	-2.3	-2.3
3	8	287.4	287.4	0.0	-2.3	-2.3
3	8	291.0	291.0	-0.3	-2.3	-2.0
3	8	294.4	294.4	-3.9	-3.5	0.4
3	8	297.9	297.9	-7.8	-7.2	0.6
3	8	301.3	301.3	-11.4	-10.9	0.5
3	8	304.8	304.8	-15.0	-14.7	0.3
3	8	308.2	308.2	-15.0	-17.4	-2.4
3	8	311.7	311.7	-15.0	-17.4	-2.4
3	8	314.2	314.2	-15.0	-17.4	-2.4
3	9	277.1	277.1	0.0	-1.1	-1.1

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
3	9	273.7	273.7	0.0	-1.1	-1.1
3	9	270.2	270.2	0.0	-1.1	-1.1
3	9	266.8	266.8	0.0	-1.1	-1.1
3	9	263.3	263.3	0.0	-1.1	-1.1
3	9	259.9	259.9	3.6	2.1	-1.5
3	9	256.4	256.4	7.4	5.9	-1.5
3	9	253.0	253.0	11.0	9.3	-1.7
3	9	249.4	249.4	14.9	13.3	-1.6
3	9	246.0	246.0	15.0	13.7	-1.3
3	9	242.5	242.5	15.0	13.7	-1.3
3	9	239.1	239.1	15.0	13.7	-1.3
3	9	277.1	277.1	0.0	-1.1	-1.1
3	9	280.5	280.5	0.0	-1.1	-1.1
3	9	284.0	284.0	0.0	-1.1	-1.1
3	9	287.4	287.4	0.0	-1.1	-1.1
3	9	291.0	291.0	0.0	-1.7	-1.7
3	9	294.4	294.4	-3.6	-5.2	-1.6
3	9	297.9	297.9	-7.5	-8.9	-1.4
3	9	301.3	301.3	-11.1	-12.8	-1.7
3	9	304.8	304.8	-15.0	-15.9	-0.9
3	9	308.2	308.2	-15.0	-15.9	-0.9
3	9	311.7	311.7	-15.0	-15.9	-0.9
3	9	314.2	314.2	-15.0	-15.9	-0.9
3	10	277.1	277.1	5.0	-3.2	-8.2
3	10	275.0	275.0	5.0	-3.2	-8.2
3	10	272.9	272.9	5.0	-3.2	-8.2
3	10	270.8	270.8	5.0	-3.2	-8.2
3	10	268.8	268.8	5.0	-3.2	-8.2
3	10	266.7	266.7	5.0	0.0	-5.0
3	10	264.6	264.6	9.6	7.0	-2.6
3	10	262.5	262.5	16.0	13.9	-2.1
3	10	260.5	260.5	22.0	20.4	-1.6
3	10	258.4	258.4	28.3	26.8	-1.5
3	10	256.3	256.3	30.0	26.8	-3.2
3	10	254.2	254.2	30.0	26.8	-3.2
3	10	277.1	277.1	5.0	-3.1	-8.1
3	10	279.2	279.2	5.0	-3.1	-8.1
3	10	281.3	281.3	5.0	-3.1	-8.1
3	10	283.4	283.4	3.3	-3.1	-6.4
3	10	285.4	285.4	-3.3	-3.1	0.2
3	10	287.5	287.5	-6.2	-8.1	-1.9

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
3	10	289.5	289.5	-9.2	-16.1	-7.0
3	10	291.6	291.6	-15.0	-24.0	-9.0
3	10	293.8	293.8	-21.7	-32.0	-10.3
3	10	295.9	295.9	-30.0	-32.0	-2.0
3	10	298.0	298.0	-30.0	-32.0	-2.0
3	10	300.1	300.1	-30.0	-32.0	-2.0
3	11	277.1	277.1	5.0	-2.4	-7.4
3	11	275.0	275.0	5.0	-2.4	-7.4
3	11	272.9	272.9	5.0	-2.4	-7.4
3	11	270.8	270.8	5.0	-2.4	-7.4
3	11	268.8	268.8	5.0	-2.4	-7.4
3	11	266.7	266.7	5.0	2.3	-2.7
3	11	264.6	264.6	10.2	8.8	-1.4
3	11	262.5	262.5	16.4	15.6	-0.8
3	11	260.5	260.5	22.4	22.0	-0.4
3	11	258.4	258.4	28.8	27.3	-1.5
3	11	256.3	256.3	30.0	27.3	-2.7
3	11	254.2	254.2	30.0	27.3	-2.7
3	11	277.1	277.1	5.0	-2.4	-7.4
3	11	279.2	279.2	5.0	-2.4	-7.4
3	11	281.3	281.3	5.0	-2.4	-7.4
3	11	283.4	283.4	3.3	-2.4	-5.7
3	11	285.4	285.4	-2.5	-5.6	-3.1
3	11	287.5	287.5	-8.3	-13.7	-5.4
3	11	289.5	289.5	-15.0	-21.8	-6.8
3	11	291.6	291.6	-20.8	-29.9	-9.1
3	11	293.8	293.8	-27.5	-32.1	-4.6
3	11	295.9	295.9	-30.0	-32.1	-2.1
3	11	298.0	298.0	-30.0	-32.1	-2.1
3	11	300.1	300.1	-30.0	-32.1	-2.1
3	12	277.1	277.1	5.0	-1.1	0.0
3	12	275.0	275.0	5.0	-1.1	0.0
3	12	272.9	272.9	5.0	-1.1	0.0
3	12	270.8	270.8	5.0	-1.1	0.0
3	12	268.8	268.8	5.0	-1.1	-0.1
3	12	266.7	266.7	5.0	5.6	-12.7
3	12	264.6	264.6	11.1	12.5	-25.3
3	12	262.5	262.5	17.3	19.2	-38.0
3	12	260.5	260.5	23.3	25.7	-50.0
3	12	258.4	258.4	30.0	28.3	-50.0
3	12	256.3	256.3	30.0	28.7	-50.0

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
3	12	254.2	254.2	30.0	28.5	-50.0
3	12	277.1	277.1	5.0	-1.0	0.0
3	12	279.2	279.2	5.0	-1.0	0.0
3	12	281.3	281.3	5.0	-1.0	0.0
3	12	283.4	283.4	4.2	-1.0	0.0
3	12	285.4	285.4	-1.7	-1.0	0.0
3	12	287.5	287.5	-7.5	-9.9	12.4
3	12	289.5	289.5	-14.2	-17.7	24.4
3	12	291.6	291.6	-20.0	-26.0	37.0
3	12	293.8	293.8	-26.7	-30.7	50.0
3	12	295.9	295.9	-30.0	-30.7	50.0
3	12	298.0	298.0	-30.0	-30.7	50.0
3	12	300.1	300.1	-30.0	-30.7	50.0
3	13	277.1	277.1	-5.0	-3.2	1.8
3	13	275.0	275.0	-5.0	-3.2	1.8
3	13	272.9	272.9	-5.0	-3.2	1.8
3	13	270.8	270.8	-5.0	-3.2	1.8
3	13	268.8	268.8	-4.2	-3.2	1.0
3	13	266.7	266.7	4.7	-5.5	-10.2
3	13	264.6	264.6	13.5	2.6	-10.9
3	13	262.5	262.5	22.3	11.1	-11.2
3	13	260.5	260.5	30.0	19.0	-11.0
3	13	258.4	258.4	30.0	26.6	-3.4
3	13	256.3	256.3	30.0	26.6	-3.4
3	13	254.2	254.2	30.0	26.6	-3.4
3	13	277.1	277.1	-5.0	-3.2	1.8
3	13	279.2	279.2	-5.0	-3.2	1.8
3	13	281.3	281.3	-5.0	-3.2	1.8
3	13	283.4	283.4	-5.0	-3.2	1.8
3	13	285.4	285.4	-5.0	-12.6	-7.6
3	13	287.5	287.5	-12.8	-19.3	-6.4
3	13	289.5	289.5	-21.0	-25.4	-4.4
3	13	291.6	291.6	-30.0	-32.2	-2.2
3	13	293.8	293.8	-30.0	-32.8	-2.8
3	13	295.9	295.9	-30.0	-32.8	-2.8
3	13	298.0	298.0	-30.0	-32.8	-2.8
3	13	300.1	300.1	-30.0	-32.8	-2.8
3	14	277.1	277.1	-5.0	-2.4	2.6
3	14	275.0	275.0	-5.0	-2.4	2.6
3	14	272.9	272.9	-5.0	-2.4	2.6
3	14	270.8	270.8	-5.0	-2.4	2.6

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
3	14	268.8	268.8	-3.4	-2.4	1.0
3	14	266.7	266.7	5.4	-2.4	-7.8
3	14	264.6	264.6	14.2	4.7	-9.5
3	14	262.5	262.5	23.1	13.1	-10.0
3	14	260.5	260.5	30.0	20.9	-9.1
3	14	258.4	258.4	30.0	27.2	-2.8
3	14	256.3	256.3	30.0	27.2	-2.8
3	14	254.2	254.2	30.0	27.2	-2.8
3	14	277.1	277.1	-5.0	-2.4	2.6
3	14	279.2	279.2	-5.0	-2.4	2.6
3	14	281.3	281.3	-5.0	-2.4	2.6
3	14	283.4	283.4	-5.0	-2.4	2.6
3	14	285.4	285.4	-5.0	-10.3	-5.3
3	14	287.5	287.5	-11.7	-17.2	-5.6
3	14	289.5	289.5	-21.0	-23.6	-2.6
3	14	291.6	291.6	-29.2	-30.2	-1.1
3	14	293.8	293.8	-30.0	-32.2	-2.2
3	14	295.9	295.9	-30.0	-32.2	-2.2
3	14	298.0	298.0	-30.0	-32.2	-2.2
3	14	300.1	300.1	-30.0	-32.2	-2.2
3	15	277.1	277.1	-5.0	-1.1	0.0
3	15	275.0	275.0	-5.0	-1.1	0.0
3	15	272.9	272.9	-5.0	-1.1	0.0
3	15	270.8	270.8	-5.0	-1.1	0.0
3	15	268.8	268.8	-2.2	-1.1	-0.1
3	15	266.7	266.7	6.5	0.0	-12.7
3	15	264.6	264.6	15.4	8.9	-25.3
3	15	262.5	262.5	24.3	17.1	-38.0
3	15	260.5	260.5	30.0	25.2	-50.0
3	15	258.4	258.4	30.0	27.6	-50.0
3	15	256.3	256.3	30.0	27.5	-50.0
3	15	254.2	254.2	30.0	28.6	-50.0
3	15	277.1	277.1	-5.0	-1.1	0.0
3	15	279.2	279.2	-5.0	-1.1	0.0
3	15	281.3	281.3	-5.0	-1.1	0.0
3	15	283.4	283.4	-5.0	-1.1	0.0
3	15	285.4	285.4	-5.0	-6.9	0.0
3	15	287.5	287.5	-10.5	-13.7	12.4
3	15	289.5	289.5	-19.8	-20.0	24.4
3	15	291.6	291.6	-28.0	-26.9	37.0
3	15	293.8	293.8	-30.0	-30.9	50.0

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
3	15	295.9	295.9	-30.0	-30.9	50.0
3	15	298.0	298.0	-30.0	-30.9	50.0
3	15	300.1	300.1	-30.0	-30.9	50.0
4	1	277.1	277.9	-15.0	-40.2	-25.2
4	1	276.6	277.4	-5.0	-29.5	-24.5
4	1	276.0	276.8	5.0	-19.4	-24.4
4	1	275.5	276.3	15.0	-12.3	-27.3
4	1	274.9	275.7	25.0	-0.9	-25.9
4	1	274.4	275.2	35.0	8.7	-26.3
4	1	273.9	274.6	45.0	18.3	-26.7
4	1	273.3	274.1	50.0	27.4	-22.6
4	1	272.8	273.5	50.0	38.0	-12.0
4	1	272.2	272.9	50.0	43.0	-7.0
4	1	277.1	277.9	-15.0	-37.5	-22.5
4	1	277.6	278.5	-25.0	-47.0	-22.0
4	1	278.2	279.0	-35.0	-48.9	-13.9
4	1	278.7	279.6	-45.0	-52.3	-7.3
4	1	279.3	280.1	-50.0	-54.0	-4.0
4	1	279.9	280.7	-50.0	-53.6	-3.6
4	1	280.4	281.3	-50.0	-53.9	-3.9
4	1	281.0	281.8	-50.0	-53.8	-3.8
4	1	281.5	282.4	-50.0	-53.7	-3.7
4	1	282.1	282.9	-50.0	-53.7	-3.7
4	2	277.1	277.7	-10.0	-32.7	-22.7
4	2	276.6	277.4	-5.0	-23.6	-18.6
4	2	276.0	276.8	5.0	-13.6	-18.6
4	2	275.5	276.3	15.0	-4.9	-19.9
4	2	274.9	275.7	25.0	5.6	-19.4
4	2	274.4	275.2	35.0	15.4	-19.6
4	2	273.9	274.6	45.0	24.3	-20.7
4	2	273.3	274.1	50.0	33.0	-17.0
4	2	272.8	273.5	50.0	43.1	-6.9
4	2	272.2	272.9	50.0	47.9	-2.1
4	2	277.1	277.7	-10.0	-33.5	-23.5
4	2	277.6	278.2	-20.0	-43.2	-23.2
4	2	278.2	278.8	-30.0	-49.3	-19.3
4	2	278.7	279.3	-40.0	-53.0	-13.0
4	2	279.3	279.9	-50.0	-52.9	-2.9
4	2	279.9	280.4	-50.0	-52.9	-2.9
4	2	280.4	281.0	-50.0	-52.9	-2.9
4	2	281.0	281.5	-50.0	-52.9	-2.9

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
4	2	281.5	282.1	-50.0	-52.9	-2.9
4	2	282.1	282.6	-50.0	-52.9	-2.9
4	3	277.1	277.4	-5.0	-22.2	-17.2
4	3	276.6	276.8	5.0	-14.1	-19.1
4	3	276.0	276.3	15.0	-3.8	-18.8
4	3	275.5	275.7	25.0	4.9	-20.1
4	3	274.9	275.2	35.0	16.7	-18.3
4	3	274.4	274.6	45.0	25.2	-19.8
4	3	273.9	274.1	50.0	33.5	-16.5
4	3	273.3	273.5	50.0	44.8	-5.2
4	3	272.8	272.9	50.0	50.4	0.4
4	3	272.2	272.4	50.0	49.8	-0.2
4	3	277.1	277.4	-5.0	-29.0	-24.0
4	3	277.6	277.9	-15.0	-36.6	-21.6
4	3	278.2	278.5	-25.0	-46.7	-21.7
4	3	278.7	279.0	-35.0	-51.4	-16.4
4	3	279.3	279.6	-45.0	-53.7	-8.7
4	3	279.9	280.1	-50.0	-51.3	-1.3
4	3	280.4	280.7	-50.0	-51.3	-1.3
4	3	281.0	281.3	-50.0	-51.3	-1.3
4	3	281.5	281.8	-50.0	-51.3	-1.3
4	3	282.1	282.4	-50.0	-51.3	-1.3
4	4	277.1	277.9	0.0	-3.3	-3.3
4	4	275.0	275.7	0.0	-3.3	-3.3
4	4	272.9	274.1	0.0	-3.3	-3.3
4	4	270.8	271.6	0.0	-3.3	-3.3
4	4	268.8	269.6	0.0	-3.3	-3.3
4	4	266.7	267.4	4.2	-2.6	-6.8
4	4	264.6	265.5	10.0	3.5	-6.5
4	4	262.5	263.5	15.8	9.6	-6.2
4	4	260.5	261.3	22.5	15.8	-6.7
4	4	258.4	259.1	25.0	21.8	-3.2
4	4	256.3	257.1	25.0	22.0	-3.0
4	4	254.2	255.2	25.0	22.0	-3.0
4	4	277.1	277.9	0.0	-3.3	-3.3
4	4	279.2	280.1	0.0	-3.3	-3.3
4	4	281.3	282.1	0.0	-3.3	-3.3
4	4	283.4	284.3	0.0	-3.0	-3.0
4	4	285.4	286.2	-2.5	-8.5	-6.0
4	4	287.5	288.5	-9.2	-16.2	-7.0
4	4	289.5	290.4	-15.0	-21.7	-6.7

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
4	4	291.6	292.6	-21.7	-28.7	-7.0
4	4	293.8	294.6	-25.0	-28.7	-3.7
4	4	295.9	296.8	-25.0	-28.7	-3.7
4	4	298.0	298.7	-25.0	-28.7	-3.7
4	4	300.1	300.9	-25.0	-28.7	-3.7
4	5	277.1	277.7	0.0	-2.2	-2.2
4	5	275.0	275.7	0.0	-2.2	-2.2
4	5	272.9	273.5	0.0	-2.2	-2.2
4	5	270.8	271.6	0.0	-2.2	-2.2
4	5	268.8	269.3	0.0	-2.2	-2.2
4	5	266.7	267.4	4.2	-2.0	-6.2
4	5	264.6	265.2	10.8	5.0	-5.8
4	5	262.5	263.0	17.5	11.4	-6.1
4	5	260.5	261.0	23.3	18.4	-4.9
4	5	258.4	259.1	25.0	23.2	-1.8
4	5	256.3	256.9	25.0	23.2	-1.8
4	5	254.2	254.9	25.0	23.1	-1.9
4	5	277.1	277.7	0.0	-2.2	-2.2
4	5	279.2	279.9	0.0	-2.2	-2.2
4	5	281.3	282.1	0.0	-2.2	-2.2
4	5	283.4	284.0	0.0	-2.0	-2.0
4	5	285.4	286.0	-1.7	-7.8	-6.1
4	5	287.5	288.2	-8.3	-14.4	-6.1
4	5	289.5	290.1	-14.2	-18.8	-4.6
4	5	291.6	292.3	-20.8	-27.0	-6.2
4	5	293.8	294.6	-25.0	-27.4	-2.4
4	5	295.9	296.5	-25.0	-27.4	-2.4
4	5	298.0	298.7	-25.0	-27.4	-2.4
4	5	300.1	300.7	-25.0	-27.4	-2.4
4	6	277.1	277.7	0.0	-0.9	-0.9
4	6	275.0	275.4	0.0	-0.9	-0.9
4	6	272.9	273.2	0.0	-0.9	-0.9
4	6	270.8	271.3	0.0	-0.9	-0.9
4	6	268.8	269.3	0.0	-0.9	-0.9
4	6	266.7	267.1	5.0	1.7	-3.3
4	6	264.6	264.9	11.7	8.1	-3.6
4	6	262.5	263.0	17.5	14.4	-3.1
4	6	260.5	261.0	23.3	20.5	-2.8
4	6	258.4	258.8	25.0	24.4	-0.6
4	6	256.3	256.6	25.0	24.4	-0.6
4	6	254.2	254.7	25.0	24.4	-0.6

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
4	6	277.1	277.7	0.0	-0.9	-0.9
4	6	279.2	279.6	0.0	-0.9	-0.9
4	6	281.3	281.8	0.0	-0.9	-0.9
4	6	283.4	283.8	0.0	-0.9	-0.9
4	6	285.4	286.0	-1.7	-4.3	-2.6
4	6	287.5	287.9	-7.5	-11.4	-3.9
4	6	289.5	289.8	-13.3	-17.1	-3.8
4	6	291.6	292.1	-20.0	-22.6	-2.6
4	6	293.8	294.3	-25.0	-26.1	-1.1
4	6	295.9	296.2	-25.0	-26.1	-1.1
4	6	298.0	298.4	-25.0	-26.1	-1.1
4	6	300.1	300.4	-25.0	-26.1	-1.1
4	7	277.1	277.1	0.0	-3.4	-3.4
4	7	273.7	273.8	0.0	-3.4	-3.4
4	7	270.2	270.4	0.0	-3.4	-3.4
4	7	266.8	266.8	0.0	-3.4	-3.4
4	7	263.3	263.5	0.0	-3.4	-3.4
4	7	259.9	259.9	3.0	-1.6	-4.6
4	7	256.4	256.3	6.2	1.8	-4.4
4	7	253.0	253.3	9.0	5.0	-4.0
4	7	249.4	249.4	12.5	8.5	-4.0
4	7	246.0	246.3	12.5	9.3	-3.2
4	7	242.5	242.7	12.5	9.3	-3.2
4	7	239.1	239.4	12.5	9.3	-3.2
4	7	277.1	277.1	0.0	-3.1	-3.1
4	7	280.5	280.7	0.0	-3.1	-3.1
4	7	284.0	284.0	0.0	-3.1	-3.1
4	7	287.4	287.4	0.0	-3.1	-3.1
4	7	291.0	291.0	0.0	-4.5	-4.5
4	7	294.4	294.6	-3.2	-7.4	-4.2
4	7	297.9	297.9	-6.2	-10.7	-4.5
4	7	301.3	301.2	-9.2	-12.9	-3.7
4	7	304.8	304.8	-12.5	-15.9	-3.4
4	7	308.2	308.1	-12.5	-15.9	-3.4
4	7	311.7	311.7	-12.5	-15.9	-3.4
4	7	314.2	314.2	-12.5	-15.9	-3.4
4	8	277.1	277.1	0.0	-2.3	-2.3
4	8	273.7	273.8	0.0	-2.3	-2.3
4	8	270.2	270.4	0.0	-2.3	-2.3
4	8	266.8	267.1	0.0	-2.3	-2.3
4	8	263.3	263.5	0.0	-2.3	-2.3

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
4	8	259.9	259.9	3.0	-0.4	-3.4
4	8	256.4	256.6	6.0	3.2	-2.8
4	8	253.0	253.3	9.0	6.1	-2.9
4	8	249.4	249.7	12.3	9.4	-2.9
4	8	246.0	246.3	12.5	10.4	-2.1
4	8	242.5	242.7	12.5	10.4	-2.1
4	8	239.1	239.4	12.5	10.4	-2.1
4	8	277.1	277.4	0.0	-2.3	-2.3
4	8	280.5	280.7	0.0	-2.3	-2.3
4	8	284.0	284.3	0.0	-2.3	-2.3
4	8	287.4	287.6	0.0	-2.3	-2.3
4	8	291.0	291.2	-0.2	-3.5	-3.3
4	8	294.4	294.6	-3.2	-6.2	-3.0
4	8	297.9	298.2	-6.5	-9.4	-2.9
4	8	301.3	301.5	-9.5	-12.5	-3.0
4	8	304.8	304.8	-12.5	-15.0	-2.5
4	8	308.2	308.4	-12.5	-15.0	-2.5
4	8	311.7	311.7	-12.5	-15.0	-2.5
4	8	314.2	314.2	-12.5	-15.0	-2.5
4	9	277.1	277.1	0.0	-0.9	-0.9
4	9	273.7	273.5	0.0	-0.9	-0.9
4	9	270.2	270.2	0.0	-0.9	-0.9
4	9	266.8	266.8	0.0	-0.9	-0.9
4	9	263.3	263.2	0.0	-0.9	-0.9
4	9	259.9	259.9	3.0	1.5	-1.5
4	9	256.4	256.3	6.2	4.8	-1.4
4	9	253.0	253.0	9.3	7.9	-1.4
4	9	249.4	249.4	12.5	11.2	-1.3
4	9	246.0	246.1	12.5	11.8	-0.7
4	9	242.5	242.5	12.5	11.8	-0.7
4	9	239.1	239.1	12.5	11.8	-0.7
4	9	277.1	277.1	0.0	-0.7	-0.7
4	9	280.5	280.4	0.0	-0.7	-0.7
4	9	284.0	284.0	0.0	-0.7	-0.7
4	9	287.4	287.4	0.0	-0.7	-0.7
4	9	291.0	291.0	0.0	-1.6	-1.6
4	9	294.4	294.3	-3.0	-4.5	-1.5
4	9	297.9	297.9	-6.2	-7.7	-1.5
4	9	301.3	301.2	-9.2	-10.6	-1.4
4	9	304.8	304.8	-12.5	-13.5	-1.0
4	9	308.2	308.1	-12.5	-13.5	-1.0

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
4	9	311.7	311.5	-12.5	-13.5	-1.0
4	9	314.2	314.2	-12.5	-13.5	-1.0
4	10	277.1	277.9	5.0	1.8	-3.2
4	10	275.0	276.0	5.0	1.8	-3.2
4	10	272.9	274.1	5.0	1.8	-3.2
4	10	270.8	271.6	5.0	1.8	-3.2
4	10	268.8	269.6	5.0	1.8	-3.2
4	10	266.7	267.7	5.0	2.0	-3.0
4	10	264.6	265.7	7.3	7.2	-0.1
4	10	262.5	263.2	13.3	12.0	-1.3
4	10	260.5	261.3	18.0	16.5	-1.5
4	10	258.4	259.1	23.3	22.0	-1.3
4	10	256.3	257.1	25.0	22.0	-3.0
4	10	254.2	255.2	25.0	22.1	-2.9
4	10	277.1	277.9	5.0	1.8	-3.2
4	10	279.2	280.1	5.0	1.8	-3.2
4	10	281.3	282.1	5.0	1.8	-3.2
4	10	283.4	284.3	2.7	1.8	-0.9
4	10	285.4	286.2	-2.0	-5.3	-3.3
4	10	287.5	288.5	-7.3	-13.7	-6.4
4	10	289.5	290.4	-12.0	-20.1	-8.1
4	10	291.6	292.6	-17.3	-29.3	-12.0
4	10	293.8	294.6	-22.0	-28.6	-6.6
4	10	295.9	296.8	-25.0	-28.6	-3.6
4	10	298.0	298.7	-25.0	-28.6	-3.6
4	10	300.1	300.9	-25.0	-28.6	-3.6
4	11	277.1	277.7	5.0	2.9	-2.1
4	11	275.0	275.7	5.0	2.9	-2.1
4	11	272.9	273.5	5.0	2.9	-2.1
4	11	270.8	271.6	5.0	2.9	-2.1
4	11	268.8	269.3	5.0	2.9	-2.1
4	11	266.7	267.4	5.0	3.5	-1.5
4	11	264.6	265.2	8.7	8.3	-0.4
4	11	262.5	263.2	13.3	14.1	0.8
4	11	260.5	261.3	18.0	18.7	0.7
4	11	258.4	259.1	23.3	22.8	-0.5
4	11	256.3	256.9	25.0	23.1	-1.9
4	11	254.2	254.9	25.0	23.2	-1.8
4	11	277.1	277.7	5.0	2.9	-2.1
4	11	279.2	279.9	5.0	2.9	-2.1
4	11	281.3	282.1	5.0	2.9	-2.1

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
4	11	283.4	284.0	3.3	3.4	0.1
4	11	285.4	286.0	-1.3	-3.8	-2.5
4	11	287.5	288.2	-6.7	-11.7	-5.0
4	11	289.5	290.1	-11.3	-18.0	-6.7
4	11	291.6	292.3	-16.7	-25.6	-8.9
4	11	293.8	294.6	-22.0	-27.3	-5.3
4	11	295.9	296.5	-25.0	-27.3	-2.3
4	11	298.0	298.7	-25.0	-27.3	-2.3
4	11	300.1	300.7	-25.0	-27.3	-2.3
4	12	277.1	277.7	5.0	4.1	-0.9
4	12	275.0	275.4	5.0	4.1	-0.9
4	12	272.9	273.2	5.0	4.1	-0.9
4	12	270.8	271.3	5.0	4.1	-0.9
4	12	268.8	269.3	5.0	4.1	-0.9
4	12	266.7	267.1	5.0	6.1	1.1
4	12	264.6	265.2	8.7	11.3	2.6
4	12	262.5	263.0	14.0	16.6	2.6
4	12	260.5	261.0	18.7	21.1	2.4
4	12	258.4	258.8	24.0	24.5	0.5
4	12	256.3	256.9	25.0	24.5	-0.5
4	12	254.2	254.7	25.0	24.5	-0.5
4	12	277.1	277.7	5.0	4.1	-0.9
4	12	279.2	279.6	5.0	4.1	-0.9
4	12	281.3	281.8	5.0	4.1	-0.9
4	12	283.4	283.8	4.0	4.1	0.1
4	12	285.4	286.0	-1.3	-1.3	0.0
4	12	287.5	287.9	-6.0	-8.5	-2.5
4	12	289.5	289.8	-10.7	-15.0	-4.3
4	12	291.6	292.1	-16.0	-22.6	-6.6
4	12	293.8	294.3	-21.3	-26.2	-4.9
4	12	295.9	296.2	-25.0	-26.2	-1.2
4	12	298.0	298.4	-25.0	-26.2	-1.2
4	12	300.1	300.4	-25.0	-26.2	-1.2
4	13	277.1	277.7	-5.0	-8.4	-3.4
4	13	275.0	275.7	-5.0	-8.4	-3.4
4	13	272.9	273.8	-5.0	-8.4	-3.4
4	13	270.8	271.6	-5.0	-8.4	-3.4
4	13	268.8	269.6	-3.0	-8.4	-5.4
4	13	266.7	267.4	5.0	-8.4	-13.4
4	13	264.6	265.2	13.0	-0.5	-13.5
4	13	262.5	263.2	20.0	7.0	-13.0

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
4	13	260.5	261.3	25.0	14.3	-10.7
4	13	258.4	259.4	25.0	22.3	-2.7
4	13	256.3	257.1	25.0	22.1	-2.9
4	13	254.2	255.2	25.0	22.1	-2.9
4	13	277.1	277.9	-5.0	-8.4	-3.4
4	13	279.2	279.9	-5.0	-8.4	-3.4
4	13	281.3	282.1	-5.0	-8.4	-3.4
4	13	283.4	284.3	-5.0	-8.2	-3.2
4	13	285.4	286.2	-5.0	-13.0	-8.0
4	13	287.5	288.2	-10.0	-19.1	-9.1
4	13	289.5	290.4	-18.0	-23.7	-5.7
4	13	291.6	292.3	-25.0	-28.6	-3.6
4	13	293.8	294.6	-25.0	-28.5	-3.5
4	13	295.9	296.8	-25.0	-28.5	-3.5
4	13	298.0	298.7	-25.0	-28.5	-3.5
4	13	300.1	300.7	-25.0	-28.5	-3.5
4	14	277.1	277.7	-5.0	-7.3	-2.3
4	14	275.0	275.7	-5.0	-7.3	-2.3
4	14	272.9	273.5	-5.0	-7.3	-2.3
4	14	270.8	271.6	-5.0	-7.3	-2.3
4	14	268.8	269.3	-2.0	-7.3	-5.3
4	14	266.7	267.4	5.0	-6.2	-11.2
4	14	264.6	265.5	12.0	2.1	-9.9
4	14	262.5	263.2	20.0	9.5	-10.5
4	14	260.5	261.3	25.0	16.7	-8.3
4	14	258.4	259.1	25.0	23.1	-1.9
4	14	256.3	256.9	25.0	23.1	-1.9
4	14	254.2	254.9	25.0	23.1	-1.9
4	14	277.1	277.7	-5.0	-7.3	-2.3
4	14	279.2	279.9	-5.0	-7.3	-2.3
4	14	281.3	281.8	-5.0	-7.3	-2.3
4	14	283.4	284.0	-5.0	-7.6	-2.6
4	14	285.4	286.0	-5.0	-11.4	-6.4
4	14	287.5	288.2	-10.0	-16.8	-6.8
4	14	289.5	290.1	-17.0	-21.2	-4.2
4	14	291.6	292.3	-25.0	-26.6	-1.6
4	14	293.8	294.6	-25.0	-27.4	-2.4
4	14	295.9	296.5	-25.0	-27.4	-2.4
4	14	298.0	298.7	-25.0	-27.4	-2.4
4	14	300.1	300.7	-25.0	-27.4	-2.4
4	15	277.1	277.4	-5.0	-5.9	-0.9

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
4	15	275.0	275.4	-5.0	-5.9	-0.9
4	15	272.9	273.2	-5.0	-5.9	-0.9
4	15	270.8	271.3	-5.0	-5.9	-0.9
4	15	268.8	269.3	-2.0	-5.9	-3.9
4	15	266.7	267.1	6.0	-2.5	-8.5
4	15	264.6	265.2	13.0	5.0	-8.0
4	15	262.5	263.0	21.0	12.7	-8.3
4	15	260.5	261.0	25.0	19.4	-5.6
4	15	258.4	258.8	25.0	24.4	-0.6
4	15	256.3	256.9	25.0	24.4	-0.6
4	15	254.2	254.7	25.0	24.4	-0.6
4	15	277.1	277.4	-5.0	-5.8	-0.8
4	15	279.2	279.6	-5.0	-5.8	-0.8
4	15	281.3	281.8	-5.0	-5.8	-0.8
4	15	283.4	283.8	-5.0	-5.8	-0.8
4	15	285.4	286.0	-5.0	-8.8	-3.8
4	15	287.5	287.9	-9.0	-14.0	-5.0
4	15	289.5	289.8	-16.0	-18.7	-2.7
4	15	291.6	292.1	-24.0	-24.3	-0.3
4	15	293.8	294.3	-25.0	-25.9	-0.9
4	15	295.9	296.2	-25.0	-25.9	-0.9
4	15	298.0	298.4	-25.0	-26.0	-1.0
4	15	300.1	300.4	-25.0	-26.0	-1.0