Power Hardware-in-the-Loop Evaluation of PV Inverter Grid Support on Hawaiian Electric Feeders

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Austin Nelson, Kumaraguru Prabakar, Adarsh Nagarajan, Shaili Nepal, and Anderson Hoke
National Renewable Energy Laboratory

Marc Asano, Reid Ueda, and Earle Ifuku
Hawaiian Electric Company

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Abstract—As more grid-connected photovoltaic (PV) inverters become compliant with evolving interconnections requirements, there is increased interest from utilities in understanding how to best deploy advanced grid-support functions (GSF) in the field. One efficient and cost-effective method to examine such deployment options is to leverage power hardware-in-the-loop (PHIL) testing methods. This paper describes a study wherein two Hawaiian Electric feeder models were converted to real-time models using an OPAL-RT real-time digital testing platform, and integrated with models of GSF capable PV inverters that were modeled from characterization test data. The integrated model was subsequently used in PHIL testing to evaluate the effects of different fixed power factor and volt-watt control settings on voltage regulation of the selected feeders. The results of this study were provided as inputs for field deployment and technical interconnection requirements for grid-connected PV inverters on the Hawaiian Islands.

Index Terms—advanced PV inverter, grid–support functions, power hardware-in-the-loop, real-time simulator, volt-watt control

I. INTRODUCTION

This paper describes a collaboration between the National Renewable Energy Laboratory (NREL) and the Hawaiian Electric Companies to understand the effects of deploying advanced grid-support functions (GSF) on select Hawaiian electrical distribution feeders. This topic has become increasingly important with the large amount of distributed photovoltaic (PV) on the islands, as well as new requirements for GSFs on distributed PV inverters introduced by revised interconnection standards such as UL1741 SA and IEEE1547, as well as utility-specific requirements such as Hawaiian Electric's Rule 14H [1-3]. This paper focuses on implementation of volt-watt control (VWC) and fixed power factor (FPF) operation, which are of interest for regulating over-voltage scenarios on feeders with large amounts of distributed rooftop PV.

Two distribution feeders were selected by Hawaiian Electric for this study, and were subsequently transformed into reduced-order, real-time models on the OPAL-RT real-time digital simulation platform using techniques described in [4]. A series of baseline, hardware only certification-style tests were run on four different commercially-available advanced PV inverters that are commonly used on the Hawaiian Islands to evaluate their steady state and dynamic responses to grid events with different GSFs enabled. This data was subsequently used to integrate PV inverter models with the feeder models, with the total power ratings modeled after those found on the feeders in several current and future PV growth scenarios. The real-time model was subsequently used to evaluate the

effect of different FPF and VWC settings on over-voltage conditions using power hardware-in-the-loop (PHIL) testing techniques. The testing results were subsequently provided to Hawaiian Electric to help confirm the performance capabilities of advanced inverters prior to field deployment and to define the ranges of settings for UL1741 SA certification of the GSF contained in its Source Requirement Document.

An overview of similar PHIL based methods for testing GSFs is described in [5], but lacks the use of real-world feeder models as part of the test platform. Studies such as [6] assess the performance of inverters with GSFs using PHIL techniques with feeder models that capture both voltage and frequency dynamics, based on IEEE standard test feeder models rather than real-world feeder models. Similarly, [7] examines the impacts of GSFs on anti-islanding detection and [8] assesses fault ride-through performance using PHIL techniques, but neither implements modeled PV inverters with GSF capability in the real-time models.

The work presented in this study uniquely combines the following elements: 1) PHIL testing is executed with reduced-order, real-time models of distribution feeders in the field, 2) the real-time models have integrated "legacy" PV without GSF capability, and "advanced" PV inverter models with GSF capability that are based on the results of baseline tests used to characterize these two classes of rooftop PV inverter models, and 3) the PHIL tests combine physical hardware of advanced inverters that are GSF capable with the feeder model, coupled with the two classes of advanced and legacy PV models in order to assess the impacts of GSF on voltage support functions, among other GSFs.

II. PV INVERTER BASELINE TESTING

Four different commercially available grid PV inverters, referred to herein as Inverters 1-4, that are common on the Hawaiian Islands were selected for this study. These inverters were first characterized for their performance with different GSFs enabled. The GSFs of interest in this study were: voltage ride-through (VRT), frequency ride-through (FRT), fixed power factor operation, volt-watt control, ramp rate control, and soft start reconnection. Volt-var control was also characterized in baseline tests, but was not examined in subsequent PHIL tests. Combined activation of FPF and VWC were the primary functions of interest for PHIL testing, so only these functions are discussed in this paper; comprehensive tests results for all GSFs can be found in [9]. The inverters in this study included microinverters, a single-phase residential inverter, and a three-phase commercial inverter with DC optimizer inputs.

1

Inverters were individually connected to a bi-directional AC power supply (AMETEK MX-45) that acted as the grid simulator, and each inverter was sourced from an appropriately sized PV simulator from the AMETEK TerraSAS family. For most tests, the grid simulator voltage or frequency was varied according to a pre-defined profile, and the inverter's response was recorded for changing grid dynamics. All test procedures were based on a combination of requirements under Rule 14H and a draft version of UL 1741 Supplement SA, which was officially published in September 2016, several months after the baseline tests were completed [1,3]. Where necessary, the test procedures were modified with the goal of demonstrating a representative sample of each inverter's GSF capabilities.

FPF operation was validated for each inverter at 0.90, 0.95 absorbing (negative) power factor at 10%, 20%, 60%, and 100% nameplate power levels. Each inverter was manually programmed for the power factor set point and allowed to run at steady state. Larger errors occurred at the 10% power level, but at power levels ≥20%, most inverters had errors <0.5% of the expected value; the maximum error at these power levels was 1.3%.

A series of three VWC curves—referred to as "mild", "moderate" and "aggressive" based on their slopes—were defined for both baseline and PHIL testing, as shown in Figure 1. Each curve is characterized by a starting voltage where power curtailment begins and a final voltage where the inverter has linearly curtailed power to zero. The basic test sequence involved a series of voltage steps through each segment of the VWC curve, capturing at least three data points within each segment, as required by UL1741 SA. Each voltage step was held for at least twice the programmed settling time to ensure steady state operation. After stepping up to the maximum voltage, the AC source voltage was then stepped down to nominal, repeating each of the same operating voltages.
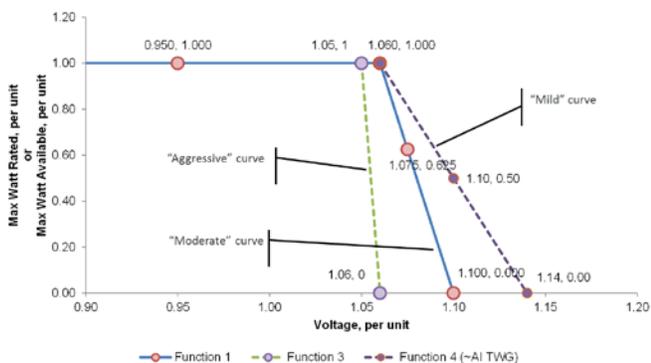

Figure 1. VWC curves used for baseline and PHIL testing

In addition to the characteristic curves, inverters were characterized for several other types of responses. Two of the four inverters could be programmed for either "nameplate power" or "snapshot power" modes, which distinguish between the baseline power level from which curtailment levels are determined. Additionally, different time responses—the time required to reach a new power set point for a step change in voltage—were tested for each inverter. Finally, tests were repeated at various power levels (33%, 66%, and 100%) to observe the different dynamics between nameplate power mode and snapshot power mode.

An example set of time series plots is shown in Figure 2, demonstrating the response of Inverter 2 when programmed for the aggressive curve at 100% output power. This figure shows the basic test sequence wherein voltage was increased in discrete steps until zero power output was achieved, and then decreased along the same profile. A comprehensive listing of all measured and expected values for each voltage step across all tests cases for all inverters, as well as additional time series and summary plots, are provided in [9]. In general, the errors between expected and actual power outputs were small for all inverters, except in some cases of the aggressive curve.
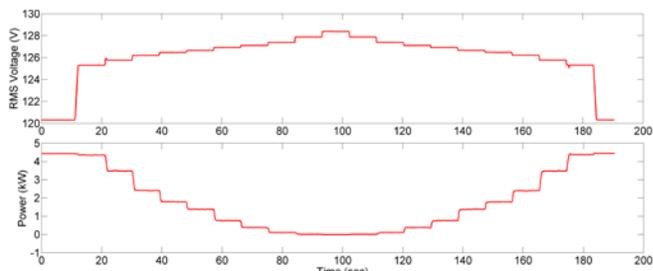

Figure 2. Inverter 2 VWC time series data for the aggressive curve at 100% output power

The time-domain response of the inverters was of particular interest for building models for PHIL testing, due to different implementations by different inverter manufacturers. Figure 3 shows an example time response due to a step change in voltage for Inverter 3 when programmed for a 50 second first-order time constant. This inverter consistently reached ~95% of the target value in approximately 120 seconds, regardless of the magnitude of change in power, implying a 40 second time constant when modeled as a first order exponential function. Alternatively, Inverter 2 had a linear response in power for a step change in voltage, which was programmable as the time for a 100% change in power, so the time response slope was dependent on the step size in power.
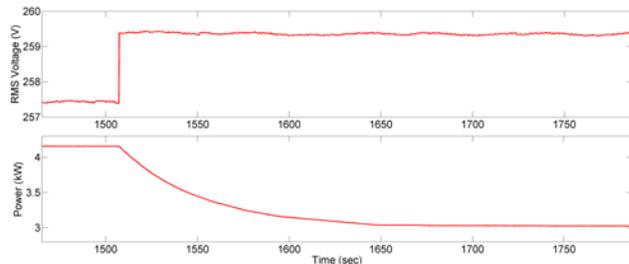

Figure 3. Inverter 3 VWC test segment with 50 second exponential time response for a step change in grid voltage

III. REAL-TIME MODEL DEVELOPMENT

Hawaiian Electric identified two distribution feeders of interest for the purpose of this study, which are referred to herein as Feeder 1 and Feeder 2, and both have high PV penetration with Feeder 1 having ~50% and Feeder 2 having ~200% PV penetration as a percentage of peak load. The feeder models consisted of several thousand nodes and were provided to

2

NREL in Synergi Electric's load flow software. Such a complex model could not be run on a real-time platform within an acceptable loop time step, so several techniques were used to create a reduced-order model in the real-time environment before integrating the PV inverter models.

A. Feeder Model Conversion to Real-Time

The two feeder models were first converted into OpenDSS, and then reduced to equivalent models consisting of eight nodes in OpenDSS based on an algorithm that allocated loads to the retained nodes and determined line parameters that resulted in the smallest voltage error compared to the original OpenDSS model. Additionally, legacy PV generators in the original feeder model were allocated to their closest geographically located node. Details of this multi-part conversion along with validation data is provided in [4] and [9].

For real-time PHIL testing, the OpenDSS reduced-order models were translated into Matlab/Simulink, for use in the OPAL-RT real-time digital testing platform. The outputs from the OpenDSS feeder reduction included the source impedance parameters, line lengths between nodes, line impedances between nodes, and loads at each node. The feeder head voltage source was an ideal three-phase voltage source behind a three-phase resistive-inductive (RL) source impedance; the primary voltage source was set for 7.2 kV at 60 Hz and was scaled to 105% of nominal for many tests that were required to create the high voltage conditions to test the performance of the VWC. A network of eight nodes on the primary was created using RL line impedances and a local three-phase unbalanced real and reactive power (PQ) load; each load was based on maximum daily values, and contained a programmable scaling factor for adjustments.

Each model also contained a single distribution secondary circuit to act as the point of interconnection for the inverters under test, simulating a small collection of households on a single transformer. The secondary circuits were connected at a location specified by Hawaiian Electric near the feeder head source with a distribution transformer. Similar to the primary circuit, each secondary node was connected via a RL line impedance, and each had a local PQ load. The Feeder 2 model contained six nodes on the secondary and the Feeder 1 model contained 13 nodes on the secondary. Inverter 4 was a three-phase inverter, and was therefore connected directly to the primary circuit through a transformer and RL line impedance.

B. PV Inverter Model Development

The next aspect to the real-time model was the inclusion of PV inverter models to represent different scenarios. Four different advanced inverter types were placed at each of the eight primary nodes, and each type was tuned based on characteristics observed during baseline hardware tests. One set of inverter models was based on Inverter 2 baseline test results due to the prevalence of this inverter on the feeders of interest. All other inverter types on these feeders were represented by a single model based on Inverter 3 test results. The key difference between these inverter types was the time response in VWC mode, as previously discussed.

Each of these two inverter types was additionally split between "legacy" and "advanced", each with different GSF ca-

pability. Advanced inverters were programmed with VRT and FRT limits specified in Rule 14H, while legacy inverters had the standard voltage and frequency trip limits specified in IEEE1547-2003. Advanced inverters had ramp rate and soft start control, while legacy inverters responded to changes in irradiance instantaneously and ramped to full power instantaneously after a grid event. Most importantly, advanced inverters could have FPF and/or VWC enabled as a user input, while legacy inverters were not capable of this functionality. The time response was modeled after the results from the baseline tests, but the VWC curves were based on ideal behavior, rather than tuned for the very small deviations from expected output found in the baseline testing.

The advanced inverters were modeled as power-controlled current sources that were driven by control logic that accounted for the maximum power rating of the inverter type, the irradiance input, the voltage at the node of interest, any enabled GSFs, and a number of user inputs. The power factor input was used to directly calculate the phase angle of the current output and the VWC function was implemented through look-up tables. The current output of all four model inverter types at each feeder primary node was summed together and injected into the node in aggregate.

The overall rating for the two different classes of PV inverter types was based on data provided by Hawaiian Electric on existing legacy PV systems, queued advanced PV systems, and future projected advanced PV penetrations. All future PV systems were assumed to be capable of all GSFs, and the VWC and FPF tests for present and future projected PV capacity were run in the base cases and also in two retrofit cases. One retrofit case had 25% of legacy inverters retrofitted to advanced inverters, and the second case had 50% legacy retrofitted to advanced inverters.

After the reduced-order model parameters were loaded into the Simulink model, all node voltages were verified to be the same as the reduced-order OpenDSS model voltages for each phase in each feeder model. For further comparison between the two model types, node voltages comparisons were made between the two models for different PV penetration scenarios. This analysis is detailed in [4], showing the maximum error for any of these phase voltages was 0.50%, and the mean error across all voltages was 0.26%.

IV. PHIL TEST SETUP

PHIL testing is a hybrid between software simulations and hardware tests, whereby a physical power hardware device interfaces with a model through intermediary hardware, and the hardware under test is able to dynamically interact with changes in the model, and vice versa. The PHIL concept is depicted in Figure 4 for multi-inverter test cases. The real-time model was broken into a master subsystem and two slave subsystems computed in parallel so that the logic could be executed on multiple processing cores and real-time performance could be maintained at an acceptable time step. The reduced-order feeder models were executed in the master subsystem, and the test inverters were "connected" to a particular node of choice on the secondary circuit in the feeder models. The output of the model through this connection was a low-voltage sinusoidal signal representing the voltage at the node of

choice. The low-voltage signal was routed to the grid simulator, which acted as an amplifier and created the reference voltage for the tested advanced inverter. The key concept that "closes the loop" in PHIL testing is the output current from the hardware inverter was measured with a current transducer, and fed back into the simulation in real-time. The node voltage within the model then interacts dynamically with the hardware under test.
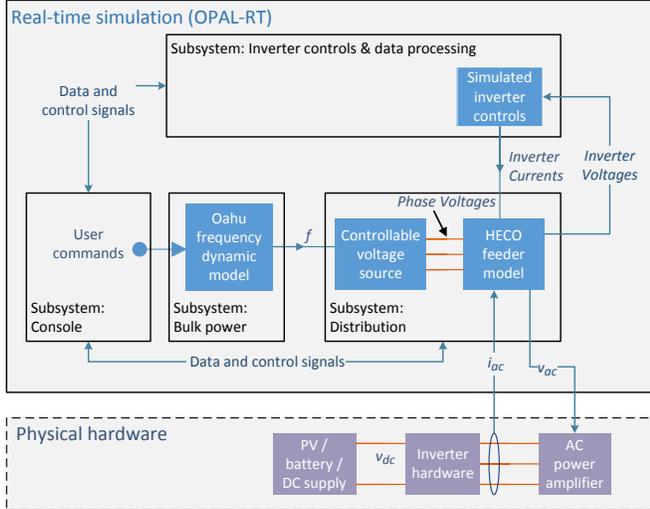

Figure 4. PHIL testing configuration for multi-inverter experiments

Additional features were added to the model in the user interface, including the ability to change advanced PV inverter ratings, select VWC functions, create irradiance change profiles, set a FPF, and trigger data logging from the model, among other things. All models were executed at fixed time steps between 180-260 μs, depending on the complexity of the model and test case. Several important control features were also implemented in the real-time model in order to improve stability of the model, similar to those discussed in [10].

V. PHIL TESTING WITH REAL-TIME MODEL

The complete real-time model with hardware PV inverter setup was used to test all GSFs of interest, but the primary focus was on combinations of VWC with FPF control in order to examine the effects on node voltages during dynamic changes in irradiance. The standard test case consisted of linearly ramping irradiance from a very low value to a very high (e.g., 20% to 100% of rated PV input) over a relatively short period of time (typically 40 seconds), both in the simulation and hardware domains. Although this represents a very fast change in cloud cover across a feeder area, it is still representative of a real-world situation, and allowed tests to be run over a reasonably short duration. A number of other variables were used to raise circuit voltages high enough to trigger the VWC function, including setting the source voltage to 105% of nominal (top of the ANSI Range A), minimizing loads throughout the network, and adding legacy PV inverters to the secondary circuit. All advanced PV inverters (modeled and hardware) were programmed for a 50 second time constant.

There were several variables of interest across all test cases, so a different combination of these variables was used for the different hardware inverters in order to maximize the number of variables investigated within the time available for this study. The variables changed for each test included power factor setting, VWC characteristic curve, nameplate/snapshot mode, present/future PV penetration ratings, inverter retrofit proportion, and feeder model. A summary of all test variables is shown in Table I.

TABLE I.   TEST SUMMARY FOR VWC WITH FPF PHIL TESTS

Parameter	Inverter 1	Inverters 2 & 3	Inverter 4
Power Factor	0.90, 0.95, 0.98, 1.00	0.90, 0.95, 1.00	0.90, 0.95, 1.00
VWC Curves	None, Moderate, Aggressive	None, Moderate, Mild	None, Moderate, Aggressive, Mild
VWC Mode	Snapshot, Nameplate	Nameplate	Nameplate
PV Ratings	Future	Present, Future	Future
Retrofit Proportions	0%	0%, 25%, 50%	0%
Feeder Models	1, 2	1, 2	1, 2
Test Count	40	108	24

A set of sample results are shown in Figure 5 and Figure 6, demonstrating the effect of implementing both GSFs on Inverter 1 on the Feeder 1. In these test cases, irradiance was ramped between 200-1000 W/m^2 in 40 seconds, and the primary nodes had future PV ratings with no retrofits. Figure 5 is a baseline test case with VWC disabled and all existing inverters operating at unity power factor, which caused a voltage rise up to 108.2% of nominal at the inverter. When 0.95 power factor with the moderate VWC curve was implemented in Figure 6, output power was curtailed to 44% and the voltage rise was reduced by 1.3%. This figure additionally shows the reactive power that was sourced by the modeled inverters and the hardware inverter, further mitigating the voltage rise. Both plots show the inverter voltage and power outputs (black solid line), as well as the primary node PV inverter output power and secondary node voltages (colored lines); primary voltages have been omitted since very little change occurred for this test case.
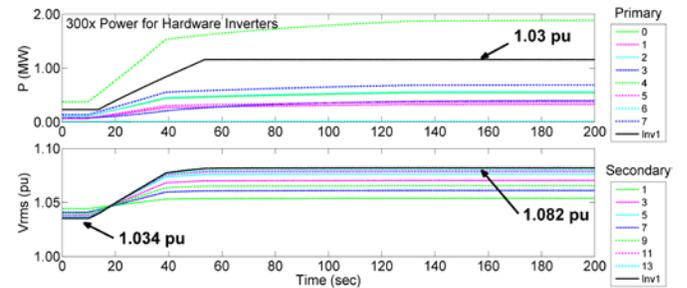

Figure 5. VWC with FPF waveform plot, Inverter 1, PF = 1.0, no VWC curve, snapshot mode, future, 0% retrofit, Feeder 1

Figure 7 shows a summary of all test cases for Inverter 1 on the Feeder 1. These plots show the final voltage measured at the inverter terminals (left) and the final output power of the hardware inverter (right) as a function of VWC curve (x-axis), power factor (color), and mode (marker style). These data show that VWC had a significant impact on voltages, leading

4

to 1-2% more voltage reduction for the moderate and aggressive curves. The aggressive curve enforced nearly 100% power curtailment in these test cases; the moderate curve led to varied power curtailment. Operating in snapshot mode led to greater power reductions and lower voltages. Finally, power factor had a modest effect, resulting in noticeable voltage reductions on the order of several tenths of a percent for a several point reduction in power factor.
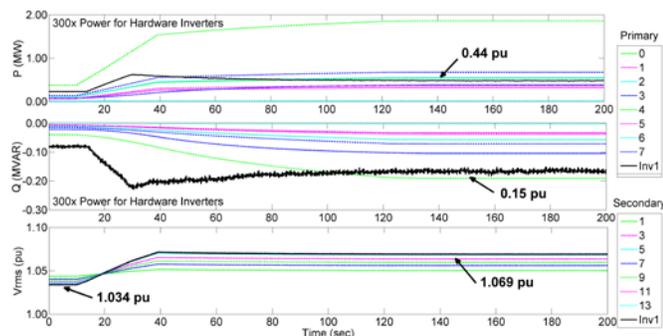

Figure 6. VWC with FPF waveform plot, Inverter 1, PF = 0.95, moderate VWC curve, snapshot mode, future, 0% retrofit, Feeder 1

The results for the Feeder 1 were unique from those of the Feeder 2, where neither the operating mode nor the VWC setting had much impact on voltages, but power factor had a much more significant effect. One major difference between the feeders was the proportion of advanced inverters, in addition to differences in topology, line impedances, and loads. A comprehensive set of test results, comparison plots, and analyses are provided for all inverters and all test cases in [9]. Voltage regulation varied across all test cases, depending on the inverter type, inverter location, feeder model, and variables of interest.
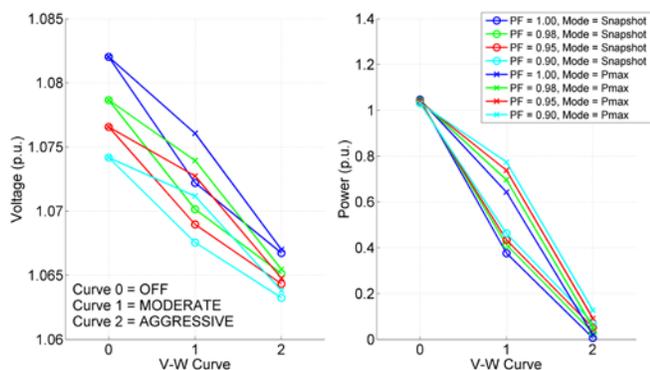

Figure 7. VWC with FPF summary data for Inverter 1 on Feeder 1, showing final inverter voltages (left) and final inverter output power (right)

CONCLUSIONS

The tests presented here examined the impact of various PV inverter-based grid support functions on two simulated Hawaiian distribution feeders. The distribution feeder models were derived in simplified form from models of actual Oʻahu circuits, with actual legacy PV systems and projected future advanced PV systems represented in the model. Several novel feeder model reduction techniques were implemented, and the behavior of the modeled PV systems was based on laboratory tests of advanced PV inverters performing grid support functions. Using PHIL techniques, four advanced PV inverters from different manufacturers were connected to real-time simulations of the circuits, and were used to evaluate six grid support functions in various scenarios. Most scenarios focused on different combinations of fixed power factor operation and volt-watt control, with a goal of evaluating the impact of those functions on the selected feeders. The impacts of these functions varied depending on the feeder model, inverter type, inverter location, and GSF settings. The final report presenting the comprehensive results has been submitted to the Hawaiʻi Public Utilities Commission.

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5