Hawaiian Electric Advanced Inverter Grid Support Function Laboratory Validation and Analysis

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Technical Report
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December 2016

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List of Acronyms

AC	Alternating current
DC	Direct current
EMT	Electromagnetic transient
FIT	Feed-in tariff
FPF	Fixed power factor
FRT	Frequency ride-through
GSF	Grid support function
HFRT	High frequency ride-through
HIL	Hardware-in-the-loop
HVRT	High voltage ride-through
IEEE	Institute of Electrical and Electronic Engineers
kWh	Kilowatt-hour
LFRT	Low frequency ride-through
LVRT	Low voltage ride-through
MAITAI	Manufacturing Alliance of Inverters Technical Assessment of Integration Issues
MSA	Manufacturer's stated accuracy
NEM	Net Energy Metering
NREL	National Renewable Energy Laboratory
NORH	Normal high operating region (per Rule 14H)
NORL	Normal low operating region (per Rule 14H)
OFR	Overfrequency ride through (per Rule 14H)
OVR	Overvoltage ride-through (per Rule 14H)
PHIL	Power hardware-in-the-loop
PLL	Phase locked loop
PQ	Real and reactive power
pu	Per unit
PV	Photovoltaic
RL	Resistive-inductive
RMS	Root mean square
SIA	Standard Interconnection Agreement
SITWG	Smart Inverter Technical Working Group
SRD	Source Requirements Document
UL	Underwriters Laboratories
UFR	Underfrequency ride-through (per Rule 14H)
UVR	Undervoltage ride-through (per Rule 14H)
VRT	Voltage ride-through
VVC	Volt-var control
VWC	Volt-watt control
µs	Microsecond

Executive Summary

The Hawaiian Electric Companies[1] sought the support of the U.S. Department of Energy's National Renewable Energy Laboratory (NREL) to assist the Companies' efforts to meet the Hawai'i Public Utilities Commission (HPUC) Order[2] to collaborate with inverter manufacturers to develop a test plan for the highest priority advanced photovoltaic (PV) inverter functions that do not yet have Nationally Recognized Testing Laboratory certification to Underwriters Laboratories (UL) Standard 1741. In the HPUC Order, the Companies were also directed to test a variety of advanced inverters to assess their performance with respect to the high priority grid supportive functions for Hawai'i's operating requirements and to submit its findings to the HPUC.

The Companies' stated objectives for this test plan were to better understand how to utilize the performance capabilities of advanced inverter functions to allow the interconnection of distributed energy resource (DER) systems to support the new Customer Self-Supply, Customer Grid-Supply, and other future DER programs.

The purpose of this project was to: 1) characterize how the tested grid supportive inverters performed the functions of interest, 2) evaluate the grid supportive inverters in an environment that emulates the dynamics of O'ahu's electrical distribution system, and 3) gain insight into the benefits of the grid support functions on selected O'ahu island distribution feeders.

The following four inverter manufacturer members from the Companies' Smart Inverter Technical Working Group (SITWG) contributed inverter hardware and technical support for testing under this project: Apparent Inc., Enphase Energy, SolarEdge Technologies, and SMA America. A total of five inverters were tested: two models from Enphase and one model each from the other three manufacturers. The Enphase inverters consisted of one "legacy" inverter model (i.e. a model not capable of providing some or all of the grid supportive functions contemplated by UL 1741 Supplement SA) and one model of grid supportive inverters. The inverters from Apparent, SMA, and SolarEdge were all grid supportive models.

The selection of grid supportive inverters represented a broad spectrum of technologies including one split-phase residential-scale string inverter, assemblies of three types of microinverters, and one three-phase 480 V small commercial string inverter. The Companies expanded the scope of inverter testing to include the Enphase legacy inverters in order to better characterize the baseline performance of existing legacy PV systems since the Enphase legacy inverters have such a dominate presence on the Hawaiian island grids.

The Hawaiian Electric Companies tariff for Interconnection of Distributed Generating Facilities with the Company's Distribution System (Rule 14H) defines a total of eleven grid supportive functions. Of the eleven functions, the Companies with input from the members of their SITWG identified seven grid functions to be tested by NREL. The SITWG also provided NREL with

[1] Hawaiian Electric Company, Inc.; Maui Electric Company, Limited; and Hawai'i Electric Light Company, Inc. are collectively referred to as the "Hawaiian Electric Companies" or "Companies".
[2] Order No. 33258, Docket No. 2014-0192, Instituting a Proceeding to Investigate Distributed Energy Resource Policies.

technical review and feedback on the test plan and testing requirements at various points throughout the project.

The seven grid support functions tested were:

- Fixed power factor operation
- Volt-watt control
- Volt-var control (baseline testing only)
- Voltage ride-through
- Frequency ride-through
- Ramp rate control
- Soft start reconnection

Some combinations of these functions were also tested simultaneously to the extent the specific inverter model was able to support the combined activation of functions.

The tests conducted under this project fall into two categories. The first category, referred to here as "baseline" testing, consisted of conventional lab testing, in which the input and output terminals of the inverter under test were connected to DC and AC power supplies, the AC voltage or frequency was varied systematically, or the available DC input power was varied, and the inverter's response was recorded. For the baseline tests, the test procedures were based on a draft version of the recently-published UL 1741 Supplement SA. The goal of testing was not to certify inverters, but rather to characterize their responses for the grid support functionality. A total of over 238 baseline tests were performed across the five inverters.

The second category of tests consisted of power hardware-in-the-loop (PHIL) tests, which coupled computer simulation with hardware testing. In the PHIL tests, real-time models of two of Hawaiian Electric's electrical distribution feeders were run, and the simulated voltage at a distribution secondary location was used to drive the voltage waveforms of an AC power supply connected to a PV inverter. The measured AC current from the inverter was fed back into the feeder model, such that the inverter and the simulated distribution system were dynamically connected. Thus the PHIL tests simulated placing the inverter under test on a real feeder. In addition to the hardware inverter, the simulated feeder contained many simulated legacy and grid supportive PV inverters whose ratings were based on the inverters actually deployed (or expected to be deployed) on the real feeder. The simulated grid supportive PV inverters emulated the behavior of the hardware inverters characterized in the baseline tests. This allowed the PHIL tests to evaluate the impact of very large numbers of grid supportive PV inverters configured in various ways performing the selected grid support functions. A total of over 250 PHIL tests were performed across four inverter models; the legacy Enphase inverters were not tested in PHIL.

The PHIL tests simulated two O'ahu island distribution circuits with high levels of legacy distributed rooftop PV (penetration levels of 88% and 140% of gross daytime minimum load as of the end of 2015). Scenarios reflecting Hawaiian Electric's forecast of PV penetration by 2021 were also tested in PHIL. Due to the computational speed limitations of the PHIL system, a reduced-order model of each distribution circuit was developed and used for the PHIL tests. At one location on each feeder model a detailed distribution secondary circuit model was connected, and the hardware inverters were connected at load nodes on that secondary. Because some of the grid support functions tested here responded to the AC voltage at the inverter's terminals, the inclusion of the secondary circuits with their associated impedances was crucial.

The PHIL tests followed a test matrix jointly developed by the Hawaiian Electric Companies and NREL, with the collaborative review and input from the members of the Companies' SITWG. Only six of the seven grid supportive functions listed above were tested in PHIL. Volt-var control was added to the project scope by NREL after the initial design of the test matrix in response to the recommendations from the members of the SITWG and was not tested in PHIL. Simple scenarios designed to observe the behavior and impact of the functions in realistic environments were used in the PHIL tests of ride-through, ramp rate control, and soft start reconnection.

The majority of the PHIL tests focused on various combinations of fixed power factor operation and volt-watt control. The test matrix included testing present-day (2016) scenarios and future forecasted (2021) scenarios of PV penetration for each circuit. It was assumed for the purposes of these PHIL tests that all PV added after early 2016 would be capable of providing grid support functions, though it should be noted that this may not be strictly accurate because queued PV systems under the NEM (net energy metering) tariff are not required by contract to provide such services. Due to the very large number of legacy inverters on each circuit, the matrix included scenarios with 0%, 25%, and 50% of the legacy inverters retrofitted for grid supportive functions. In some PHIL tests, two different hardware inverters models were connected at neighboring locations on the same secondary, which would allow any undesired dynamic interactions between the two inverters to be observed.

Conclusions and recommendations from baseline testing

In the baseline tests, all grid supportive PV inverters tested were able to perform all of the functions tested satisfactorily, with the following comments and qualifications:

- All manufacturers are expected to be able to pass the UL 1741 SA tests by the time certification is required in Hawai'i (12 months after the publication of UL 1741 SA). UL 1741 SA was published on September 7, 2016, and manufacturers are expected to begin the certification process very soon if they have not already begun.[3]

- The UL 1741 SA certification process requires that each utility provide a Source Requirements Document (SRD) specifying the ranges of parameters to be certified for each function. Because California represents a much larger market than Hawai'i, it is recommended that the Hawai'i utilities (or any other utilities not using California Rule 21 grid support settings) work closely with inverter manufacturers to ensure inverters are available to meet their specifications.[4]

- Configuring grid support functions individually is time-consuming and error-prone. Pre-configured location-specific function profiles (sometimes called "country settings") are recommended for widespread field deployment. It is possible that a given island may

[3] The availability of UL 1741 SA certified inverters in Hawai'i is largely dependent on the certification plans of inverter manufacturers, product availability timing by inverter manufacturers, and other market forces of the solar industry.

[4] The Hawaiian Electric Companies are also engaged in ongoing technical discussions as part of the update to IEEE Standard 1547. Technical discussion topics include modes for the volt-watt function.

require more than one profile in the coming years, with different profiles used in different field conditions.

- Testing and certification of grid support functions by OSHA-recognized Nationally Recognized Testing Laboratories using standardized test procedures will provide improved assurance that all GSFs operate as expected, and is recommended whenever possible.

- Some inverter manufacturers had not seen the UL 1741 SA draft in advance (or had seen an old version), so some test details were a surprise, requiring slight test modifications and/or iterations on inverter firmware or settings.

- Functions (or combinations of functions) not required in another grid code were not supported in all inverters. In particular, ramp rate control during normal operations was less likely to be fully supported at the time of testing. In addition, simultaneously enabling volt-var control and volt-watt control was only supported by two of the test inverters at the time of testing. However, the current draft of the revision to IEEE Standard 1547 requires many DERs to be capable of enabling both functions, so many inverter manufacturers are expected to develop this capability going forward.

Limitations and qualifications of PHIL test scenarios

In addition to the above baseline test conclusions, several conclusions can be drawn from the PHIL tests. Before reviewing the conclusions from PHIL tests, it is very important to keep in mind the following limitations of the PHIL test scenarios:

- Each PHIL test examined a brief test scenario covering a time window of several minutes. In addition, each feeder model contained only one secondary circuit. Only limited information can be obtained from these tests about other locations on the circuit or other points in time. Therefore only limited conclusions can be drawn about the effects of the functions on annual voltage profiles, and still fewer conclusions can be made about the effects of these functions on annual PV energy production. These important considerations are the reasons that NREL and the Hawaiian Electric Companies have proactively begun a follow-up Voltage Regulation Operational Strategies (VROS) project to examine these effects. The VROS simulation study is expected to be one of the key planning initiatives of the Hawaiian Electric Companies' Advanced Inverter Program for 2017.

- The volt-watt and fixed power factor PHIL tests were intentionally designed to create high voltages that would provide interesting test cases for the volt-watt function, since that function does not have any effect until voltages are fairly high (greater than 105% of nominal voltage or 1.05 pu, for the volt-watt curves used here).

- Utility-side measures for reducing high service voltages such as tap-changer control modifications, circuit upgrades, and deployment of other voltage regulation devices were not examined in this study.

- These test results are feeder-specific. The two feeders tested have very high levels of PV: 88% to 140% of gross daytime minimum load in the 2016 scenarios, and 141% to 539% in the 2021 scenarios. Therefore, caution should be used in applying these conclusions directly to other feeders with lower PV penetrations. However, that should not be taken to mean that feeders with lower levels of PV should not have grid support functions enabled. In fact, it is recommended that grid support functions be enabled even on low PV penetration feeders if higher penetrations are expected, to avoid future high voltage problems when PV levels increase.

Conclusions and recommendations from PHIL testing

With the above qualifications in mind, salient conclusions and recommendations from the PHIL testing include the following:

- All four inverters used for PHIL testing were able to reliably perform volt-watt control and fixed power factor control simultaneously.

- In the PHIL tests with two hardware inverters connected at neighboring locations, no undesired dynamic interactions were observed from volt-watt control or fixed power factor.

- PHIL test results showed both volt-watt control and absorbing power factor operation to be effective tools to manage high voltage conditions in many scenarios. Based on this work, it is recommended that Hawaiian Electric continue to require 0.95 power factor (absorbing) operation at least until other reactive power functions (e.g. volt-var control) can be certified. However, it is noted that adding inverters with grid support functions will not necessarily fix voltage issues in all cases.

- As implemented here, operating at a power factor of 0.95 (absorbing) serves as the primary method of reducing high voltages. Volt-watt control was implemented such that it becomes active only at voltages outside ANSI Range A. This strikes a balance between minimizing the reduction of PV generation while still helping ensure utility service voltages comply with ANSI reliability requirements.

- The effects of volt-watt control and fixed power factor depended strongly on the total rating of inverters performing the grid supportive functions, the ratio of grid supportive inverters to legacy inverters, and the circuit being tested. In scenarios with a large number of grid support capable inverters relative to the total rating of legacy inverters, operating at a power factor of 0.95 (absorbing) tended to reduce the voltage such that the volt-watt function was not very active. However, in scenarios with smaller numbers of inverters performing grid support, circuit voltages were higher and the volt-watt function became more active. In other words, a “critical mass” of grid supportive inverters is needed to effectively mitigate high voltages, and that critical mass depends on factors including load, legacy PV penetration, circuit impedance and topology, and the specific grid support functions and parameters in use. Based on the need to establish this critical mass of grid supportive inverters for effective voltage management, and subject to the qualifications above, it may be reasonable to activate a moderate volt-watt curve in

addition to 0.95 (absorbing) power factor operation to help mitigate very high voltages when they occur. A reasonable volt-watt curve may be one that leads to power reduction when the voltage is outside the ranges specified in ANSI C84.1-2011, such as the "moderate" curve tested here. This would be expected to result in some loss of PV production for some individual systems, but would also be expected to enable more PV deployment circuit-wide sooner while awaiting the time required for costly circuit upgrades in many cases.

- There is a large number of legacy NEM PV systems currently slated to be installed that are not scheduled to provide grid support functions because they were approved before the requirement for installation of grid supportive PV inverters. The continued installation of legacy inverters that do not provide grid-supportive functions will continue to have an impact on hosting capacity into the future. Modifications of these legacy NEM PV systems to enable grid support before installation would likely help to prevent high-voltage issues.

Additional discussion of inverter-based voltage regulation functions can be found in the conclusions of the report.

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1 Introduction

The Hawaiian Electric Companies have collaborated with the U.S. Department of Energy's National Renewable Energy Laboratory (NREL) to conduct laboratory testing, modeling, and analysis of selected solar photovoltaic (PV) inverters at NREL's Energy Systems Integration Facility (ESIF). This inverter testing project was performed in response to an order from the Hawai'i Public Utilities Commission as part of the Distributed Energy Resources Policy Proceeding (Docket No. 2014-0192). The testing focused on selected grid support functions available from the inverters.

Seven grid support functions were tested:

1) Voltage ride-through (VRT)
2) Frequency ride-through (FRT)
3) Fixed power factor operation (FPF)
4) Volt-watt control (VWC)
5) Volt-var control (VVC, baseline testing only)
6) Ramp rate control
7) Soft start reconnection

Some combinations of these functions were also tested simultaneously. Functions 1-3 were already actively in use on Hawaiian grids, and the remaining four functions are proposed for future activation.

The Hawaiian Electric Companies and NREL collaborated with the Hawaiian Electric Companies' Smart Inverter Technical Working Group (SITWG) in the design and execution of the project. The SITWG consists of members of the PV industry with interest and expertise in grid integration of PV inverters and systems in Hawai'i. Early on it was decided by Hawaiian Electric, NREL, and members of the SITWG to design the project to serve multiple goals:

1) Characterize the inverters' performance of grid support functions (GSFs).
2) Evaluate the inverters in an environment that emulates the dynamics of a Hawai'i electrical distribution system.
3) Evaluate the impact of the grid support functions on the Hawai'i distribution system.

This first goal was met through conventional laboratory testing, where the input and output terminals of the inverter under test were connected to DC and AC power supplies, the AC voltage or frequency or the available DC input power was varied systematically, and the inverter's response was recorded. These conventional tests are referred to in this report as *baseline tests*. They served both to verify that the inverters could satisfactorily perform the functions and to characterize the dynamic performance of the inverters for use in meeting second and third goals.

At the time of testing, no standardized test plan existed for grid support inverter functions. For the baseline tests, the test procedures were based on a draft version of UL 1741 Supplement SA, which has now been published and incorporated into UL 1741 [1]. The intent of the baseline testing was not to certify inverters, but rather to characterize their responses for the new grid support functionality.

The second and third goals were achieved using power hardware-in-the-loop (PHIL) testing, which combines computer simulation and hardware testing into a single dynamic test environment [2], [3]. The PHIL tests conducted here simulated models of O‘ahu distribution feeders in real-time with one or two hardware inverters connected and many more aggregated inverters connected to the simulated distribution circuits. Thus, these tests characterized the performance of the inverters in an environment that emulated the dynamics of real Hawaiian distribution feeders. To allow the distribution models to be solved in real time, the original Synergi feeder models were reduced to simpler models and converted to dynamic simulations using a technique described in Section 2 and in [4]. The power flow of the reduced models was validated against the power flow of the original models at various loading levels. Distribution secondary circuits provided by Hawaiian Electric were connected to a single point in each feeder as points of interconnection for the hardware inverters under test. The distribution secondary circuits enabled more realistic simulation of service voltages at the hardware inverters. For tests of volt-watt control and fixed power factor operation, the PHIL tests were intentionally designed to create high voltages that would provide interesting test cases for the volt-watt function, which is only active at high voltages. The PHIL tests were not designed to simulate any specific moments in time, but rather to simulate events that would allow the behavior of the GSFs to be examined.

The members of the SITWG were solicited to submit GSF-capable PV inverters for testing. More inverter manufacturers applied to participate than could be accommodated. Hawaiian Electric and NREL developed a set of criteria to down-select. The criteria included the ability of the inverters to perform the selected GSFs, the prevalence of the inverter type in the Hawaiian market, the ability of the manufacturer to provide documentation and technical support during testing, and the desire to test a diverse range of products. The selected manufacturers were:

- Apparent, Inc.
- Enphase Energy
- SMA America
- SolarEdge Technologies

All four of the manufacturers voluntarily provided PV inverters capable of performing the selected GSFs and technical support throughout the testing. In addition, due to the prevalence of Enphase inverters in the fleet of legacy inverters on Hawai‘i, a second Enphase model representative of the Enphase legacy fleet was added to the baseline testing phase. The legacy Enphase inverter was only tested for the subset of the functions that it could perform with certified firmware versions.

At the time of testing, no standardized test plan or certification process existed for the functions under test. Therefore, with the exception of the legacy Enphase inverter, all inverters were necessarily being testing outside of the range of operation for which they were certified at the time.

1.1 Power Hardware-in-the-Loop Testing

Each PHIL test simulated one of two different distribution feeder models provided by Hawaiian Electric. The two feeders are referred to as M34 and K3L. Both have high levels of PV installed, with higher levels projected by Hawaiian Electric in the future, as shown in Table 1. These high levels of PV provide an opportunity to examine the impact of GSFs that may be suited to locations with high voltages due at least partially to PV backfeed. Additional information on the two feeders is presented in the next section.

Table 1. PV penetration levels of simulated feeders

	PV as % of peak load		PV as % of gross daytime minimum load	
Year	**K3L**	**M34**	**K3L**	**M34**
January 2016, actual	45%	60%	88%	140%
2021, projected	72%	232%	141%	539%

Note that PHIL testing provides many advantages but is also subject to certain limitations. A primary advantage of PHIL testing is that it allows hardware for which an accurate model is not known or available to be coupled with a simulation in closed-loop fashion. For example, as done here, proprietary PV inverter technology can be incorporated into a simulation of a distribution system. A second advantage relative to pure hardware testing is that the simulated model can be easily modified through software changes. For example, one can ask questions like "what if the solar irradiance increases by 80%? How will that affect the voltage at the hardware inverter's location, and how will the inverter react?" Additionally, abnormal grid events can be simulated on the feeder model to evaluate inverter response. Such conditions may not otherwise be possible or desirable to test in the field.

A primary limitation of PHIL relative to pure simulation is that PHIL runs at wall-clock time; i.e. simulating a year-long time window would take one year. For this reason each PHIL test described here lasts only minutes. This imposes some limits on the strength of conclusions that can be drawn from these tests. A second limitation of PHIL testing is that the real-time model must be solved once per discrete simulation time step, which in these tests was very short. The size of the discrete time step must be short enough to accurately capture all dynamics of interest in the test, including both those of the hardware system and those of the simulated system. In these tests, it was decided that the real-time grid model should be an electromagnetic transient (EMT) model in order to capture the sub-line-cycle dynamics of the functions under test. To simulate an AC power system and accurately reproduce a 60 Hz sine wave, the EMT model must have a time step around two orders of magnitude faster than a 60 Hz line cycle, i.e. roughly 200 microseconds or less. A full distribution feeder model containing hundreds of nodes could not be solved that quickly on the hardware available to the project. To allow such fast time steps, reduced-order distribution models were developed that can be solved in the available time, as described in Section 2.

Various aspects of the real-time PHIL model were validated as described in Sections 2 and 4. In addition, the PHIL techniques used here are similar to those used in past work by NREL and others, where they have been shown to match pure hardware test results within an acceptable margin of error [5]–[8]. Another approach to validation of PHIL tests accuracy is to compare to a pure simulation without hardware in the loop, as done in [9]. While a full validation of the exact PHIL setup used here via live field testing is not within the scope of this study, the validation of individual components of the PHIL system and the use of techniques that have been validated in past work give good confidence that the test results are accurate within an acceptable error margin.

The bulk of the PHIL tests examined various scenarios designed to test the two voltage regulation functions included in the test plan: VWC and FPF. These tests examined the following variables:

- Volt-watt curve
- Volt-watt mode. Two options: based on rated power or based on pre-disturbance power
- Inverter power factor
- PV penetration level: present (2016) versus future (2021)
- Portion of PV systems retrofitted for advanced functions

For the tests of FRT, a real-time model of the O‘ahu bulk power system frequency dynamics was developed, as described in Section 4. The frequency dynamic model was tuned to emulate historical recorded frequency events. The output of the frequency model was used to drive the AC frequency of the distribution system model. This allowed the FRT function to be tested using field-realistic underfrequency and overfrequency events. The real time O‘ahu bulk power system model used here was an early version of the model used in an ongoing NREL-led project examining grid frequency support from distributed energy resources.

Detailed descriptions of the PHIL tests can be found in Section 5.

2 Network Reduction Algorithm to Develop Distribution Feeders for Real-Time Simulators

The first task was to translate two selected feeder models into OpenDSS based on Synergi Electric (Synergi) load flow software models provided by Hawaiian Electric. The OpenDSS models were subsequently developed into reduced feeders, which were then modeled in the OPAL-RT real-time simulation platform in the EMT domain. This allowed the feeder models to be used in PHIL experimentation. The models simulate the medium voltage distribution system down to the level of the primary of the distribution transformers. Selected low voltage secondaries were added after the model reduction.

In order to develop the OPAL-RT model and execute within an acceptable time step in an EMT simulation, the OpenDSS model was reduced to eight nodes, based on an algorithm that allocated loads to the retained nodes and determined line parameters that resulted in the smallest voltage error compared to the original OpenDSS model.

This task consisted of the following activities, described in further detail in the rest of this section:

- Synergi to OpenDSS model conversion
- OpenDSS model verification
- OpenDSS model reduction and verification
- PV generator node identification
- Conversion to OPAL-RT and verification

2.1 Synergi to OpenDSS Model Conversion

This section describes the process involved in Synergi to OpenDSS model conversion. A brief description about the characteristics of the selected feeders will be provided prior to the details about model conversion.

Hawaiian Electric identified two distribution feeders for the purpose of study. The identified feeders are referred as K3L and M34. Both feeders have high PV penetration levels. The total PV generation rating on K3L was 45% of peak load in 2015 and is projected to be 72% of peak load in 2021. On M34 the 2015 total rating of PV generation was 60% of peak load, and it is projected to be 232% of peak load in 2021. The characteristics of selected feeders are listed in Table 2. Geographical views of the Synergi and OpenDSS models are shown in Figure 1 and Figure 2.

Table 2. Characteristics of selected feeders

Characteristic	K3L	M34
Feeder length	3 miles	10 miles
Peak load	6.7 MVA	6.5 MVA
Daytime minimum load	3.4 MW	2.8 MW
Rated PV generation, Jan. 2016	3.0 MW	3.9 MW
Rated PV generation, 2021	4.8 MW	15.1 MW
Capacitor banks	0	0
Node count	1740	2569

The Synergi to OpenDSS conversion was accomplished with an automated Python script tool that takes network configuration (.xml) and line configuration (.txt) as input. To use the tool, the feeder model provided by Hawaiian Electric in Microsoft Access database format was opened in Synergi and then exported in Extensible Markup Language (XML) format. Additionally, the line impedance information was also extracted from Synergi using the Synergi's "line construction" report and used as an input by the tool. The conversion tool took the two files described (the feeder in XML format and the line construction report in text format) as inputs and created a folder with the OpenDSS circuit model files. The user then opened the master circuit file and ran it in OpenDSS.

The conversion software code was programmed in Python and was structured such that properties for each instance of a Synergi object are collected for all objects in the feeder file in XML format, and then operated on via syntactical and mathematical conversions to create a corresponding OpenDSS element, associated DSS file, and master circuit file.

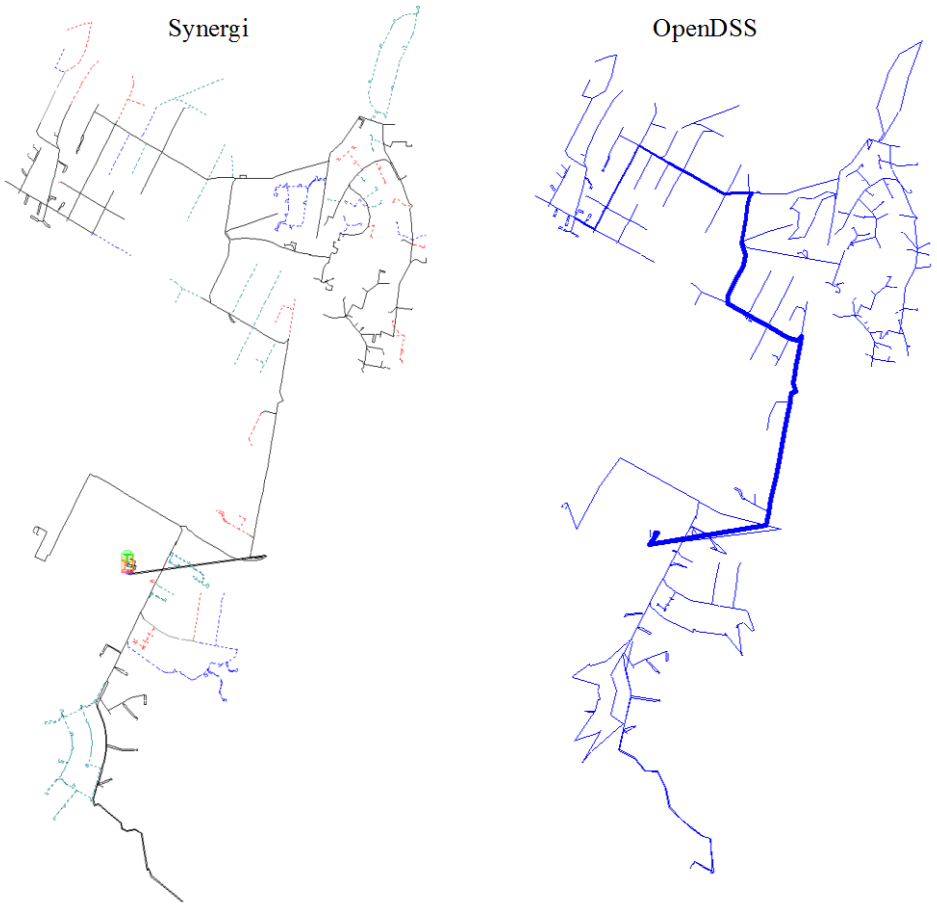

Figure 1. Geographical view of K3L distribution feeder in Synergi (left) and OpenDSS (right)

Figure 2. Geographical view of M34 distribution feeder in Synergi (left) and OpenDSS (right)

Specifically, the conversion process read the XML file and identified, collected, and categorized objects and their parameters for all object blocks within the XML file. As can be seen in Figure 3, the object blocks were identified by the symbol "<" with six space characters of indentation from the margin. After the object type was identified, a function defined for that object type was called and the values for each property were collected. The called function then assigned the collected property values to the container for that object type. In the functions, the values were not altered and the names of each object were kept the same as assigned in the Synergi XML file, which assisted in the debugging process. The next step in the conversion process was to create objects in the OpenDSS script using the collected Synergi objects and their properties. A view of the syntax identification process is presented in Figure 3.

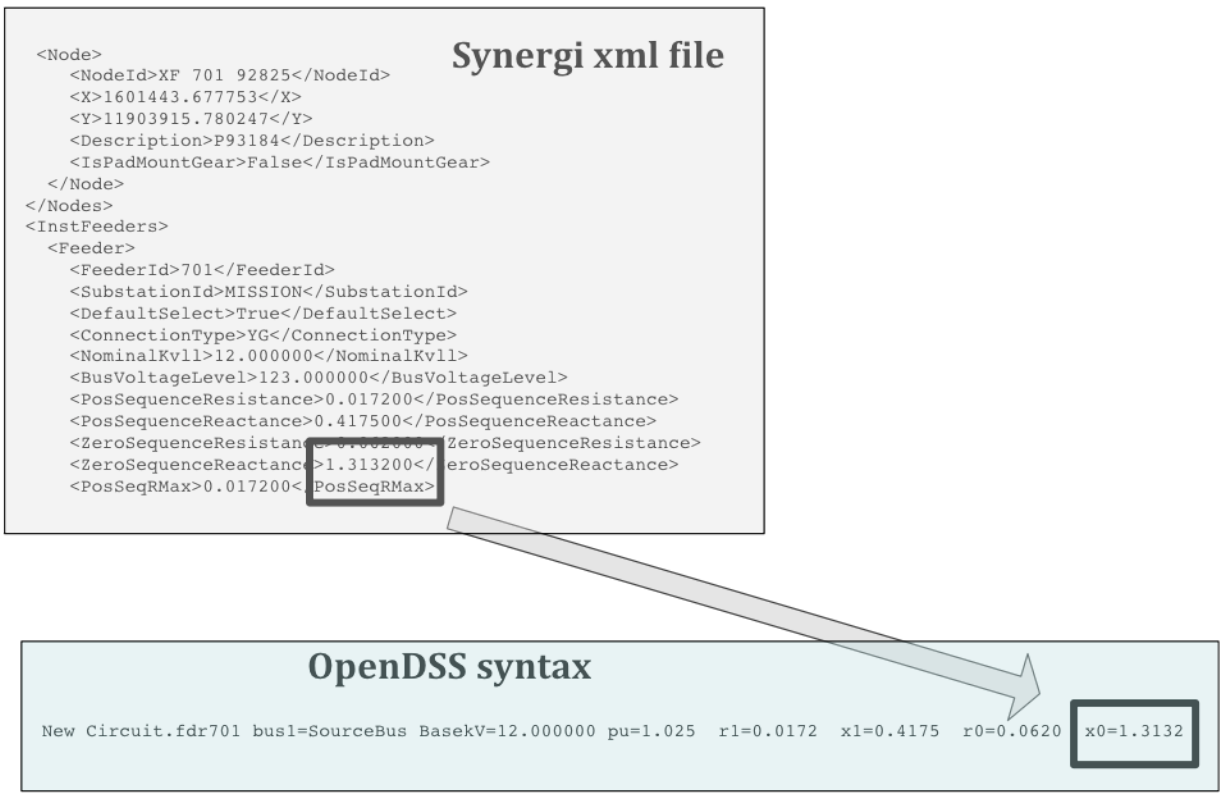

Figure 3. Diagrammatic view of Synergi to OpenDSS model conversion depicting the syntax identification process

The process of converting objects in Synergi to the equivalent objects in the OpenDSS script was not always a direct one-to-one conversion. Object types that exist in Synergi did not always exist in OpenDSS and vice versa. This was also true for the properties of objects. Switches, reclosers, and fuses were not separate objects in OpenDSS. The conversion tool created short, low-impedance lines with switching capabilities for these components.

Finally, the converted OpenDSS script was written to a master file, and separate DSS files for each object type were created. The master file initiated a new circuit that created a voltage source and source bus. The voltage and source impedances were specified based on data from the Synergi model. The master file also redirected to DSS component files containing scripts for the different object types separated into different categories.

2.2 OpenDSS Model Verification

The verification of the OpenDSS model was performed with a goal of achieving the following metrics:

- The feeder topology for the converted model should be similar to the original Synergi model based on visual inspection.
- The differences between the node voltages for the converted model and the original Synergi model should be less than 3%, with most errors being below 0.5%.

Figure 1 and Figure 2 show the feeder topology in Synergi and the converted model in OpenDSS, and it can be seen that the line distances and coordinates were appropriately converted. The subsequent step for verification compared the node voltages obtained from OpenDSS with the Synergi voltages. Figure 4 and Figure 5 show the voltage profiles and voltage errors (obtained at full load) as a function of distance and as a histogram for the respective feeders.

It can be seen that the voltage errors were always less than 3%; in fact all voltage errors were less than 1%, and most errors were less than 0.2%. As is typical, the voltage errors increased towards the end of the feeder.

The sequence impedance at each node looking back towards the feeder head (i.e. the short circuit impedance) was also compared for each feeder, as further validation. Figure 6 and Figure 7 show the sequence impedance errors for K3L and M34, respectively. The maximum error in sequence impedance was below 2.6%, and the number of occurrences of sequence impedance errors over 1.5% was low, as shown in Figure 6 and Figure 7. The sequence impedance errors on the Mikilua feeder were slightly larger than for Kahala because Mikilua is longer, and errors in sequence impedance can accumulate over the length of a feeder.

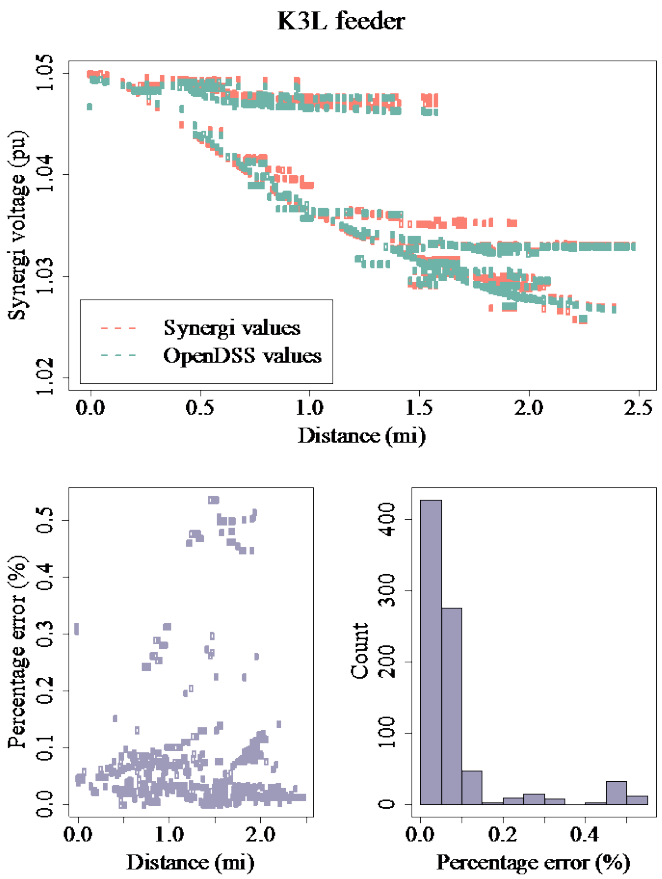

Figure 4. Percentage error of voltage with respect to distance from the feeder head for K3L feeder

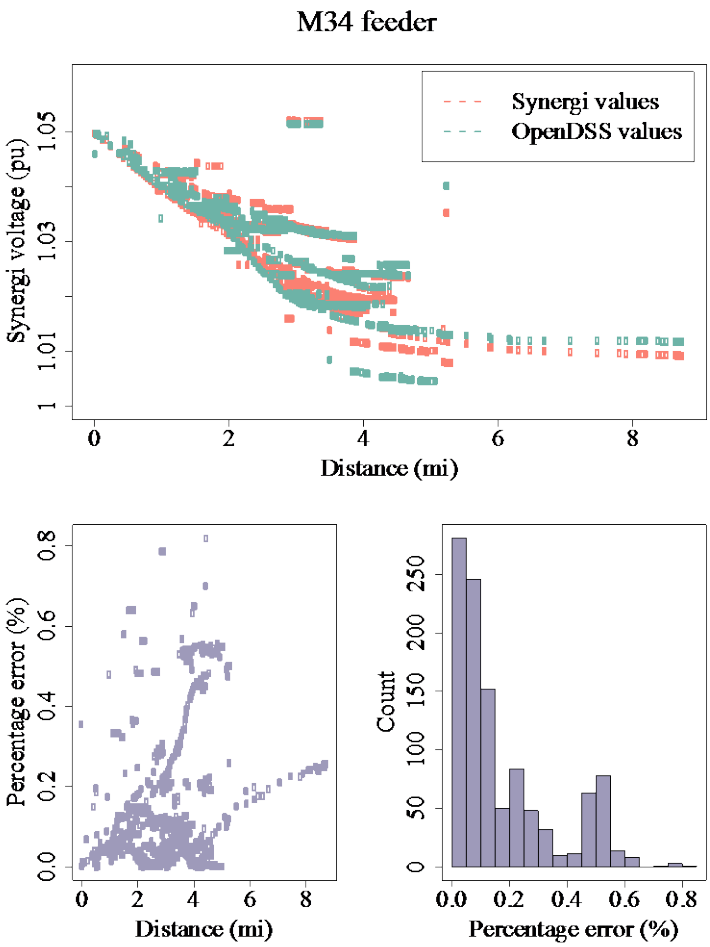

Figure 5. Percentage error of voltage with respect to distance from the feeder head for M34 feeder

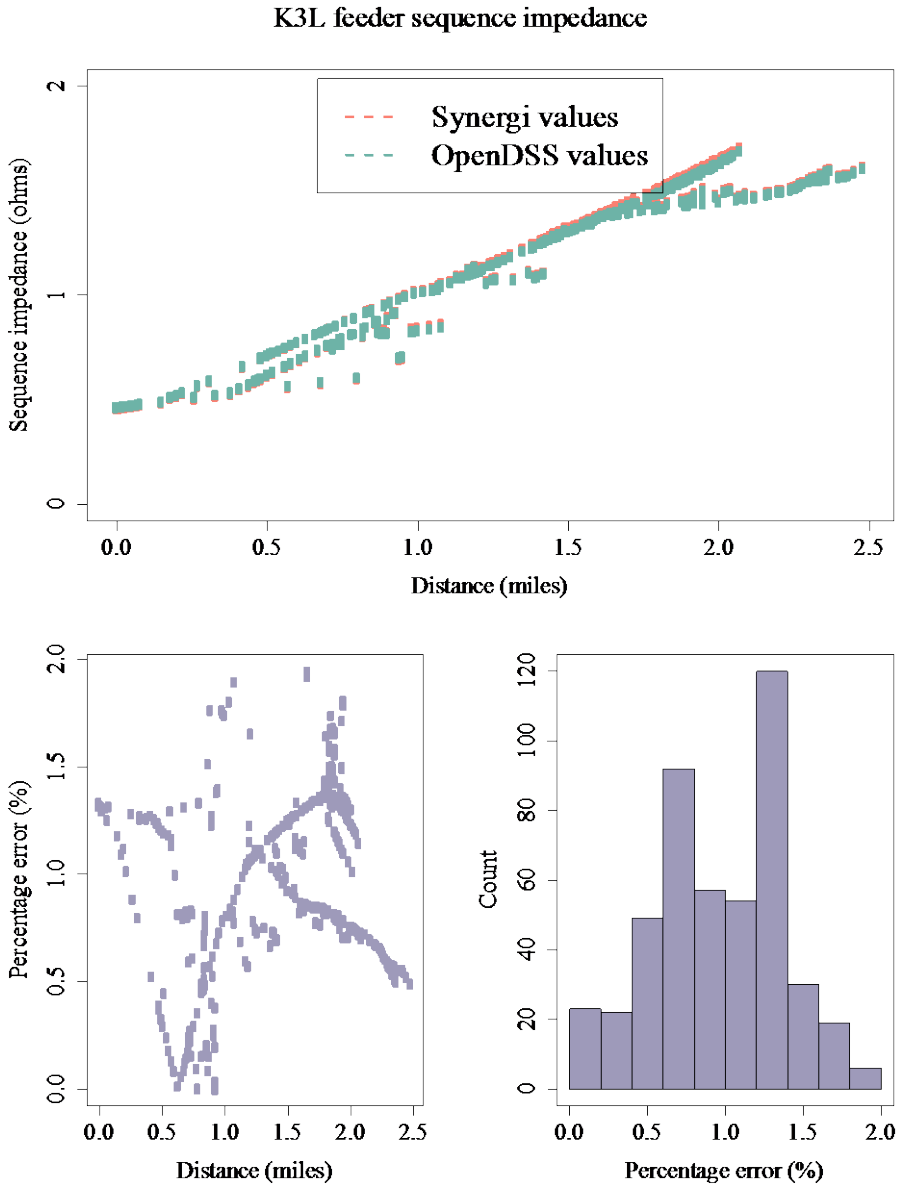

Figure 6. Percentage error of sequence impedances with respect to distance from the feeder head for K3L feeder

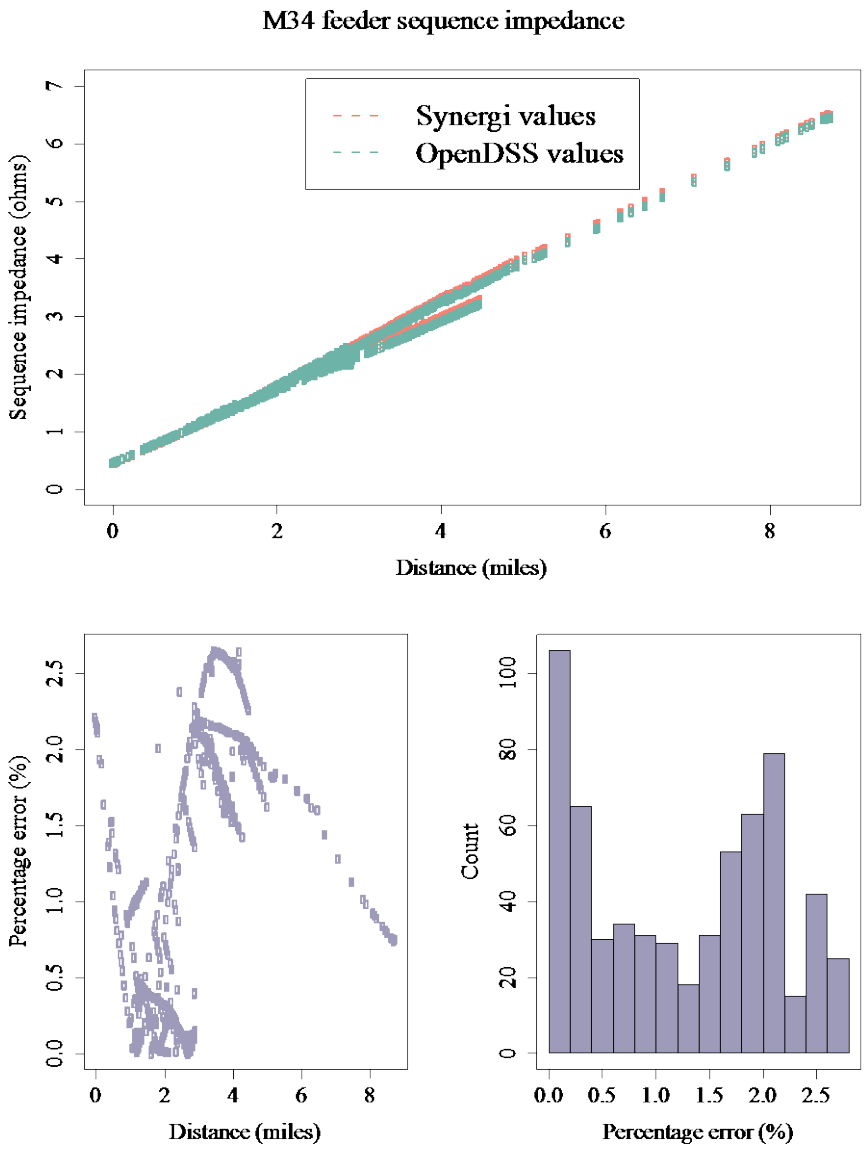

Figure 7. Percentage error of sequence impedances with respect to distance from the feeder head for M34 feeder

2.3 Network Reduction

Since the OPAL-RT real-time simulator that was available for the PHIL experiments cannot solve the entire network model of few thousand nodes in real time within a reasonably fast time step, a reduced order model was developed using a technique described in [4]. The module reduction process is summarized here.

2.3.1 Model Reduction Methodology

The original feeders with around 2000 nodes were reduced to eight nodes using an iterative bottom up approach, where the user chooses the nodes to be retained. Figure 8 shows the nodes that were retained for each feeder as well as the locations of the distribution secondary circuits used for PHIL testing.

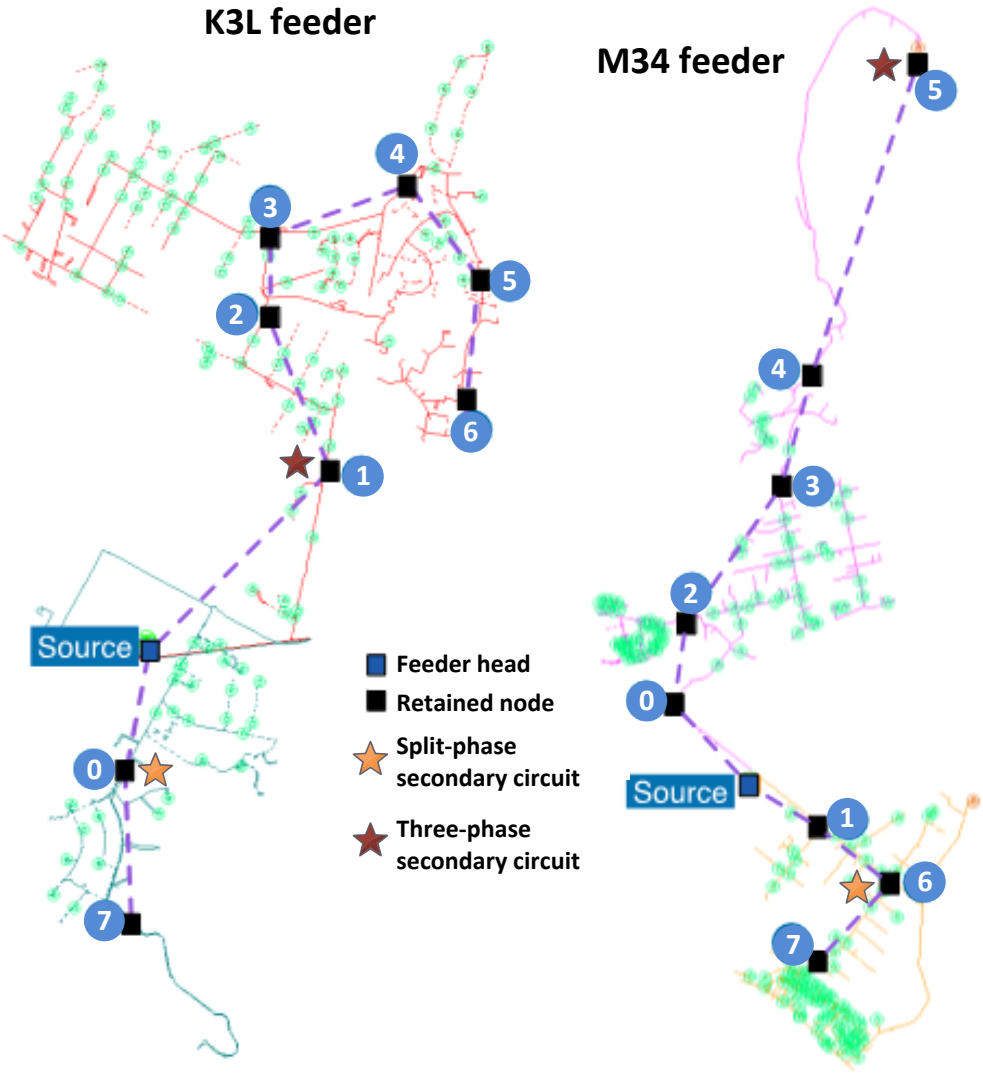

Figure 8. View of the original feeders with the nodes that were retained

The model reduction process ran up to 50,000 Monte-Carlo simulations, varying line-lengths based on a random number generator. The algorithm identified the combination of line-lengths for all lines for which the voltage errors were minimized. Figure 9 outlines the process of network reduction. Additional details of this network reduction technique are described in [4].

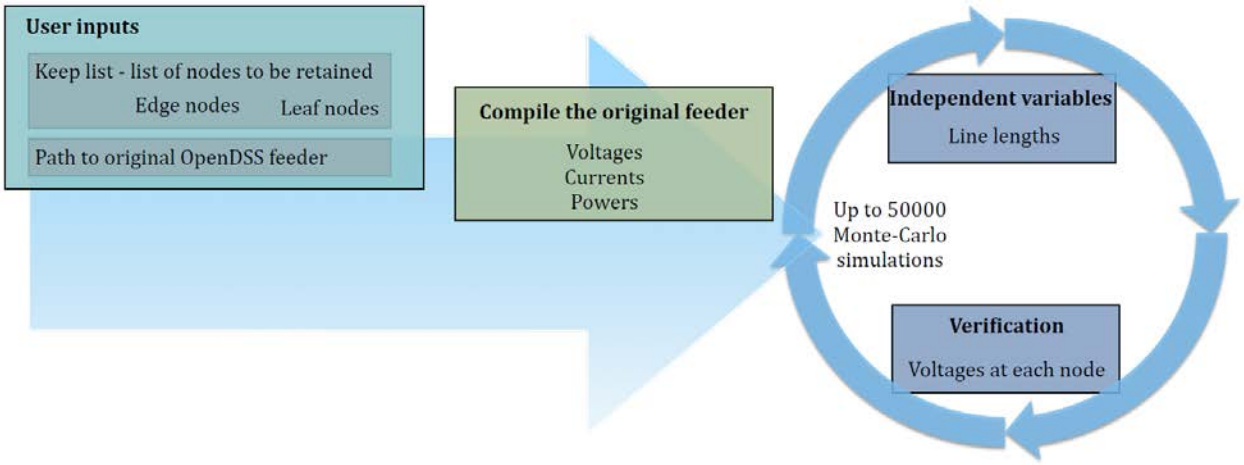

Figure 9. Key steps of the network reduction process

2.3.2 Reduced Order Model Verification

The accuracy of reduced feeder models was verified by comparing the reduced feeder voltages with the original Synergi and OpenDSS models. In order to ensure that the reduced feeder was adequate for all load levels, the voltages for 100%, 75%, and 50% loads were compared. The comparison was done with the load set to the peak load, 75% of peak load and 50% of peak load. The reduced OpenDSS model voltages are compared to the full OpenDSS model voltages at the retained nodes for both feeders in Figure 10 and Figure 11.

Figure 10 and Figure 11 present the averaged three-phase voltages at each retained node for K3L feeder and M34 feeder, respectively. Additionally, the retained node-voltages are compared to the original OpenDSS model. The percentage errors for each retained node at different loading conditions are presented as well. The reduced K3L feeder when compared with the original OpenDSS model had a maximum error of 0.6% across all three load conditions. The reduced M34 feeder when compared with the original OpenDSS model had a maximum error of 0.8% across all three load conditions.

Table 3 and Table 4 tabulate the voltages for each phase and each retained node for K3L feeder and M34 feeder, respectively, for both the reduced OpenDSS models and the original Synergi models. Voltage errors on each phase are tabulated as well. These Synergi comparisons were run only at full load. These tables show a good match between the reduced feeder and the original Synergi model. The reduced K3L feeder when compared with the Synergi model had maximum error of 0.58%. The reduced M34 feeder when compared with the Synergi model had maximum error of 0.55%.

Based on these validations, the accuracy of the model conversion and reduction was deemed adequate for the purposes of this study.

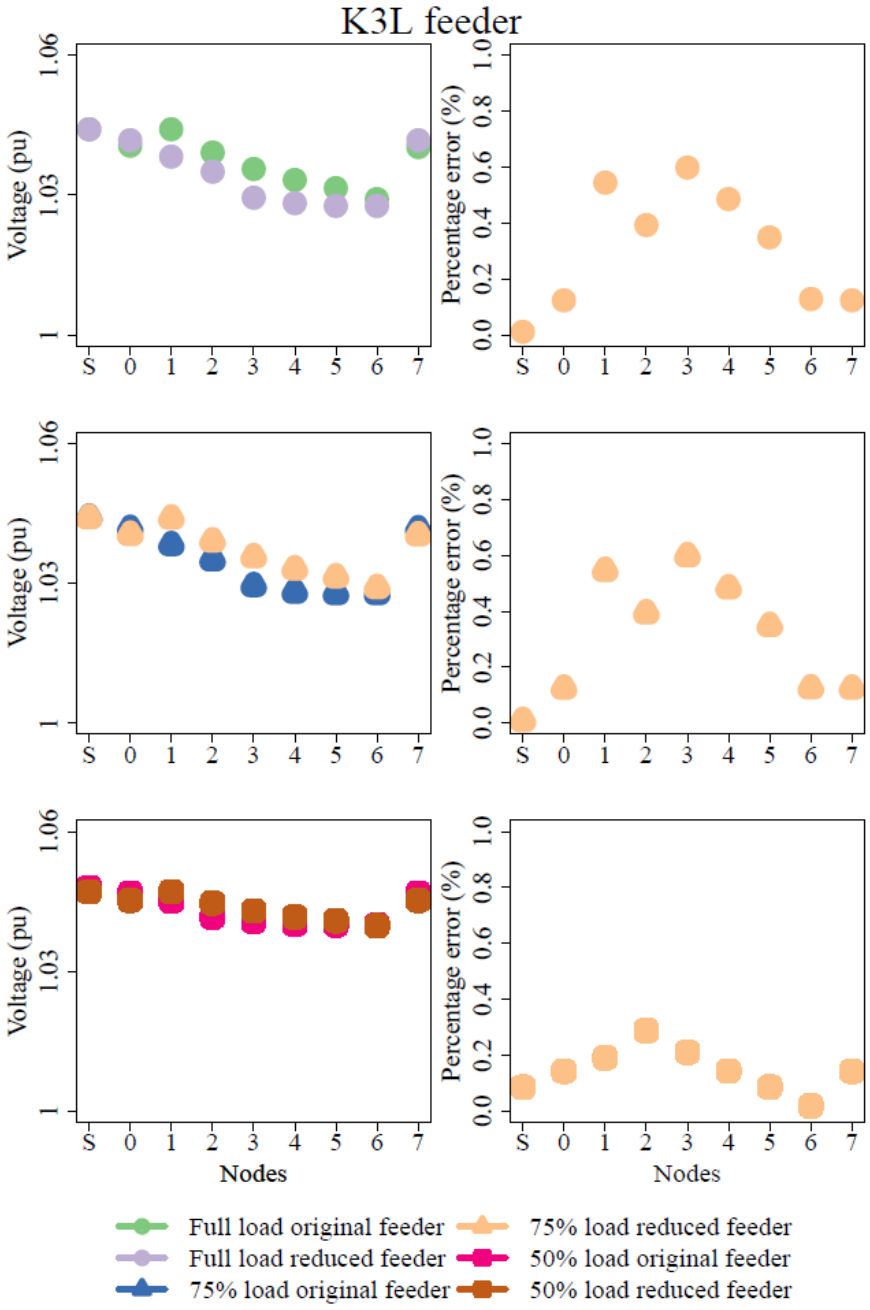

Figure 10. Voltages at the retained nodes for the reduced order OpenDSS model and the original OpenDSS model for K3L feeder

Table 3. Voltage comparison between Synergi model and reduced order OpenDSS model for K3L feeder at full load

Bus	Phase	Synergi voltage [pu]	OpenDSS voltages [pu]	Error [%]
SOURCE	A	1.0476	1.0441	0.335
	B	1.0474	1.0442	0.306
	C	1.0477	1.0458	0.182
NODE 0	A	1.0408	1.0405	0.029
	B	1.0480	1.0420	0.576
	C	1.0479	1.0430	0.470
NODE 1	A	1.0439	1.0440	0.010
	B	1.0423	1.0442	0.182
	C	1.0440	1.0457	0.163
NODE 2	A	1.0368	1.0391	0.226
	B	1.0335	1.0382	0.453
	C	1.0379	1.0413	0.327
NODE 3	A	1.0349	1.0357	0.077
	B	1.0315	1.0346	0.300
	C	1.0343	1.0389	0.443
NODE 4	A	1.0335	1.0331	0.039
	B	1.0305	1.0319	0.136
	C	1.0355	1.0371	0.154
NODE 5	A	1.0333	1.0314	0.179
	B	1.0303	1.0311	0.075
	C	1.0356	1.0356	0.002
NODE 6	A	1.0333	1.0291	0.403
	B	1.0302	1.0297	0.049
	C	1.0355	1.0362	0.068
NODE 7	A	1.0476	1.0404	0.692
	B	1.0479	1.0419	0.576
	C	1.0478	1.0429	0.465

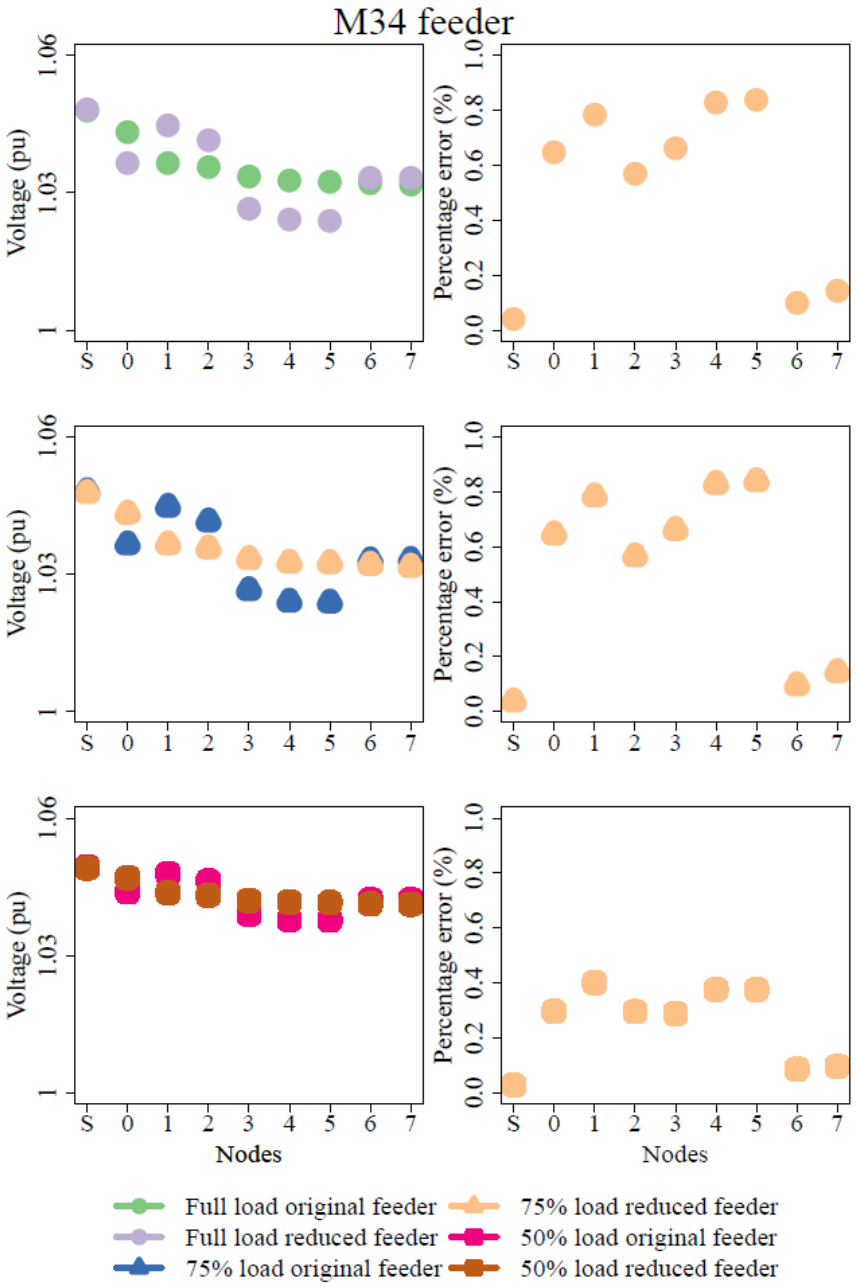

Figure 11. Voltages at the retained nodes for the reduced order OpenDSS model and the original OpenDSS model for M34 feeder

Table 4. Voltage comparison between Synergi model and reduced order OpenDSS model for M34 feeder at full load

Bus	Phase	Synergi voltage [pu]	OpenDSS voltages [pu]	Error [%]
SOURCE	A	1.048	1.048	0.00
	B	1.049	1.047	0.15
	C	1.042	1.042	0.03
NODE 0	A	1.042	1.037	0.49
	B	1.051	1.046	0.42
	C	1.010	1.009	0.02
NODE 1	A	1.044	1.043	0.05
	B	1.048	1.047	0.09
	C	1.033	1.030	0.31
NODE 2	A	1.041	1.036	0.48
	B	1.037	1.035	0.14
	C	1.032	1.030	0.17
NODE 3	A	1.037	1.033	0.32
	B	1.047	1.044	0.28
	C	0.999	0.997	0.20
NODE 4	A	1.033	1.033	0.01
	B	1.045	1.043	0.15
	C	0.995	0.995	0.04
NODE 5	A	1.038	1.033	0.50
	B	1.049	1.043	0.55
	C	0.998	0.995	0.32
NODE 6	A	1.037	1.032	0.45
	B	1.033	1.032	0.11
	C	1.027	1.026	0.05
NODE 7	A	1.036	1.032	0.39
	B	1.035	1.030	0.42
	C	1.032	1.026	0.53

2.4 PV Generator Node Identification

Residential PV generators are typically distributed along feeder line. During the process of network reduction described above, there is a need to identify the nearest retained node to which each PV generator should be connected in the reduced feeder. As a part of this task, a methodology was developed to identify the nearest retained node to which each PV generator needs to be connected. The implemented algorithm chose either the nearest upstream or downstream retained node (except feeder head), as described below.

Figure 12 presents the PV generator node identification process. A visual representation is provided in which a PV generator in between two retained nodes was assigned to either the upstream or downstream-retained node. The retained node to which each PV generator is connected is determined using an algorithm that adjusts the power output of each PV generator individually and selects the retained node whose voltage changes most with changes in PV power. This algorithm involved running as many simulations as the number of PV generators, with each simulation creating a step raise in PV generation. After each simulation the PV generator was assigned to the retained node with maximum change in voltage and current. The output of the algorithm was manually spot-checked to ensure that it was selecting nodes accurately.

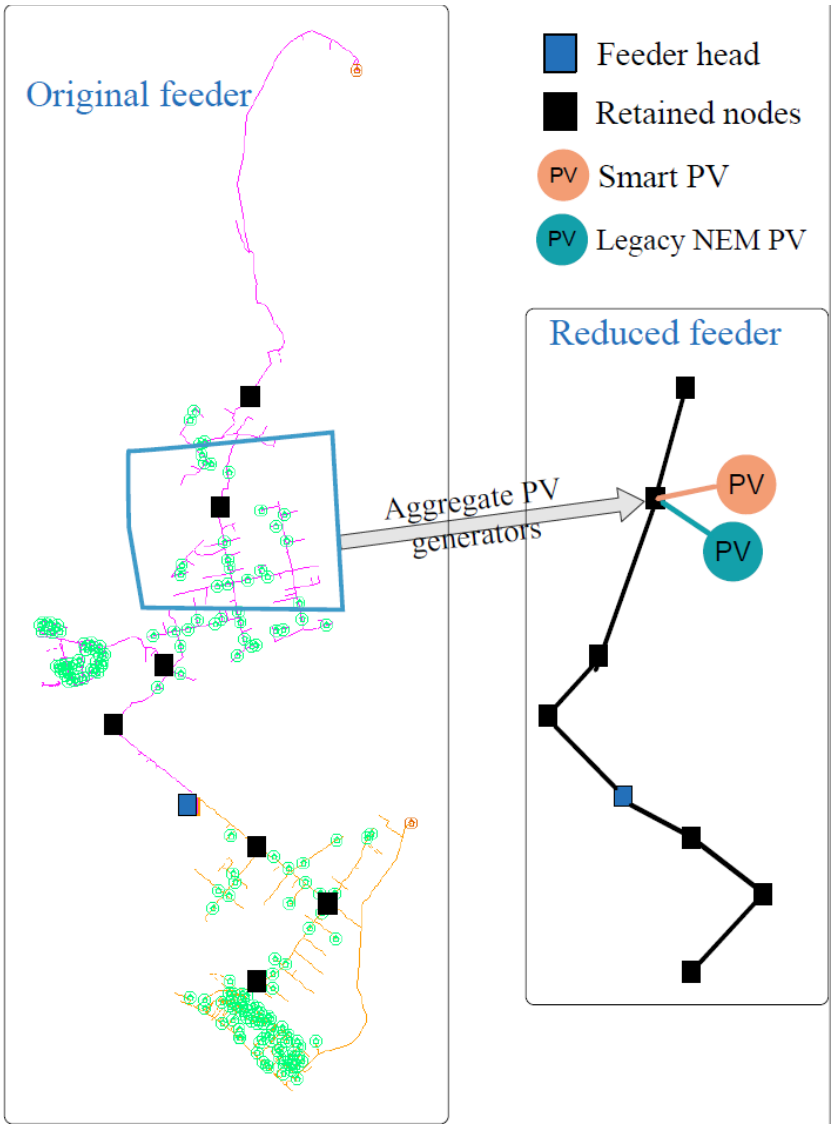

Figure 12. Conceptual representation of PV generator node identification methodology

The process of aggregating PV systems introduces some assumptions and simplifications. In a real distribution feeder, each PV system experiences different irradiance and temperature conditions. When aggregated, the diversity of irradiance between systems disappears. In addition, each PV system on a real feeder sees a slightly different voltage, which leads to different behavior, especially for voltage-related functions such as voltage ride-through and volt-watt control. In contrast, all PV systems aggregated into a single location experience the same voltage. Thus, the aggregated PV systems only approximate the real-world behavior of the individual systems; they do not capture it exactly.

3 Baseline Testing

A series of baseline tests were run on five different commercially available inverters that are commonly used in Hawaiian Electric's operating territory. The purpose of these baseline tests was to evaluate each inverter manufacturer's ability to meet new grid support function (GSF) requirements, and also to use the test results as inputs for inverter models that were subsequently integrated with the real-time feeder models.

3.1 Test Descriptions and Setup

All test procedures were based on a combination of requirements under Hawaiian Electric Rule No. 14, Paragraph H, *Interconnection of Distributed Generating Facilities with the Company's Distribution* System (Rule 14H), and a draft version of UL 1741 SA, which was officially published on September 7, 2016, several months after the baseline tests were completed [1], [10]. Where necessary, the test procedures were modified to meet time requirements of the project and/or the capabilities of the inverters under test with a goal of demonstrating a representative sample of each inverter's GSF capabilities. All test plans were agreed upon with Hawaiian Electric prior to execution. The seven functions of interest for baseline testing included voltage ride-through (VRT), frequency ride-through (FRT), fixed power factor operation (FPF), soft start reconnection, ramp rate control, volt-var control (VVC), and volt-watt control (VWC). An additional subset of tests that included a combination of VVC with VWC was run for some inverters. Details of each test procedure and results are provided below.

The inverters of interest were selected from products commonly used on the Hawaiian Island grid, and from manufacturers who were willing to participate in this study, following a process described in the introduction. Inverter types included microinverters, a split-phase string inverter, and a three-phase commercial model. A summary of basic test inverter operating parameters is shown in Table 5. Note that Inverter 1 is an assembly of 120 VAC microinverters connected line to neutral, with half connected to each line.

Table 5. Basic specifications of test inverters

Inverter	Nominal Power	Voltage Configuration	Phase Configuration
1	16 x 230W = 3.68 kW	120/240 VAC	Split Phase
2	16 x 280 W = 4.48 kW	120/240 VAC	Split Phase
3	6.0 kW	240 VAC	Single Phase*
4	20.0 kW	277/480 VAC	Three Phase
5	14 x 250 W = 3.50 kW	120/240 VAC	Split Phase

***Inverter 3 can be configured for split phase or single phase operation; the latter was used for the purposes of this study.**

All inverters were connected to a bi-directional AC voltage source, which served as the grid simulator for all tests. The AC voltage source for this study was the MX-45 from Ametek, with three independently controllable phases, rated for a total power of 45 kVA.

Each inverter was also powered with an appropriately sized PV simulator from the Ametek TerraSAS family. These PV simulators can be programmed for specific PV panel characteristics, and also can simulate programmable dynamic events such as changes in irradiance and temperature. The PV simulators have high slew rate control, in order to simulate PV response to rapidly changing conditions, such as maximum power point tracking perturbations. All microinverters (Inverters 1, 2 and 5) were powered with PV simulators rated at either 80 VDC / 10.5 A or 60 VDC / 14 A. Inverter 3 was powered with a 600 VDC / 25 A supply. Inverter 4 was power with a 1000 VDC / 40 A supply.

All waveform data was captured using a Yokogawa DL850 oscilloscope at minimum sampling rates of 20 kHz, and power measurements were recorded with a Yokogawa WT1800 power analyzer at 50 ms or 100 ms update rates (10 or 20 Hz). Currents were measured with Yokogawa 701930 or 701931 current probes (10 mV/A), DC voltages were measured with Yokogawa 700924 differential voltage probe, and AC voltage was directly inputs to the data acquisition cards.

3.2 Voltage Ride Through Tests

3.2.1 Voltage Ride Through Procedures

All inverters were programmed to operate under the voltage trip limits specified in Rule 14H Table 4a.g and summarized in Table 6. Where possible, inverters were programmed with a configurable Hawaii profile that already included these settings as well as a 0.95 power factor setting. If necessary, these trip points were manually programmed.

Table 6. Voltage ride through magnitude and durations according to Rule 14H

Operating Region	Voltage Range (% Nominal)	Ride Through Until	Maximum Trip Time
Overvoltage 2 (OVR2)	V > 120	No Ride Through	0.16 sec
Overvoltage 1 (OVR1)	120 ≥ V > 110	0.92 sec	1.0 sec
Normal Operation (NORH, NORL)	110 ≥ V ≥ 88	Indefinite	Indefinite
Undervoltage 1 (UVR1)	88 > V ≥ 70	20 sec	21 sec
Undervoltage 2 (UVR2)	70 > V ≥ 50	10-20 sec	11-21 sec
Undervoltage 3 (UVR3)	V < 50	No Ride Through	0.50 sec

Each of the five ride-through regions was tested by programming a voltage magnitude profile with rise, fall and hold times and magnitudes defined by UL1741 SA. Successful ride-through was demonstrated in the OVR1, UVR1 and UVR2 regions; trip times were tested in the OVR2 and UVR3 regions. Two different ride-through durations were tested in the UVR2 region, both at

the 10 second and 20 second limits of the adjustable range. All tests were repeated at 100% and 20% inverter output power, creating 12 test cases per inverter. Inverter 5 was a legacy model not capable of all GSFs, and did not have a programmable UVR2 setting, so UVR2 tests were not run on this model.

Note that the UL 1741 SA VRT test procedure intentionally creates a difficult test for the inverter to ride through by maximizing the size of the voltage transient. HVRT tests are run by starting near the bottom of the normal operating region (i.e. just above 88%) and quickly raising the voltage above the threshold of the test, with a rise time of "less than or equal to the larger of 1 cycle or 1% of the ride-through region duration." Just before the overvoltage ride-through time window has passed, the voltage is returned to just above 88% with a fall time equal to the rise time. The LVRT test is run in a similar manner, starting near the top of the normal operating region (just below 110%). Thus the VRT tests confirm the ability of the inverter to not only ride through the abnormal voltage condition for the programmed time, but also to tolerate very fast changes in voltage as may be seen in the field during remote fault events.

Per UL 1741 SA, the exact voltage profile used in VRT tests depends on the manufacturer's stated accuracy of voltage. The voltage profiles approach each boundary within 1.5·(manufacturer's stated accuracy); for details please see UL 1741 SA [1].

3.2.2 Voltage Ride-Through Results

All inverter manufacturers successfully passed the ride-through tests completed in this study. A representative set of time series plots is shown in Figure 13 for Inverter 2 at 100% output power for the OVR1 and UVR2 (20 second ride-through) test cases. Note that all inverters curtailed power to some degree for low voltage ride-through events due to internal current limits on power electronics. The amount of power curtailment varied for each inverter type.

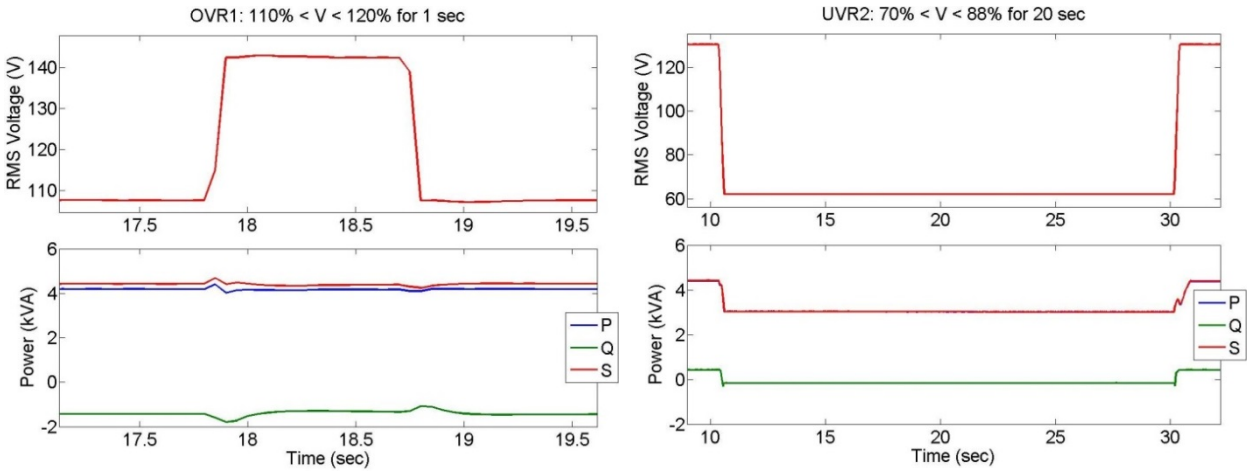

Figure 13. OVR1 (left) and UVR2 (right) test cases for Inverter 2 at 100% output power

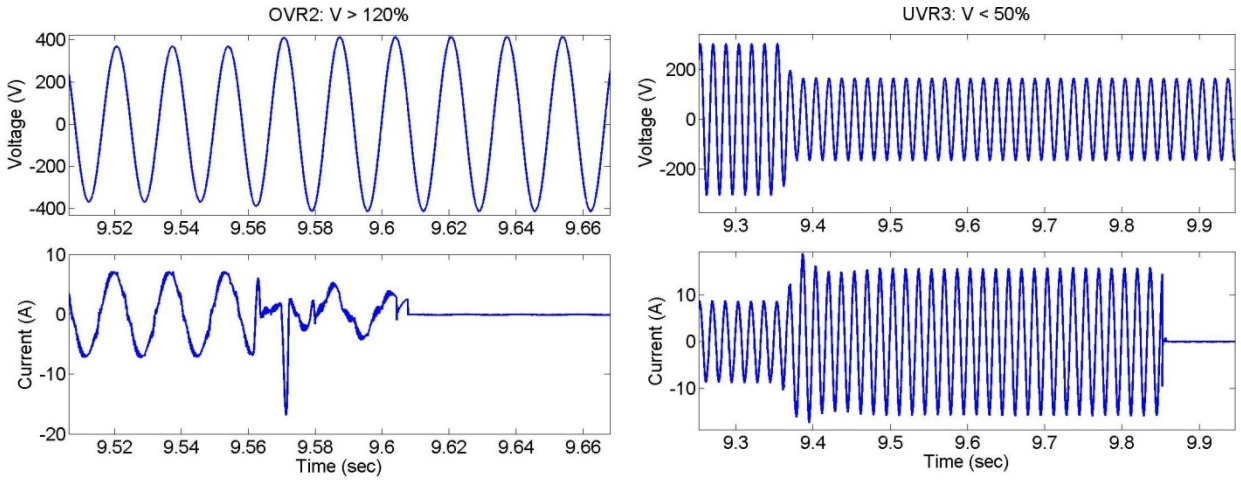

Figure 14. OVR2 (left) and UVR3 (right) test cases for Inverter 3 at 20% output power

For trip tests – OVR2 and UVR3 – all test inverters successfully tripped within the required trip times (160 ms and 500 ms, respectively). Waveform plots of an overvoltage and undervoltage trip event for Inverter 3 at 20% output power are shown in Figure 14. A summary table of all VRT test results is shown in Table 7. All test cases where the test inverter successfully rode through are marked as "PASS", and the trip times are given for trip tests. Trip times are measured from the time that the last voltage peak was beyond the trip threshold until output current measured zero.

Table 7. Voltage ride through test results summary

VRT Test	Output Power (%)	Expected Result	Inverter (trip times in milliseconds)				
			1	2	3	4	5
OVR2	100	Trip ≤ 160 ms	158	22	13	157	105
OVR2	20	Trip ≤ 160 ms	156	105	37	160	105
OVR1	100	Ride Through	PASS	PASS	PASS	PASS	PASS
OVR1	20	Ride Through	PASS	PASS	PASS	PASS	PASS
UVR1	100	Ride Through	PASS	PASS	PASS	PASS	PASS
UVR1	20	Ride Through	PASS	PASS	PASS	PASS	PASS
UVR2 (10 sec)	100	Ride Through	PASS	PASS	PASS	PASS	N/A
UVR2 (10 sec)	20	Ride Through	PASS	PASS	PASS	PASS	N/A
UVR2 (20 sec)	100	Ride Through	PASS	PASS	PASS	PASS	N/A
UVR2 (20 sec)	20	Ride Through	PASS	PASS	PASS	PASS	N/A
UVR3	100	Trip ≤ 500 ms	500	288	478	500	272
UVR3	20	Trip ≤ 500 ms	500	296	478	500	279

For the UVR3 tests for both Inverters 1 and 4, the measured trip times were very close to the 500 ms limit. If manufacturer stated accuracy (MSA) of voltage measurements is taken in to account to determine when a voltage threshold has been exceeded, both inverters easily trip within the 500 ms limit.

Inverter 4 had some nuisance trips due to the aggressive ramp rate of the OVR1 tests; the test procedures called for a ramp from 89.5% of nominal voltage to 118.5% of nominal in a single AC cycle. The inverter manufacturer was unaware of the aggressive ramp rates called for in the UL1741 SA draft document at the time the testing commenced. The product was able to pass the OVR1 tests with a ramp time of 100 ms instead of 16 ms. The inverter manufacturer subsequently provided a firmware modification, and the product successfully passed the original test with the faster ramp rate.

3.3 Frequency Ride-Through Tests

3.3.1 Frequency Ride-Through Procedures

Similar to VRT testing, all inverters were programmed to operate under the frequency trip limits specified in Rule 14H Table 4a.g and summarized in Table 8. Where possible, inverters were programmed with a configurable Hawai‘i profile that already included these settings as well as 0.95 power factor setting. If necessary, these trip points were manually programmed.

Table 8. Frequency ride-through magnitude and durations per Rule 14H

Operating Region	Frequency Range (Hz)	Ride Through Until	Maximum Trip Time
Overfrequency 2 (OFR2)	f > 64.0 or 65.0	No Ride Through	0.16 sec
Overfrequency 1 (OFR1)	64.0 ≥ f > 63.0	20 sec	21 sec
Normal Operation (NORH, NORL)	63.0 ≥ f ≥ 57.0	Indefinite	Indefinite
Underfrequency 1 (UFR1)	57.0 > f ≥ 56.0	20 sec	21 sec
Underfrequency 2 (UFR2)	56.0 > f	No Ride Through	0.16 sec

Each of the ride-through regions was tested by programming a frequency magnitude profile with rise, fall, and hold times and magnitudes defined by UL 1741 SA. Rise and fall times were selected to be 2 Hz/sec, which is within the range specified in UL 1741 SA and significantly steeper than expected and measured rates of change of frequency in worst-case O‘ahu events. Successful ride-through was demonstrated in the OFR1 and UFR1 regions; trip times were tested in the OFR2 and UFR2 regions. Two different ride-through magnitudes were tested in the UFR1 region, both at the 63.0 Hz and 64.0 Hz limits of the adjustable range. Additionally, the NORH and NORL regions were tested by operating the inverters continuously for several minutes at a frequency within 1.5x the MSA of frequency at both the high and low limits. All ride-through tests were repeated at 100% and 20% inverter output power, creating 12 test cases per inverter.

Inverter 5 was a legacy model not capable of programing the OFR1 setting beyond 64.0 Hz, so only ten tests were run on this model.

As with VRT tests, it is worth noting that the UL 1741 SA FRT test procedure intentionally creates a difficult test for the inverter to ride through by maximizing the size of the frequency transient. HFRT tests are run by starting near the bottom of the normal operating region (i.e. just above 57 Hz) and quickly raising the frequency above the threshold of the test, with a rise time of at least 1 Hz per second. After the overfrequency window has passed, the frequency is then returned to just above 57 Hz with a fall time equal to the rise time. The LFRT test is run in a similar manner, starting near the top of the normal operating region (just below 63 Hz). Thus the VRT tests confirm the ability of the DER to not only ride through the abnormal frequency condition for the programmed time, but also to tolerate very fast changes in frequency as may be seen in the field during contingency events many years in the future.

3.3.2 Frequency Ride-Through Results

All inverter manufacturers successfully passed the ride-through tests completed in this study. A representative set of time series plots is shown in Figure 15 for Inverter 4 at 100% output power for the OFR1 and UFR1 test cases. Additionally, all steady state tests passed as expected.

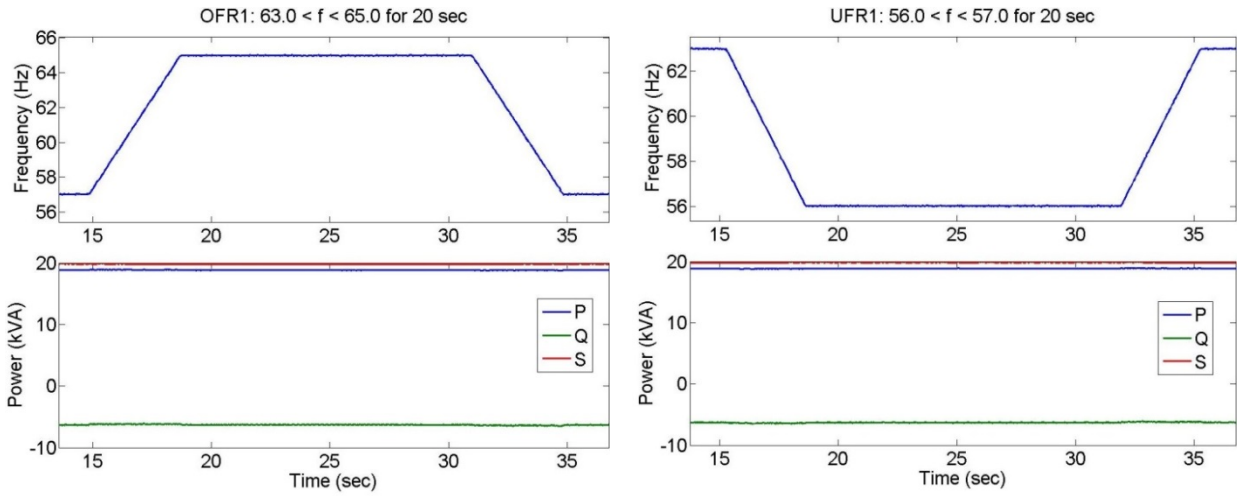

Figure 15. OFR1 (left) and UFR1 (right) test cases for Inverter 4 at 100% output power

For trip tests – OFR2 and LFR2 – all test inverters successfully tripped within the required trip time of 160 ms. Waveform plots of an overfrequency and underfrequency trip event for Inverter 5 at 20% output power are shown in Figure 16. Note that the measured frequency was post-processed using Matlab/Simulink [11] in order to capture the rapid trip times using a cycle by cycle computation of frequency. The power analyzer frequency calculation was to slow to be used for evaluating these test results.

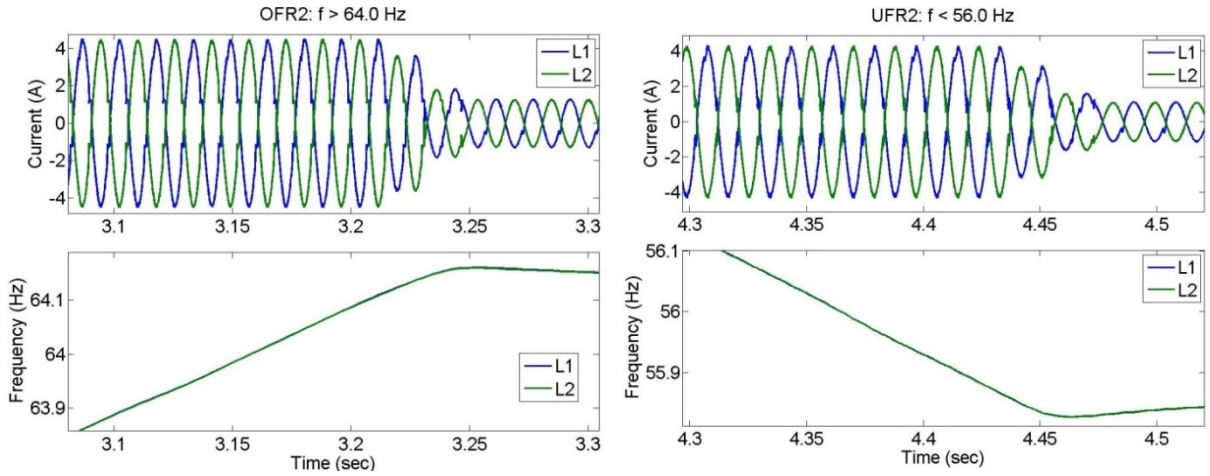

Figure 16. OFR2 (left) and UFR3 (right) test cases for Inverter 5 at 20% output power

A summary table of all FRT test results is shown in Table 9. All test cases where the test inverter successfully rode through are marked as "PASS", and the trip times are given for trip tests.

Table 9. Frequency ride-through test result summary

VRT Test	Output Power (%)	Expected Result	Inverter Trip Times (milliseconds)				
			1	2	3	4	5
OFR2	100	Trip ≤ 160 ms	71*	150	103	155	93
OFR2	20	Trip ≤ 160 ms	87*	131	108	150	92
OFR1 (63 Hz)	100	Ride Through	PASS	PASS	PASS	PASS	PASS
OFR1 (63 Hz)	20	Ride Through	PASS	PASS	PASS	PASS	PASS
OFR1 (64 Hz)	100	Ride Through	PASS	PASS	PASS	PASS	N/A
OFR1 (64 Hz)	20	Ride Through	PASS	PASS	PASS	PASS	N/A
UFR1	100	Ride Through	PASS	PASS	PASS	PASS	PASS
UFR1	20	Ride Through	PASS	PASS	PASS	PASS	PASS
UFR2	100	Trip ≤ 160 ms	33*	138	116	160	125
UFR2	20	Trip ≤ 160 ms	116*	140	119	159*	106
NORH	100	Run Continuous	PASS	PASS	PASS	PASS	PASS
NORL	100	Run Continuous	PASS	PASS	PASS	PASS	PASS

***See discussion below**

For the trip tests for both Inverters 1 and 4, the measured trip times were close to or exceeded the 160 ms limit if the manufacturer's stated accuracy (MSA) of frequency measurements is not taken into account to determine when a frequency threshold had been exceeded. Once MSA of frequency is accounted for, the measured trip time is easily within the 160 ms limit, as shown in Table 9.

Inverter 1 and Inverter 4 experienced nuisance trips due to the steep ramp rate of the FRT tests. Both inverter manufacturers were unaware of the steep ramp rates called for in the UL 1741 SA draft document at the time the testing commenced. Inverter 1 passed the tests with a frequency ramp rate of 0.75 Hz/sec rather than 2.0 Hz/sec, and Inverter 4 passed all tests with some anti-islanding parameters adjusted for some test cases. The manufacturer of Inverter 4 was made aware that adjustments to its firmware may be needed to pass UL 1741 SA (which readers will recall was not publicly available at the time of testing). The manufacturer of Inverter 1 made firmware adjustments that subsequently resulted in the avoidance of tripping on high rates of change of frequency prior to the PHIL tests, and demonstrated successful ride-through of worst-case O‘ahu events in those tests.

3.4 Fixed Power Factor Tests

Two different power factor values were tested at four different power levels for each inverter: 0.90 and 0.95 power factor were tested at 10%, 20%, 60% and 100% of rated output power for each inverter. All inverters were tested in pure FPF mode, not in what UL 1741 SA calls “fixed power factor mode with active power priority (PFAP)”, because Rule 14H calls for FPF, not PFAP. The fundamental component of power factor was measured, and the average power factor over approximately one minute of data acquisition was used to compute the recorded values. Using the generator sign convention, a negative power factor was considered absorbing VARs, with current leading voltage (reduces voltage at the point of interconnection). Each inverter was programmed either through a manual process specified for the manufacturer, or by using a preset Hawaii 14H profile for the 0.95 power factor cases. Inverter 5 was a legacy inverter and could only operate at unity power factor, so no results are reported.

When inverters are tested for certification purposes (which is not the goal here), the lowest power at which power factor is tested is specified by the manufacturer, and it must comply with the SRD for the utility in question. Many inverter manufacturers are expected to specify a range of 20% to 100% of rated power. The tests at 10% power were conducted to investigate the behavior of the inverters below the range where the accuracy of FPF is guaranteed.

A summary of all test results is show in Table 10, and representative plots of power measurements during two different power factor tests for Inverter 2 and Inverter 3 are shown in Figure 17. The largest errors occurred at the 10% power level, but at power levels ≥20%, most inverters had error <0.5% of the expected value; the maximum error at these power levels was 1.3%. Finite line impedances may have contributed to some of the error and offsets.

Table 10. Fixed power factor test result summary

Power Factor	Output Power (% of Rated)	Inverter Number and Power Factor			
		1	2	3	4
0.90	10	0.890	0.905	0.897	0.931
0.90	20	0.887	0.901	0.905	0.900
0.90	60	0.886	0.898	0.905	0.899
0.90	100	0.890	0.897	0.904	0.899
0.95	10	0.945	0.954	0.942	0.982
0.95	20	0.945	0.951	0.951	0.950
0.95	60	0.946	0.949	0.953	0.948
0.95	100	0.944	0.948	0.952	0.949

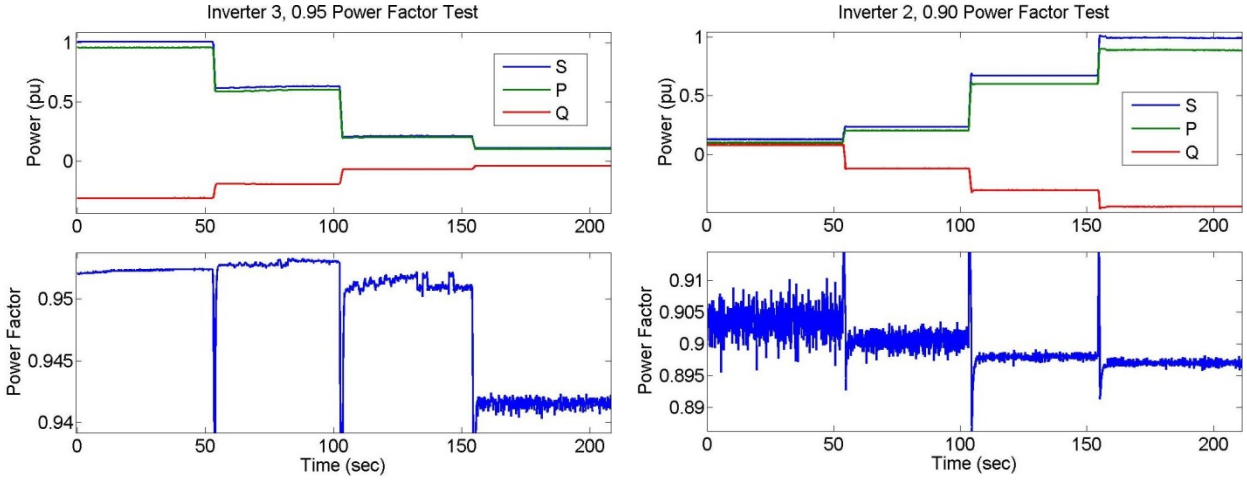

Figure 17. Inverter 3 output power at 0.95 power factor (left) and Inverter 2 output power at 0.90 power factor (right)

3.5 Normal Ramp Rate Tests

The purpose of ramp rate testing was to verify that the rate of change of output power could be controlled for rapid upward changes in input power – typically due to irradiance changes. PV inverters without stored or reserved energy cannot typically control downward power ramp rates, so those were not tested. Three different ramp rates were tested for each inverter where this function was programmable, and the available power on the DC input was stepped from ~10% of rated power to >100% of rated power. Each inverter was tested at its default or fastest ramp rate, its slowest stated ramp rate, and 0.33%/sec (ramp to full power in 300 sec). If the 0.33%/sec fell outside the slowest programmable ramp rate, the average value of the fastest and slowest rates was tested. Inverter 5 was a legacy inverter that did not have this function available, and Inverter 3 likewise did not have this function available to program; a baseline test case was recorded for each of these inverters to record its default performance.

The results of the ramp rate tests are summarized in Table 11. Test results are only shown in cases where the setting was tested for the particular inverter, which was dependent on the stated range of ramp times. "Default" refers to test cases where the inverter was programmed to its maximum ramp time and/or default value if not programmable. In cases where a range of ramp times is reported, it is subjective as to when the ramp time starts and stops. Some manufacturers have a non-linear response time, and it is not clear at which point on the tail of the curve the ramp time is complete. Two examples of such test results for Inverter 1 are shown in Figure 18 for ramp rates of 5%/second and 0.33%/second. As published, UL 1741 SA states that the ramp rate test criteria apply between 10% and 90% of rated power, so the smaller of the two numbers listed for Inverter 1 applies. However, this test UL criterion has changed from the draft that existed at the time of testing.

Table 11. Normal ramp rate test results summary

	Inverter Number				
	1	**2**	**3**	**4**	**5**
Manufacturer stated range of ramp times (%/sec)	0.33 – 25.0	0.08 – 1.00	N/A	0.10 - Infinite	N/A
Expected Ramp Time (sec)	**Measured Ramp Time (sec)**				
Default / Fastest	5.3 – 16.4	1.0	1.0	1.0	2.1
270	239 – 302	286	N/A	267	N/A
18.0	15.9 – 27.8	N/A	N/A	N/A	N/A
90.0	76.6 – 101.3	N/A	N/A	N/A	N/A
900	N/A	N/A	N/A	895	N/A
1125	N/A	1215	N/A	N/A	N/A

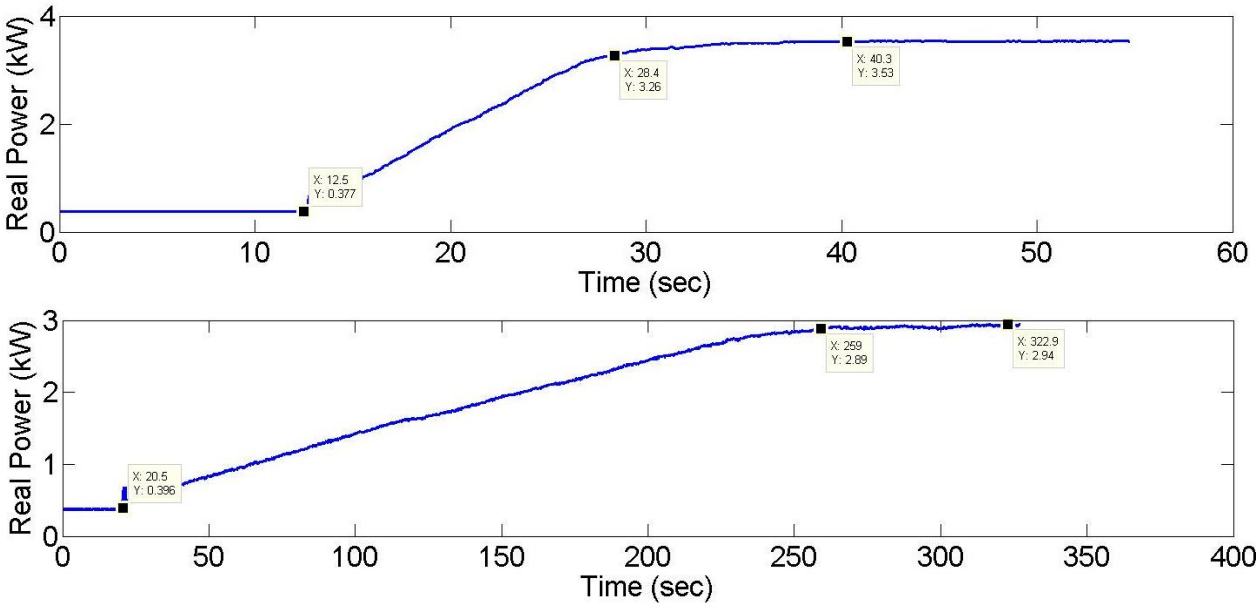

Figure 18. Inverter 1 output power for ramp rates of 5%/sec (top) and 0.33%/sec (bottom); data tips show how different ramp times were calculated in Table 11.

Notably, two of the five inverters did not implement ramp rate control at all, and for those that did, the ranges of adjustability varied significantly. This may be because there has been little demand for ramp rate control outside Hawai‘i. However, because UL 1741 SA contains a test for ramp rate control and does not specify it as an optional function, more inverters are expected to implement it in the near future.

3.6 Soft Start Tests

Similar to the ramp rate tests, the purpose of soft start testing was to verify that the rate of change of output power could be controlled during the startup sequence. Inverters are required to remain disconnected from the utility for at least 300 seconds following a trip due to an abnormal grid condition (beyond ride-through boundaries). These tests verified that at least 300 seconds passed before restart and then tested the actual power ramp time for each inverter. Three different ramp rates were tested for each inverter, and a grid event was induced on the grid simulator in order to force the inverter to trip. Each inverter was tested at its default or fastest ramp rate, the slowest stated ramp rate, or 0.33%/sec (ramp to full power in 300 sec). If the 0.33%/sec fell outside the slowest programmable ramp rate, the average value of the fastest and slowest rates was tested. Inverter 5 was a legacy inverter that did not have this function available; a baseline test case was recorded for this inverter to record its default performance.

The results of the ramp rate tests are summarized in Table 12. Test results are only shown in cases where the setting was tested for the particular inverter, which was dependent on the stated range of ramp times. “Default” refers to test cases where the inverter was programmed to its maximum ramp time and/or default value if not programmable. Similar to ramp rate tests, there was often some subjectivity to the start/stop times of the power ramps, as some manufacturers had non-linear responses, and some were grid-connected but not exporting power prior to

ramping up output current. As with normal operating ramp rate, the UL 1741 SA test criteria have shifted since these tests were conducted. The available ranges for the soft start ramp time vary widely.

Table 12. Soft start ramp rate test results summary

	Inverter Number				
	1	**2**	**3**	**4**	**5**
Manufacturer stated range of ramp times (%/sec)	0.1 – 5.0	0 – 1,000	20 – 10,000	0.17 - Infinite	N/A
Expected Ramp Time (sec)	**Measured Ramp Time (sec)**				
Default / Fastest	N/A	0.2	5.0	0.9	1.5 – 3.5
20	27.4*	N/A	N/A	N/A	N/A
300	346.6	308.0	307.1	295.1	N/A
600	N/A	N/A	N/A	592.3	N/A
1000	1115*	N/A	N/A	N/A	N/A
6000	N/A	6307	6107	N/A	N/A

***Inverter was within 98% of full power by the expected ramp time**

A summary of the restart times is shown in Table 13 for each of the test cases reported in Table 12. Inverters are required to wait *at least* 300 seconds prior to restarting, but there is not a specification that it starts before some time window. Therefore, shorter restart times are not considered better, but instead reflect different approaches to startup routines within the inverter controllers. Each inverter waited 300 seconds as required.

Table 13. Soft start ramp rate restart times

Test Number	**Inverter Number and Restart Time (sec)**				
	1	**2**	**3**	**4**	**5**
1	339.8	303.1	307.8	347.5	317.6
2	339.6	303.0	305.6	348.3	N/A
3	339.6	307.0	305.4	348.6	N/A

A representative example plot is shown in Figure 19 for Inverter 4 programmed with a soft start ramp rate of 0.33%/sec (300 seconds to full power). This plot shows a large transient (drop) in the AC voltage at the beginning, causing the inverter to start a 300 second countdown. The inverter subsequently started up and ramped to full power at the specified ramp rate.

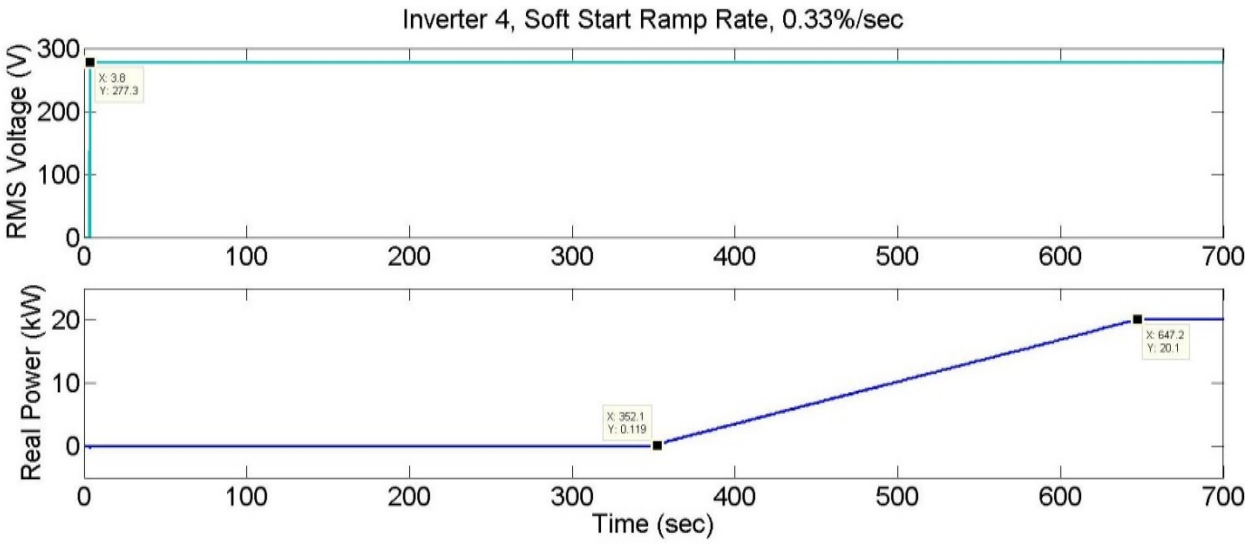

Figure 19. Inverter 4 output power for soft start ramp rate of 0.33%/sec

3.7 Volt-Watt Tests

3.7.1 Volt-Watt Test Procedures

Inverters with VWC are of increasing interest due to their ability to lower the terminal voltage by reducing output power during overvoltage situations. A series of baseline tests were derived from the UL 1741 SA draft standard to build inverter models with VWC for subsequent PHIL testing. A series of three VWC curves – referred to as "mild", "moderate" and "aggressive" based on their slopes – were defined for these tests, as shown in Figure 20. Each curve is characterized by a starting voltage where power reduction begins and a final voltage at which point the inverter has linearly reduced power to zero. The moderate and aggressive curves were suggested by Hawaiian Electric. The mild curve was derived from suggestions made by the Manufacturing Alliance of Inverters Technical Assessment of Integration Issues (MAITAI) group, which is partially overlapping in membership with the SITWG. The SITWG was consulted but did not submit additional suggestions. The basic test sequence involved a series of voltage steps through each segment of the VWC curve, capturing at least three data points within each segment, as required by UL 1741 SA. Each voltage step was held for a period of time that allowed each inverter to settle into a steady operating state. After stepping up to the maximum voltage, the AC source voltage was then stepped down to nominal, repeating each of the same operating voltages.

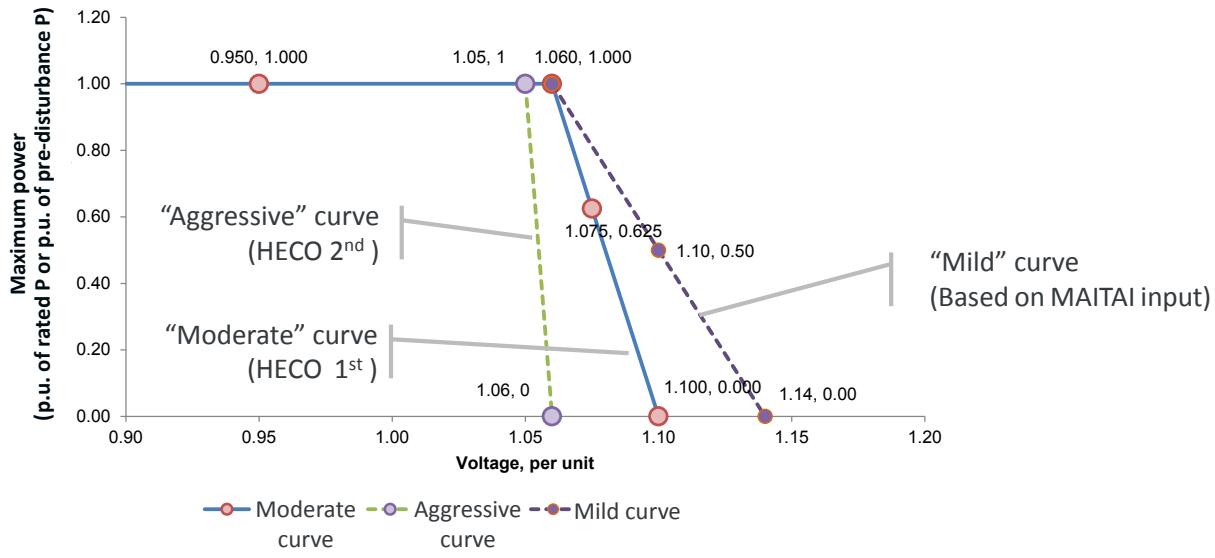

Figure 20. Three different VWC curves used in baseline testing

In addition to the characteristic curves, inverters were characterized for several other types of variation in VWC parameters. Those included two different modes of VWC, and variations in the time-domain response of the VWC function. The following paragraphs describe the variations tested.

Two of the four inverters (Inverter 5 did not have VWC capability) could be programmed for either "nameplate power" mode (also referred to as P_{max} or P_{rated} mode) or "snapshot power" mode (also referred to as $P_{pre\text{-}disturbance}$ mode). In nameplate power mode, the peak of the VWC curve is based on the nameplate inverter rated power. In snapshot power mode, the peak of the VWC is based on the inverter output power at the time the voltage entered the sloping portion of the VWC curve. In snapshot power mode, power reduction begins as soon as the corner voltage of the VWC curve is reached, regardless of the present power level. In nameplate power mode, power reduction follows a fixed voltage-power curve based on the nameplate rated power, so when power is below rated, power reduction does not start until the voltage excursion has reached a point on the volt-watt curve that matches the present output power.

Additionally, different time responses were tested for each inverter. The time response refers to the time to change from one power output level to the next following a step change in grid voltage. For the purposes of this study, the *time constant* refers to the characteristic time constant for a first-order exponential function, such that the inverter is ~95% of the way to its desired set point in three time constants. Readers are advised to use caution as the criteria and terminology relating to time-domain response vary among different standards and SRDs.

Tests were repeated at various power levels to observe the different dynamics between nameplate power mode and snapshot power mode. Each of the test cases is summarized in Table 14 below. Because nameplate mode and snapshot mode have identical responses when operating at 100% power, only snapshot mode was tested at this power.

Table 14. VWC test cases for baseline testing stage

Test Case	Curve Type	Start Voltage (pu)	Stop Voltage (pu)	Time Constant (s)	Input Power (%)	Mode
1	Moderate	1.06	1.10	50	100	Snapshot
2	Moderate	1.06	1.10	1	100	Snapshot
3	Moderate	1.06	1.10	100	100	Snapshot
4	Moderate	1.06	1.10	1	66	Snapshot
5	Moderate	1.06	1.10	1	33	Snapshot
6	Aggressive	1.05	1.06	1	100	Snapshot
7	Mild	1.06	1.14	1	100	Snapshot
8	Moderate	1.06	1.10	1	66	Nameplate
9	Moderate	1.06	1.10	1	33	Nameplate

3.7.2 Volt-Watt Test Results

All inverters successfully ran as expected for the series of tests outlined in Table 14. Not all functionality could be enabled for all inverter types because not all manufacturers supported all options at the time. The tests that were run for each inverter are highlighted in Table 15. Inverters 2 and 4 did not support snapshot mode at the time of testing, so all tests were conducted in nameplate mode, and tests 4 and 5 were skipped as they would have been identical to tests 8 and 9 for those inverters.

Table 15. VWC tests run for each inverter

Test Case	Inverter 1	Inverter 2	Inverter 3	Inverter 4
1				
2				
3				
4				
5				
6				
7				
8				
9				

= RUN

= NOT RUN

A typical set of time series waveform plots is show in Figure 21, demonstrating the difference between snapshot mode and nameplate mode using the moderate curve at 66% output power for Inverter 1 (test cases 4 and 8, respectively). In the top plots, the AC voltage was stepped up and back down along a pre-defined profile that was based on the VWC curve of interest. In the nameplate mode, power reduction did not start until higher voltages, following a characteristic curve based on full power operation. In snapshot mode, power reduction began earlier, as soon as the AC voltage exceeded the start voltage. There was a small amount of settling time for the final power output, and steady state was reached prior to the subsequent voltage step. Power was not reduced down to zero, since that required a final voltage step beyond the 110% overvoltage trip limit.

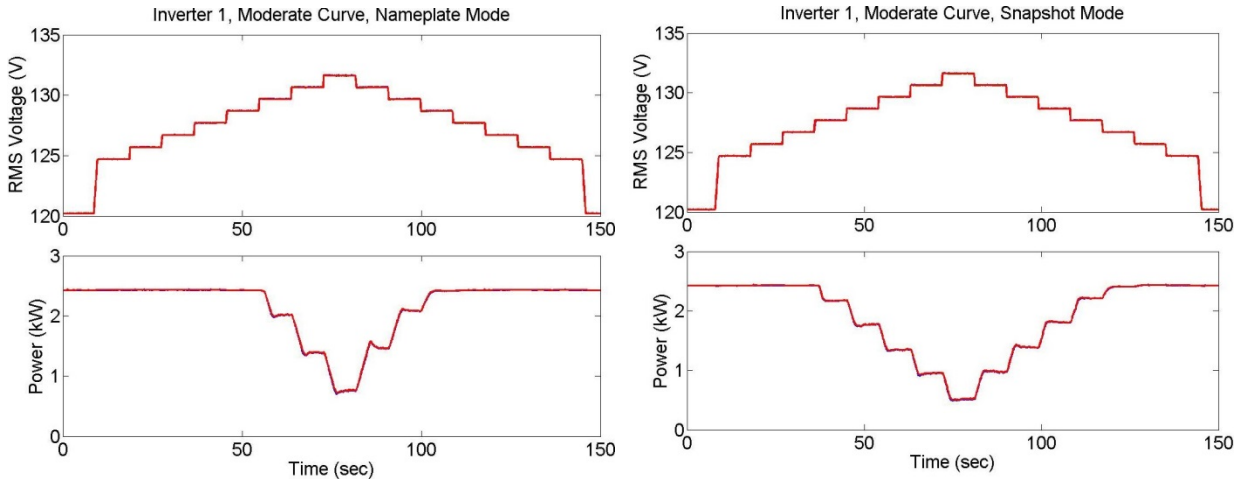

Figure 21. Inverter 1 VWC time series data illustrating the different between nameplate power mode (left) and snapshot power mode (right), moderate curve, 66% output power

A set of summary VWC characteristic curves is shown in Figure 22. These curves show the steady state voltage and power operating points from a set of time series plots similar to those shown in Figure 21. These are the same test cases as in Figure 21, but are for Inverter 3 rather than Inverter 1. Note that the measured curve appears twice in each plot in Figure 22 and similar figures: once measured as voltage increased, and once measured as voltage decreased. These curves likewise highlight the difference between nameplate and snapshot modes at 66% output power, where power reduction did not start until higher voltages, but then reduced at a steeper slope. At the time of testing, Rule 14H was not specific as to how the slope of the VWC should be defined in snapshot mode, so the test criteria were adapted to the inverter's implementation. As of this writing, Hawaiian Electric's draft SRD calls for the slope of the VWC in both snapshot and nameplate modes to be independent of the pre-disturbance power, but that had not been specified at the time of testing.

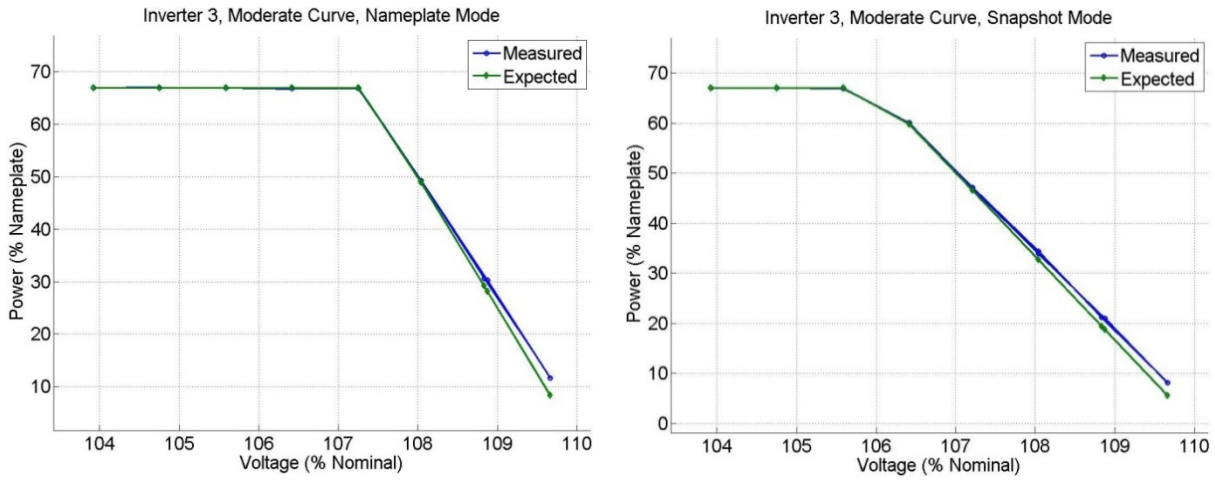

Figure 22. Inverter 3 VWC summary curves illustrating the difference between nameplate power mode (left) and snapshot power mode (right). Both used the moderate curve, 66% output power

The VWC summary curves also illustrate the relative error between the expected output power and the measured output power. A comprehensive listing of all measured and expected values for each voltage step across all tests cases for all inverters (used to create the plots such as Figure 22) is found in Appendix A. Note that the error values in Appendix A are relative to ideal VWC curves and do not take into account manufacturer's stated accuracies of voltage or power. Also note that many inverters had high error values when using the aggressive curve and when expected output powers were very small. When using the aggressive VWC curve, error values were often high because a very small difference in measured voltage leads to a very large difference in power. For many inverters, the MSA of voltage is 1%, so the aggressive curve goes from 100% power to 0% power over a voltage change equal to the MSA. Additionally, small drops in voltage across test cabling (and across the cables connecting one microinverter to another) can lead to differences in measured versus expected power, especially when using the aggressive curve. This is effect is amplified for Inverter 1, which readers will recall is an assembly of single-phase microinverters connected line to neutral. The additional voltage drop in the neutral wiring results in a doubling of the voltage change between one microinverter and another, and hence an increase in the variation of power from one inverter to another in VWC mode. This effect is strongest with the aggressive volt-watt curve. Also note that the issue of cable voltage drops leading to different outputs for each microinverter in a string is not confined to microinverters. The same issue would be seen in a system consisting of more than one string or central inverter. Higher error values also often occurred near the high voltage (low power) end of the volt-watt curve, likely because of minimum output power levels for each inverter. Finally, it is likely that test case 6 for Inverter 1 was run with incorrect VWC settings, so the errors in that test may not be representative of the inverter's true behavior.

Figure 23 illustrates the reduced accuracy often seen when using the aggressive curve by presenting both the moderate and aggressive curve results for Inverter 4. Note that the accuracy of the aggressive curve response is lower.

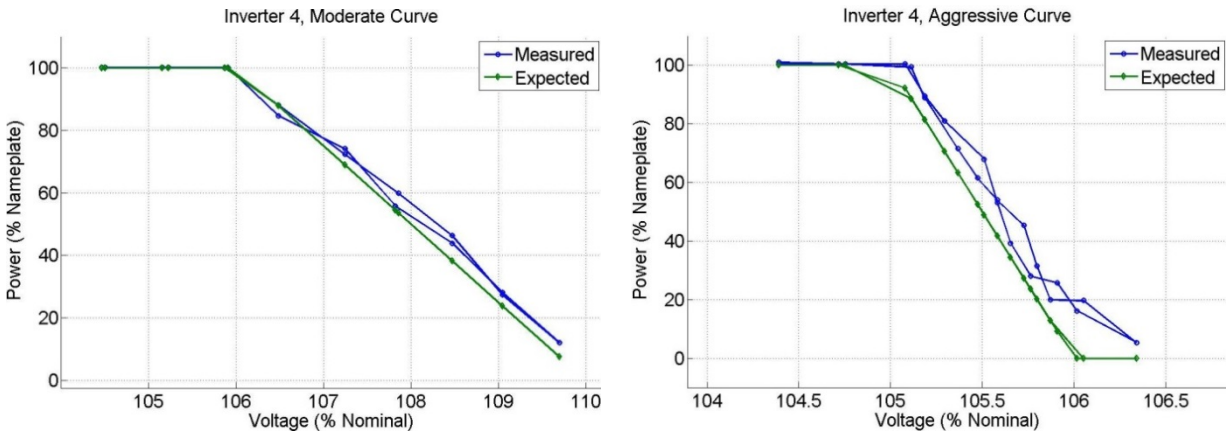

Figure 23. Inverter 4 VWC summary curves for the moderate curve (left) and aggressive curve (right) at 100% output power

An additional set of time series plots is shown in Figure 24, showing the difference between the moderate (left) and aggressive (right) curves for Inverter 2 operating at 100% output power (test cases 2 and 6, respectively). The aggressive curve required lower voltages to create a large excursion in output power, as expected. Figure 25 shows VWC summary plots demonstrating the difference between the moderate (left) and mild (right) curves (test cases 2 and 7). Both curves began power reduction at 106% of nominal voltage, but follow significantly different slopes, as specified in the characteristic curves.

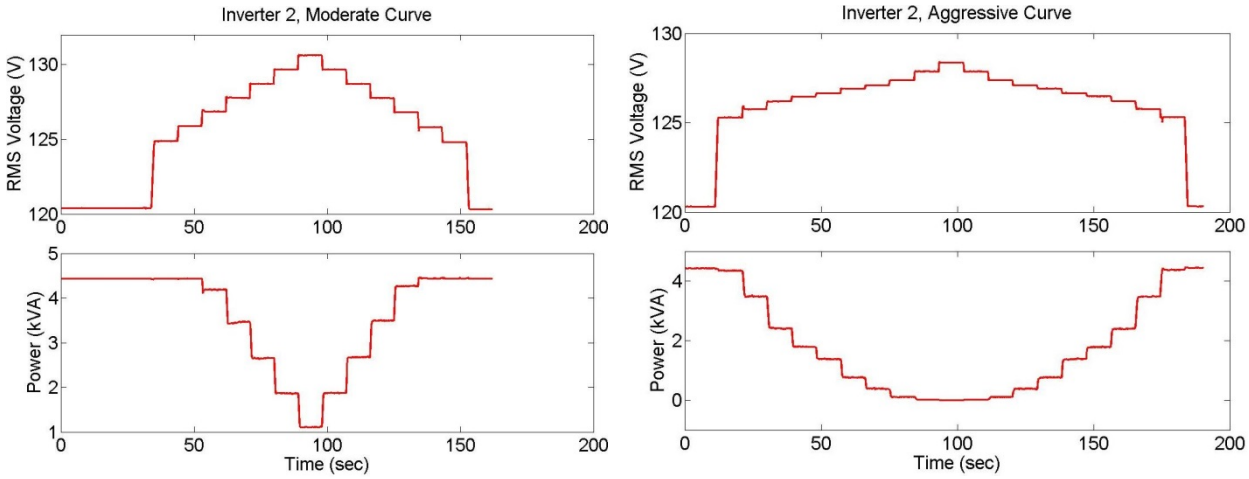

Figure 24. Inverter 2 VWC time series data for the moderate curve (left) and aggressive curve (right) at 100% output power

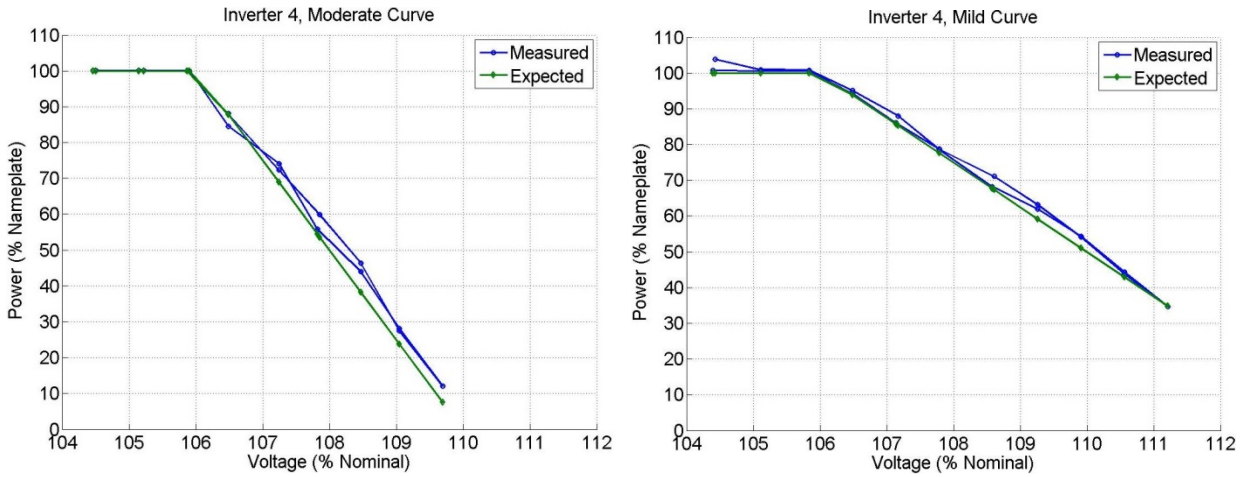

Figure 25. Inverter 4 VWC summary curves for the moderate curve (left) and mild curve (right) at 100% output power

Finally, the time-domain response of the inverters was of particular interest for building models for PHIL testing. Figure 26 shows two different types of time-domain responses: one for Inverter 3 (left) and one for Inverter 2 (right), using a 50 second time constant (test case 1). Both plots show the time response of output power for a single voltage step during a 100% output power test using the moderate curve. When programmed for a 50 second time constant, Inverter 3 had an exponential time response, taking several time constants to reach the target response, *regardless of the step size in power*. This inverter consistently reached ~95% of the target value in approximately 120 seconds, implying a 40 second time constant when modeled as a first order exponential function. This correction factor between expected behavior and actual behavior was accounted for in the PHIL modeled inverters.

In contrast, Inverter 2 had a linear response in power for a step change in voltage. The time response was programmable as the linear time for a 100% change in power, so the linear time response slope was therefore *dependent on the step size in power*. For these tests, the inverter was programmed to achieve a 100% change in output power in 150 seconds, in order to approximate three 50 second time constants to make a full excursion. Figure 26 shows the inverter output power changing by ~18% in ~27 seconds, which is proportional to a 100% change in 150 seconds.

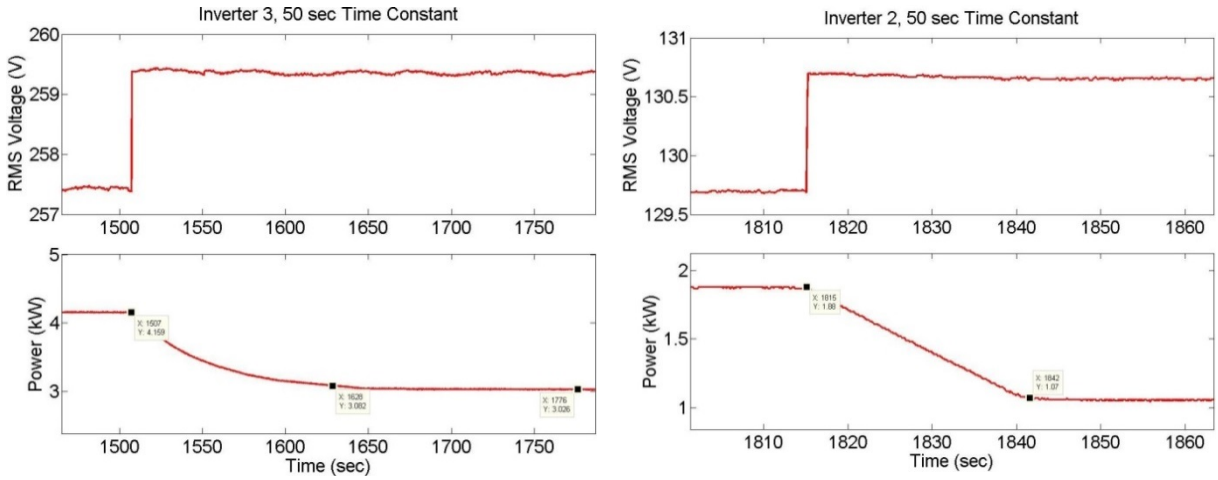

Figure 26. Inverter 3 VWC test segment with 50 second exponential time response (left) and Inverter 2 VWC test segment with time response at 100% full power in 150 seconds.

Appendix A shows all of the expected and measured values for the baseline volt-watt tests, as well as the percentage error in expected output power. In most cases, the error was no greater than several percentage points, which was within the MSA in voltage and power measurements for each test inverter. Larger errors tended to occur for the aggressive curve because this curve required a 100% power excursion for a 1% change in AC voltage. The MSA in voltage measurement was 1% for most manufacturers, so any small deviations between the voltage measured by the inverter and the voltage measured by the test instrumentation resulted in large errors in the expected values. Additionally, there was a finite voltage drop in the cabling between the inverter terminals and the points where the instrumentation was placed, although efforts were made to minimize the cable run between the two. This problem was further exacerbated for the microinverters, as a finite voltage drop occurred between each inverter, so inverters in the same system may have been commanded to different output power levels. In a field PV system consisting of multiple string inverters, the same issue would likely be seen. These issues of measurement tolerances and cable voltage drops will be present in any field installation and will result in a more stochastic response for the aggressive curve. For these reasons, the aggressive curve is not recommended for implementation.

3.8 Volt-Var Tests

3.8.1 Volt-Var Test Procedures

Volt-var control is of interest due to its ability to regulate voltage while minimizing the amount of real power reduction; additionally, both overvoltage and undervoltage scenarios can be regulated, and vars are only absorbed/produced if the voltage is in fact high or low. A series of three VVC were defined for these tests, as shown in Figure 27, and the test procedures were derived from the draft version of UL 1741 SA. Each curve is characterized by a dead band around nominal voltage, a linear region for increasing/decreasing reactive power, and maximum reactive power limits. These curves are referred to as the "mild" (blue), "moderate" (purple), and "aggressive" (tan) curves based on their slopes. The curves were selected to represent the range of possible curves that might be implemented: the aggressive curve is likely more aggressive

than would be used in the field, the mild curve is likely on the mild end of what would be used in the field, and moderate curve is between the two.

Note that the curves in Figure 27 are based on the assumption that maximum reactive power was 50% of the inverter's rated kVA; the peak reactive power used for these curves was scaled according to each test inverter's maximum reactive power capability. Each of the curves was symmetrical, except the linear endpoints for the mild curve resided at the under/overvoltage trip levels (88% and 110%). For each test, AC voltage was stepped through each segment of the VVC curve, capturing at least three data points within each segment, as required by UL 1741 SA. Each voltage step was held for a period of time that allowed each inverter to settle into a steady operating state. Voltage was first stepped down to a minimum value, was ramped back to nominal, and then was stepped up incrementally to a maximum value; the voltage profiles were dependent on the curve type.

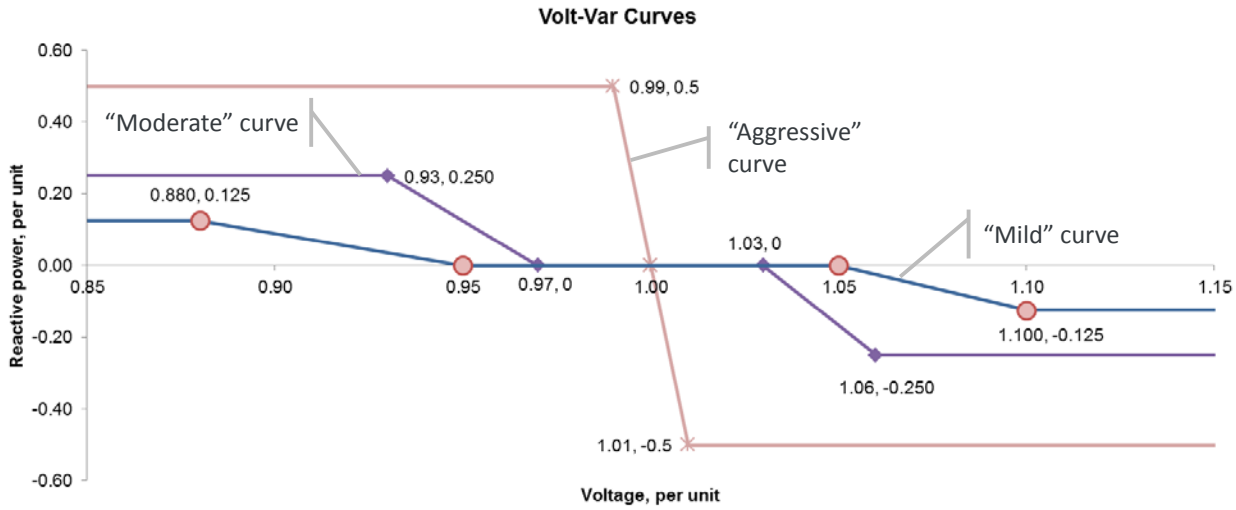

Figure 27. Mild, moderate, and aggressive VVC curves used in baseline testing

In addition to the characteristic curves in Figure 27, inverters were tested for several other behaviors. UL1741 SA includes capacitive and inductive offsets in the dead band region, with a magnitude of 5% of maximum reactive power. Inverters were also tested at varying power levels and at different response times, if programmable. The response times follow the same conventions discussed in the previous section. Each test case for this function is summarized in Table 16.

Table 16. VVC test cases for baseline testing stage

Test Case	Curve Type	Offset	Max Reactive Power	Time Constant (s)	Input Power (%)	Mode
1	Moderate	None	Qmax/2	1	100	Qmax
2	Moderate	None	Qmax/2	1	60	Qmax
3	Moderate	None	Qmax/2	1	20	Qmax
4	Moderate	Capacitive	Qmax/2	1	100	Qmax
5	Moderate	Inductive	Qmax/2	1	100	Qmax
6	Aggressive	None	Qmax	1	100	Qmax
7	Mild	None	Qmax/4	1	100	Qmax
8	Moderate	None	Qmax/2	10	100	Qmax

3.8.2 Volt-Var Test Results

All inverters successfully ran as expected for the series of tests outlined in Table 16. Not all functionality was available for all inverter types; the tests that were run for each inverter are highlighted in Table 17. Inverters 1 and 2 did not have a programmable time response, so they were operated at the default time response. The aggressive curve was skipped on Inverter 4 because the inverter output power was high enough to change the voltage beyond the limits of ±1% specified by the curve, leading to oscillations from maximum positive reactive power to maximum negative reactive power; see below for further discussion on this curve and measurement accuracy. With respect to operating mode, UL 1741 SA specifies separate tests for real power priority as opposed to reactive power priority, which impacts operation near rated nameplate power. Note that Hawaiian Electric's SRD at the time of this writing calls for reactive power priority. Inverters 1, 3 and 4 were only capable of reactive power priority, and Inverter 2 was only capable of real power priority. Inverter 1 was run on a modified profile for test case 8 in order to resolve the effect of changing the time response, since this inverter's time response limits the change in Var output per second rather than providing a fixed step response. This test required operating the moderate curve up to maximum reactive power rather than 50% of the maximum.

Table 17. VVC tests run for each inverter

Test Case	Inverter 1	Inverter 2	Inverter 3	Inverter 4
1				
2				
3				
4				
5				
6				
7				
8				

= RUN = NOT RUN

A typical time series waveform plot is show in Figure 28, showing the differences between the moderate curve and the mild curve for Inverter 2 (test cases 2 and 7, respectively). As expected, larger voltage excursions were required to reach the extremes in reactive power for the mild curve, and the magnitude of maximum reactive power was defined by the curve type. The 60% output power test case is shown to illustrate the differences in curves because no reactive power is provided for the 100% output power case on Inverter 2, since real power is prioritized for this inverter. These data also demonstrate the test procedure where voltage was ramped down to a minimum value, ramped back to nominal, and then up to a maximum value defined by the curve type.

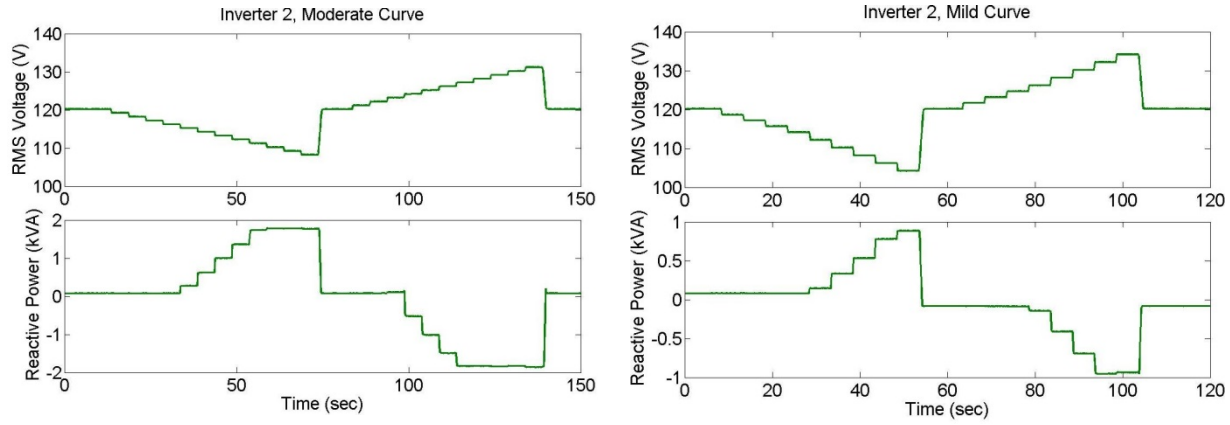

Figure 28. Inverter 2 VVC time series plots with moderate curve at 60% output power (left) and with mild curve at 100% output power (right)

A pair of VVC characteristic curve summary plots is shown in Figure 29 for Inverter 4. These figures likewise highlight the differences between the moderate curve (test case 1) and the mild curve (test case 7) with different dead bands, slopes, and maximum reactive power regions. Note that the constant maximum reactive power region for the mild curve was not tested since those voltages exceed voltage trip limits. These curves show the differences between the measured and expected values, and a complete summary for all test points is found in Appendix B.

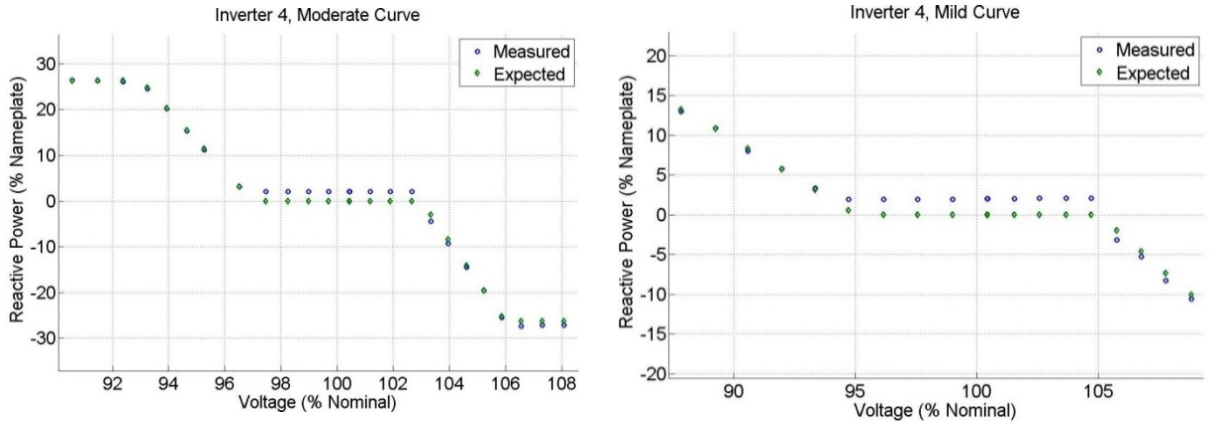

Figure 29. Inverter 4 VVC summary curves with moderate curve at 100% output power (left) and with mild curve at 100% output power (right)

Figure 30 shows time series data demonstrating the effect of changing the time response for Inverter 3 (test cases 1 and 8). Just as in the VWC testing, Inverter 3 had a first-order exponential time response, reaching ~95% of the new set point in three time constants, regardless of the magnitude of the new reactive power set point. These tests were run at 100% output power using the moderate curve.

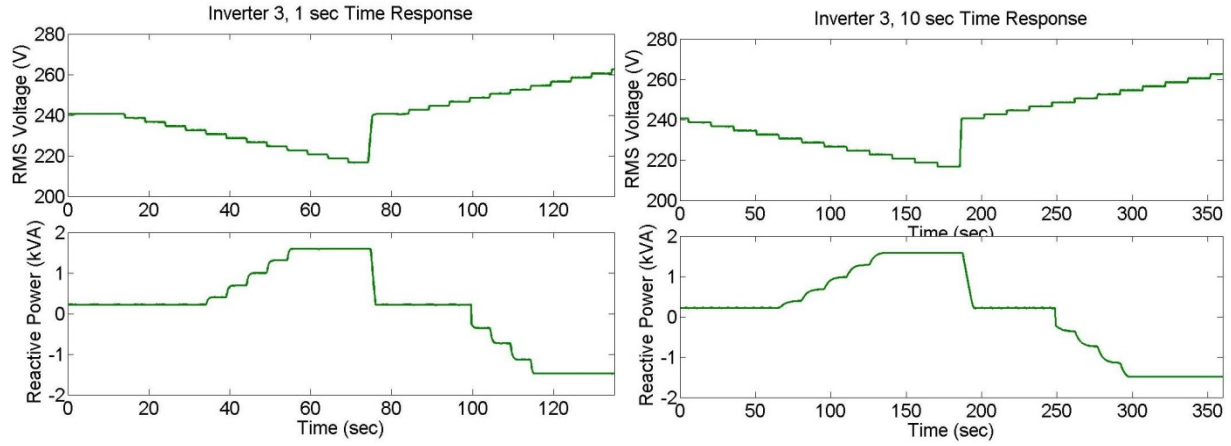

Figure 30. Inverter 3 VVC time series responses with 1 second time response (left) and 10 second time response (right), moderate curve, both at 100% output power

Finally, Figure 31 shows the VVC characteristic curve summary plots for the capacitive and inductive offset cases (tests 4 and 5, respectively). These plots show the results for Inverter 1 using the moderate curve and 100% output power. Note there is a small positive/negative reactive power offset in the dead band near nominal voltage for the capacitive/inductive cases, as expected.

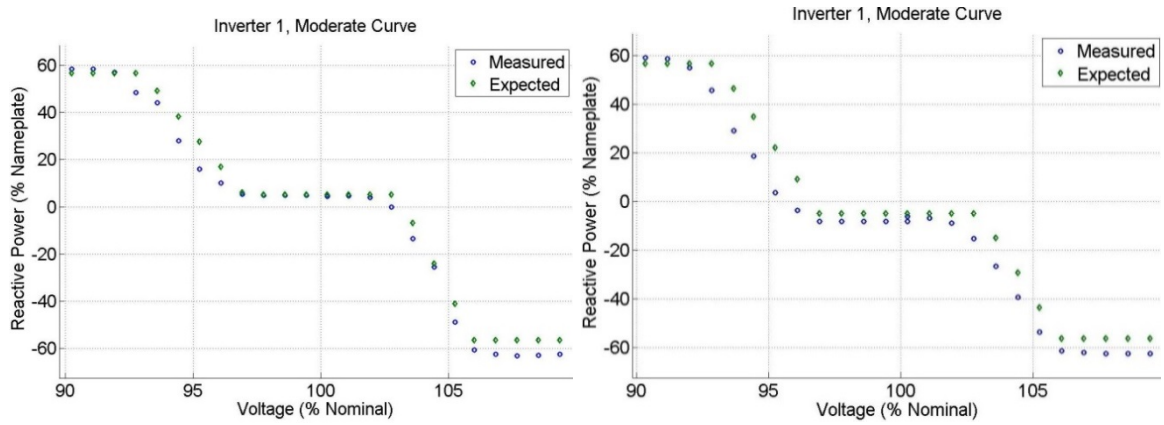

Figure 31. Inverter 1 VVC summary plots showing capacitive offset (left) and inductive offset (right), 100% output power, moderate curve

Similar to the VWC tests, the relative error between expected and measured reactive power is shown in Appendix B. Although the errors are relatively small in many cases, there are multiple factors contributing to these errors. The MSA in voltage and power measurements could total a couple of percentage points for each manufacturer, and the aggressive curve required a full excursion between maximum positive and negative reactive power for a change of ±1% in voltage. This problem was compounded in microinverters where voltage measurements were different along the string of inverters (as would also be the case for a system of multiple string inverters in the field). Additionally, wire impedances created finite voltage drops between the inverter terminals and the instrumentation. To the extent that currents are higher in volt-var mode than in volt-watt mode, the issue of cable voltage drops leading to less-predictable output is amplified in volt-var mode. The highest power inverter (Inverter 4) was able to create a significant enough change in voltage across the wire impedance that it oscillated between maximum positive and negative reactive power when programmed with the aggressive curve due to the effect of its reactive power on its own terminal voltage. Thus the aggressive VVC curve is not recommended for use in the field. Even if a deadband were inserted in the aggressive curve, the slope is likely too steep to provide predictable behavior. The problematic element of the aggressive curve is its slope; neither the lack of a deadband nor the fact that it uses the full reactive power capability of the inverter is necessarily problematic from a grid operational perspective.

3.9 Volt-Watt with Volt-Var Tests

The potential to operate inverters with both VVC and VWC enabled is of interest as the advantages of both modes can potentially be leveraged to regulate overvoltage scenarios. VVC can be implemented at lower overvoltage ranges to regulate the voltage while minimizing real power production losses. VWC can then be implemented for higher voltages to act as reinforcement if the overvoltage scenario is more extreme. As such, several baseline tests were completed with both VWC and VVC enabled. This dual functionality was not required by existing standards or SRDs at the time of testing, and it was only available and tested on Inverter 1 and Inverter 4. However, the IEEE draft standard P1547 is expected to require many distributed energy resources to be capable of simultaneously implementing both when it is published. Likewise, Hawaiian Electric is moving towards requiring inverters be capable of simultaneously enabling VWC and VVC in Rule 14H in the near future.

The curves were selected from the moderate selections shown in the previous section so that more stable behavior would be expected than that observed in the aggressive cases. As seen in Figure 32, the moderate VWC curve from previous tests was used for both dual functionality tests, and then two different VVC curves were tested. The first curve (blue) is the moderate curve from previous VVC testing. The second curve (purple) is a modified version of the moderate curve used in previous VVC testing. The magnitude and slopes were retained, but the highest voltage point was shifted increased by 2%. The purpose of this shift was to create overlap between the two functions' active regions in the 103-106% of nominal voltage range. The undervoltage portion of the VVC curves was not tested for these tests since VWC is not active in that region. The voltage profiles and test procedures were similar to those used in previous VWC and VVC tests, as adapted from the draft UL 1741 SA document. Both tests were run at 100% output power and at the fastest time response.

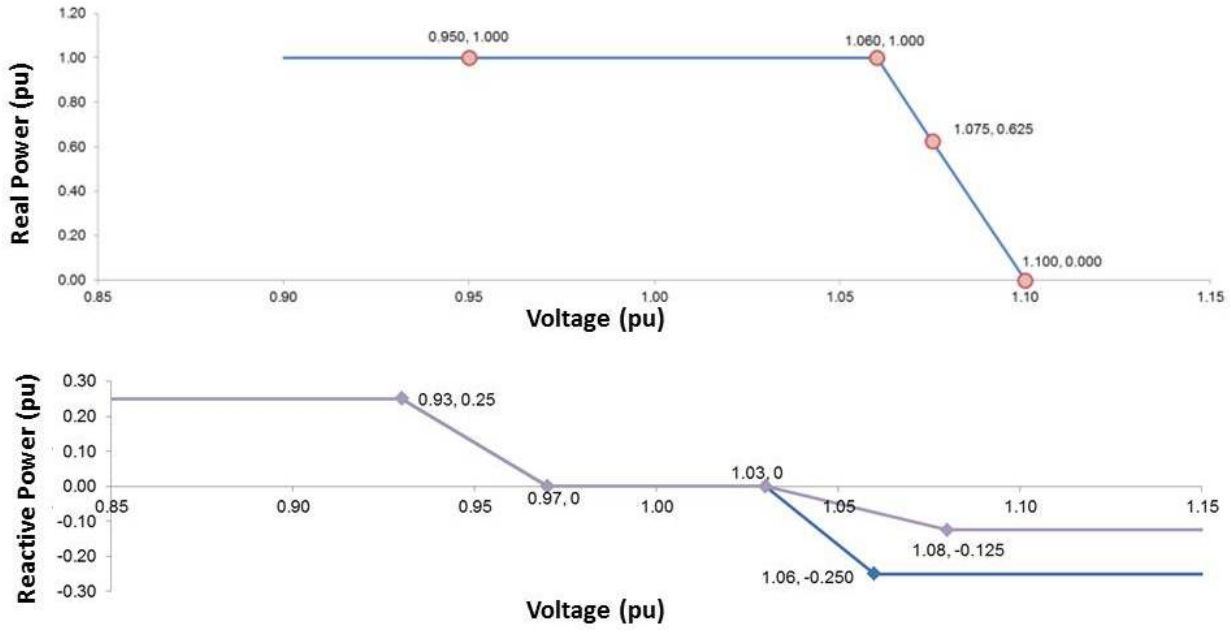

Figure 32. Moderate VWC curve (top) and both moderate and "modified moderate" VVC curves (bottom) used for dual functionality test cases.

The summary curves each of the two test cases for Inverter 4 are shown in Figure 33. The first test case (left) shows reactive power reaching its maximum negative value before real power reduction begins around 106% of nominal voltage. The second test case (right) shows a similar behavior, but with the overlap between nonzero reactive power and less than full rated real power in the 103-106% of nominal range.

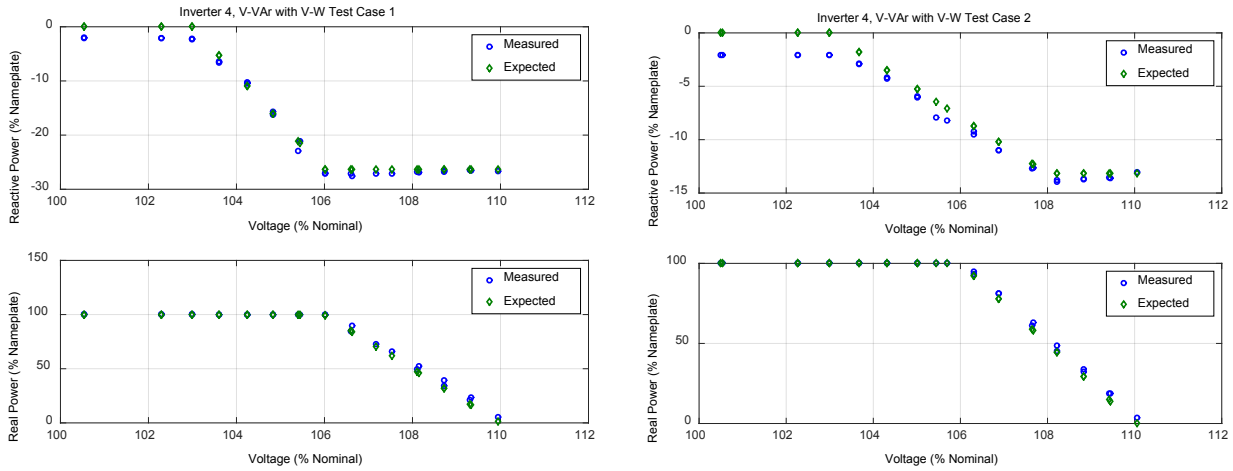

Figure 33. Inverter 4 combination VWC and VVC summary curves using moderate (left) and modified mild (left) VVC curves along with the moderate VWC curve

The results for both inverters are summarized in Appendix C. The summary plots for Inverter 1 are more complicated than the ideal scenario because maximum reactive power was provided up to a limit of ±0.85 power factor. Therefore, as real power was reduced at the higher end of the voltage range, reactive power likewise decreased.

3.10 Baseline Testing Conclusions

In general, all GSFs of interest in the baseline testing performed as expected, and the test data provided valuable inputs to the subsequent PHIL inverter models. All test inverters passed the FRT and VRT requirements as expected, with some unexpected behavior due to voltage or frequency ramp rate requirements that were not previously known by the manufacturers. Fixed power factor operation performed as expected, with some minor deviations from the expected set points, mostly at very low power levels.

The normal and soft start ramp rates were also close to the expected values, with some deviations due to differences in startup routines and judgments in the timing of the ramp rates. Only a subset of the inverters was able to implement normal operating ramp rate control. The available ranges of adjustment for both ramping functions varied widely from inverter to inverter.

All VWC and VVC tests generally behaved as expected, within the limitations of what was programmable for each test inverter. For both functions, the aggressive curves (i.e. steep slopes) were in many cases problematic due to issues with accurately measuring and maintaining the inverter terminal voltages. The problematic behavior of the steep curves was not unexpected; these curves are steeper than would be recommended for use in the field.

Two of the four inverters were capable of operating with VWC and VVC simultaneously enabled, and several test cases were run to demonstrate this functionality. These tests showed the behavior to be as expected, and not problematic. Note that VVC was run in reactive power priority mode in these tests. Simultaneous VWC with VVC in *real* power priority mode was not tested.

The results from the VRT, FRT, ramp rate, soft start, FPF, and VWC test results were subsequently used to develop inverter models for PHIL testing in the next phase of the project. VVC was not tested in PHIL because it was added to the list of functions at a later date.

4 Real-Time PHIL Model Development

For real-time PHIL testing, the OpenDSS reduced-order models produced using the procedure in Section 2 was translated into Matlab/Simulink. Aggregated inverter models were added to the reduced feeder model based on data on existing and future PV systems provided by Hawaiian Electric. This resulted in complete real-time models of each feeder populated with legacy and advanced PV inverters. The real-time models developed in Simulink were subsequently loaded to the OPAL-RT real-time digital simulator in order to run the suite of PHIL experiments discussed in the next section.

4.1 Feeder Model Conversion to Real-Time

The first step in real-time model development was to translate the reduced OpenDSS feeder models into Simulink models that make use of the SimPowerSystems toolbox. The outputs from the OpenDSS feeder reduction described above include the source impedance parameters, line lengths between nodes, line impedances between nodes, and loads at each node. The feeder head voltage source was an ideal three-phase voltage source behind a three-phase resistive-inductive (RL) source impedance; the voltage source was set for 7.2 kV (line-neutral) operation at 60 Hz (except for FRT tests, described below). The feeder head voltage was scaled to 105% of nominal for many tests that were required to create overvoltage scenarios. A network of eight nodes on the primary was created using RL line impedances with the spatial layout following that which was depicted in Figure 8 (repeated here as Figure 34 for convenience). Each node also contained a local three-phase unbalanced real and reactive power (PQ) load; each load was based on maximum daily values, and so each contained a programmable scaling factor that could be used as an input parameter to adjust load levels for different test cases. When setting up each test, the load scaling factor was adjusted to a value between the feeder's peak load and its gross minimum daytime load. Each load represented an aggregate of the load on each phase in that location in the full feeder model. Finally, each node also contained four types of aggregated PV inverter, as described below.

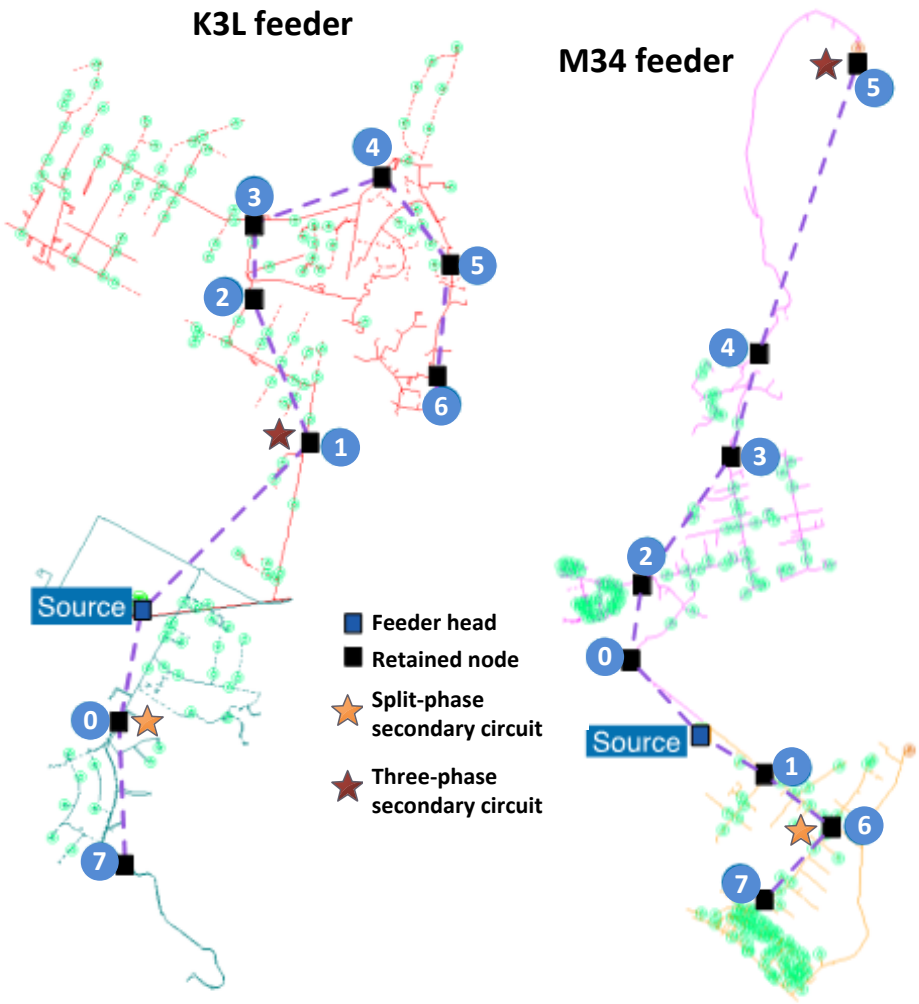

Figure 34. View of the original feeders with the nodes that were retained

Each model also contained a single distribution secondary circuit to act as the point of interconnection for the inverters under test. The secondary circuits were connected at a location specified by Hawaiian Electric near the feeder head source with a 7200/120 V transformer (transformer parameters found in Appendix D). Each secondary was provided by Hawaiian Electric and represented a small collection of households on a single transformer in a neighborhood. Similar to the primary circuit, each secondary node was connected via an RL line impedance, and each had a local PQ load. The M34 model contained six nodes on the secondary and the K3L model contained 13 nodes on the secondary. Figure 35 and Figure 36 show the topologies of the distribution secondary circuits for the K3L and M34 respectively, including the customer node numbers, the modeled PV systems, and the points of interconnection for the PHIL-interfaced hardware PV inverters under test. The M34 secondary is a fairly typical residential secondary. The K3L secondary is long and has a relatively high number of customers (but is still within the typical range of O‘ahu secondaries).

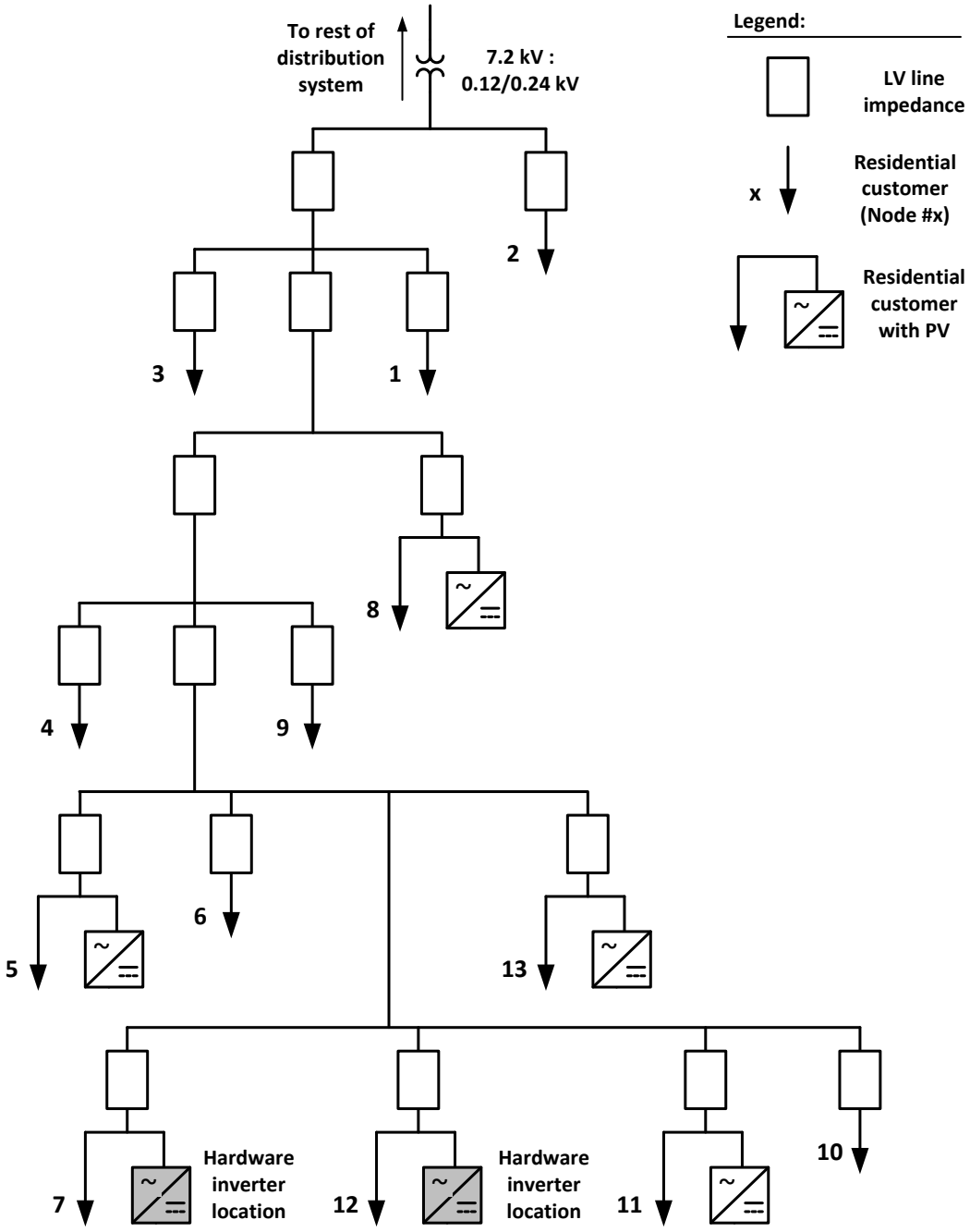

Figure 35. Distribution secondary circuit used for K3L feeder model

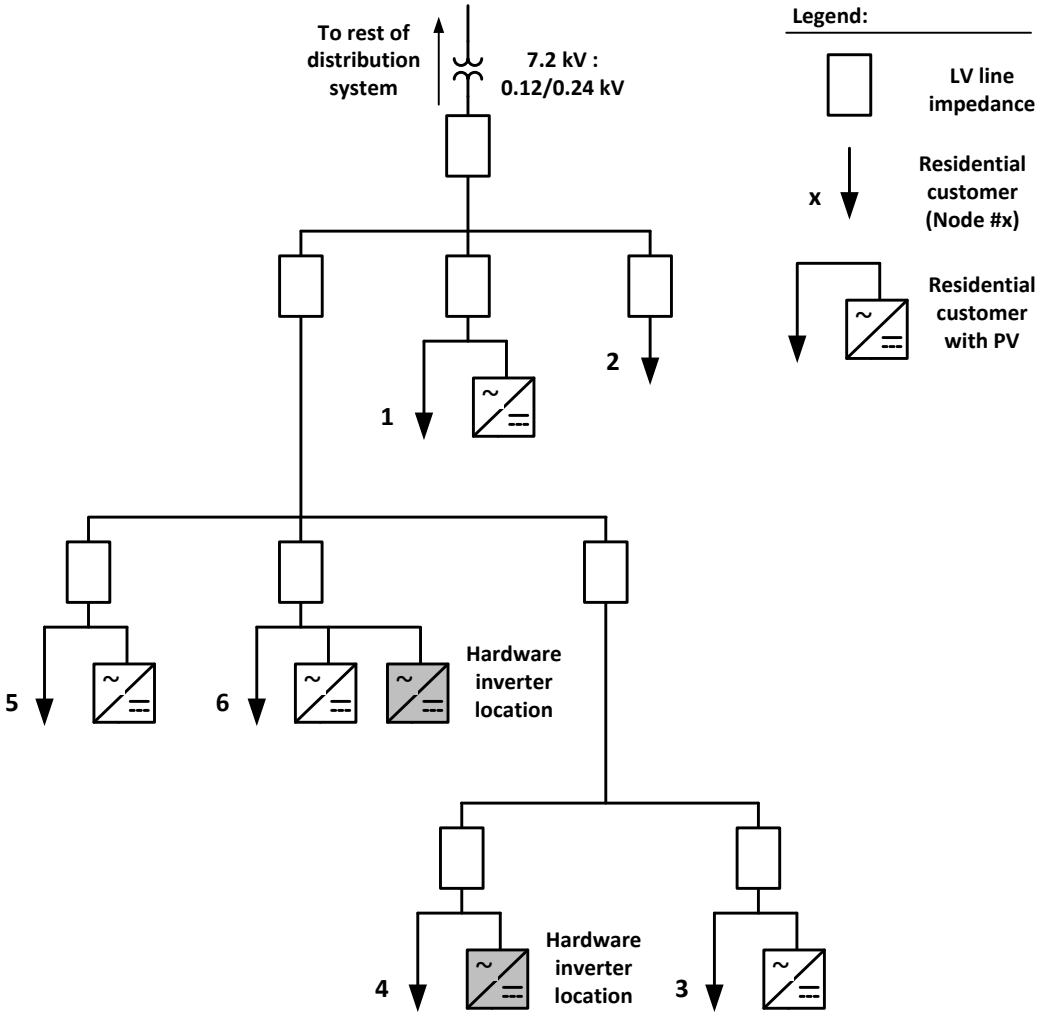

Figure 36. Distribution secondary circuit used for M34 feeder model

Inverter 4 was a three-phase inverter, and was therefore not connected to the single-phase secondary circuit. Instead, a transformer and RL line impedance were placed between the point of interconnection for this inverter and the three-phase primary network. Details of the three-phase secondary line and transformer parameters are found in Appendix D.

4.2 PV Inverter Model Development

The next aspect to the real-time model was the inclusion of PV inverter models to represent different scenarios. Four different inverter types were placed at each of the eight primary nodes, and each type was tuned based on characteristics observed during baseline hardware tests. One set of inverter models was based on the Enphase baseline test results due to the prevalence of this inverter class in the feeders of interest. All other inverter types on these feeders were represented by a single model based on one of the other test inverters. Each of these two inverter types was additionally split between "legacy" and "advanced", each with different GSF capability. Inverter types are henceforth referred to as "legacy" or "advanced" paired with "Enphase" or "other", as in Table 18. The total ratings of legacy and advanced inverters at each node were adjusted for

each test based on the number of inverters capable of the function being tested, as described later in this section.

The key difference between legacy and advanced inverter types was the GSF capabilities. Advanced inverters were programmed with VRT and FRT limits specified in 14H, while legacy inverters had the standard voltage and frequency trip limits specified in IEEE 1547-2003 [12]. Advanced inverters had ramp rate and soft start control, while legacy inverters responded to changes in irradiance instantaneously and ramped to full power instantaneously after a grid event. The restart times highlighted in Table 13 were used for both legacy and advanced inverters, but were tuned slightly differently for Enphase as opposed to non-Enphase inverters. Advanced inverters were programmed to operate at 0.95 power factor (unless a test scenario called for a different power factor), as required by Rule 14H, whereas legacy inverters operated at unity power factor. Finally, advanced inverters could have VWC enabled as a user input, while legacy inverters were not capable of this functionality. The time response was modeled after the results from the baseline tests, but the VWC curves were based on ideal behavior, rather than tuned for the very small deviations from expected output found in the baseline testing. Features of each of the inverter types are summarized in Table 18.

Table 18. Functional differences between different inverter model types

Inverter Type	FRT / VRT Settings	Default Power Factor	Ramp Rate Enabled (Y/N)	Soft Start Enabled (Y/N)	V-W Enabled (Y/N)	V-W Time Response
Legacy Enphase	IEEE1547-2003	1.0	No	No	No	N/A
Legacy Other	IEEE 1547-2003	1.0	No	No	No	N/A
Advanced Enphase	Rule 14H (Oct 2015)	0.95	Yes	Yes	Yes	Linear
Advanced Other	Rule 14H (Oct 2015)	0.95	Yes	Yes	Yes	Exponential

The inverters were modeled as power-controlled current sources that were driven by control logic that accounted for the maximum power rating of the inverter type, the irradiance input, the voltage at the node of interest, any enabled GSFs, and a number of user inputs. The output of the control block was a magnitude and phase angle of the desired current output that was used to drive the ideal current source. The user could select the power factor of the advanced inverters, VWC curve type, irradiance profile characteristics, and PV inverter ratings for each of six different scenarios (described below). The inverter control blocks limited the apparent power output with the inverter rating and irradiance inputs. The irradiance input was either a constant value or linearly ramping value, depending on the test type.

The power factor input was used to directly calculate the phase angle of the current output; a phase-locked loop (PLL) block was used to calculate the phase angle of the voltage input and ensure the current waveform led/lagged by the appropriate phase shift. The VWC function was

implemented through look-up tables, based on the VWC characteristic curve selection. The user could also select nameplate (P_{max}) or snapshot ($P_{pre\text{-}disturbance}$) mode and logic was implemented in the VWC control block to account for instantaneous power when the function was triggered in snapshot mode. The VWC block produced the desired real power output, which was combined with FPF information to create a reactive power set point. Saturation blocks were used to verify that the overall apparent power did not exceed the overall rating of the inverter type, and reductions were made in real and reactive power, if necessary. Finally, the apparent power was divided by the local voltage magnitude to calculate the magnitude of the current output. The VWC control block also contained logic to limit the output power change by an exponential or linear time constant, depending on the inverter type.

The inverter models were validated individually by comparing simulation output to hardware test data from the baseline tests. In addition, they were validated in the PHIL model by comparing simulated output to expected output for a variety of test cases.

The legacy inverter controllers were much simpler, and calculated the current magnitude based on the inverter ratings, irradiance input, and the instantaneous voltage magnitude. The phase angle offset was always set to zero for unity power factor operation, and the phase angle of the current always followed the angle output of a PLL block on the voltage signal.

The current output of all four inverter types at each feeder primary node was summed together and injected into the node in aggregate. A high level overview of the complete real-time model for the K3L feeder is shown in Figure 37. The reduced order primary is on the upper half and the secondary circuit on the bottom portion of the figure. Aggregated loads (pink) and inverters (red) appear at each of the eight primary nodes. Orange rectangles are metering locations. The location of the point of interconnection for the hardware inverter for PHIL testing is shown at the bottom. As indicated in Figure 35, there were modeled PV inverters added to the secondary as well (for both feeder models). These inverters were all simple legacy inverters, and the ratings are described in the PHIL test results below. The power ratings of these secondary-connected PV inverters were adjusted as needed to create the desired test scenarios.

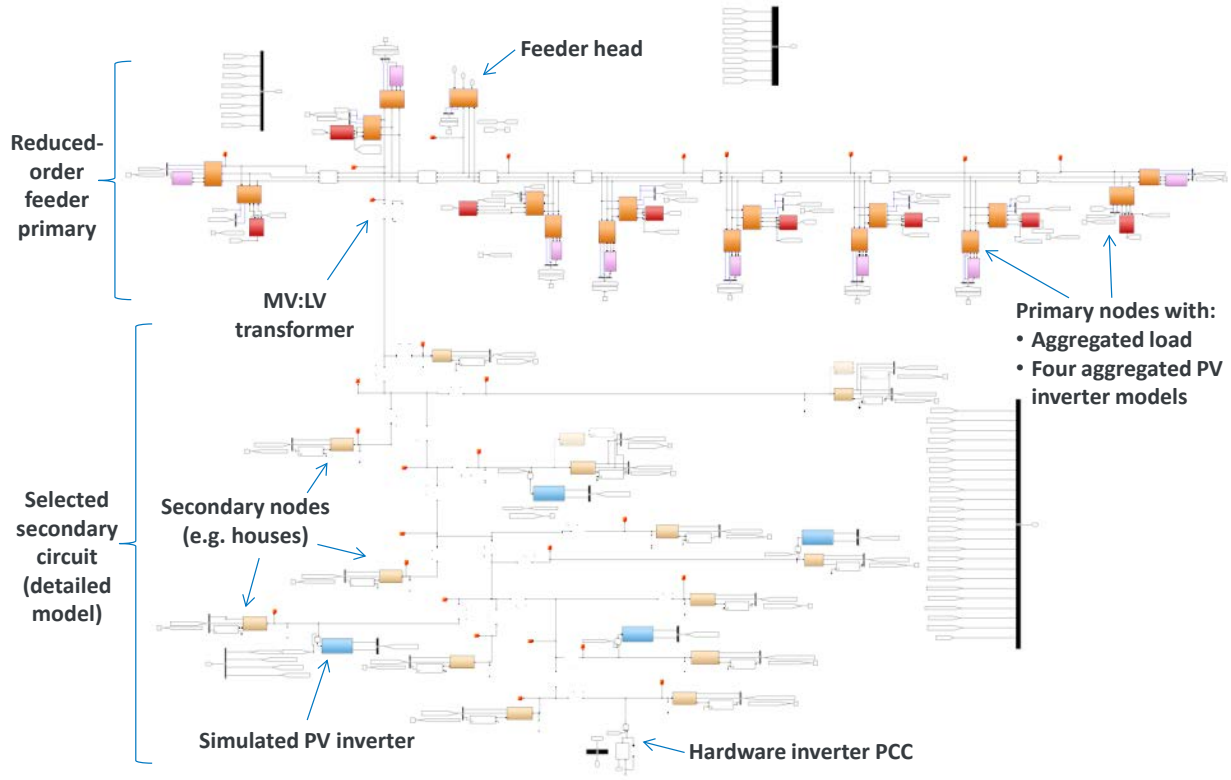

Figure 37. Overview of complete real-time model for the K3L feeder with modeled PV inverters

The overall rating for the different PV inverter types was based on data provided by Hawaiian Electric on existing PV systems, queued PV systems, and future projected PV penetrations. The existing and queued PV systems included systems under all tariffs: NEM systems, feed-in tariff (FIT) systems, and Standard Interconnection Agreement (SIA) systems. For each existing and queued system, the actual inverter type, ride-through capability status of the inverter, and the location of the system on the feeder were obtained from Hawaiian Electric interconnection data. The total power rating of each PV type at each node for the 2016 case with no retrofitting was taken directly from the interconnection data. For future cases where more PV was needed, the number of NEM systems at each node was scaled up proportionally until the desired feeder-level PV penetration was reached, based on Hawaiian Electric projections for each circuit. This is not meant to imply that future PV systems will be NEM systems, but rather that future PV systems will be *distributed* on the feeders similarly to existing NEM systems.

All future PV systems were assumed to be capable of all GSFs, though this does not actually reflect the situation on the ground. For the 2016 test scenarios, many inverters were capable of ride-through, as indicated in Hawaiian Electric's interconnection data. This was reflected in the ratings of the modeled inverters. In contrast, none of the 2016 inverters were capable of the other GSFs; the 2016 case is effectively based on December 31, 2015, before 0.95 power factor operation was required. Therefore the base 2016 case (with no retrofit) had zero inverters capable of VWC or FPF.

The volt-watt and fixed power factor tests for each year (2016 and 2021) were run in the base cases and also in two retrofit cases. One retrofit case had 25% of inverters retrofitted to be capable of GSFs, and the second had 50% retrofitted.

A summary of the aggregate power ratings for legacy and advanced inverter types for the VWC and FPF test scenarios is provided in Table 19. Detailed tables for the total rating for each inverter type in each of the six test scenarios are found in Appendix E.

Table 19. Total ratings of different inverter model types for the M34 circuit (top) and the K3L circuit (bottom), for volt-watt and fixed PF tests

Year	Portion of Retrofit Inverters	Legacy PV (MW)	Advanced PV (MW)	Total PV (MW)	Advanced PV : Total PV Ratio (%)
2016	None	3.9	0.0	3.9	0%
	25%	2.9	1.0	3.9	25%
	50%	1.9	1.9	3.9	50%
2021	None	3.9	11.2	15.1	74%
	25%	2.9	12.1	15.1	81%
	50%	1.9	13.1	15.1	87%

Year	Portion of Retrofit Inverters	Legacy PV (MW)	Advanced PV (MW)	Total PV (MW)	Advanced PV : Total PV Ratio (%)
2016	None	3.0	0.0	3.0	0%
	25%	2.3	0.8	3.0	25%
	50%	1.5	1.5	3.0	50%
2021	None	3.0	1.8	4.8	37%
	25%	2.3	2.5	4.8	53%
	50%	1.5	3.3	4.8	68%

4.3 Dynamic Frequency Model Development

The majority of tests only required the feeder voltage source to operate at 60 Hz, except for the FRT tests, which required a more sophisticated system model for frequency dynamics. In order to accomplish this, a simplified model of the bulk system frequency dynamics of the O‘ahu power system was developed, as shown in Figure 38. This model simulated the frequency dynamics of the bulk generators on O‘ahu including simple models of the individual governor and turbine dynamics, PV, and load, as modeled in [13]. The aggregate net power of all generators was fed into a transfer function representing the aggregate inertia and load damping of the entire system. This model was based on one developed in [14]. The model also incorporated underfrequency load shedding and frequency trip settings of distributed PV systems, which are represented in aggregate. It solved only for bulk system frequency dynamics and did not solve

the bulk system power flow. This allowed the model to be solved quickly enough to be used in a discrete real-time simulation with a time step small enough to accurately reproduce a ~60 Hz sinusoidal waveform. Worst-case underfrequency events were simulated by tripping the largest synchronous generator. Overfrequency events were simulated by imposing a large downward step in the load. This frequency dynamic model is an early version of the O'ahu frequency dynamic model being used in a separate Department of Energy funded research project investigating the use of distributed resources for grid frequency support.

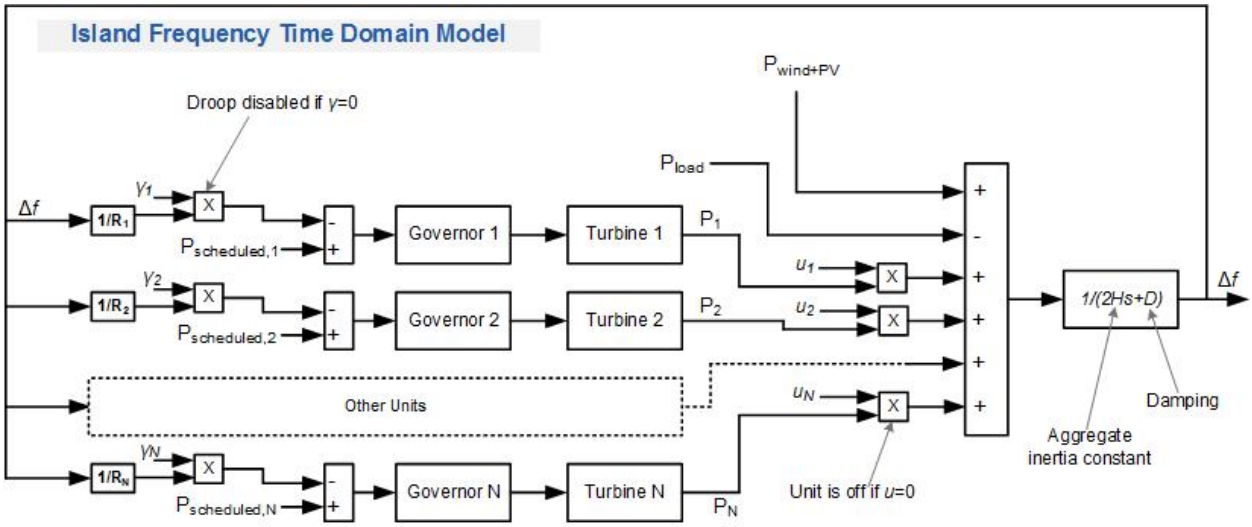

Figure 38. Simplified bulk system frequency dynamic model used for FRT tests

The bulk system frequency model was validated against measured frequency data from historical frequency events. An example of the validation is shown in Figure 39.

As in [3], the frequency calculated in the bulk system model was used to drive the frequency of the feeder voltage sources in the real-time feeder model. Additional details of the bulk system frequency model and its integration with the distribution model will be provided in a future publication. Using this realistic model of the bulk power system allowed realistic frequency events to be simulated. This gave additional confidence that the inverters under test could successfully ride through real N-1 frequency contingency events in the field.

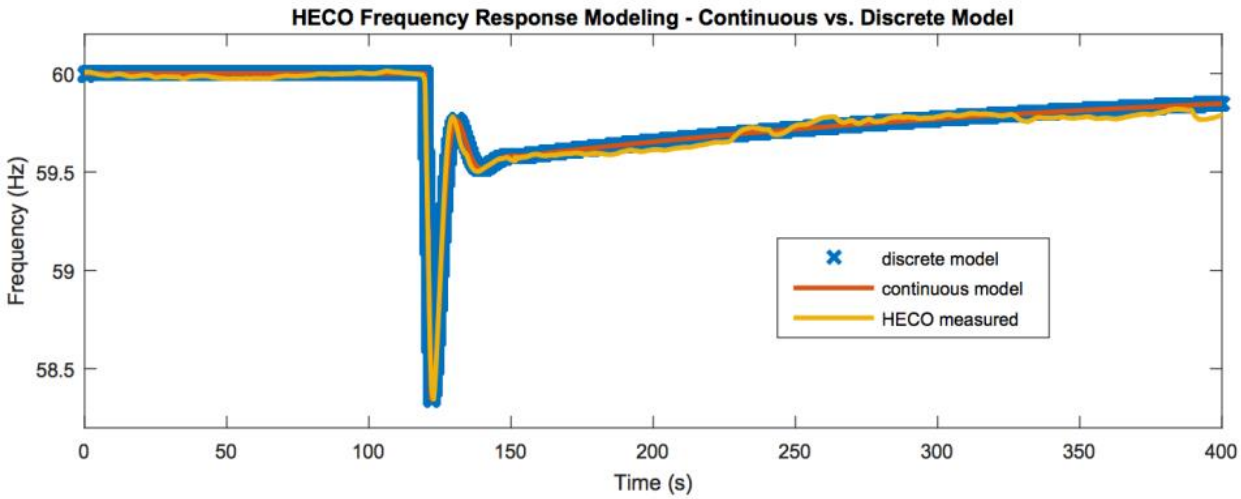

Figure 39. Validation of the real-time frequency dynamic against measured data from a historical frequency event

4.4 OpenDSS to Simulink Model Comparisons

After the reduced order model parameters were loaded into the Simulink model, all node voltages were manually verified to be the same as the reduced-order OpenDSS model voltages for each phase. This was done for each feeder model. For further comparison between the two model types, node voltages comparisons were made between the two models for different PV penetration scenarios. The M34 feeder model was tested with the future, no retrofit PV ratings, with the PV scaled to 0%, 50% and 100% of full rated power. The load scale factor was set to 0.866 (gross daytime minimum load for that feeder) and the source voltage was set to 105% of nominal. Figure 40 shows the comparison of voltages on each phase at each of the primary nodes under the three test scenarios. As seen in the figure and summarized in Table 20, the maximum error for any of these voltages was 0.5%, and the mean error across all voltages was 0.26%.

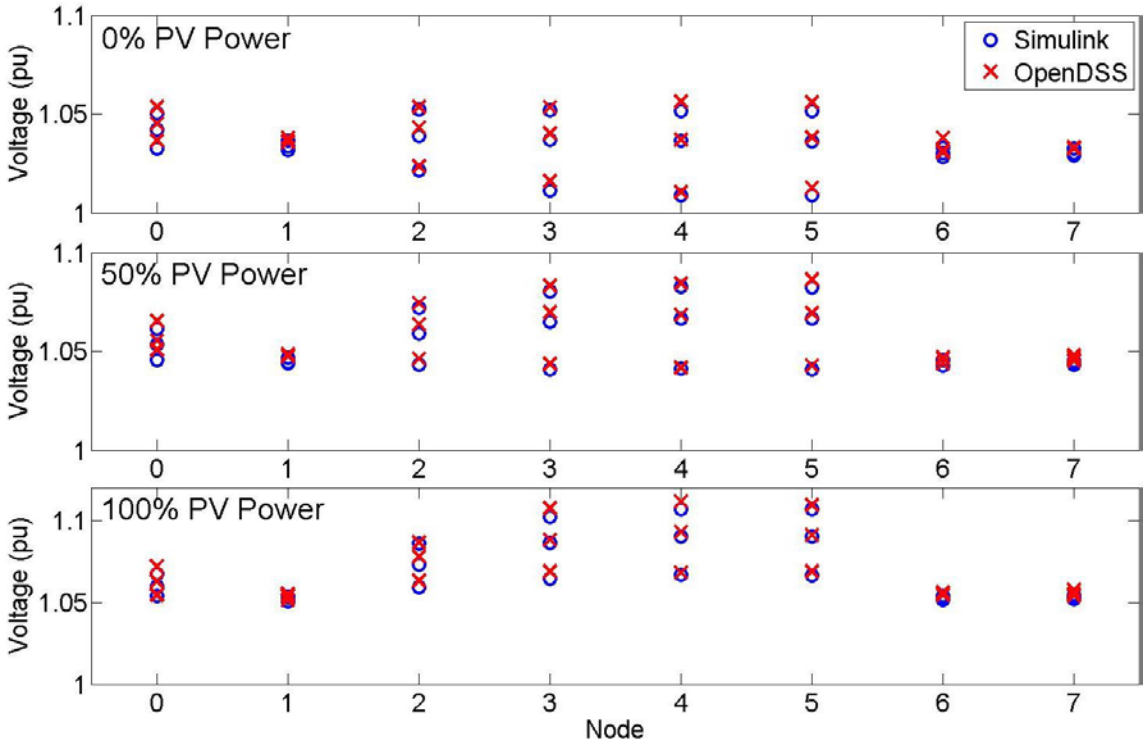

Figure 40. Comparison of phase voltages between reduced order OpenDSS model and Simulink model for 0% (top), 50% (middle) and 100% (bottom) PV inverter output power on the M34 model

Table 20. Mean and maximum phase voltage errors for M34 feeder model at varying PV ratings

	Phase A		Phase B		Phase C	
PV Rating (%)	Mean Error (%)	Max Error (%)	Mean Error (%)	Max Error (%)	Mean Error (%)	Max Error (%)
0	0.23	0.39	0.27	0.50	0.33	0.48
50	0.29	0.47	0.25	0.40	0.27	0.48
100	0.22	0.46	0.27	0.47	0.23	0.43

5 Power Hardware-in-the-Loop Tests

The completed feeder models with different types of modeled inverters were then simulated on the OPAL-RT real-time platform for a series of PHIL tests. The purpose of these tests was to examine the effects that GSFs such as VRT, FRT, FPF, soft start, ramp rate, and VWC would have on node voltages if they were to be deployed on these feeders in the field. Using the reduced order feeder model, a complex system can be executed on a real-time platform, such that PHIL experiments are possible. PHIL testing can provide data that is more reliable than modeling alone, as all of the complexities of the physical hardware are included in the test dynamics.

The PHIL test setup is described first, followed by an explanation of each type of test run under this test platform and the associated test results.

5.1 Test Setup

PHIL testing is a hybrid between software simulations and hardware tests, whereby a physical power hardware device interfaces with a model through intermediary hardware, and the hardware under test is able to dynamically interact with changes in the model and vice versa. The PHIL concept is depicted in Figure 41 for multi-inverter test cases. The real-time model was broken into a master subsystem and two slave subsystems computed in parallel so that the logic could be executed on multiple processing cores and real-time performance could be maintained at an acceptable time step. The reduced order feeder models were executed in the master subsystem, and the test inverters were "connected" to a particular node of choice on the secondary circuit in the feeder models. The output of the model through this connection was a low-voltage sinusoidal signal representing the voltage at the node of choice. The low-voltage signal was routed to the AC power supply (grid simulator), which acted as an amplifier and created the reference voltage for the test inverter. The grid simulator was a bi-directional power supply capable of sourcing and sinking power, and was the same hardware used in the baseline testing. Each physical inverter was also connected to a PV simulator on its DC input, which was used to act as a constant power source for some tests, or was varied to simulate irradiance changes for other tests.

The key concept that "closes the loop" in PHIL testing is that the output current from the hardware inverter was measured with a current transducer, and fed back into the simulation in real time. The node voltage within the model then interacts dynamically with the hardware under test. Concurrently, multiple other elements were interacting with the feeder model in software, which could also lead to changes in the voltage seen at the inverter terminals. First, the feeder model was sourced by a controllable voltage source at the feeder head. In some tests (ramp rate, soft start, VWC and FPF), this was a fixed ideal voltage source. For VRT tests, a pre-programmed voltage profile was executed to simulate sags/swells in the reference voltage. Finally, for FRT tests, the dynamic frequency model described previously was implemented to enforce changes in the source frequency, as depicted in Figure 41. In parallel, all of the PV inverter controller models were running, which had additional impacts on the node voltages of the feeder model depending on their output characteristics.

Additional features were added to the model in the user interface, including the ability to change PV inverter ratings, select VWC functions, create irradiance change profiles, set a FPF, and

trigger data logging from the model, among other things. The use of such features is described in detail in each of the test procedures below. All models were executed at fixed time steps between 180-260 µs, so that the output waveform was updated on the order of 64-92 times per 60 Hz AC cycle.

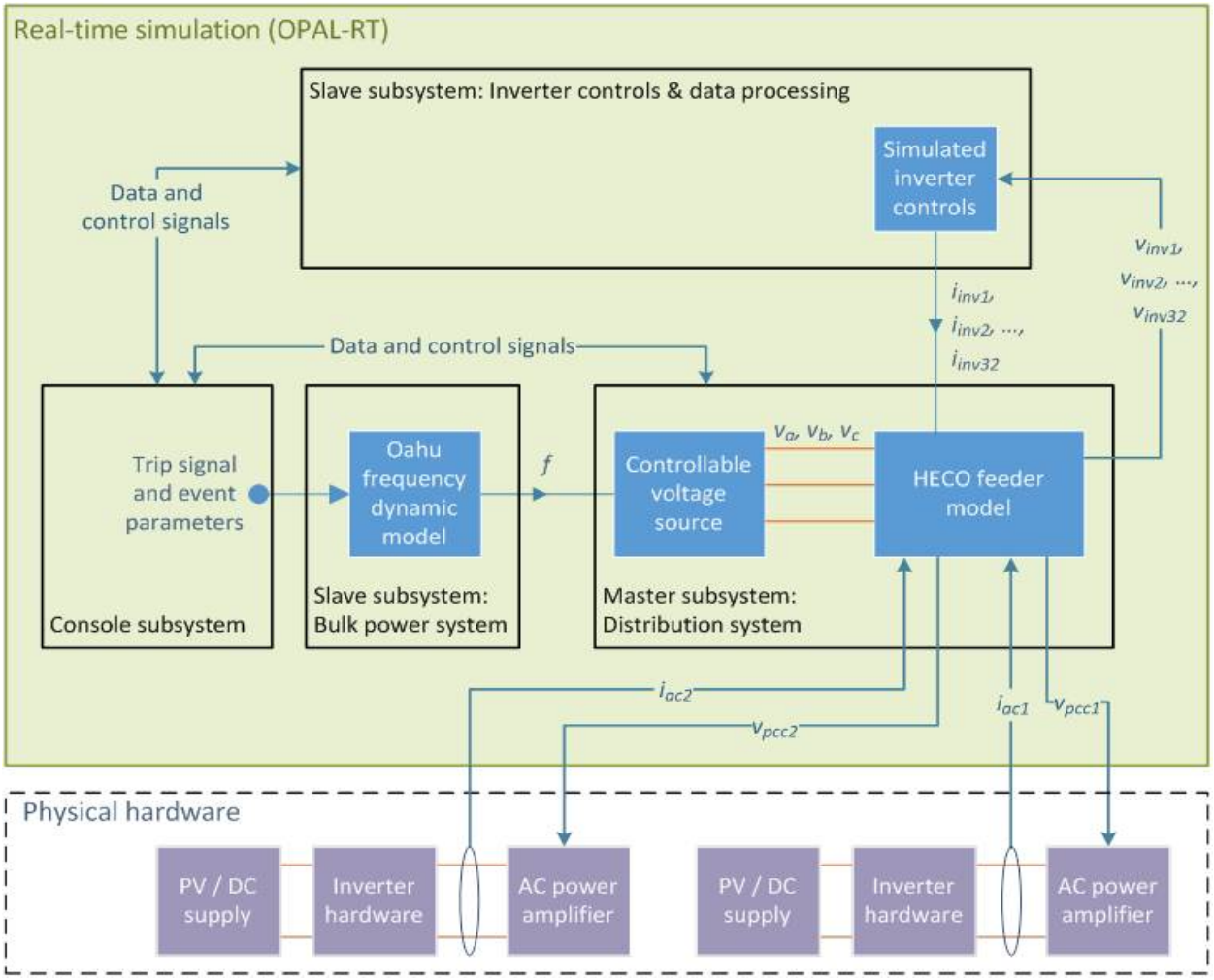

Figure 41. PHIL conceptual block diagram for multiple inverter testing

Several important control features were also implemented in the real-time model in order to improve stability of the model. The noise on the current feedback signal is effectively amplified onto the voltage output signal in this type of model, so efforts are required to attenuate it. The current signal fed back into the model was passed through a first order low-pass filter with cutoff frequencies between 200 Hz and 500 Hz. This low-pass filter introduces a phase shift in the current signal. This phase shift, coupled with compounding delays due to non-zero discrete time steps and latencies in the AC amplifier response time have the effect of creating an increasing phase shift between voltage and current, as observed by the model. This phase shift effectively looks like additional reactive power at the inverter terminals, which can affect the node voltage, depending on the line impedance. In order to counteract this phase shift, a phase-lead filter was introduced on the outgoing voltage signal in order to compensate for the delay. This filter was tuned on a case by case basis, depending primarily on the low-pass filter cutoff frequency. Additional details on these compensation techniques are discussed in [15].

Recalling that the secondary circuit for each model was provided on a 120 V base, several techniques were used to translate that voltage level to the appropriate value for the hardware inverter. Inverter 3 was operated from a 240 V single phase connection, so the node voltage sent to the grid simulator was doubled and the incoming measured current was also doubled. Inverters 1 and 2 were 120/240 V split phase connections, so the single node voltage was applied directly to one of the grid simulator phases, and that same signal was inverted and applied to a second phase, ensuring the appropriate 180 degree phase shift. Finally, Inverter 4 was a three-phase model, so the correct voltages were derived from a modeled transformer connected to the primary, as previously discussed.

The hardware components used to achieve the PHIL testing are summarized in Table 21. All waveform data were recorded at a minimum sampling rate of 20 kHz and all power analyzer data were logged at an update rate of either 50 ms or 100 ms, depending on the nature of the test.

Table 21. Test equipment descriptions

Function	Model	Description / Comments
AC Power Supply (Grid Simulator)	Ametek MX-45	45 kVA, bi-directional, three independent phases
PV Simulator (microinverters)	Ametek TerraSAS	14x 60 V, 14 A and 6x 80 V, 10.5 A
PV Simulator (Inverter 3)	Ametek TerraSAS	600 V, 25 A
PV Simulator (Inverter 4)	Ametek TerraSAS	4x 1000 V, 10 A
Current Sense (Data Acquisition)	Yokogawa 701930 Current Probe	10 mV/A, 150 A max
Current Sense (Data Acquisition)	Yokogawa 701931 Current Probe	10 mV/A, 500 A max
Waveform Acquisition	Yokogawa DL850 Scopecorder	Minimum 20 kHz sampling
Power Analyzer	Yokogawa WT1800	10-20 Hz update rate
Current Sense (Real-Time Feedback)	LEM LF 205-S/SP3	Current transducer, 100 mA : 100 A

For all test series, Inverter 1 was tested alone and was placed on a node on the secondary circuit, far from the transformer that connected to the primary, as shown in Figure 37; Inverters 2 and 3 were always tested concurrently, and were placed on two different nodes on the secondary circuit, far from the transformer; Inverter 4 was always tested alone, but was placed behind a transformer and line impedance, directly connected to the primary, as previously discussed. In the K3L model, Inverter 4 was connected close to the feeder head voltage source, but in the M34 model it was connected at the last node farthest from the feeder head voltage source. These locations were selected to maximize the voltage rise seen by the test inverter.

The VWC and FPF functions were tested more extensively than the other GSFs because the feeder-level effects of those functions were of greater interest.

5.2 Ramp Rate PHIL Tests

Ramp rate tests were of interest to verify that each inverter manufacturer executed the function properly and to observe the changes in system voltages for rapid changes in irradiance. Each

inverter was programmed for the O‘ahu profile (using 0.95 power factor) and three different ramp rates were tested: 10%/minute, 20%/minute and the default ramp rate. Differences in the programmability of each test inverter are discussed below. The irradiance input for the modeled inverters and the hardware inverters was ramped linearly from 20% of maximum rated PV power to >100% of maximum power in 40 seconds. Simulating a uniform irradiance profile across an entire feeder is not intended to re-create a particular real-world situation, but rather to create a scenario that exercises the ramp rate function.

For tests at the default ramp rate, it was expected that the irradiance ramp was much slower than the default rate, so inverters were expected to follow the irradiance change. Tests at the other two ramp rates were expected to achieve full power operation in the expected ramp time.

An example test result for Inverter 1 on the K3L feeder is shown in Figure 42. As in all time-series plots of PHIL data in this report, the dashed lines in these figures show aggregate modeled inverter voltages and powers at primary and secondary nodes, and the solid lines represent hardware inverter values. The numbers in the legend represent node numbers on the feeder primary and secondary. Using the 20%/minute setting, the inverter ramped to the full power rating in approximately 237 seconds (a ramp time of 240 seconds was expected for an 80% change in power). Primary node voltages initially increased due to a rapid addition of real power from legacy inverters with the irradiance change, but slowly decreased as advanced inverters ramped up both real and reactive power outputs. The 0.95 power factor setting results in absorbing Vars, and hence leads to a slight decrease in voltage at this location. The exact effect of FPF will be location-specific.

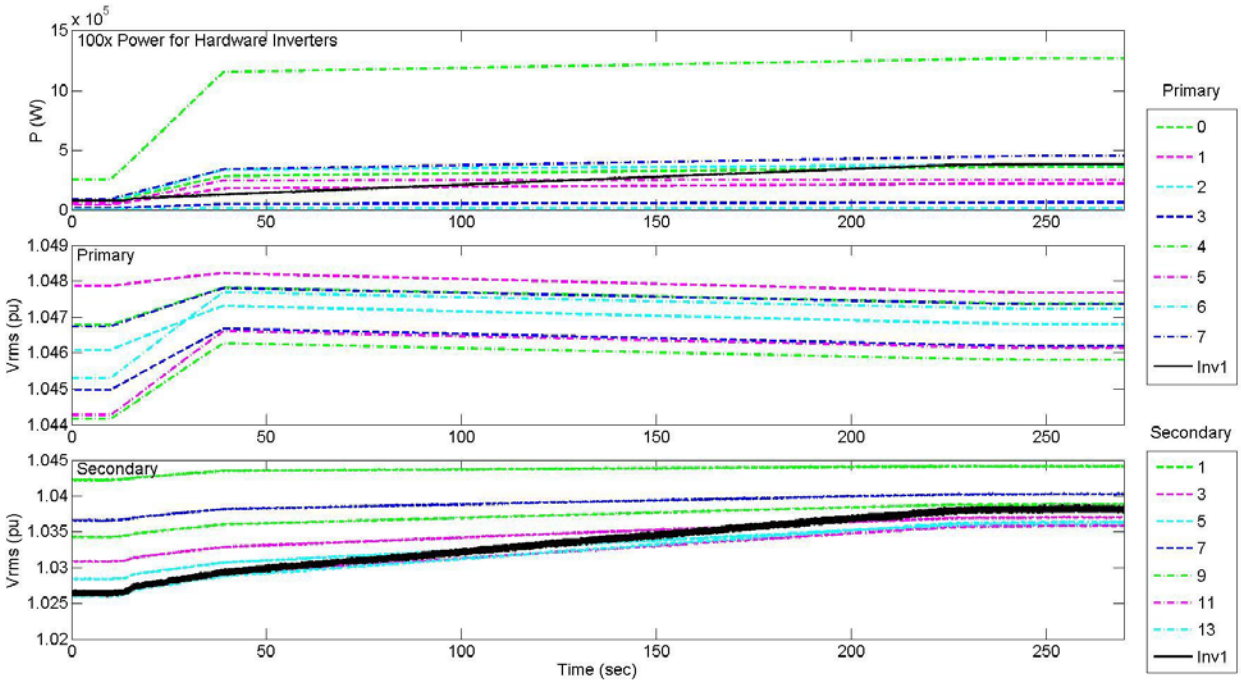

Figure 42. Normal ramp rate of 20% per minute for Inverter 1 on the K3L feeder.

All inverters ramped to full power within the expected ramp time for all test cases, with some deviations due to rounding the programmed ramp rate (e.g. for the 10%/min test case for Inverter 1, the ramp rate was rounded to 0.17%/second rather than 0.1666%/second). The start and final voltages for all test cases is summarized in Table 22. Note that the start and finishing voltages are the same independent of ramp rate, but the amount of time to achieve those voltages depended on the ramp rate. All tests were run with a load factor of 0.450 in the K3L model and 0.866 in the M34 (the respective gross daytime minimum loads); no inverters were placed on the secondary circuit for these tests.

Table 22. Ramp Rate Test Results Summary

Feeder Model	Ramp Rate	Inverter 1		Inverters 2 and 3		Inverter 4	
		Start Voltage (pu)	Final Voltage (pu)	Start Voltage (pu)	Final Voltage (pu)	Start Voltage (pu)	Final Voltage (pu)
K3L	Off	1.026	1.036	1.031	1.056	1.049	1.051
K3L	10%/min	1.026	1.036	N/A*	N/A*	1.049	1.051
K3L	20%/min	1.026	1.036	1.031*	1.056*	1.049	1.051
M34	Off	1.014	1.013	1.016	1.013	1.053	1.058
M34	10%/min	1.014	1.013	N/A*	N/A*	1.053	1.058
M34	20%/min	1.014	1.013	1.016*	1.013*	1.053	1.058

*Inverter 3 did not have programmable ramp rate capability, so it was run at default values with Inverter 2. The minimum ramp rate for Inverter 2 was 1%/sec (60%/min), so the 10%/min test was skipped and the 20%/min test was run at this minimum value.

5.3 Soft Start PHIL Tests

Soft start tests were of interest to verify that each inverter manufacturer executed the function properly and to observe the changes in system voltages due to many inverters restarting simultaneously. Each inverter was programmed for the O‘ahu profile (using 0.95 absorbing power factor) and three different soft start ramp rates were tested: 10%/minute, 1.1%/minute (if available) and the default ramp rate. Differences in the programmability of each test inverter are discussed below. A grid transient was introduced at the beginning of the test to induce a voltage trip in the inverters and initiate a 300 second restart timer. The inverters are required to wait at least 300 seconds before restarting after grid events, and the actual restart times of the modeled inverters was based on the times observed in the baseline tests. Following the 300 second delay, the modeled and hardware inverters ramped at the target rate.

An example test result for Inverters 2 and 3 on the M34 feeder is shown in Figure 43. Programmed with the 10%/minute setting, all inverters were first intentionally tripped offline due to a large voltage transient at the beginning of the test. The inverters then ramped to the full power rating in approximately ten minutes, as expected. Primary node voltages initially increased due to a rapid addition of real power from legacy inverters upon restart, but slowly decreased as advanced inverters ramped up both real power and (absorptive) reactive power.

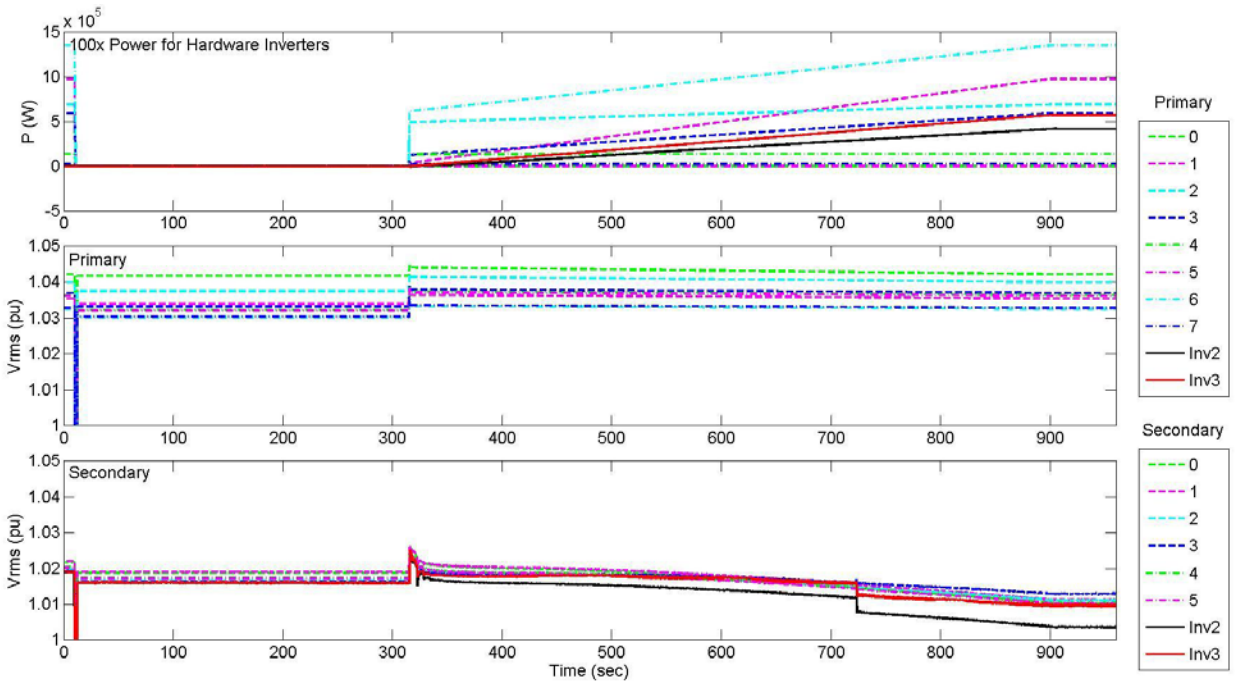

Figure 43. Soft start ramp rate of 10% per minute for Inverters 2 and 3 on the M34 feeder.

All inverters ramped to full power within the expected ramp time for all test cases, with some exceptions due to limitations on soft start ramp rates. The start and final voltages for all test cases are summarized in Table 23. Note that the final voltages are the same for a given test regardless of ramp rate, but the amount of time to achieve those voltages depended on the ramp rate. The same is true of the starting voltages. All tests were run with a load factor of 0.450 in the K3L model and 0.866 in the M34; no inverters were placed on the secondary circuit for these tests. The ramp times used for the modeled inverter were derived from baseline test results.

Table 23. Soft Start Test Results Summary

Feeder Model	Ramp Rate	Inverter 1		Inverters 2 and 3		Inverter 4	
		Start Voltage (pu)	Final Voltage (pu)	Start Voltage (pu)	Final Voltage (pu)	Start Voltage (pu)	Final Voltage (pu)
K3L	Off	1.024	1.036	1.048	1.051	1.024	1.056
K3L	10%/min	1.024	1.036	1.048	1.051	1.024	1.056
K3L	1.1%/min	N/A*	N/A*	N/A*	N/A*	1.024	1.056
M34	Off	1.016	1.013	1.052	1.058	1.016	1.013
M34	10%/min	1.016	1.013	1.052	1.058	1.016	1.013
M34	1.1%/min	N/A*	N/A*	N/A*	N/A*	1.016	1.013

***See discussion below**

Inverter 1 had a minimum ramp rate of 6%/min, so the 1.1%/min test was not run. Likewise, Inverter 4 had a minimum ramp rate of 10%/min, so the 1.1%/min test was not run. Inverter 2 had a minimum ramp rate of 6%/min, and was run at this rate with Inverter 3 for the 1.1%/min test. Inverter 3 could only be programmed for whole number percentage point ramp rates, so the 1.1%/min test was run at 1%/min.

5.4 Voltage Ride-Through PHIL Tests

5.4.1 Voltage Ride-Through Test Description

For VRT tests, inverters were operated under IEEE 1547-2003 VRT settings and later with Rule 14H settings in order to observe the effects of having a large amount of inverters trip off simultaneously versus have a smaller portion trip off while advanced inverters rode through the event. The modeled inverters were programed with the ratings shown in Table 24. Inverter ratings were based on Hawaiian Electric records of VRT and FRT capabilities of installed PV systems. Advanced inverters were capable of Rule 14H ride-through settings, but all legacy inverters had IEEE 1547-2003 default settings.

Table 24. Aggregate PV Inverter Ratings at Each Primary Node for VRT and FRT Tests

Primary node	Inverter Ratings (kW), M34, present (2016), No retrofit				Inverter Ratings (kW), K3L, present (2016), No retrofit			
	Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other	Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
0	0.0	0.0	0.0	0.0	201.3	46.0	66.9	51.4
1	14.6	22.1	45.2	940.9	111.8	48.1	12.2	50.6
2	419.9	69.6	58.4	149.4	206.0	111.7	17.9	43.4
3	74.2	49.8	60.7	429.9	17.4	24.1	13.4	9.1
4	89.1	6.0	40.6	5.0	468.7	635.5	95.2	78.3
5	0.0	0.0	0.0	0.0	128.8	114.0	3.0	7.7
6	425.1	188.9	130.5	644.6	11.8	0.0	0.0	0.0
7	19.8	0.0	7.1	0.0	150.9	139.0	134.3	34.7

A pair of pre-defined voltage profiles was selected for both high voltage ride through (HVRT) and low voltage ride through (LVRT) scenarios. These profiles were designed to fully exercise the Rule 14H trip limits in both time and magnitude at all OVR and UVR levels. The legacy inverters were expected to trip while the Rule 14H inverters were expected to ride through the event. The tests were repeated on both feeder models, with each set of ride-through parameters, and for both LVRT and HVRT cases, for a total of eight different test cases per inverter.

The HVRT ride through time is the same between IEEE 1547-2003 and Rule 14H - up to one second. However, Rule 14H requires a ride through duration of 0.92 seconds, whereas IEEE1547 only says that inverters must trip *within* 1.0 seconds (i.e. they may trip anywhere between 0 and 1.0 seconds after the start of the voltage event). In order to create a test case that would trip legacy inverters, all the legacy inverters were programmed with a trip time of 0.50 seconds for voltages between 110% and 120% of nominal. The voltage profile included an overvoltage

transient lasting ~0.70 seconds in this region, which forced inverters modeled with IEEE 1547-2003 settings to trip, but allowed inverters modeled with Rule 14H settings to ride through. When programmed with Rule 14H settings, hardware inverters were expected to ride through this event, but with IEEE 1547-2003 settings, hardware inverters could optionally trip or stay online, depending on the internal defaults under this profile. For legacy inverters in the field that are programmed with IEEE 1547-2003 trip settings, both tripping and remaining online are allowed for voltage events between 110% and 120% of nominal lasting between 0 and 1 second. In reality, some will trip very quickly and others will ride through up to almost one second.

The phase lead filter for phase angle correction was not implemented in this model since additional reactive power observed from the inverters was not a primary concern. No inverters were included on the secondary circuits. K3L models were run with a load factor of 0.45 and M34 models were run with a load factor of 0.86. Modeled and hardware inverters were all run at 100% output power throughout the test.

5.4.2 Voltage Ride-Through Test Results

A representative LVRT test case is shown in Figure 44 for the K3L feeder model, using Inverter 1. The voltage profile was designed to stay around 60% of nominal voltage for ~8.5 seconds, move to 80% of nominal for an additional ~9.0 seconds, and then stay near 94% of nominal for an additional ~5.0 seconds. As seen in the figure, all inverters tripped during the undervoltage event when all were set for the IEEE 1547-2003 trip settings, including the hardware inverters (left). When the ride-through capable inverters were set for Rule 14H settings, the Rule 14H portion remained online – including the hardware inverter – throughout the entire event (right). Note that each primary node has many legacy inverters and some ride-through capable inverters connected. Thus the total inverter power at each primary node is significantly reduced following the voltage event due to the legacy portion tripping, but he power does not drop to zero because the ride-through capable portion continues to produce power. As expected, there was some additional power reduction during the low voltage event due to internal current limits on the inverters, as in the baseline tests.

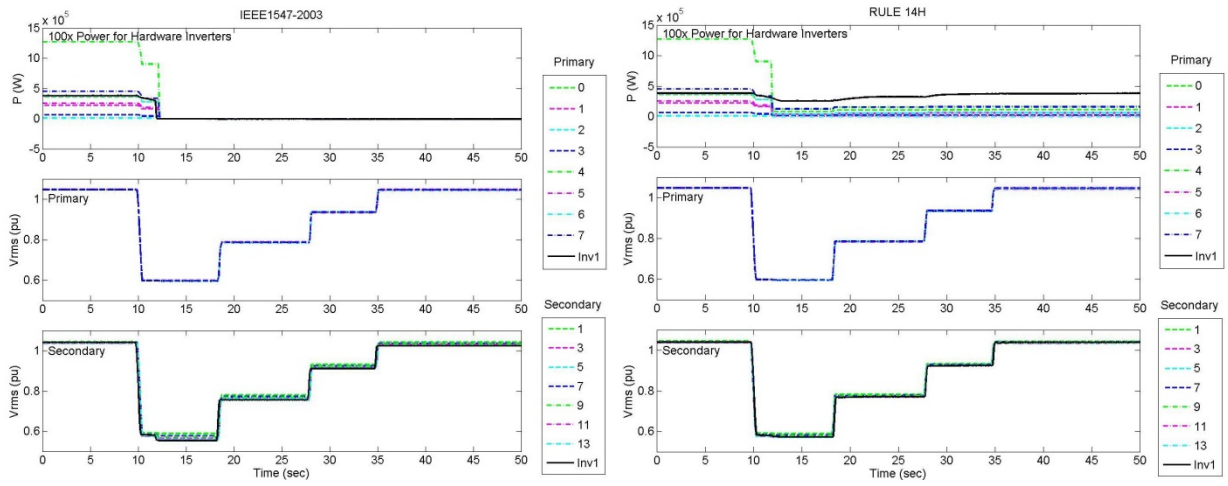

Figure 44. Inverter 1 LVRT test cases using IEEE 1547-2003 settings (left) and Rule 14H settings (right), K3L model

A representative HVRT test case is shown in Figure 45 for the M34 feeder mode using Inverters 2 and 3. This voltage profile was designed to reach ~115% of nominal for <1 second, and then dwell at ~108% of nominal for an additional ~14 seconds. Just as in the LVRT test cases, all inverters tripped when set to IEEE 1547-2003 settings, but only the legacy proportion tripped for the Rule 14H test.

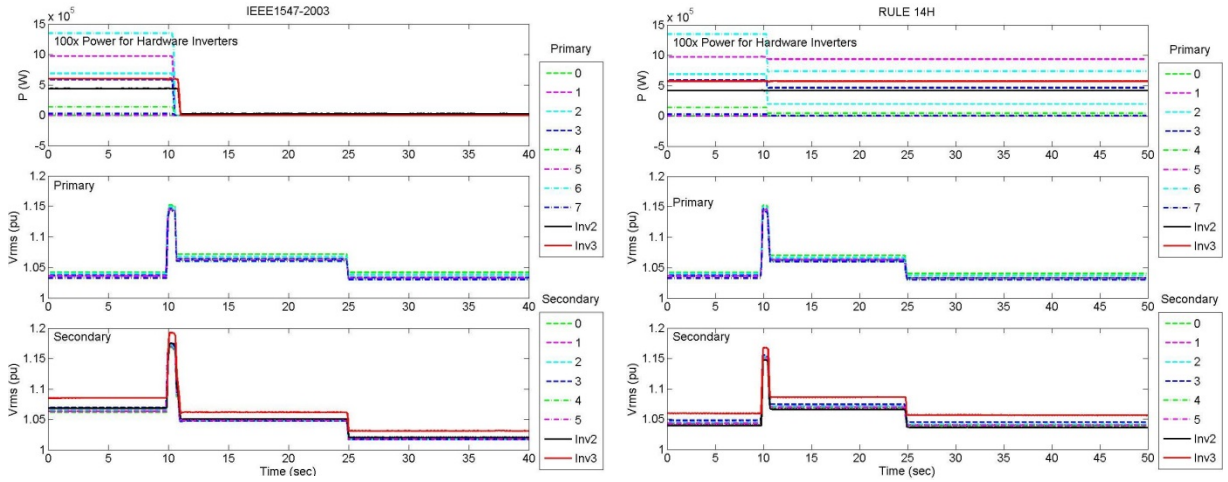

Figure 45. Inverters 2 and 3 HVRT test cases using IEEE 1547-2003 settings (left) and Rule 14H settings (right), M34 model

A summary of all VRT test results is shown in Table 25, including the hardware inverter terminal voltages both before and after the ride-through event. The "Ride Through" column indicates whether the hardware inverter(s) remained connected. As noted above, the expected behavior of HVRT tests with 1547-2003 settings is indeterminate – both tripping and remaining online are allowed for the HVRT voltage profile, since the inverters are allowed to trip anytime between 0 and 1 second into the event. For all Rule 14H HVRT and LVRT tests, the inverters were required to ride through, and did. The voltages reported for Inverter 4 (three-phase) are the highest voltage of any of the three phases. In general, there was a voltage drop of several percentage points when a significant number of inverters tripped due to IEEE 1547-2003 settings. Otherwise voltage deviations were relatively small. All tests cases where Table 25 indicates that "some" inverters rode through occurred on HVRT tests on microinverters. In these tests, a small portion of the microinverters tripped, most likely due to the fact that there is an increasing voltage rise as you move up the string of inverters, leading to some inverters observing voltage magnitudes above the 120% threshold.

Table 25. VRT Test Results Summary

Feeder Model	HVRT / LVRT	Trip Settings	Inverter Number	Ride Through (Y/N)	Start Voltage (V)	Final Voltage (V)
K3L	HVRT	IEEE1547	1	Yes	1.041	1.040
K3L	HVRT	Rule 14H	1	Yes	1.039	1.038
K3L	LVRT	IEEE1547	1	No	1.040	1.023
K3L	LVRT	Rule 14H	1	Yes	1.040	1.038
M34	HVRT	IEEE1547	1	Some	1.037	1.034
M34	HVRT	Rule 14H	1	Yes	1.025	1.022
M34	LVRT	IEEE1547	1	No	1.037	1.019
M34	LVRT	Rule 14H	1	Yes	1.025	1.021
K3L	HVRT	IEEE1547	2	Some	1.065	1.037
K3L	HVRT	Rule 14H	2	Yes	1.054	1.053
K3L	LVRT	IEEE1547	2	No	1.065	1.025
K3L	LVRT	Rule 14H	2	Yes	1.055	1.054
M34	HVRT	IEEE1547	2	Yes	1.068	1.020
M34	HVRT	Rule 14H	2	Yes	1.039	1.036
M34	LVRT	IEEE1547	2	No	1.068	1.019
M34	LVRT	Rule 14H	2	Yes	1.039	1.036
K3L	HVRT	IEEE1547	3	No	1.076	1.048
K3L	HVRT	Rule 14H	3	Yes	1.056	1.055
K3L	LVRT	IEEE1547	3	No	1.075	1.038
K3L	LVRT	Rule 14H	3	Yes	1.070	1.070
M34	HVRT	IEEE1547	3	Yes	1.085	1.031
M34	HVRT	Rule 14H	3	Yes	1.059	1.057
M34	LVRT	IEEE1547	3	No	1.085	1.030
M34	LVRT	Rule 14H	3	Yes	1.060	1.056
K3L	HVRT	IEEE1547	4	Yes	1.057	1.057
K3L	HVRT	Rule 14H	4	Yes	1.051	1.050
K3L	LVRT	IEEE1547	4	No	1.057	1.047
K3L	LVRT	Rule 14H	4	Yes	1.051	1.050
M34	HVRT	IEEE1547	4	Yes	1.061	1.057
M34	HVRT	Rule 14H	4	Yes	1.055	1.050
M34	LVRT	IEEE1547	4	No	1.061	1.051
M34	LVRT	Rule 14H	4	Yes	1.055	1.051

5.5 Frequency Ride-Through PHIL Tests

5.5.1 Frequency Ride-Through Test Description

For FRT tests, inverters were operated under IEEE 1547-2003 FRT settings and later with Rule 14H settings in order to observe the effects of having a large amount of inverters trip off simultaneously versus having a smaller portion trip off while advanced inverters rode through the event. The modeled inverters were programed with the ratings shown in Table 24, above. Inverter ratings were based on Hawaiian Electric records of VRT and FRT capabilities of installed PV systems. Advanced inverters were capable of Rule 14H ride-through settings, but all legacy inverters had IEEE 1547-2003 default trip settings.

A pair of frequency profiles was created for both high frequency ride-through (HFRT) and low frequency ride-through (LFRT) scenarios. These profiles simulated rapid loss of load and loss of generation scenarios, and make use of the O‘ahu frequency model previously discussed; they were designed to emulate frequency events on the severe end of the plausible range. The expected behavior was for IEEE 1547-2003 inverters to trip while Rule 14H inverters would ride-through the event. The tests were repeated on both feeder models, with each set of ride-through parameters, and for both LVRT and HVRT cases, for a total of eight different test cases per inverter.

The phase lead filter for phase angle correction was not implemented in this model since additional reactive power observed from the inverters was not a primary concern. No inverters were included on the secondary circuits. K3L models were run with a load factor of 0.45 and M34 models were run with a load factor of 0.86. Modeled and hardware inverters were all run at 100% output power throughout the test.

5.5.2 Frequency Ride-Through Test Results

A representative LFRT test case is shown in Figure 46 for the K3L feeder model, using Inverters 2 and 3. The frequency transient reached a minimum value of 58.36 Hz and stabilized in a 5-10 second time window. As seen in the figure, all inverters tripped during the underfrequency event when all were set for the IEEE 1547-2003 trip settings, including the hardware inverters (left). When the ride-through capable inverters were set for Rule 14H settings, the Rule 14H portion remained online – including the hardware inverters – throughout the entire event (right). There was some voltage ripple during the rapid changes in frequency in the Rule 14H tests, but inverter power remained relatively stable.

A representative HFRT test case is shown in Figure 47 for the M34 feeder model using Inverter 4. The frequency transient reached a maximum value of 60.90 Hz and recovered in a 5-10 second time window. Note that overfrequency tripping of legacy PV inverters on other feeders was not modeled in these tests; if it were modeled it would result in a second contingency event, possibly including underfrequency conditions. As seen in the figure, all inverters likewise tripped during the first overfrequency event when set for the IEEE1547 settings (left), but a portion remained online – including the hardware inverters – throughout the entire event when set for Rule 14H settings (right). There was again some voltage ripple during the rapid changes in frequency in the Rule 14H tests, but inverter power remained relatively stable.

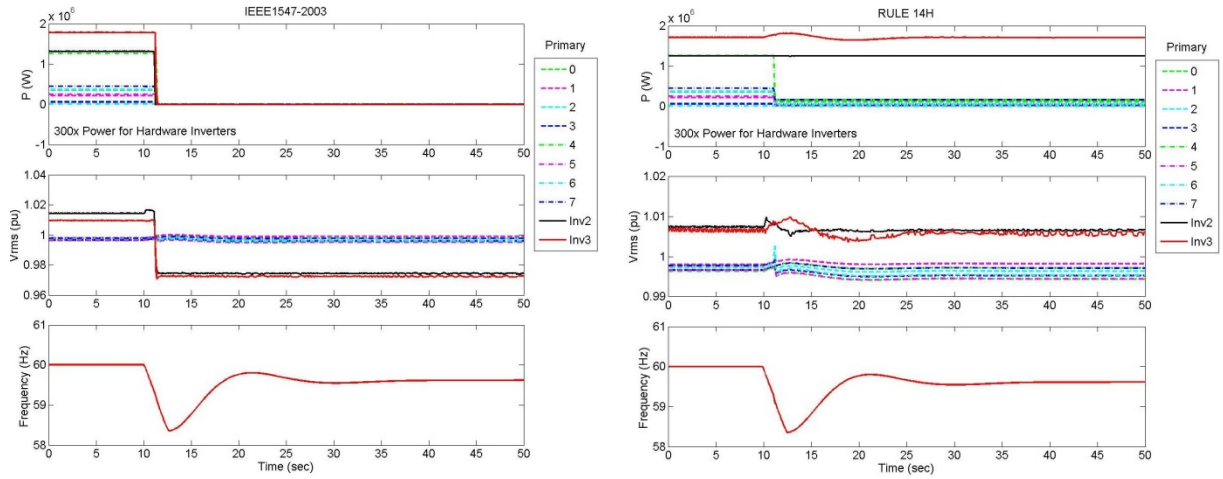

Figure 46. Inverters 2 and 3 LFRT test cases using IEEE1547-2003 settings (left) and Rule 14H settings (right), K3L model

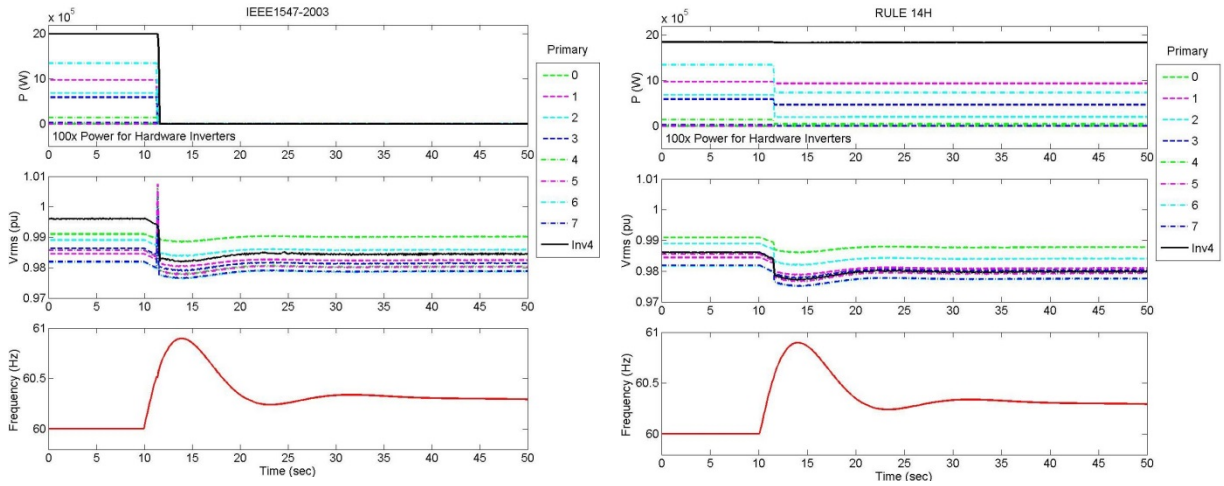

Figure 47. Inverter 4 HFRT test cases using IEEE1547-2003 settings (left) and Rule 14H settings (right), M34 model

A summary of all test results is shown in Table 26, including the inverter terminal voltages both before and after the ride through event. The response of the hardware inverter is noted in the column marked “Ride Through”. As expected, when set for the IEEE 1547-2003 settings, the hardware inverters tripped in all tests. When set for Rule 14H settings, they rode through all events, also as expected. Thus these tests validate the ability of the inverters tested to ride through realistic worst-case frequency events. Just like in the VRT tests, there was a voltage drop of several percentage points when a significant number of inverters tripped due to IEEE1547 settings. Otherwise voltage deviations were relatively small. Because the PHIL tests only captured the behavior of the PV inverters on a single feeder, the effect on frequency is not captured. This effect will be captured in ongoing work under the Grid Modernization Laboratory Call regional partnership for Hawai‘i, which is not covered in this report.

Table 26. FRT Test Results Summary

Feeder Model	HFRT / LFRT	Trip Settings	Inverter Number	Ride Through (Y/N)	Start Voltage (V)	Final Voltage (V)
K3L	HFRT	IEEE1547	1	No	0.992	0.974
K3L	HFRT	Rule 14H	1	Yes	0.991	0.990
K3L	LFRT	IEEE1547	1	No	0.993	0.973
K3L	LFRT	Rule 14H	1	Yes	0.991	0.991
M34	HFRT	IEEE1547	1	No	0.978	0.960
M34	HFRT	Rule 14H	1	Yes	0.966	0.960
M34	LFRT	IEEE1547	1	No	0.978	0.966
M34	LFRT	Rule 14H	1	Yes	0.965	0.965
K3L	HFRT	IEEE1547	2	No	1.016	0.975
K3L	HFRT	Rule 14H	2	Yes	1.008	1.007
K3L	LFRT	IEEE1547	2	No	1.014	0.974
K3L	LFRT	Rule 14H	2	Yes	1.007	1.007
M34	HFRT	IEEE1547	2	No	1.016	0.963
M34	HFRT	Rule 14H	2	Yes	0.986	0.980
M34	LFRT	IEEE1547	2	No	1.015	0.967
M34	LFRT	Rule 14H	2	Yes	0.986	0.985
K3L	HFRT	IEEE1547	3	No	1.010	0.973
K3L	HFRT	Rule 14H	3	Yes	1.006	1.006
K3L	LFRT	IEEE1547	3	No	1.010	0.972
K3L	LFRT	Rule 14H	3	Yes	1.006	1.005
M34	HFRT	IEEE1547	3	No	1.032	0.974
M34	HFRT	Rule 14H	3	Yes	1.006	0.999
M34	LFRT	IEEE1547	3	No	1.019	0.965
M34	LFRT	Rule 14H	3	Yes	1.006	1.004
K3L	HFRT	IEEE1547	4	No	1.011	1.000
K3L	HFRT	Rule 14H	4	Yes	1.001	1.000
K3L	LFRT	IEEE1547	4	No	1.011	1.000
K3L	LFRT	Rule 14H	4	Yes	1.001	1.001
M34	HFRT	IEEE1547	4	No	0.996	0.984
M34	HFRT	Rule 14H	4	Yes	0.986	0.980
M34	LFRT	IEEE1547	4	No	0.996	0.987
M34	LFRT	Rule 14H	4	Yes	0.986	0.983

5.6 Volt-Watt with Fixed Power Factor PHIL Tests

Both VWC and FPF function have the potential to mitigate overvoltage events in the field where large proportions of distributed PV exist, and it is of interest to understand the impacts that each function would have in the field. A series of VWC curves and FPF values were selected for these tests to evaluate such impacts and help inform how such functions may be deployed in the field.

5.6.1 VWC with FPF Test Description

The objective in each test setup was to create a steady-state overvoltage condition in order to trigger the VWC function, running in conjunction with various power factor values. The mechanism to force such a condition was to quickly ramp irradiance from a low level to a full power level at the modeled inverters and at the hardware inverter. Typical tests would linearly ramp irradiance such that the available input power to the inverters ramped from 20% of maximum PV power to over 100% of maximum PV power over the course of 40 seconds. Although this represents a very fast change in cloud cover across a feeder area, it is still representative of a simplified real-world situation, and allowed tests to be run at a reasonably quick pace.

Overvoltage situations were enforced through several variables in addition to the irradiance change. The load factor (multiplier on peak loads on the primary) was adjusted in each feeder model, with lower load factors creating lower loads and higher voltages. Additionally, some legacy PV inverters were added to the secondary circuit to force back-feeding of the secondary transformer and cause larger voltage rises; the only inverter(s) capable of VWC and FPF on the secondary were the hardware inverters under test. Finally, the source voltage at the feeder head was always set to 105% of nominal, so that voltages across the network started up near the top of ANSI Range A. In real-world situations, a variety of other situations can lead to raised voltage levels similar to those tested here, including:

- Long secondary main conductors
- Long secondary service drops
- Too many customers on a service transformer
- Small conductors on either primary and/or secondary
- Large load at specific locations on a circuit, which requires high LTC taps to account for voltage drop

The PHIL tests did not attempt to directly emulate each of these conditions. Instead they created high voltage conditions using the means described earlier. The VWC curves were designed so they became active at or just above the top of ANSI Range A (105% of nominal). The test scenarios were designed so that the hardware inverter voltage was just below the VWC active region when the inverters were at low power at the beginning of the tests.

Recall that the inverters on the eight primary nodes in each feeder model consisted of a mix of legacy Enphase inverters, GSF-capable Enphase inverters, generic legacy inverters, and generic GSF-capable inverters. The aggregate power ratings of each type of inverter were determined from Hawaiian Electric data and projections, as described in Section 4.

For each test case, the input irradiance at both hardware and modeled inverters was linearly ramped from a starting value to a final value in 40 seconds. All inverters (modeled and hardware) were programmed for a 50 second time response for the VWC function, and all tests were run for at least 150 seconds after completion of the irradiance ramp in order to ensure that steady-state operation had been reached. All time series plots show voltages and powers throughout the network as recorded by the model, but hardware inverter voltages and power are

reported from the power analyzer in the lab. An analysis of the effects on node voltage, the change in node voltage, and the change in inverter power is provided for each of the test cases below.

There were several variables of interest across all test cases, so a different combination of these variables was used for the different hardware inverters in order to maximize the number of variables investigated within the time available for this study. The variables tested included:

- Power Factor: 0.90, 0.95, 0.98 or 1.00 (absorbing reactive power)
- Volt-Watt Curve: None, Mild, Medium or Aggressive (as defined in baseline tests)
- VWC Mode: Snapshot ($P_{pre\text{-}disturbance}$) or Nameplate ($P_{max}$) (as defined in baseline tests)
- PV Ratings: Six combinations based on present vs. future and the retrofit proportion (0%, 25% or 50%); summarized in Appendix E.
- Feeder Model: K3L or M34

For each inverter, Table 27 highlights the variables of interest for each test inverter. Every combination of each of the listed variables was completed, leading to the total number of tests found in the last row.

Table 27. Test case summary for VWC with FPF PHIL tests

Parameter	Inverter 1	Inverter 2 and Inverter 3	Inverter 4
Power Factor	0.90, 0.95, 0.98, 1.00	0.90, 0.95, 1.00	0.90, 0.95,1.00
VWC Curves	None, Moderate, Aggressive	None, Moderate, Mild	None, Moderate, Aggressive, Mild
VWC Mode	Snapshot, Nameplate	Nameplate	Nameplate
PV Ratings (Present/Future)	Future (2021)	Present (2016), Future (2021)	Future (2021)
Retrofit Proportion	0%	0%, 25%, 50%	0%
Feeder Models	K3L, M34	K3L, M34	K3L, M34
Total Test Count	**40***	**108**	**24**

***The product of all variables for Inverter 1 leads to 48 tests, but running snapshot and nameplate modes with VWC turned off is redundant, thus eliminating eight test cases**

Because the tests of Inverter 1 and Inverter 4 present simpler cases where only the 2021 scenarios with no retrofitting is examined, those tests are presented first, followed by the more complex case of Inverters 2 and 3, where all six combinations of {present, future} and {0%, 25%, 50%} retrofit are examined.

5.6.2 VWC with FPF Test Results

For each test inverter, an example set of time-series plots is shown to highlight the changes in circuit and inverter behavior when a particular variable of interest is changed. All time-series plots show the total power at each primary node from all four types of modeled inverter, along with the hardware inverter output power (typically scaled up to be legible on the plot).

Summary plots of all tests for each inverter on each feeder are also presented to highlight the differences in inverter node voltages and inverter output power for all test cases. Test result data are compiled into tables in Appendix F, but all of the same information is embedded in the summary plots in this section.

Table 19, which showed the total ratings of inverters of various types for the various test scenarios, is reproduced here as Table 28 for convenience. When viewing the VWC and FPF test results below, it is useful to keep in mind both of the following:

- The aggregate ratings of legacy PV and advanced PV
- The ratio of legacy to advanced PV in each test scenario.

Specifically, note that the M34 feeder reaches very high ratios of advanced to legacy PV in the 2021 cases. Recall also that each cell in the second and third columns of Table 28 represents the sum of 16 aggregate inverters (two inverter types at each of eight nodes), listed in Appendix E.

Table 28. Total ratings of different inverter model types for the M34 circuit (top) and the K3L circuit (bottom), for volt-watt and fixed PF tests

Year	Portion of Retrofit Inverters	Legacy PV (MW)	Advanced PV (MW)	Total PV (MW)	Advanced PV : Total PV Ratio (%)
2016	None	3.9	0.0	3.9	0%
	25%	2.9	1.0	3.9	25%
	50%	1.9	1.9	3.9	50%
2021	None	3.9	11.2	15.1	74%
	25%	2.9	12.1	15.1	81%
	50%	1.9	13.1	15.1	87%

Year	Portion of Retrofit Inverters	Legacy PV (MW)	Advanced PV (MW)	Total PV (MW)	Advanced PV : Total PV Ratio (%)
2016	None	3.0	0.0	3.0	0%
	25%	2.3	0.8	3.0	25%
	50%	1.5	1.5	3.0	50%
2021	None	3.0	1.8	4.8	37%
	25%	2.3	2.5	4.8	53%
	50%	1.5	3.3	4.8	68%

The ratios of advanced PV to total PV in the last column of Table 28 can be used to classify test scenarios into three groups in terms of the proportions of advanced PV, which readers will see was a major driver of the impact of GSFs. The 2016 scenarios generally represent low to moderate advanced inverter proportions. The 2021 K3L scenarios represent moderate advanced

inverter proportions. And the M34 scenarios represent high advanced inverter proportions. It is worth noting that none of these scenarios examines the case of very low but non-zero proportions of advanced inverters.

5.6.2.1 Inverter 1 Test Results

The variables of interest for Inverter 1 testing were nameplate vs. snapshot mode, power factor, and VWC curve type. All tests were completed with an irradiance ramp between 200-1000 W/m^2 in 40 seconds. Four 6.0 kW inverters were added to the K3L secondary circuit to increase the voltage, and the load factor was set to 0.450. Four 4.5 kW inverters were added to the M34 secondary to increase the voltage, and the load factor was set to 0.866.

The Inverter 1 tests were run using the future (2021) test case with no retrofitting of legacy inverters. In this scenario, 37% of the total PV on K3L was capable of grid support, and 74% of the total PV on M34 was capable of grid support. The aggregate ratings of each type of inverter at each primary node are shown in Table 29.

Table 29. Aggregate PV Inverter Ratings at Each Primary Node for Inverter 1 VWC and FPF Tests

Primary node	Inverter Ratings (kW), M34, future (2021), No retrofit				Inverter Ratings (kW), K3L, future (2021), No retrofit			
	Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other	Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
0	0.0	0.0	0.0	0.0	268.2	97.4	133.5	48.5
1	59.8	963.0	85.9	618.3	124.0	98.6	58.9	46.8
2	478.3	219.0	1037.5	1899.4	224.0	155.0	106.3	73.6
3	134.9	479.6	409.2	2459.1	30.8	33.2	14.6	319.7
4	129.7	11.1	263.5	1026.2	563.8	713.8	282.1	329.3
5	0.0	0.0	0.0	0.0	131.8	121.7	62.5	57.8
6	555.6	833.5	1479.0	1869.1	11.8	0.0	5.6	0.0
7	26.9	0.0	29.2	0.0	285.2	173.7	142.0	86.5
Total	1385.1	2506.1	3304.2	7872.1	1639.4	1393.4	805.6	962.2

The effect of the moderate VWC and non-unity power factor is demonstrated in Figure 48 and Figure 49. The dashed lines in these figures are related to aggregate modeled inverters at each primary node, and the solid lines represent hardware inverter values. The numbers in the legend represent node numbers on the feeder primary and secondary, as defined in Section 4. Figure 48 is a baseline test case with VWC disabled and all inverters operating at unity power factor, which caused a voltage rise up to 108.2% of nominal at the hardware inverter location. When 0.95 power factor with the moderate VWC curve was implemented in Figure 49, output power was reduced through VWC to 44% and the voltage rise was reduced by 0.013 pu. This figure additionally shows the reactive power that was absorbed by the modeled inverters and the hardware inverter, further mitigating the voltage rise.

Figure 50 shows a summary of all test cases for the M34 feeder. These plots show the final voltage measured at the inverter terminals (left), the change in inverter terminal voltage from the beginning to the end of each test (middle), and the final output power of the hardware inverter (right).

When viewing these results, recall that these tests looked at a scenario with 74% of PV using advanced inverters, a high proportion. With that in mind, the plots in Figure 50 demonstrate the following observations for the 2021 M34 feeder:

- VWC was only active for tests at or near unity power factor. In other tests, the VWC curve type had little impact on the inverter voltage, as non-unity power factor operation tended to reduce the voltage enough that VWC was not active in most cases.
- When active, the aggressive VWC caused significant real power reduction, as expected, but resulted in minimal changes in the inverter voltage because test conditions tended to produce high voltages even in the absence of the grid-supportive hardware inverter.
- The relative effect of nameplate (P_{max}) versus snapshot ($P_{pre\text{-}disturbance}$) modes of VWC was small because, for the reasons stated above, VWC on the whole had a small impact in this set of tests.
- Power factor selection had a much more significant impact on voltages, causing several percentage points of difference for each step in power factor. The 0.90 power factor setting actually led to slight reductions in voltage over the course of each test even as inverter real power increased because reactive power absorption also increased. The high effectiveness of non-unity power factor in reducing voltages was related to the high aggregate rating of FPF-capable inverters and the high ratio of FPF-capable inverters to legacy inverters.

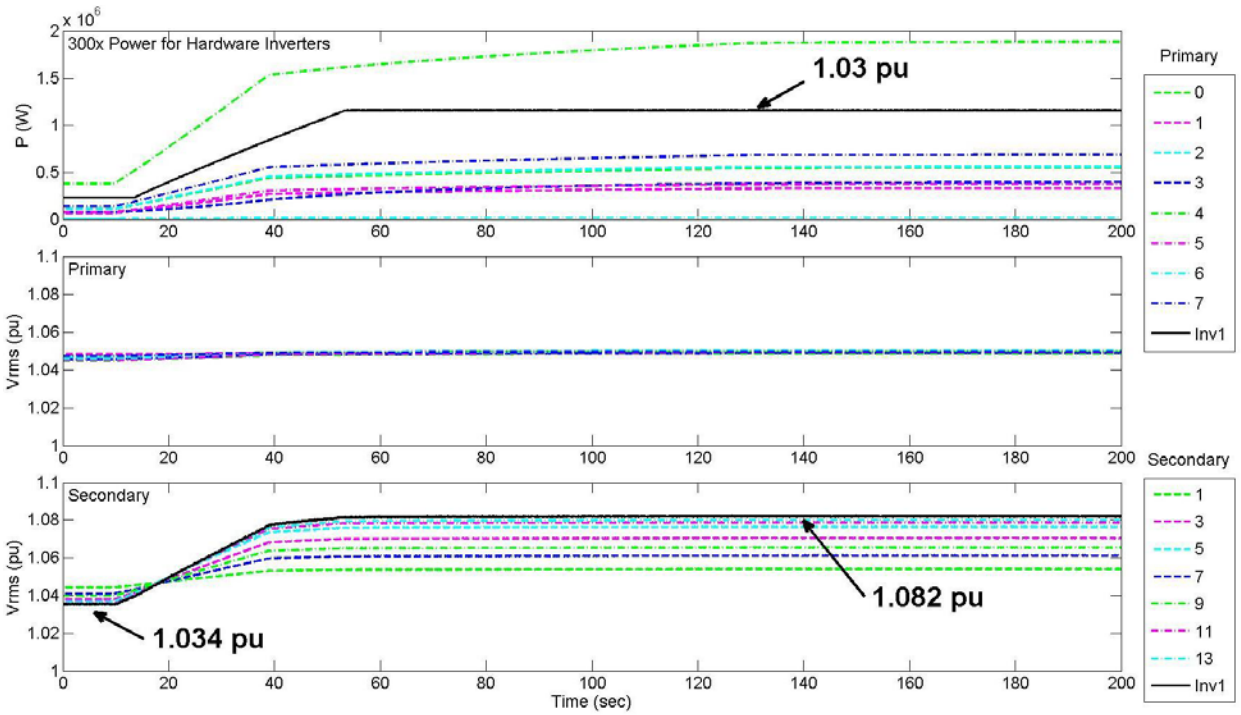

Figure 48. VWC with FPF waveform plot, Inverter 1, PF = 1.0, no VWC curve, snapshot mode, future, 0% retrofit, K3L feeder

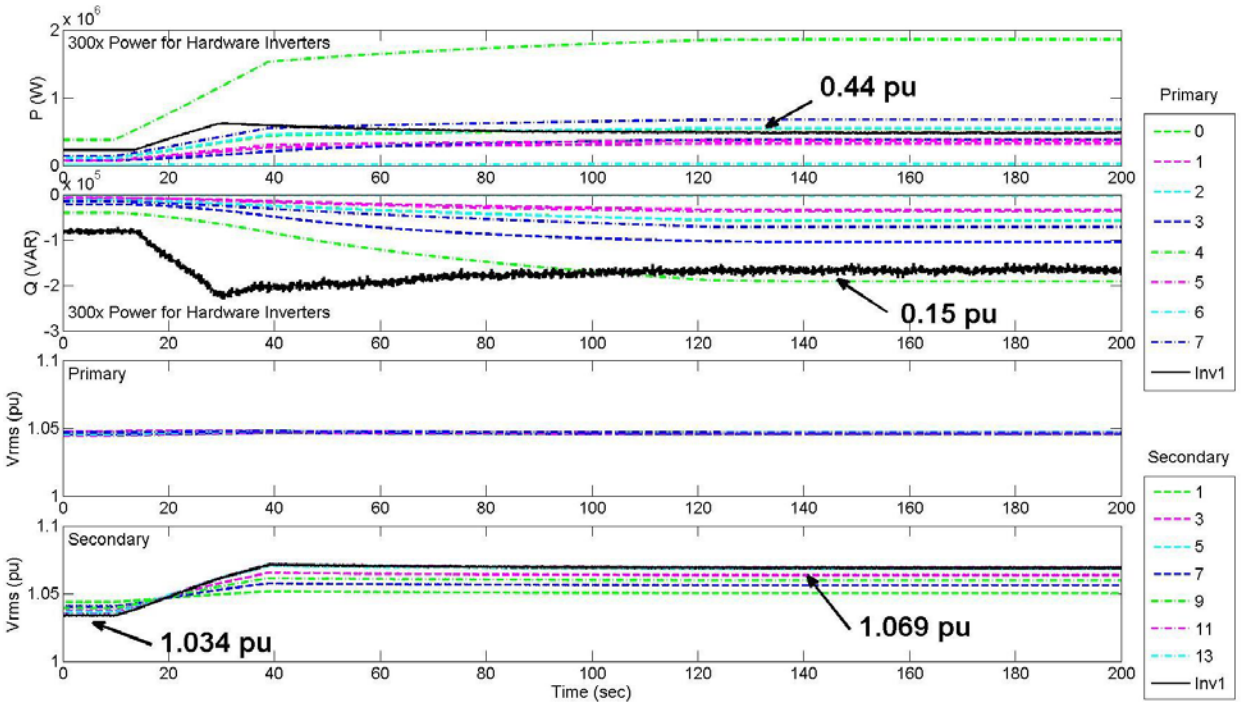

Figure 49. VWC with FPF waveform plot, Inverter 1, PF = 0.95, moderate VWC curve, snapshot mode, future, 0% retrofit, K3L feeder

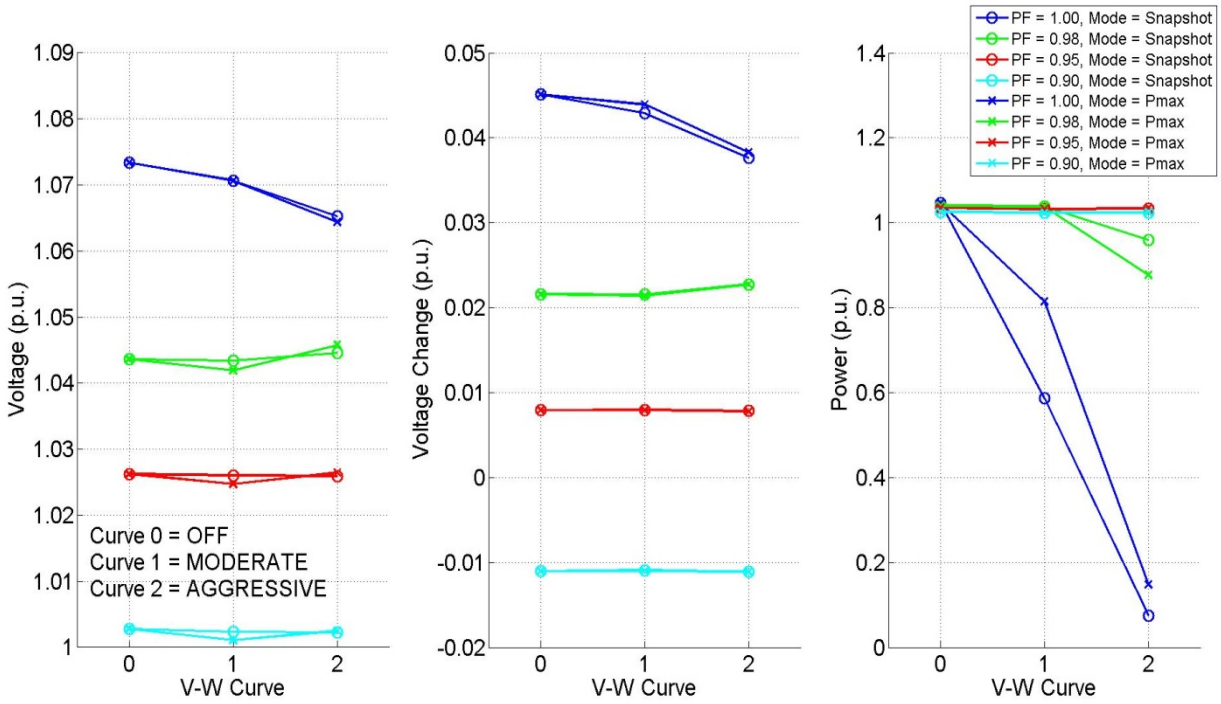

Figure 50. VWC with FPF summary data for Inverter 1 on M34, showing final inverter voltages (left), change in voltage over the course of each test (middle), and final inverter output power (right)

Figure 51 shows a summary of all Inverter 1 test cases for the K3L feeder. When comparing Figure 51 to Figure 50, it is important to take note of the scale of the y-axes, which covers a much smaller range in Figure 51. Also note that in the 2021 K3L case tested here 37% of PV is capable of advanced functions, about half of that in the 2021 M34 feeder, but still a not a low proportion by any means. The following observations can be made for the tests of Inverter 1 on K3L:

- The VWC had a more significant impact on voltages, leading to 0.01-0.02 pu more voltage reduction for the moderate and aggressive curves.
- The aggressive curve enforced nearly 100% reduction in power in these test cases; the moderate curve led to varied power reduction.
- Operating in snapshot ($P_{pre\text{-}disturbance}$) mode led to greater power reductions and lower voltages, in contrast to the M34 tests.
- Power factor had a less significant impact than in the M34 case, but still resulted in noticeable voltage reductions. The difference in conclusions for M34 versus K3L is largely due to the fact that K3L had a smaller number of GSF-capable inverters, both in absolute terms and relative to the number of legacy inverters.

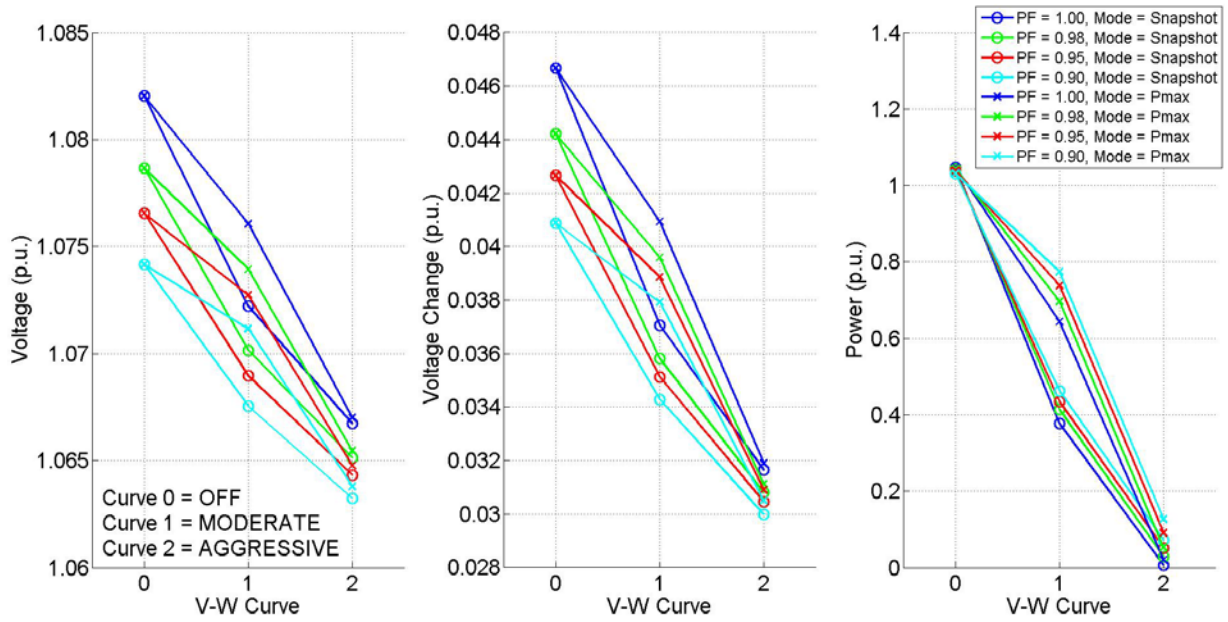

Figure 51. VWC with FPF summary data for Inverter 1 on K3L, showing final inverter voltages (left), change in voltage over the course of each test (middle), and final inverter output power (right)

5.6.2.2 Inverter 4 Test Results

The variables of interest for Inverter 4 testing were power factor and VWC curve type – all four VWC curves were tested for this inverter. K3L tests were completed with an irradiance ramp between 200-1000 W/m^2 in 40 seconds; M34 tests were completed with an irradiance ramp between 200-700 W/m^2 in 40 seconds. The split-phase secondary circuits were not included in these tests as this inverter was connected to the primary through a three-phase transformer and line impedance. A load factor of 0.35 was used on K3L tests and a load factor of 0.93 was used for M34 tests to provide the desired initial voltage conditions.

As with Inverter 1, the Inverter 4 tests were run using the future (2021) test case with no retrofitting of legacy inverters. The aggregate ratings of each type of inverter at each primary node were as shown in Table 29, above. A primary difference between tests of this inverter and tests of Inverter 1 is that Inverter 4 was connected on its own small commercial secondary rather than on a residential secondary with neighboring legacy inverters.

The effect of the aggressive VWC curve with 0.95 power factor is demonstrated in Figure 52 and Figure 53. Figure 52 is a baseline test case with VWC disabled and all inverters operating at unity power factor, which caused a voltage rise up to 109.3% of nominal at the hardware inverter. Note that there was substantial phase imbalance, so all voltages cited refer to the largest voltage, at phase B. When the aggressive VWC curve was implemented in Figure 53, final output power was reduced to 23% and the voltage rise was reduced by 0.016 pu. The example plots using the aggressive curve at unity power factor were selected because these show the rare case where the VWC function was activated for this inverter. For test cases at non-unity power factor, the voltage rise was not substantial enough to activate the VWC function.

Figure 54 shows a summary of all test cases for the 2021 M34 feeder (which again had 74% advanced PV). Recall that for these tests, irradiance was ramped only to 700 W/m^2, so the inverter power is never above roughly 0.75 pu. The following observations were made:

- VWC was only active for tests at unity power factor. The VWC curve type had little impact on the inverter voltage, except with the aggressive curve, which had some impact in unity power factor tests.
- The small increase in voltage for the moderate volt-watt curve relative to the mild curve is due to non-idealities in the test setup.
- Power factor selection had a much more significant impact on voltages, largely due to the high aggregate rating of GSF-capable inverters. A power factor of 0.95 caused ~0.03-0.04 pu reduction in voltage, and 0.90 power factor caused ~0.06 pu reduction in voltage at the inverter. The 0.90 power factor also was large enough to cause voltage reductions despite up to 50 percentage point increases in real power resulting from the irradiance ramp. These voltage reductions resulted from increased reactive power absorption by the inverters.
- The aggressive curve caused >0.5 pu reduction in real power for some tests, which led to a 0.01-0.02 pu reduction in voltage.

Figure 55 shows a summary of all test cases for the 2021 K3L feeder (which had 37% advanced PV), demonstrating the following observations:

- VWC was only activated for one test at unity power factor. The VWC curve type had little impact on the inverter voltage, except with the aggressive curve at unity power factor.
- Power factor selection had a more significant impact on voltages than VWC. A power factor of 0.95 caused a ~0.01 pu reduction in voltage, and 0.90 power factor caused a ~0.015 pu reduction in voltage at the inverter. Both power factors were low enough to cause voltage reductions despite up to 80 percentage point increases in real power resulting from the irradiance ramp.
- The aggressive curve caused ~0.5 pu reduction in real power for some tests, which led to a very small reduction in voltage.
- Voltage changes were relatively small in general on this feeder; the K3L feeder was very stiff on the primary side, so the GSFs had a limited effect.

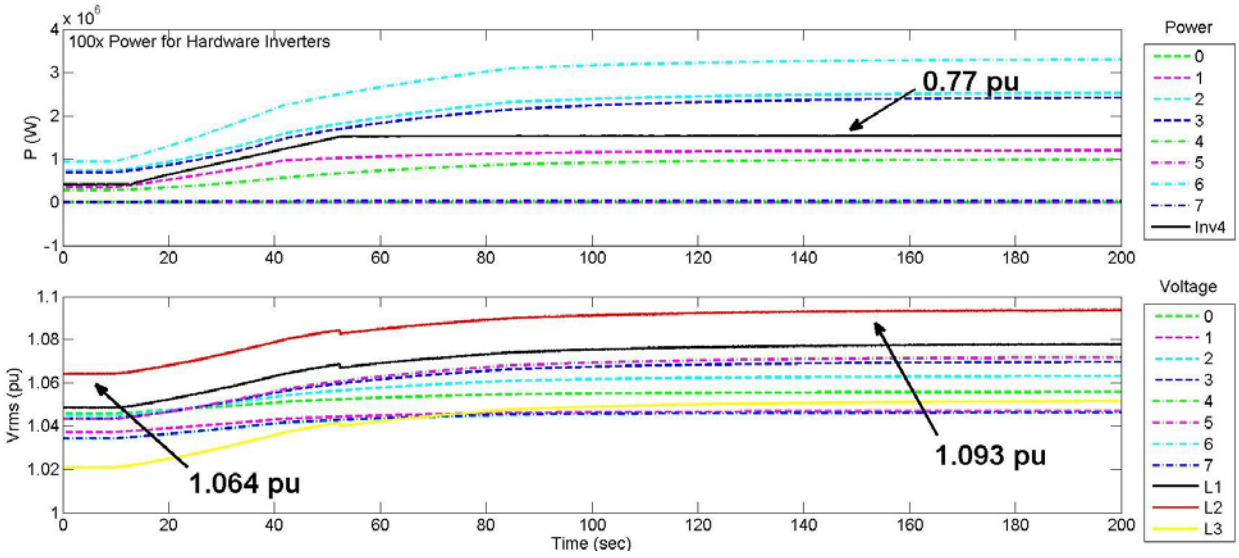

Figure 52. VWC with FPF waveform plot, Inverter 4, PF = 1.0, no VWC curve, nameplate mode, future, 0% retrofit, M34 feeder

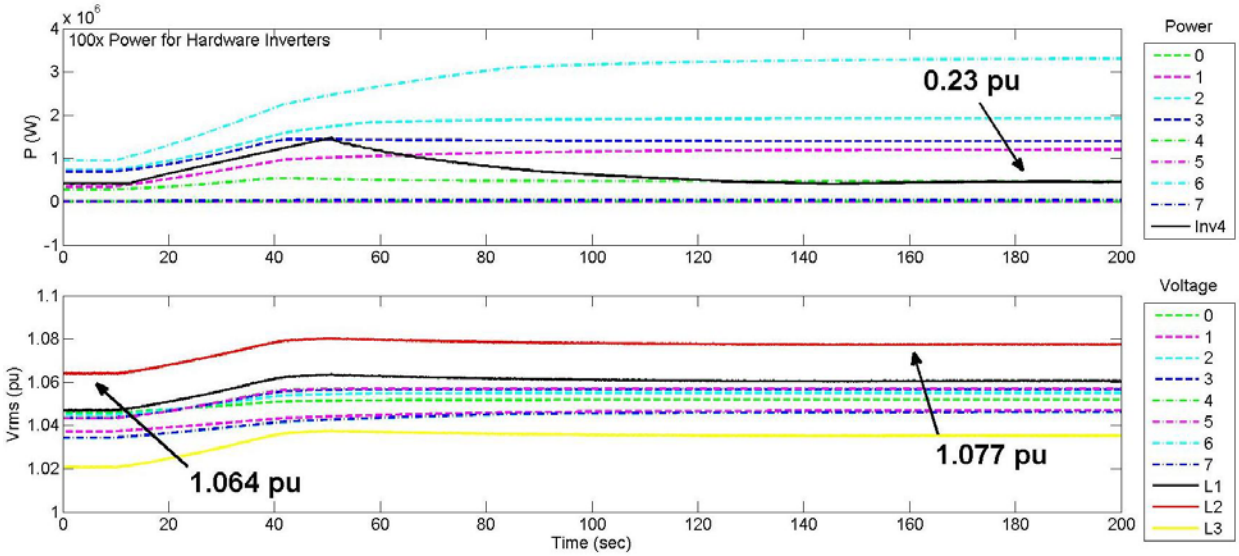

Figure 53. VWC with FPF waveform plot, Inverter 4, PF = 1.0, aggressive VWC curve, nameplate mode, future, 0% retrofit, M34 feeder

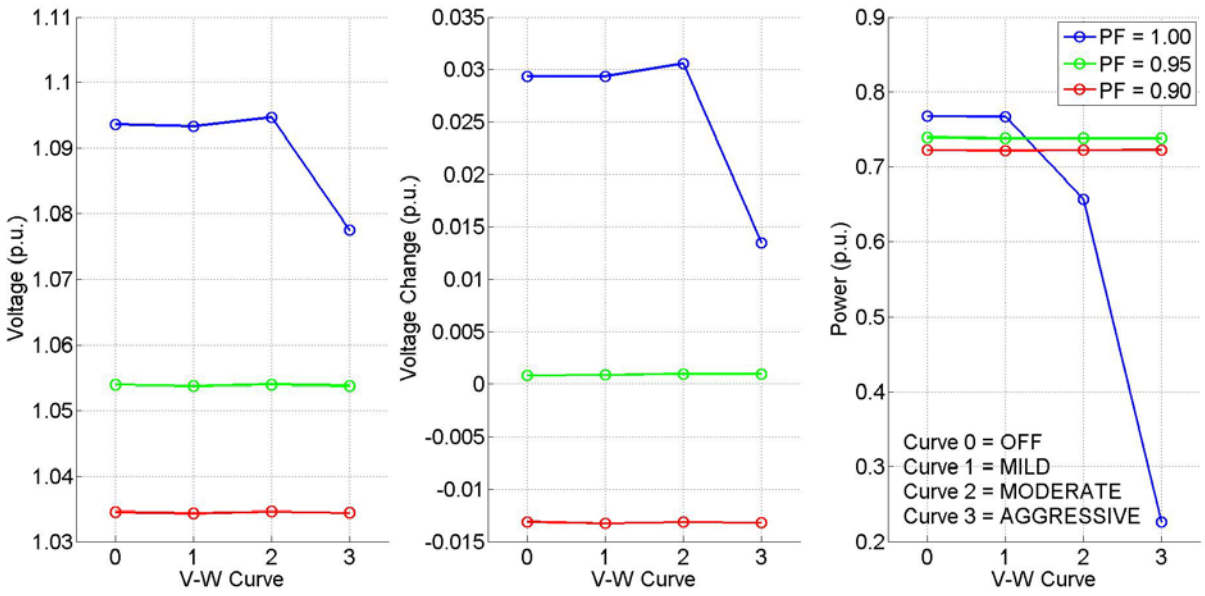

Figure 54. VWC with FPF summary data for Inverter 4 on M34, showing final inverter voltages (left), change in voltage over the course of each test (middle), and final inverter output power (right)

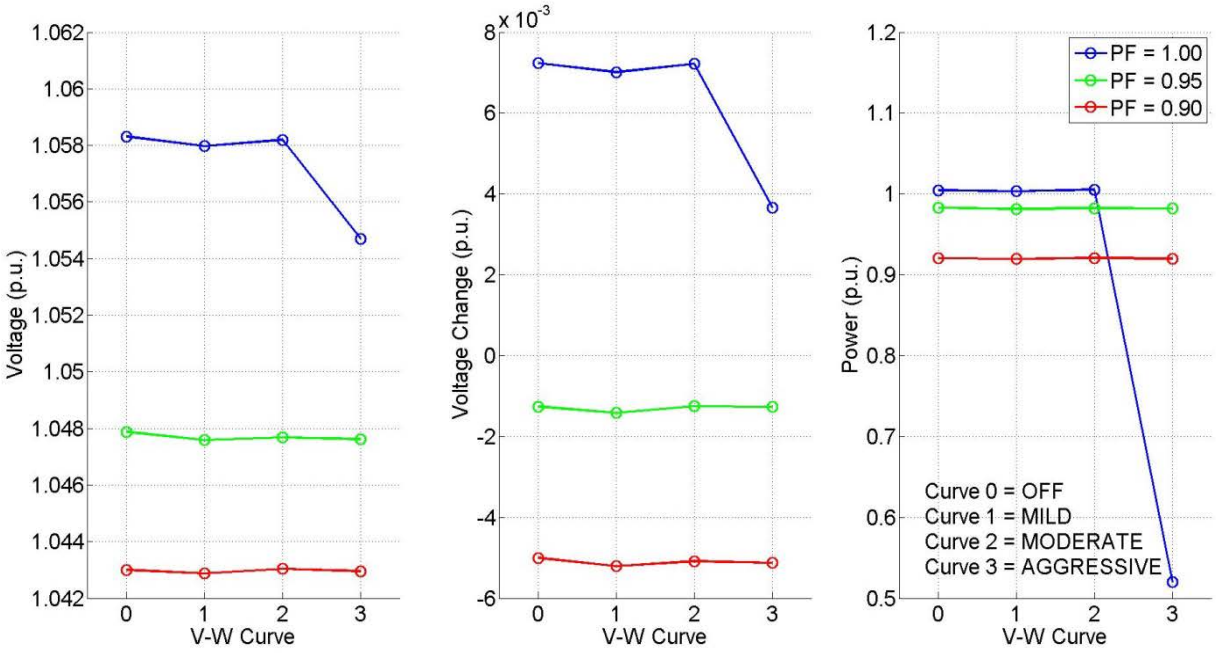

Figure 55. VWC with FPF summary data for Inverter 4 on K3L, showing final inverter voltages (left), change in voltage over the course of each test (middle), and final inverter output power (right)

5.6.2.3 Inverters 2 and 3 Test Results

The largest number of test iterations was run on Inverters 2 and 3 together, with the major difference being that all six PV ratings scenarios (0%, 25% and 50% retrofit in both present and future case) were tested along with variations to power factor and VWC curve type. All tests for both feeders were completed with an irradiance ramp from 200 to 1000 W/m^2 in 40 seconds. Four 2.5 kW inverters were added to the K3L secondary circuit to increase the voltage and the load factor was set to 0.45. Four 10.0 kW inverters were added to the M34 secondary to increase the voltage, and the load factor was set to 0.866.

Referring back to Table 28 shows the quantities of advanced and legacy PV for each of the six PV rating scenarios, which are useful to keep in mind when viewing the results below. This set of tests is the only set to examine all six scenarios, and thus can provide insight into the impacts of advanced PV proportions on GSF effectiveness. The information in that table can be roughly summarized as follows:

- 2016 scenarios for both feeders: low to moderate advanced PV levels
- 2021 scenarios for K3L: moderate to high advanced PV levels
- 2021 scenarios for M34: high advanced PV levels.

The effect of the moderate VWC and non-unity power factor for different PV ratings is demonstrated in Figure 56 and Figure 57. Figure 56 is a baseline test case with VWC disabled and all inverters operating at unity power factor, which caused a voltage rise up to 107.0% of nominal at Inverter 3. When 0.95 power factor with the moderate VWC curve was implemented in Figure 57, also with future PV ratings which included more inverters operating at 0.95 power factor, output power was reduced slightly to 95% of nominal and the voltage rise was reduced by 0.04 pu. This figure additionally shows the reactive power that was sourced by the modeled inverters and the hardware inverter, further mitigating the voltage rise.

Figure 58 shows a summary of all test cases for the M34 feeder for Inverter 3. The summary plots are very similar between Inverter 2 and 3, showing the same trends, given their close proximity to one another on the secondary circuit, so only one example is shown for each test inverter. Note that these plots are different than those shown in the previous sections, as they show the effects on voltage and inverter power as a function of the six PV rating settings shown on the x-axis.

Figure 58 shows the following observations:

- The VWC curve type had negligible impacts on the inverter voltage for this scenario. The VWC function caused large power reductions in some unity power factor tests, but had little effect on the inverter voltage.
- Future PV rating scenarios cause increased voltages for the unity power factor case, but reduced voltages for the non-unity power factor cases. The impact of additional reactive power absorption counteracted the increased real power in the circuit.
- Non-unity power factor operation could reduce voltages or hold them steady even with 0.8 pu increases in inverter real power across the system, across all PV rating scenarios.

- The proportion of retrofit inverters had a small but measureable impact on voltages. The effect would likely be larger if the other inverters on the same secondary with the hardware inverters were retrofitted.
- No adverse interactions were observed between the two hardware inverters, or between the two hardware inverters and other feeder elements.

Figure 59 shows a summary of all test cases for the K3L feeder for Inverter 2, demonstrating the following observations:

- The VWC curve type had more impact on the inverter voltage than in the M34 circuit, leading to 0.01-0.02 pu reductions in voltage, depending on whether the mild or moderate curve was used.
- Similarly, power factor could cause ~0.01 to 0.02 pu reductions in voltage for each 0.05 decrease in power factor value.
- Future vs. present PV ratings had a small but measurable impact on inverter voltages. Likewise, the proportion of retrofit inverters had a small but measureable impact on voltages. The effect would likely be larger if the other inverters on the same secondary with the hardware inverters were retrofitted.
- No adverse interactions were observed between the two hardware inverters, or between the two hardware inverters and other feeder elements.

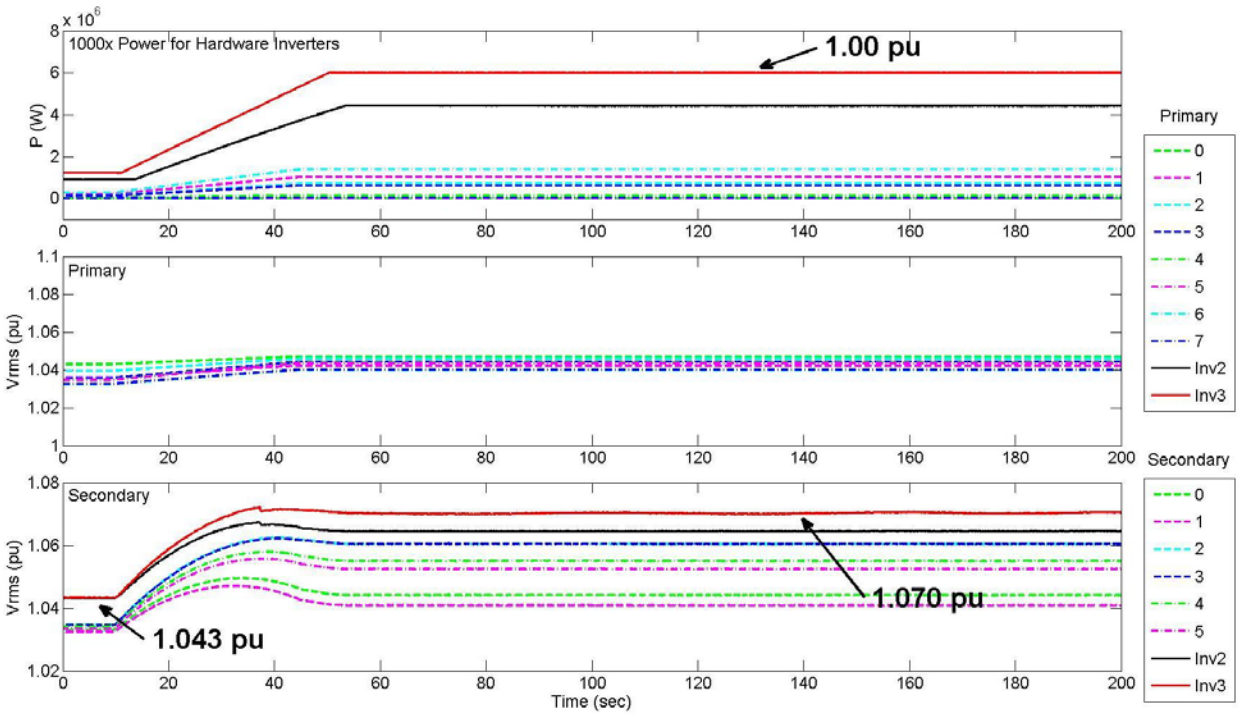

Figure 56. VWC with FPF waveform plot, Inverters 2 and 3, PF = 1.0, no VWC curve, nameplate mode, present, 0% retrofit, M34 feeder

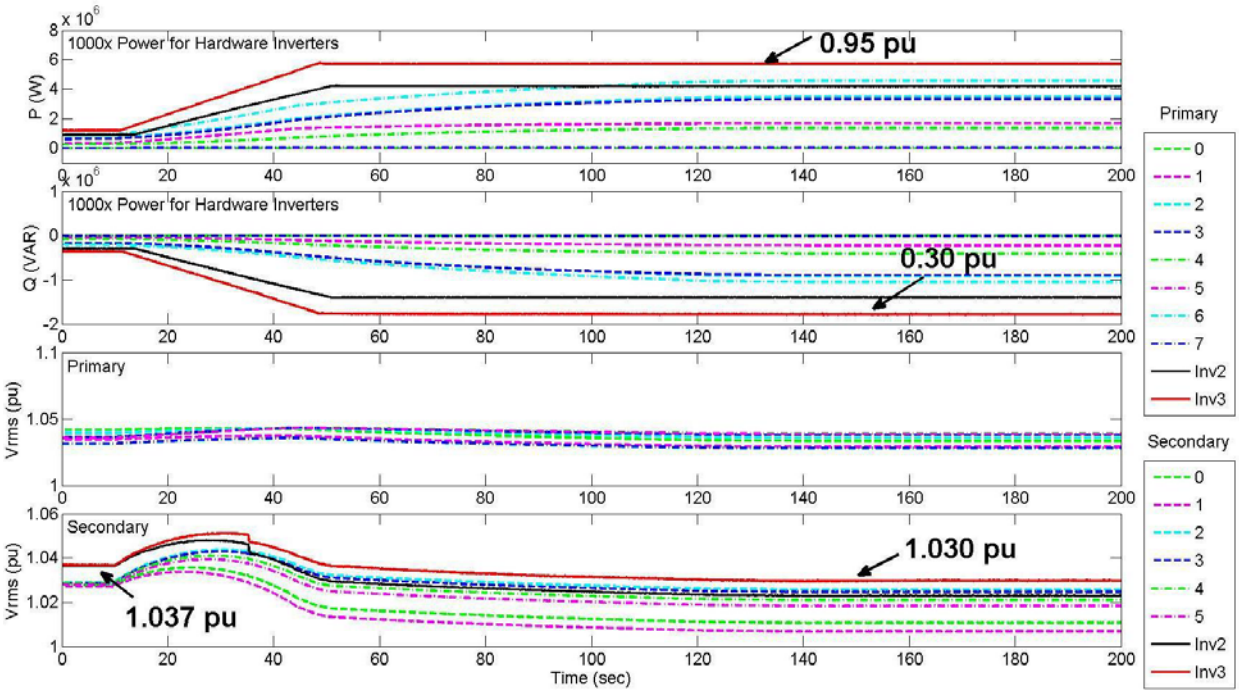

Figure 57. VWC with FPF waveform plot, Inverters 2 and 3, PF = 0.95, moderate VWC curve, nameplate mode, future, 0% retrofit, M34 feeder

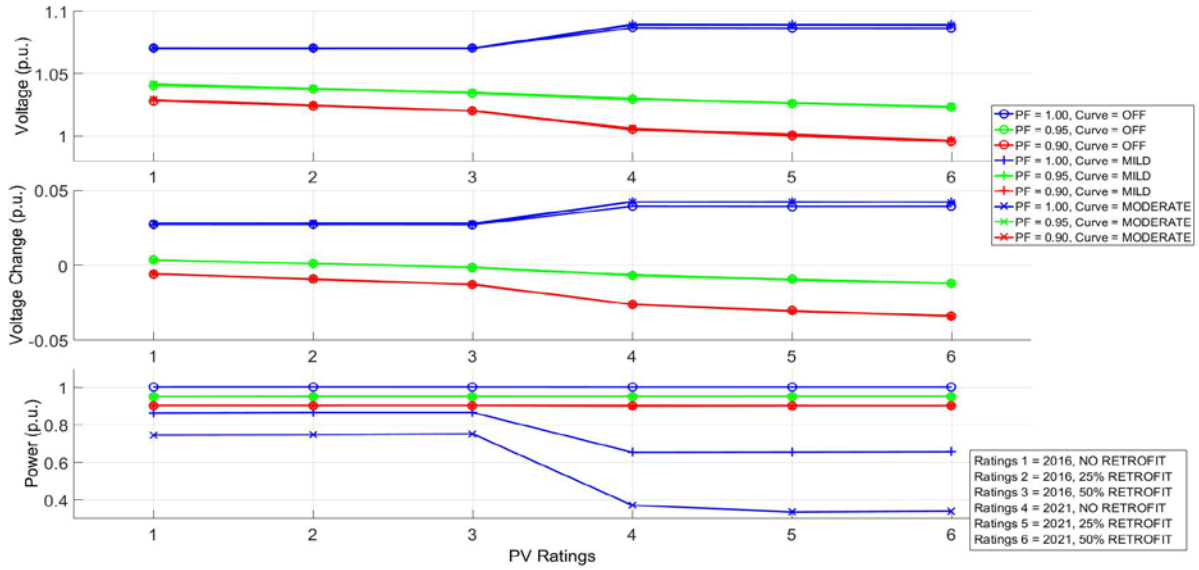

Figure 58. VWC with FPF summary for Inverter 3 on M34, showing final inverter voltages (top), change in voltage over the course of each test (middle), and final inverter output power (bottom)

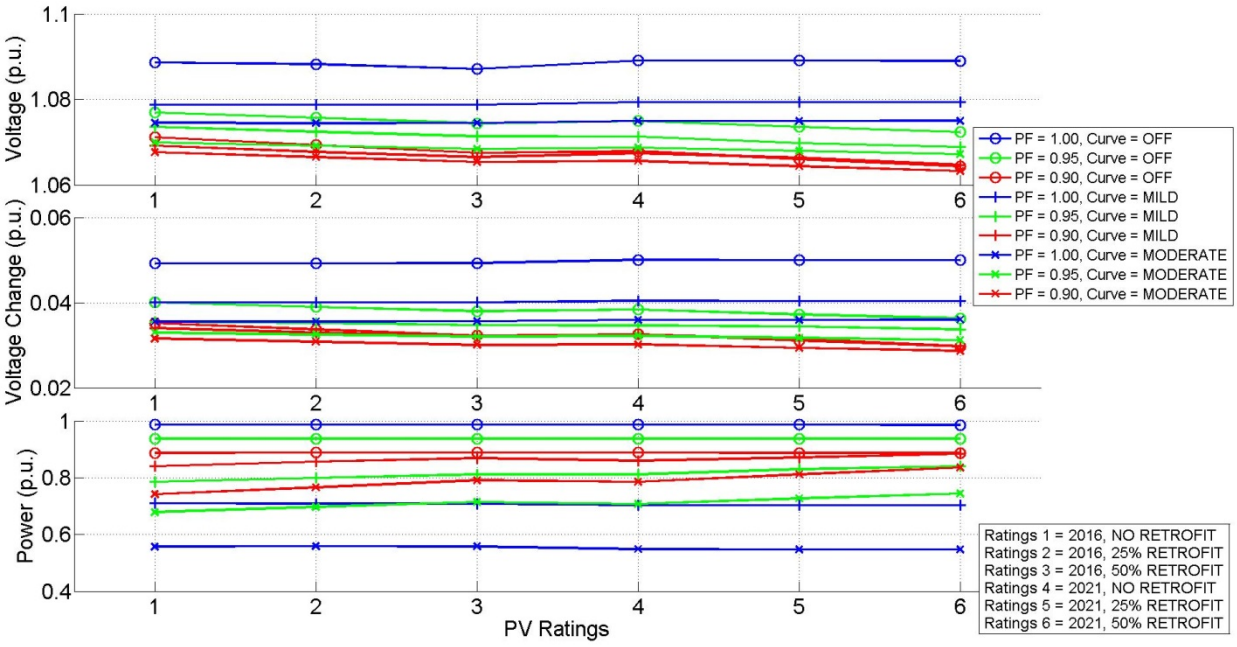

Figure 59. VWC with FPF summary for Inverter 2 on K3L, showing final inverter voltages (top), change in voltage over the course of each test (middle), and final inverter output power (bottom)

6 Conclusions

The tests presented in this report examined the impact of various solar PV inverter-based grid support functions on two simulated Hawaiian Electric distribution feeders. The distribution feeder models were derived in simplified form from models of actual O‘ahu circuits, with presently (December 2015) installed PV systems and projected future (2021) PV system installations represented in the model. The behavior of the modeled PV systems was based on laboratory tests of five PV inverters performing grid support functions. Using power hardware-in-the-loop testing, four of the five PV inverters from different manufacturers were dynamically connected to real-time simulations of the circuits, in addition to the modeled legacy and GSF-capable PV inverters. The PHIL test setup was used to evaluate six grid support functions in various scenarios. Volt-var control was not included in the PHIL tests. Most scenarios focused on different combinations of fixed power factor operation and volt-watt control, with a goal of evaluating the impact of those functions on feeder operations.

Several conclusions can be drawn from the test results, as described below. However, in interpreting these conclusions note first the following caveats:

- Each PHIL test examined a brief test scenario covering a time span of several minutes. In addition, each feeder model contained only one secondary circuit. Only limited information can be obtained from these tests about other locations on the circuit or points in time. Therefore only limited conclusions can be drawn about the effects of the functions on annual voltage profiles, and still fewer conclusions can be made about the effects of these functions on annual PV kWh production.

- The volt-watt and fixed power factor tests were intentionally designed to create high voltage conditions that would exercise the volt-watt function, which only has an impact at high voltages. Typically the feeder head voltage was set to 105% and load was set close to gross daytime minimum load. It is likely that some secondaries on the same feeders would see higher voltages, while others would see lower voltages for the same test scenarios.

- The two feeders tested have high levels of PV (between 88% and 539% of gross daytime minimum load, depending on the scenario and the feeder). They also have strong (low impedance) primaries relative to some other O‘ahu feeders. Therefore caution should be used in applying these conclusions directly to other feeders.

- The future (2021) test scenarios, which represent the majority of cases simulated, assumed that all PV added after January of 2016 would be capable of grid support. This likely overestimates the portion of PV that will be capable of grid support by 2021 given that customers in the various interconnection queues are not currently obligated to provide FPF or VWC. The 2016 retrofit test scenarios may represent more realistic near-term advanced PV ratios for these feeders.

Conclusions and recommendations resulting from this work include:

- All inverters tested were able to perform nearly all GSFs in a satisfactory manner. One exception was ramp rate control during normal operation, which two inverters did not support. All manufacturers tested are expected to be able to pass the UL 1741 SA tests by the time certification is required in Hawaii (September 2017). Testing and certification of grid support functions by OSHA-recognized Nationally Recognized Testing Laboratories (NRTLs) using standardized test procedures will provide improved assurance that all GSFs operate as expected, and is recommended whenever possible. (Note that NREL is not a NRTL.)

- Configuring individual grid support functions *ad hoc* can be both time-consuming and error-prone. Pre-configured location-specific function profiles (sometimes called "country settings") are recommended for widespread field deployment. It is possible that some islands may require more than one profile future years, with different profiles used for different field conditions.

- All four inverters tested were able to simultaneously and reliably perform FPF and VWC, and their performance closely followed expected behavior. (In contrast, only two inverters were able to simultaneously perform VWC and volt-var control at the time of testing.) In the PHIL tests with two hardware inverters connected at neighboring locations, no adverse dynamic interactions were observed from volt-watt control or fixed power factor.

- As implemented here, FPF was used as the primary inverter-based means of reducing high voltages. VWC was implemented such that it only becomes active for voltages outside of ANSI Range A (the normal voltage operating range). Implementing the two functions in this way helps minimize the impact on PV power production while still helping ensure that utility service voltages comply with ANSI requirements.

- There is some evidence that non-unity PF has more impact on reducing high voltages than VWC. For example, VWC had little impact in the M34 feeder, partly because the secondary voltages typically did not rise far into the active region of the volt-watt curve. VWC had more impact in K3L feeder cases, because voltages tended to be higher due largely to the longer secondary and the lower proportion of advanced inverters. However, these conclusions depended strongly on the feeder details and the scenario under test as well as the relative and absolute aggregate ratings of legacy and advanced PV.

- The fact that VWC had little impact in some test cases (especially 2021 cases) does not necessarily imply that it will not help reduce high voltages. Instead, it means that in those cases, FPF was reducing the voltage so that the "backup plan" of directly reducing PV power through VWC did not need to be implemented.

- Higher proportions of advanced PV tended to result in more effective voltage reduction via FPF and thus little activity from VWC. Given the fact that the 2021 cases were likely overestimating the proportion of grid support capable PV, the test results may skew towards emphasizing the impact of FPF and de-emphasizing the impact of VWC. On feeders with high legacy PV penetration, the first inverters added with FPF and VWC may see significant VWC activity and little impact on voltage until a sufficient

penetration of advanced inverters is installed. In other words, a "critical mass" of grid supportive inverters is needed to effectively mitigate high voltages, and that critical mass depends on factors including load, legacy PV penetration, circuit impedance and topology, and the specific grid support functions and parameters in use. To avoid high voltage issues (and the associated loss of power production through VWC) on feeders that do not yet have high PV penetrations, it would be advisable to activate GSFs soon, allowing a critical mass of advanced inverters to be reached before voltages reach levels where VWC is frequently active. This recommendation is partly due to the fact that technical and contractual issues may make it difficult to enable GSFs after a system is initially installed. If the appropriate technical and contractual arrangements are implemented to enable changing grid support settings post-interconnection, it may not be necessary to enable certain GSFs at the time of installation.

- For the scenarios tested, retrofitting of legacy inverters to enable FPF and VWC did not appear to have a significant impact on the feeder primary voltage level. However, retrofitting of individual inverters on the target secondaries under test was not examined, and would likely be more impactful in reducing the secondary voltages.

- Two modes of VWC were compared: one in which the volt-watt curve is fixed based on the rated power of the inverter (referred to as "nameplate" mode or "P_{max}" mode), and one in which the volt-watt curve is a function of the instantaneous inverter power at the time the AC voltage crossed a threshold. In cases where VWC had an impact, the latter method (referred to as "$P_{pre\text{-}disturbance}$" or "snapshot" mode), was somewhat more impactful (though not overwhelmingly more impactful). The relative impact of the two modes will be case-specific since it depends on the way many continuously-changing variables line up in time. Those variables include customer-specific irradiance profiles, individual customer load profiles, and feeder-level voltage controls. VWC in P_{max} mode will result in greater annual PV kWh production for individual customers, whereas VWC in $P_{pre\text{-}disturbance}$ mode provides a more predictable and effective mitigation of high voltages, potentially allowing more total PV on each feeder.

- Test results varied significantly between the two feeders. Factors that impacted this included the amounts of legacy and GSF-capable PV on the feeder, the impedance characteristics of the feeder (both magnitude and X/R ratio, and both primary and secondary), and the feeder load characteristics. Because all three of these factors differed significantly between the two feeders, it is difficult to draw a conclusion as to which factors are more important based on these tests alone.

- These tests focused on the combination of FPF and VWC because FPF was beginning to be deployed at the time, and VWC could potentially help reduce high voltages when FPF alone was not entirely effective. While these two functions, especially FPF, were shown to be effective in reducing voltage, FPF is not without drawbacks. For example, inverters operating in FPF mode will absorb Vars whether or not the voltage is high, even reducing the voltage in locations where it is already low. In addition, the Vars absorbed must be supplied by the rest of the system, and will incur losses as they travel through the system. For these reasons, it may be advantageous to examine volt-var as an alternative to fixed power factor (possibly also combined with volt-watt).

Several research questions that arose in the course of in this work are being examined under a Cooperative Research and Development Agreement (CRADA) between NREL and the Hawaiian Electric Companies at the time of this writing. The objective of this CRADA, referred to as the Voltage Regulation Operational Strategies (VROS) project, is to examine various inverter-based voltage regulation functions (volt-var, volt-watt, and fixed power factor) through annual time-series simulations using detailed feeder models, including detailed secondaries throughout each feeder. At the time of this writing, not all inverter manufacturers are able to provide all combinations of voltage regulation functions (as shown in this report), but this is expected to change in the near future. The outcomes of the VROS study are expected to include conclusions regarding the effectiveness of various configurations of the voltage regulation functions on annual voltage profiles and annual PV energy production.

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Appendix A – Volt-Watt Baseline Test Data

Test case (column 2) can be cross-referenced with Table 14.

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
1	1	124.5	124.7	100.0	100.0	0.0
1	1	125.5	125.7	100.0	100.0	0.0
1	1	126.5	126.7	100.0	96.6	-3.4
1	1	127.5	127.7	89.6	88.1	-1.4
1	1	128.5	128.7	68.8	74.9	6.1
1	1	129.5	129.7	47.9	59.3	11.4
1	1	130.5	130.6	29.2	42.4	13.2
1	1	131.5	131.6	8.3	21.8	13.4
1	1	130.5	130.6	29.2	37.3	8.1
1	1	129.5	129.7	47.9	52.3	4.3
1	1	128.5	128.7	68.8	68.1	-0.7
1	1	127.5	127.7	89.6	82.8	-6.8
1	1	126.5	126.7	100.0	93.5	-6.5
1	1	125.5	125.7	100.0	100.0	0.0
1	1	124.5	124.7	100.0	100.0	0.0
1	2	124.5	124.8	100.0	100.3	0.3
1	2	125.5	125.8	100.0	100.3	0.3
1	2	126.5	126.8	100.0	96.6	-3.4
1	2	127.5	127.7	89.6	87.6	-2.0
1	2	128.5	128.7	68.8	74.0	5.3
1	2	129.5	129.7	47.9	60.5	12.5
1	2	130.5	130.7	27.1	42.4	15.3
1	2	131.5	131.6	8.3	23.4	15.1
1	2	130.5	130.7	27.1	35.3	8.2
1	2	129.5	129.7	47.9	52.0	4.1
1	2	128.5	128.7	68.8	67.2	-1.5
1	2	127.5	127.7	89.6	83.6	-6.0
1	2	126.5	126.8	100.0	97.2	-2.8
1	2	125.5	125.8	100.0	100.3	0.3
1	2	124.5	124.8	100.0	100.0	0.0
1	3	124.5	124.7	100.0	100.0	0.0
1	3	125.5	125.7	100.0	100.0	0.0
1	3	126.5	126.7	100.00	96.9	-3.1
1	3	127.5	127.7	89.6	88.4	-1.2
1	3	128.5	128.7	68.8	74.0	5.3
1	3	129.5	129.7	47.9	55.6	7.7
1	3	130.5	130.7	27.1	42.7	15.6
1	3	131.5	131.6	8.3	19.8	11.4

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
1	3	130.5	130.7	27.1	35.9	8.8
1	3	129.5	129.7	47.9	50.8	2.9
1	4	124.5	124.7	67.0	68.6	1.6
1	4	125.5	125.7	67.0	68.6	1.6
1	4	126.5	126.7	67.0	68.6	1.6
1	4	127.5	127.7	59.7	61.3	1.6
1	4	128.5	128.7	45.8	50.0	4.2
1	4	129.5	129.7	31.9	37.9	5.9
1	4	130.5	130.6	19.4	26.8	7.4
1	4	131.5	131.6	5.6	14.4	8.9
1	4	130.5	130.6	19.4	27.1	7.7
1	4	129.5	129.7	31.9	39.0	7.0
1	4	128.5	128.7	45.8	50.8	5.0
1	4	127.5	127.7	59.7	62.4	2.7
1	4	126.5	126.7	67.0	68.1	1.1
1	4	125.5	125.7	67.0	68.6	1.6
1	4	124.5	124.7	67.0	68.6	1.6
1	5	124.5	124.7	33.0	35.6	2.6
1	5	125.5	125.7	33.0	35.6	2.6
1	5	126.5	126.7	33.0	35.6	2.6
1	5	127.5	127.7	29.9	35.6	5.7
1	5	128.5	128.6	23.6	27.7	4.1
1	5	129.5	129.6	16.7	20.6	4.0
1	5	130.5	130.6	9.7	14.1	4.4
1	5	131.5	131.6	2.8	7.1	4.3
1	5	130.5	130.6	9.7	15.3	5.5
1	5	129.5	129.6	16.7	22.0	5.4
1	5	128.5	128.6	23.6	29.1	5.5
1	5	127.5	127.7	29.9	34.5	4.6
1	5	126.5	126.7	33.0	35.6	2.6
1	5	125.5	125.7	33.0	35.6	2.6
1	5	124.5	124.7	33.0	35.6	2.6
1	6	125.0	125.2	100.0	100.0	0.0
1	6	125.5	125.7	100.0	100.0	0.0
1	6	126.0	126.2	83.3	100.0	16.7
1	6	126.3	126.5	58.3	98.3	40.0
1	6	126.5	126.7	41.7	96.9	55.2
1	6	126.8	127.0	16.7	92.7	76.0
1	6	127.0	127.2	0.0	90.7	90.7
1	6	127.3	127.5	0.0	83.3	83.3
1	6	127.8	128.0	0.0	71.2	71.2

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
1	6	128.3	128.5	0.0	59.6	59.6
1	6	128.5	128.7	0.0	55.6	55.6
1	6	128.8	128.9	0.0	46.0	46.0
1	6	130.0	130.1	0.0	16.9	16.9
1	6	130.3	130.4	0.0	14.1	14.1
1	6	130.5	130.6	0.0	8.2	8.2
1	6	130.8	130.9	0.0	2.3	2.3
1	6	131.0	131.1	0.0	2.3	2.3
1	6	131.3	131.4	0.0	2.3	2.3
1	6	131.5	131.6	0.0	2.3	2.3
1	6	131.8	131.9	0.0	2.3	2.3
1	6	132.0	132.1	0.0	2.3	2.3
1	6	131.8	131.9	0.0	2.3	2.3
1	6	131.5	131.6	0.0	2.3	2.3
1	6	131.3	131.4	0.0	2.3	2.3
1	6	131.0	131.1	0.0	2.3	2.3
1	6	128.8	128.9	0.0	36.2	36.2
1	6	128.5	128.7	0.0	43.5	43.5
1	6	128.3	128.5	0.0	50.0	50.0
1	6	127.8	128.0	0.0	65.0	65.0
1	6	127.3	127.5	0.0	79.4	79.4
1	6	127.0	127.2	0.0	85.0	85.0
1	6	126.8	127.0	16.7	90.4	73.7
1	6	126.5	126.7	41.7	95.5	53.8
1	6	126.3	126.5	58.3	97.2	38.8
1	6	126.0	126.2	83.3	99.2	15.8
1	6	125.5	125.7	100.0	100.0	0.0
1	6	125.0	125.2	100.0	100.0	0.0
1	7	124.5	124.8	100.0	100.0	0.0
1	7	125.5	125.7	100.0	97.5	-2.5
1	7	126.5	126.7	100.0	91.8	-8.2
1	7	127.5	127.7	94.8	85.0	-9.8
1	7	128.5	128.7	84.4	78.5	-5.8
1	7	129.5	129.7	74.0	67.5	-6.4
1	7	130.5	130.7	63.5	59.0	-4.5
1	7	129.5	129.7	74.0	67.2	-6.7
1	7	128.5	128.7	84.4	75.4	-9.0
1	7	127.5	127.7	94.8	84.2	-10.6
1	7	126.5	126.7	100.0	92.1	-7.9
1	7	125.5	125.7	100.0	96.6	-3.4
1	7	124.5	124.7	100.0	99.4	-0.6

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
1	8	124.5	124.7	67.0	68.6	1.6
1	8	125.5	125.7	67.0	68.6	1.6
1	8	126.5	126.7	67.0	68.6	1.6
1	8	127.5	127.7	67.0	68.6	1.6
1	8	128.5	128.7	67.0	68.6	1.6
1	8	129.5	129.7	47.9	57.1	9.1
1	8	130.5	130.7	27.1	39.5	12.5
1	8	131.5	131.6	8.3	21.8	13.4
1	8	130.5	130.7	27.1	41.2	14.2
1	8	129.5	129.7	47.9	58.8	10.8
1	8	128.5	128.7	67.0	68.4	1.4
1	8	127.5	127.7	67.0	68.6	1.6
1	8	126.5	126.7	67.0	68.6	1.6
1	8	125.5	125.7	67.0	68.6	1.6
1	8	124.5	124.7	67.0	68.6	1.6
1	9	124.5	124.7	33.0	35.6	2.6
1	9	125.5	125.8	33.0	35.6	2.6
1	9	126.5	126.7	33.0	35.6	2.6
1	9	127.5	127.7	33.0	35.6	2.6
1	9	128.5	128.7	33.0	35.6	2.6
1	9	129.5	129.6	33.0	35.6	2.6
1	9	130.5	130.6	29.2	35.3	6.1
1	9	131.5	131.6	8.3	21.8	13.4
1	9	130.5	130.6	29.2	35.3	6.1
1	9	129.5	129.6	33.0	35.6	2.6
1	9	128.5	128.7	33.0	35.6	2.6
1	9	127.5	127.7	33.0	35.6	2.6
1	9	126.5	126.7	33.0	35.6	2.6
1	9	125.5	125.7	33.0	35.6	2.6
1	9	124.5	124.7	33.0	35.6	2.6
2	1	124.5	124.8	100.0	100.0	0.0
2	1	125.5	125.8	100.0	100.0	0.0
2	1	126.5	126.8	100.0	95.7	-4.3
2	1	127.5	127.8	87.5	78.6	-8.9
2	1	128.5	128.8	66.7	60.5	-6.2
2	1	129.5	129.7	47.9	42.9	-5.0
2	1	130.5	130.7	27.1	25.3	-1.8
2	1	129.5	129.7	47.9	42.9	-5.0
2	1	128.5	128.8	66.7	60.3	-6.4
2	1	127.5	127.8	87.5	78.3	-9.2
2	1	126.5	126.8	100.0	95.5	-4.5

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
2	1	125.5	125.8	100.0	100.0	0.0
2	1	124.5	124.8	100.0	100.0	0.0
2	2	124.5	124.9	100.0	100.0	0.0
2	2	125.5	125.9	100.0	100.0	0.0
2	2	126.5	126.9	100.0	94.3	-5.7
2	2	127.5	127.8	87.5	77.6	-9.9
2	2	128.5	128.7	68.8	59.3	-9.5
2	2	129.5	129.7	47.9	41.4	-6.5
2	2	130.5	130.6	29.2	23.8	-5.4
2	2	129.5	129.7	47.9	41.6	-6.3
2	2	128.5	128.7	68.8	60.2	-8.6
2	2	127.5	127.8	87.5	78.7	-8.8
2	2	126.5	126.8	100.0	95.8	-4.2
2	2	125.5	125.8	100.0	100.2	0.2
2	2	124.5	124.8	100.0	100.0	0.0
2	3	124.5	124.8	100.0	100.0	0.0
2	3	125.5	125.8	100.0	100.0	0.0
2	3	126.5	126.8	100.0	95.7	-4.3
2	3	127.5	127.8	87.5	78.3	-9.2
2	3	128.5	128.7	68.8	60.5	-8.3
2	3	129.5	129.7	47.9	43.1	-4.8
2	3	130.5	130.6	29.2	25.3	-3.9
2	3	129.5	129.7	47.9	42.9	-5.0
2	6	125.0	125.3	100.0	98.2	-1.8
2	6	125.5	125.8	100.0	78.7	-21.3
2	6	126.0	126.2	83.3	53.8	-29.5
2	6	126.3	126.5	58.3	40.3	-18.1
2	6	126.5	126.7	41.7	31.2	-10.4
2	6	126.8	126.9	25.0	17.6	-7.4
2	6	127.0	127.1	8.3	8.4	0.0
2	6	127.3	127.4	0.0	2.3	2.3
2	6	127.8	127.9	0.0	0.0	0.0
2	6	128.3	128.4	0.0	0.0	0.0
2	6	127.8	127.9	0.0	0.0	0.0
2	6	127.3	127.4	0.0	2.3	2.3
2	6	127.0	127.1	8.3	8.4	0.0
2	6	126.8	126.9	25.0	17.2	-7.8
2	6	126.5	126.7	41.7	31.0	-10.7
2	6	126.3	126.5	58.3	40.0	-18.3
2	6	126.0	126.2	83.3	53.8	-29.5
2	6	125.5	125.8	100.0	78.5	-21.5

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
2	6	125.0	125.3	100.0	98.6	-1.4
2	7	124.5	124.8	100.0	99.8	-0.2
2	7	125.5	125.8	100.0	100.0	0.0
2	7	126.5	126.8	100.0	97.7	-2.3
2	7	127.5	127.8	93.8	88.5	-5.3
2	7	128.5	128.7	84.4	78.7	-5.6
2	7	129.5	129.7	74.0	68.6	-5.4
2	7	130.5	130.7	63.5	58.6	-4.9
2	7	129.5	129.7	74.0	68.8	-5.2
2	7	128.5	128.8	83.3	79.0	-4.4
2	7	127.5	127.8	93.8	88.7	-5.1
2	7	126.5	126.8	100.0	98.0	-2.0
2	7	125.5	125.8	100.0	100.0	0.0
2	7	124.5	124.8	100.0	100.0	0.0
2	8	124.5	124.7	67.0	68.1	1.1
2	8	125.5	125.7	67.0	68.1	1.1
2	8	126.5	126.7	67.0	68.1	1.1
2	8	127.5	127.7	67.0	68.1	1.1
2	8	128.5	128.7	67.0	59.3	-7.7
2	8	129.5	129.7	47.9	41.6	-6.3
2	8	130.5	130.6	29.2	23.8	-5.4
2	8	129.5	129.7	47.9	41.9	-6.1
2	8	128.5	128.7	67.0	59.7	-7.3
2	8	127.5	127.7	67.0	68.1	1.1
2	8	126.5	126.7	67.0	68.1	1.1
2	8	125.5	125.7	67.0	68.1	1.1
2	8	124.5	124.7	67.0	68.1	1.1
2	9	124.5	124.7	33.0	34.2	1.2
2	9	125.5	125.7	33.0	34.2	1.2
2	9	126.5	126.7	33.0	34.2	1.2
2	9	127.5	127.7	33.0	34.2	1.2
2	9	128.5	128.7	33.0	34.2	1.2
2	9	129.5	129.7	33.0	34.2	1.2
2	9	130.5	130.6	29.2	24.2	-5.0
2	9	129.5	129.7	33.0	34.2	1.2
2	9	128.5	128.7	33.0	34.2	1.2
2	9	127.5	127.7	33.0	34.2	1.2
2	9	126.5	126.7	33.0	34.2	1.2
2	9	125.5	125.7	33.0	34.2	1.2
2	9	124.5	124.7	33.0	34.2	1.2
3	1	249.0	249.6	100.0	100.0	0.0

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
3	1	251.0	251.6	100.0	100.0	0.0
3	1	253.0	253.5	100.0	100.0	0.0
3	1	255.0	255.5	88.5	86.7	-1.9
3	1	257.0	257.4	68.8	68.7	-0.1
3	1	259.0	259.4	47.9	49.9	2.0
3	1	261.0	261.3	28.1	31.1	3.0
3	1	259.0	259.3	49.0	47.8	-1.2
3	1	257.0	257.4	68.8	66.6	-2.2
3	1	255.0	255.4	89.6	85.5	-4.1
3	1	253.0	253.5	100.0	100.0	0.0
3	1	251.0	251.5	100.0	100.0	0.0
3	1	249.0	249.5	100.0	100.0	0.0
3	2	249.0	249.6	100.0	100.0	0.0
3	2	251.0	251.6	100.0	100.0	0.0
3	2	253.0	253.6	100.0	100.1	0.1
3	2	255.0	255.5	88.5	87.0	-1.5
3	2	257.0	257.4	68.8	68.3	-0.4
3	2	259.0	259.4	47.9	49.4	1.5
3	2	261.0	261.3	28.1	30.4	2.3
3	2	263.0	263.2	8.3	11.7	3.4
3	2	261.0	261.3	28.1	30.4	2.3
3	2	259.0	259.3	49.0	49.6	0.7
3	2	257.0	257.4	68.8	68.0	-0.8
3	2	255.0	255.5	88.5	86.5	-2.0
3	2	253.0	253.5	100.0	100.1	0.1
3	2	251.0	251.5	100.0	100.0	0.0
3	2	249.0	249.5	100.0	100.0	0.0
3	3	249.0	249.5	100.0	100.0	0.0
3	3	251.0	251.5	100.0	100.0	0.0
3	3	253.0	253.5	100.0	100.0	0.0
3	3	255.0	255.4	89.6	87.9	-1.7
3	3	257.0	257.4	68.8	70.5	1.8
3	3	259.0	259.3	49.0	51.5	2.5
3	3	261.0	261.3	28.1	32.9	4.8
3	3	259.0	259.3	49.0	48.2	-0.8
3	4	249.0	249.4	67.0	67.0	0.0
3	4	251.0	251.4	67.0	67.0	0.0
3	4	253.0	253.4	67.0	67.0	0.0
3	4	255.0	255.4	59.7	59.9	0.2
3	4	257.0	257.3	46.5	47.1	0.6
3	4	259.0	259.3	32.6	34.3	1.7

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
3	4	261.0	261.2	19.4	21.2	1.7
3	4	263.0	263.2	5.6	8.1	2.6
3	4	261.0	261.3	18.8	21.0	2.3
3	4	259.0	259.3	32.6	33.9	1.3
3	4	257.0	257.3	46.5	47.0	0.5
3	4	255.0	255.4	59.7	60.0	0.3
3	4	253.0	253.4	67.0	66.9	-0.1
3	4	251.0	251.4	67.0	67.0	0.0
3	4	249.0	249.4	67.0	67.0	0.0
3	5	249.0	249.3	33.0	34.1	1.1
3	5	251.0	251.3	33.0	34.1	1.1
3	5	253.0	253.3	33.0	34.1	1.1
3	5	255.0	255.2	30.6	31.7	1.1
3	5	257.0	257.3	23.3	24.6	1.4
3	5	259.0	259.2	16.7	17.9	1.2
3	5	261.0	261.2	9.7	11.1	1.4
3	5	263.0	263.1	3.1	4.0	0.8
3	5	261.0	261.2	9.7	11.1	1.4
3	5	259.0	259.2	16.7	17.9	1.2
3	5	257.0	257.3	23.3	24.6	1.4
3	5	255.0	255.3	30.2	31.6	1.4
3	5	253.0	253.2	33.0	34.1	1.1
3	5	251.0	251.2	33.0	34.1	1.1
3	5	249.0	249.3	33.0	34.1	1.1
3	6	250.0	250.5	100.0	100.0	0.0
3	6	251.0	251.5	100.0	100.0	0.0
3	6	252.0	252.4	83.3	74.3	-9.1
3	6	252.5	252.8	66.7	61.0	-5.6
3	6	253.0	253.3	45.8	45.5	-0.3
3	6	253.5	253.8	25.0	31.1	6.1
3	6	254.0	254.2	8.3	16.7	8.4
3	6	254.5	254.6	0.0	3.6	3.6
3	6	255.5	255.7	0.0	2.1	2.1
3	6	256.5	256.7	0.0	2.1	2.1
3	6	255.5	255.7	0.0	2.1	2.1
3	6	254.5	254.7	0.0	3.1	3.1
3	6	254.0	254.2	8.3	18.4	10.0
3	6	253.5	253.8	25.0	32.3	7.3
3	6	253.0	253.3	45.8	47.1	1.3
3	6	252.5	252.9	62.5	59.4	-3.1
3	6	252.0	252.4	83.3	74.6	-8.7

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
3	6	251.0	251.5	100.0	100.0	0.0
3	6	250.0	250.5	100.0	100.0	0.0
3	7	249.0	249.6	100.0	100.0	0.0
3	7	251.0	251.5	100.0	100.0	0.0
3	7	253.0	253.5	100.0	100.0	0.0
3	7	255.0	255.5	94.3	92.8	-1.5
3	7	257.0	257.5	83.9	82.9	-1.0
3	7	259.0	259.4	74.0	73.0	-1.0
3	7	261.0	261.3	64.1	65.0	0.9
3	7	263.0	263.3	53.6	53.3	-0.4
3	7	265.0	265.2	43.8	43.6	-0.2
3	7	267.0	267.3	32.8	33.6	0.8
3	7	265.0	265.3	43.2	43.5	0.3
3	7	263.0	263.3	53.6	53.4	-0.2
3	7	261.0	261.4	63.5	63.4	-0.2
3	7	259.0	259.4	74.0	73.1	-0.8
3	7	257.0	257.5	83.9	82.9	-1.0
3	7	255.0	255.5	94.3	92.7	-1.5
3	7	253.0	253.5	100.0	100.0	0.0
3	7	251.0	251.5	100.0	100.0	0.0
3	7	249.0	249.5	100.0	100.0	0.0
3	8	249.0	249.4	67.0	66.9	-0.1
3	8	251.0	251.4	67.0	67.0	0.0
3	8	253.0	253.4	67.0	67.0	0.0
3	8	255.0	255.4	67.0	67.0	0.0
3	8	257.0	257.4	67.0	67.0	0.0
3	8	259.0	259.3	49.0	49.3	0.3
3	8	261.0	261.2	29.2	30.6	1.4
3	8	263.0	263.2	8.3	11.7	3.3
3	8	261.0	261.3	28.1	30.3	2.1
3	8	259.0	259.3	49.0	49.3	0.3
3	8	257.0	257.4	67.0	66.8	-0.2
3	8	255.0	255.4	67.0	66.8	-0.2
3	8	253.0	253.4	67.0	67.0	0.0
3	8	251.0	251.4	67.0	67.0	0.0
3	8	249.0	249.4	67.0	67.0	0.0
3	9	249.0	249.3	33.0	34.1	1.1
3	9	251.0	251.3	33.0	34.1	1.1
3	9	253.0	253.3	33.0	34.1	1.1
3	9	255.0	255.3	33.0	34.1	1.1
3	9	257.0	257.3	33.0	34.1	1.1

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
3	9	259.0	259.3	33.0	34.1	1.1
3	9	261.0	261.3	28.1	30.3	2.1
3	9	263.0	263.2	8.3	11.3	3.0
3	9	261.0	261.3	28.1	30.1	2.0
3	9	259.0	259.3	33.0	34.1	1.1
3	9	257.0	257.3	33.0	34.1	1.1
3	9	255.0	255.3	33.0	34.1	1.1
3	9	253.0	253.3	33.0	34.1	1.1
3	9	251.0	251.3	33.0	34.1	1.1
3	9	249.0	249.3	33.0	34.1	1.1
4	1	288.0	288.2	100.0	100.0	0.0
4	1	290.0	290.2	100.0	100.0	0.0
4	1	292.0	292.2	100.0	100.0	0.0
4	1	294.0	294.2	96.0	98.0	2.0
4	1	296.0	296.2	78.0	81.6	3.6
4	1	298.0	298.1	60.8	63.2	2.4
4	1	300.0	300.1	42.8	48.8	6.0
4	1	302.0	302.0	25.6	30.4	4.8
4	1	304.0	304.0	7.6	11.8	4.3
4	1	302.0	302.0	25.6	30.9	5.3
4	1	300.0	300.1	42.8	47.2	4.4
4	1	298.0	298.1	60.8	63.2	2.4
4	1	296.0	296.1	78.9	82.1	3.2
4	1	294.0	294.2	96.0	98.0	2.0
4	1	292.0	292.2	100.0	100.0	0.0
4	1	290.0	290.2	100.0	100.0	0.0
4	1	288.0	288.3	100.0	100.0	0.0
4	2	288.0	289.6	100.0	100.1	0.1
4	2	290.0	291.6	100.0	100.1	0.1
4	2	292.0	293.5	100.0	100.0	0.0
4	2	294.0	295.1	87.9	84.6	-3.3
4	2	296.0	297.2	68.9	74.2	5.2
4	2	298.0	298.8	54.5	55.8	1.3
4	2	300.0	300.6	38.3	43.9	5.7
4	2	302.0	302.2	23.8	28.2	4.4
4	2	304.0	304.0	7.6	12.1	4.5
4	2	302.0	302.2	23.8	27.5	3.7
4	2	300.0	300.6	38.3	46.4	8.2
4	2	298.0	298.9	53.6	59.9	6.3
4	2	296.0	297.2	68.9	72.4	3.5
4	2	294.0	295.1	87.9	88.0	0.2

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
4	2	292.0	293.4	100.0	100.0	0.0
4	2	290.0	291.4	100.0	100.1	0.1
4	2	288.0	289.5	100.0	100.1	0.1
4	3	288.0	288.1	100.0	100.5	0.5
4	3	290.0	290.2	100.0	100.5	0.5
4	3	292.0	292.2	100.0	100.5	0.5
4	3	294.0	294.2	96.0	99.0	3.0
4	3	296.0	296.1	78.9	80.6	1.7
4	3	298.0	298.1	60.8	63.2	2.4
4	3	300.0	300.1	42.8	47.9	5.1
4	3	302.0	302.0	25.6	31.6	6.0
4	3	304.0	304.0	7.6	14.0	6.4
4	3	302.0	302.0	25.6	29.7	4.1
4	6	288.0	289.3	100.0	100.5	0.5
4	6	289.0	290.2	100.0	100.5	0.5
4	6	290.0	291.2	92.2	100.5	8.3
4	6	290.5	291.5	81.4	89.5	8.1
4	6	291.0	291.8	70.6	81.0	10.4
4	6	291.5	292.4	48.9	68.0	19.1
4	6	292.0	292.6	41.7	53.0	11.3
4	6	292.5	292.8	34.5	39.3	4.8
4	6	293.0	293.1	23.7	28.1	4.4
4	6	293.5	293.5	9.2	25.8	16.5
4	6	294.0	293.8	0.0	16.2	16.2
4	6	295.0	294.7	0.0	5.4	5.4
4	6	294.0	293.9	0.0	19.8	19.8
4	6	293.5	293.4	12.8	20.0	7.2
4	6	293.0	293.2	20.1	31.6	11.5
4	6	292.5	293.0	27.3	45.4	18.1
4	6	292.0	292.6	41.7	54.0	12.3
4	6	291.5	292.3	52.5	61.5	9.0
4	6	291.0	292.0	63.4	71.5	8.1
4	6	290.5	291.5	81.4	89.0	7.6
4	6	290.0	291.3	88.6	99.5	10.9
4	6	289.0	290.3	100.0	100.5	0.5
4	6	288.0	289.3	100.0	101.0	1.0
4	7	288.0	289.4	100.0	103.9	3.9
4	7	290.0	291.3	100.0	100.9	0.9
4	7	292.0	293.3	100.0	100.8	0.8
4	7	294.0	295.1	93.9	95.1	1.1
4	7	296.0	297.0	85.4	88.0	2.6

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
4	7	298.0	298.7	77.7	78.6	0.9
4	7	300.0	300.9	67.8	68.2	0.4
4	7	302.0	302.8	59.2	61.9	2.7
4	7	304.0	304.6	51.1	54.3	3.2
4	7	306.0	306.4	43.0	44.3	1.3
4	7	308.0	308.2	34.8	34.7	-0.1
4	7	306.0	306.4	43.0	43.8	0.8
4	7	304.0	304.6	51.1	54.2	3.1
4	7	302.0	302.8	59.2	63.3	4.0
4	7	300.0	301.0	67.3	71.1	3.7
4	7	298.0	298.7	77.7	78.8	1.1
4	7	296.0	296.9	85.8	86.1	0.3
4	7	294.0	295.1	93.9	94.3	0.4
4	7	292.0	293.3	100.0	100.7	0.6
4	7	290.0	291.3	100.0	100.7	0.6
4	7	288.0	289.3	100.0	100.8	0.8
4	8	288.0	289.1	67.0	69.0	2.0
4	8	290.0	291.1	67.0	69.5	2.5
4	8	292.0	293.1	67.0	70.0	3.0
4	8	294.0	295.1	67.0	70.4	3.4
4	8	296.0	297.1	67.0	70.9	3.9
4	8	298.0	298.8	54.5	56.1	1.6
4	8	300.0	300.5	39.2	41.9	2.7
4	8	302.0	302.1	24.7	24.3	-0.4
4	8	304.0	304.0	7.6	9.7	2.1
4	8	302.0	302.2	23.8	26.6	2.7
4	8	300.0	300.4	40.1	40.5	0.4
4	8	298.0	298.8	54.5	59.8	5.3
4	8	296.0	297.1	67.0	70.9	3.9
4	8	294.0	295.1	67.0	70.5	3.5
4	8	292.0	293.1	67.0	70.0	3.0
4	8	290.0	291.1	67.0	69.4	2.4
4	8	288.0	289.1	67.0	68.9	1.9
4	9	288.0	288.2	33.0	34.4	1.4
4	9	290.0	290.2	33.0	34.6	1.6
4	9	292.0	292.2	33.0	34.8	1.8
4	9	294.0	294.2	33.0	35.1	2.1
4	9	296.0	296.2	33.0	35.3	2.3
4	9	298.0	298.2	33.0	35.6	2.6
4	9	300.0	300.2	33.0	35.8	2.8
4	9	302.0	302.0	25.6	28.6	3.0

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Power (%)	Measured Power (%)	Power Error (% Rated)
4	9	304.0	303.8	7.6	13.3	5.7
4	9	302.0	302.0	25.6	28.3	2.6
4	9	300.0	300.1	33.0	35.8	2.8
4	9	298.0	298.2	33.0	35.5	2.5
4	9	296.0	296.2	33.0	35.3	2.3
4	9	294.0	294.2	33.0	35.1	2.1
4	9	292.0	292.2	33.0	34.8	1.8
4	9	290.0	290.2	33.0	34.5	1.5
4	9	288.0	288.2	33.0	34.3	1.3

Appendix B – Volt-Var Baseline Test Data

Test case (column 2) can be cross-referenced with Table 16.

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
1	1	120.0	120.3	0.0	-1.4	-1.4
1	1	119.0	119.3	0.0	-1.4	-1.4
1	1	118.0	118.3	0.0	-1.4	-1.4
1	1	117.0	117.3	0.0	-1.1	-1.1
1	1	116.0	116.3	1.2	-0.5	-1.7
1	1	115.0	115.3	12.9	3.5	-9.4
1	1	114.0	114.3	24.7	16.6	-8.1
1	1	113.0	113.3	36.5	26.6	-9.9
1	1	112.0	112.3	48.3	42.7	-5.6
1	1	111.0	111.3	56.5	48.9	-7.6
1	1	110.0	110.3	56.5	55.2	-1.3
1	1	109.0	109.3	56.5	58.7	2.2
1	1	108.0	108.3	56.5	58.7	2.2
1	1	120.0	120.3	0.0	3.3	3.3
1	1	121.0	121.3	0.0	-0.5	-0.5
1	1	122.0	122.3	0.0	0.0	0.0
1	1	123.0	123.3	0.0	-0.5	-0.5
1	1	124.0	124.3	-11.0	-1.6	9.4
1	1	125.0	125.3	-26.7	-28.3	-1.6
1	1	126.0	126.3	-42.4	-45.9	-3.5
1	1	127.0	127.3	-56.5	-59.8	-3.3
1	1	128.0	128.3	-56.5	-62.2	-5.7
1	1	129.0	129.3	-56.5	-61.7	-5.2
1	1	130.0	130.3	-56.5	-62.0	-5.5
1	1	131.0	131.3	-56.5	-62.2	-5.7
1	2	120.0	120.2	0.0	-0.8	-0.8
1	2	119.0	119.2	0.0	-0.8	-0.8
1	2	118.0	118.2	0.0	-0.8	-0.8
1	2	117.0	117.2	0.0	-0.8	-0.8
1	2	116.0	116.2	1.6	1.9	0.4
1	2	115.0	115.2	9.3	12.5	3.2
1	2	114.0	114.3	16.3	23.1	6.8
1	2	113.0	113.3	24.0	31.8	7.8
1	2	112.0	112.3	31.8	36.4	4.6
1	2	111.0	111.3	37.2	37.0	-0.2
1	2	110.0	110.3	37.2	37.0	-0.2
1	2	109.0	109.3	37.2	37.0	-0.2

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
1	2	108.0	108.3	37.2	37.0	-0.2
1	2	120.0	120.2	0.0	-0.5	-0.5
1	2	121.0	121.2	0.0	-1.1	-1.1
1	2	122.0	122.2	0.0	-1.4	-1.4
1	2	123.0	123.2	0.0	-1.4	-1.4
1	2	124.0	124.2	-6.2	-9.0	-2.8
1	2	125.0	125.2	-16.5	-20.7	-4.1
1	2	126.0	126.2	-26.9	-33.7	-6.8
1	2	127.0	127.2	-37.2	-39.4	-2.2
1	2	128.0	128.2	-37.2	-39.4	-2.2
1	2	129.0	129.2	-37.2	-39.4	-2.2
1	2	130.0	130.2	-37.2	-39.4	-2.2
1	2	131.0	131.2	-37.2	-39.4	-2.2
1	3	120.0	120.1	0.0	-0.3	-0.3
1	3	119.0	119.1	0.0	-0.3	-0.3
1	3	118.0	118.2	0.0	-0.3	-0.3
1	3	117.0	117.2	0.0	1.4	1.4
1	3	116.0	116.2	0.5	9.5	9.0
1	3	115.0	115.2	3.0	12.2	9.2
1	3	114.0	114.2	5.5	12.2	6.7
1	3	113.0	113.2	8.0	12.2	4.2
1	3	112.0	112.2	10.5	12.2	1.7
1	3	111.0	111.2	12.0	12.2	0.2
1	3	110.0	110.2	12.0	12.2	0.2
1	3	109.0	109.2	12.0	12.2	0.2
1	3	108.0	108.2	12.0	12.2	0.2
1	3	120.0	120.1	0.0	-0.3	-0.3
1	3	121.0	121.2	0.0	-0.3	-0.3
1	3	122.0	122.2	0.0	-0.3	-0.3
1	3	123.0	123.1	0.0	-0.3	-0.3
1	3	124.0	124.2	-2.0	-1.1	0.9
1	3	125.0	125.1	-5.0	-10.6	-5.6
1	3	126.0	126.2	-8.7	-12.2	-3.6
1	3	127.0	127.2	-12.0	-12.8	-0.8
1	3	128.0	128.2	-12.0	-12.5	-0.5
1	3	129.0	129.2	-12.0	-12.8	-0.8
1	3	130.0	130.2	-12.0	-12.5	-0.5
1	3	131.0	131.2	-12.0	-12.8	-0.8
1	4	120.0	120.3	5.0	4.9	-0.1
1	4	119.0	119.3	5.0	4.9	-0.1

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
1	4	118.0	118.3	5.0	4.9	-0.1
1	4	117.0	117.3	5.0	4.9	-0.1
1	4	116.0	116.3	6.1	5.4	-0.6
1	4	115.0	115.3	16.8	10.1	-6.7
1	4	114.0	114.3	27.5	16.0	-11.5
1	4	113.0	113.3	38.3	28.0	-10.3
1	4	112.0	112.3	49.0	44.0	-5.0
1	4	111.0	111.3	56.5	48.4	-8.1
1	4	110.0	110.3	56.5	57.1	0.6
1	4	109.0	109.3	56.5	58.4	1.9
1	4	108.0	108.3	56.5	58.4	1.9
1	4	120.0	120.3	5.0	4.3	-0.7
1	4	121.0	121.3	5.0	4.6	-0.4
1	4	122.0	122.3	5.0	4.1	-0.9
1	4	123.0	123.3	5.0	0.0	-5.0
1	4	124.0	124.3	-7.0	-13.6	-6.6
1	4	125.0	125.3	-24.0	-25.5	-1.5
1	4	126.0	126.3	-41.1	-48.9	-7.8
1	4	127.0	127.2	-56.5	-60.6	-4.1
1	4	128.0	128.2	-56.5	-62.5	-6.0
1	4	129.0	129.2	-56.5	-63.0	-6.5
1	4	130.0	130.2	-56.5	-62.8	-6.3
1	4	131.0	131.2	-56.5	-62.5	-6.0
1	5	120.0	120.3	-5.0	-8.2	-3.2
1	5	119.0	119.3	-5.0	-8.2	-3.2
1	5	118.0	118.3	-5.0	-8.2	-3.2
1	5	117.0	117.3	-5.0	-8.2	-3.2
1	5	116.0	116.3	-5.0	-8.2	-3.2
1	5	115.0	115.3	9.1	-3.8	-12.9
1	5	114.0	114.3	21.9	3.5	-18.4
1	5	113.0	113.3	34.7	18.5	-16.2
1	5	112.0	112.4	46.2	29.1	-17.2
1	5	111.0	111.4	56.5	45.7	-10.8
1	5	110.0	110.4	56.5	54.9	-1.6
1	5	109.0	109.4	56.5	58.7	2.2
1	5	108.0	108.4	56.5	59.0	2.5
1	5	120.0	120.3	-5.0	-6.3	-1.3
1	5	121.0	121.3	-5.0	-6.8	-1.8
1	5	122.0	122.3	-5.0	-9.0	-4.0
1	5	123.0	123.3	-5.0	-15.2	-10.2

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
1	5	124.0	124.3	-15.0	-26.6	-11.6
1	5	125.0	125.3	-29.3	-39.4	-10.1
1	5	126.0	126.3	-43.6	-53.8	-10.2
1	5	127.0	127.3	-56.5	-61.4	-4.9
1	5	128.0	128.3	-56.5	-62.2	-5.7
1	5	129.0	129.3	-56.5	-62.5	-6.0
1	5	130.0	130.3	-56.5	-62.5	-6.0
1	5	131.0	131.3	-56.5	-62.5	-6.0
1	6	120.0	120.3	0.0	-59.2	-59.2
1	6	119.5	119.8	10.3	-57.1	-67.4
1	6	119.0	119.3	36.2	-31.3	-67.4
1	6	118.5	118.8	62.0	4.1	-57.9
1	6	118.0	118.3	62.0	24.5	-37.5
1	6	117.5	117.8	62.0	43.2	-18.8
1	6	117.0	117.4	62.0	62.5	0.5
1	6	116.5	116.8	62.0	61.1	-0.9
1	6	120.0	120.3	-15.5	8.7	24.2
1	6	120.5	120.8	-41.3	-46.2	-4.9
1	6	121.0	121.3	-62.0	-65.2	-3.2
1	6	121.5	121.8	-62.0	-66.3	-4.3
1	6	122.0	122.3	-62.0	-66.3	-4.3
1	6	122.5	122.7	-62.0	-64.4	-2.4
1	6	123.0	123.2	-62.0	-63.6	-1.6
1	6	123.5	123.8	-62.0	-64.1	-2.1
1	7	120.0	120.3	0.0	-1.4	-1.4
1	7	118.5	118.8	0.0	-1.4	-1.4
1	7	117.0	117.3	0.0	-1.4	-1.4
1	7	115.5	115.8	0.0	-1.4	-1.4
1	7	114.0	114.3	0.0	-1.4	-1.4
1	7	112.0	112.3	5.7	2.2	-3.6
1	7	110.0	110.3	12.5	8.4	-4.0
1	7	108.0	108.4	18.9	15.5	-3.4
1	7	106.0	106.4	25.6	23.1	-2.5
1	7	104.0	104.4	28.3	27.2	-1.1
1	7	120.0	120.3	0.0	0.0	0.0
1	7	121.5	121.8	0.0	-1.1	-1.1
1	7	123.0	123.3	0.0	-1.6	-1.6
1	7	124.5	124.8	0.0	-1.9	-1.9
1	7	126.0	126.3	-1.4	-6.5	-5.1
1	7	128.0	128.3	-10.8	-14.9	-4.1

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
1	7	130.0	130.3	-20.3	-24.7	-4.4
1	7	132.0	132.3	-28.3	-30.7	-2.4
1	7	134.0	134.3	-28.3	-31.5	-3.2
1	8	108.0	108.4	62.0	62.5	0.5
1	8	120.0	120.3	0.0	-1.4	-1.4
1	8	132.0	132.3	-62.0	-61.1	0.9
1	8	120.0	120.3	0.0	-2.7	-2.7
1	9	108.0	108.4	62.0	64.9	2.9
1	9	120.0	120.4	0.0	-0.8	-0.8
1	9	132.0	132.3	-62.0	-63.6	-1.6
1	9	120.0	120.3	0.0	-1.6	-1.6
2	1	120.0	120.3	0.0	2.2	2.2
2	1	119.0	119.3	0.0	2.2	2.2
2	1	118.0	118.3	0.0	2.2	2.2
2	1	117.0	117.3	0.0	2.2	2.2
2	1	116.0	116.3	0.0	2.2	2.2
2	1	115.0	115.3	0.0	2.2	2.2
2	1	114.0	114.3	0.0	2.2	2.2
2	1	113.0	113.3	0.0	2.2	2.2
2	1	112.0	112.3	0.0	2.7	2.7
2	1	111.0	111.3	0.0	3.3	3.3
2	1	110.0	110.3	0.0	3.3	3.3
2	1	109.0	109.3	0.0	3.6	3.6
2	1	108.0	108.3	0.0	3.3	3.3
2	1	120.0	120.3	0.0	2.2	2.2
2	1	121.0	121.3	0.0	2.2	2.2
2	1	122.0	122.3	0.0	2.2	2.2
2	1	123.0	123.3	0.0	2.2	2.2
2	1	124.0	124.3	0.0	2.9	2.9
2	1	125.0	125.3	0.0	3.8	3.8
2	1	126.0	126.3	0.0	4.5	4.5
2	1	127.0	127.3	0.0	4.9	4.9
2	1	128.0	128.3	0.0	4.9	4.9
2	1	129.0	129.3	0.0	4.7	4.7
2	1	130.0	130.3	0.0	4.5	4.5
2	1	131.0	131.2	0.0	2.9	2.9
2	2	120.0	120.2	0.0	1.8	1.8
2	2	119.0	119.2	0.0	1.8	1.8
2	2	118.0	118.2	0.0	1.8	1.8
2	2	117.0	117.2	0.0	1.8	1.8

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
2	2	116.0	116.2	1.7	1.8	0.1
2	2	115.0	115.2	10.0	6.0	-4.0
2	2	114.0	114.3	17.5	13.8	-3.7
2	2	113.0	113.3	25.8	22.3	-3.5
2	2	112.0	112.3	34.2	30.4	-3.8
2	2	111.0	111.3	40.0	38.6	-1.4
2	2	110.0	110.3	40.0	39.7	-0.3
2	2	109.0	109.3	40.0	39.7	-0.3
2	2	108.0	108.3	40.0	39.5	-0.5
2	2	120.0	120.2	0.0	1.8	1.8
2	2	121.0	121.2	0.0	1.8	1.8
2	2	122.0	122.2	0.0	1.8	1.8
2	2	123.0	123.2	0.0	2.5	2.5
2	2	124.0	124.2	-6.7	-11.8	-5.2
2	2	125.0	125.2	-17.8	-22.5	-4.8
2	2	126.0	126.2	-28.9	-33.3	-4.4
2	2	127.0	127.2	-40.0	-40.8	-0.8
2	2	128.0	128.2	-40.0	-40.8	-0.8
2	2	129.0	129.2	-40.0	-41.1	-1.1
2	2	130.0	130.2	-40.0	-40.8	-0.8
2	2	131.0	131.2	-40.0	-41.5	-1.5
2	3	120.0	120.1	0.0	2.2	2.2
2	3	119.0	119.1	0.0	2.2	2.2
2	3	118.0	118.1	0.0	2.2	2.2
2	3	117.0	117.1	0.0	2.2	2.2
2	3	116.0	116.1	3.1	2.7	-0.4
2	3	115.0	115.1	13.3	11.6	-1.7
2	3	114.0	114.1	23.5	21.9	-1.6
2	3	113.0	113.1	33.7	31.7	-2.0
2	3	112.0	112.1	43.9	42.0	-1.9
2	3	111.0	111.1	49.0	49.3	0.3
2	3	110.0	110.2	49.0	49.3	0.3
2	3	109.0	109.2	49.0	49.3	0.3
2	3	108.0	108.1	49.0	49.3	0.3
2	3	120.0	120.1	0.0	2.2	2.2
2	3	121.0	121.1	0.0	2.2	2.2
2	3	122.0	122.1	0.0	2.2	2.2
2	3	123.0	123.1	0.0	2.2	2.2
2	3	124.0	124.1	-6.8	-0.2	6.6
2	3	125.0	125.1	-20.4	-22.8	-2.4

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
2	3	126.0	126.1	-34.0	-36.2	-2.1
2	3	127.0	127.1	-47.6	-46.9	0.8
2	3	128.0	128.1	-49.0	-49.8	-0.8
2	3	129.0	129.1	-49.0	-49.8	-0.8
2	3	130.0	130.1	-49.0	-49.8	-0.8
2	3	131.0	131.1	-49.0	-49.6	-0.6
2	4	120.0	120.3	2.5	4.0	1.5
2	4	119.0	119.3	2.5	4.0	1.5
2	4	118.0	118.3	2.5	4.0	1.5
2	4	117.0	117.3	2.5	4.2	1.7
2	4	116.0	116.3	3.3	4.2	1.0
2	4	115.0	115.3	11.1	9.4	-1.7
2	4	114.0	114.3	18.9	16.5	-2.4
2	4	113.0	113.3	26.7	24.1	-2.6
2	4	112.0	112.3	34.5	31.3	-3.3
2	4	111.0	111.3	40.0	38.8	-1.2
2	4	110.0	110.3	40.0	39.7	-0.3
2	4	109.0	109.3	40.0	39.7	-0.3
2	4	108.0	108.3	40.0	39.5	-0.5
2	4	120.0	120.2	2.5	4.0	1.5
2	4	121.0	121.2	2.5	4.0	1.5
2	4	122.0	122.2	2.5	4.0	1.5
2	4	123.0	123.2	2.5	3.1	0.6
2	4	124.0	124.2	-4.6	-0.7	3.9
2	4	125.0	125.2	-16.4	-20.8	-4.4
2	4	126.0	126.2	-28.2	-32.4	-4.2
2	4	127.0	127.2	-40.0	-40.8	-0.8
2	4	128.0	128.2	-40.0	-40.8	-0.8
2	4	129.0	129.2	-40.0	-40.8	-0.8
2	4	130.0	130.2	-40.0	-40.8	-0.8
2	4	131.0	131.2	-40.0	-41.5	-1.5
2	5	120.0	120.2	-2.5	**-5.1**	-2.6
2	5	119.0	119.2	-2.5	**-5.1**	-2.6
2	5	118.0	118.2	-2.5	**-4.7**	-2.2
2	5	117.0	117.2	-2.5	**-4.7**	-2.2
2	5	116.0	116.2	-2.5	**-4.5**	-2.0
2	5	115.0	115.2	8.1	3.3	-4.8
2	5	114.0	114.2	17.0	11.6	-5.4
2	5	113.0	113.2	25.8	20.8	-5.1
2	5	112.0	112.2	34.7	29.7	-5.0

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
2	5	111.0	111.2	40.0	38.8	-1.2
2	5	110.0	110.2	40.0	39.7	-0.3
2	5	109.0	109.2	40.0	39.7	-0.3
2	5	108.0	108.2	40.0	39.5	-0.5
2	5	120.0	120.2	-2.5	**-5.1**	-2.6
2	5	121.0	121.2	-2.5	**-5.1**	-2.6
2	5	122.0	122.2	-2.5	**-5.1**	-2.6
2	5	123.0	123.2	-2.5	**-5.8**	-3.3
2	5	124.0	124.2	-8.7	-14.1	-5.3
2	5	125.0	125.2	-19.2	-24.3	-5.2
2	5	126.0	126.2	-29.6	-33.9	-4.3
2	5	127.0	127.2	-40.0	-40.8	-0.8
2	5	128.0	128.2	-40.0	-40.8	-0.8
2	5	129.0	129.2	-40.0	-41.1	-1.1
2	5	130.0	130.2	-40.0	-40.8	-0.8
2	5	131.0	131.2	-40.0	-41.5	-1.5
2	6	120.0	120.3	0.0	-35.5	-35.5
2	6	119.5	119.8	13.3	6.9	-6.4
2	6	119.0	119.3	46.7	22.1	-24.6
2	6	118.5	118.8	80.0	54.5	-25.5
2	6	118.0	118.3	80.0	79.9	-0.1
2	6	117.5	117.9	80.0	81.0	1.0
2	6	117.0	117.4	80.0	81.0	1.0
2	6	116.5	116.9	80.0	81.0	1.0
2	6	120.0	120.3	-20.0	-35.3	-15.3
2	6	120.5	120.8	-53.3	-67.4	-14.1
2	6	121.0	121.3	-80.0	-80.4	-0.4
2	6	121.5	121.7	-80.0	-82.1	-2.1
2	6	122.0	122.2	-80.0	-82.1	-2.1
2	6	122.5	122.7	-80.0	-82.1	-2.1
2	6	123.0	123.2	-80.0	-82.1	-2.1
2	6	123.5	123.7	-80.0	-82.1	-2.1
2	7	120.0	120.2	0.0	1.8	1.8
2	7	118.5	118.7	0.0	1.8	1.8
2	7	117.0	117.2	0.0	1.8	1.8
2	7	115.5	115.7	0.0	1.8	1.8
2	7	114.0	114.2	0.0	1.8	1.8
2	7	112.0	112.2	4.3	3.3	-0.9
2	7	110.0	110.2	9.0	7.4	-1.7
2	7	108.0	108.2	13.8	11.8	-2.0

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
2	7	106.0	106.2	18.6	17.4	-1.2
2	7	104.0	104.2	20.0	19.9	-0.1
2	7	120.0	120.2	0.0	1.8	1.8
2	7	121.5	121.7	0.0	1.8	1.8
2	7	123.0	123.2	0.0	1.8	1.8
2	7	124.5	124.7	0.0	2.0	2.0
2	7	126.0	126.2	-0.7	3.1	3.8
2	7	128.0	128.2	-7.3	-0.7	6.7
2	7	130.0	130.2	-14.0	-15.6	-1.6
2	7	132.0	132.2	-20.0	-21.2	-1.2
2	7	134.0	134.2	-20.0	-21.0	-1.0
3	1	240.0	240.6	0.0	3.7	3.7
3	1	238.0	238.6	0.0	3.7	3.7
3	1	236.0	236.6	0.0	3.7	3.7
3	1	234.0	234.6	0.0	3.7	3.7
3	1	232.0	232.6	0.5	3.7	3.1
3	1	230.0	230.6	5.7	6.7	0.9
3	1	228.0	228.6	10.9	11.5	0.6
3	1	226.0	226.6	16.1	16.7	0.5
3	1	224.0	224.6	21.4	21.8	0.5
3	1	222.0	222.6	25.0	26.7	1.7
3	1	220.0	220.6	25.0	26.7	1.7
3	1	218.0	218.6	25.0	26.7	1.7
3	1	216.0	216.6	25.0	26.7	1.7
3	1	240.0	240.6	0.0	3.7	3.7
3	1	242.0	242.6	0.0	3.7	3.7
3	1	244.0	244.6	0.0	3.7	3.7
3	1	246.0	246.6	0.0	3.7	3.7
3	1	248.0	248.6	-4.9	-6.0	-1.1
3	1	250.0	250.6	-11.8	-12.2	-0.4
3	1	252.0	252.5	-18.4	-19.0	-0.6
3	1	254.0	254.5	-25.0	-24.5	0.5
3	1	256.0	256.5	-25.0	-24.5	0.5
3	1	258.0	258.5	-25.0	-24.5	0.5
3	1	260.0	260.5	-25.0	-24.5	0.5
3	1	262.0	262.5	-25.0	-24.5	0.5
3	2	240.0	240.4	0.0	2.7	2.7
3	2	238.0	238.4	0.0	2.7	2.7
3	2	236.0	236.4	0.0	2.7	2.7
3	2	234.0	234.4	0.0	2.7	2.7

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
3	2	232.0	232.4	1.0	2.8	1.8
3	2	230.0	230.5	6.0	7.2	1.2
3	2	228.0	228.5	11.2	12.2	1.0
3	2	226.0	226.5	16.4	17.3	0.9
3	2	224.0	224.5	21.6	22.5	0.9
3	2	222.0	222.5	25.0	26.2	1.2
3	2	220.0	220.5	25.0	26.2	1.2
3	2	218.0	218.5	25.0	26.2	1.2
3	2	216.0	216.5	25.0	26.2	1.2
3	2	240.0	240.4	0.0	2.7	2.7
3	2	242.0	242.4	0.0	2.7	2.7
3	2	244.0	244.4	0.0	2.7	2.7
3	2	246.0	246.4	0.0	2.7	2.7
3	2	248.0	248.4	-4.2	-4.3	-0.2
3	2	250.0	250.4	-11.1	-10.8	0.3
3	2	252.0	252.4	-18.1	-17.7	0.4
3	2	254.0	254.4	-25.0	-24.7	0.3
3	2	256.0	256.4	-25.0	-24.7	0.3
3	2	258.0	258.4	-25.0	-24.7	0.3
3	2	260.0	260.4	-25.0	-24.7	0.3
3	2	262.0	262.4	-25.0	-24.7	0.3
3	3	240.0	240.3	0.0	2.2	2.2
3	3	238.0	238.3	0.0	2.2	2.2
3	3	236.0	236.3	0.0	2.2	2.2
3	3	234.0	234.3	0.0	2.2	2.2
3	3	232.0	232.3	1.3	3.2	1.9
3	3	230.0	230.3	6.5	7.8	1.3
3	3	228.0	228.3	11.7	12.8	1.1
3	3	226.0	226.3	16.9	18.2	1.2
3	3	224.0	224.3	22.1	23.3	1.2
3	3	222.0	222.3	25.0	25.7	0.7
3	3	220.0	220.3	25.0	25.7	0.7
3	3	218.0	218.3	25.0	25.7	0.7
3	3	216.0	216.3	25.0	25.7	0.7
3	3	240.0	240.3	0.0	2.2	2.2
3	3	242.0	242.3	0.0	2.3	2.3
3	3	244.0	244.3	0.0	2.3	2.3
3	3	246.0	246.3	0.0	2.3	2.3
3	3	248.0	248.3	-3.8	-3.5	0.3
3	3	250.0	250.3	-10.8	-9.7	1.1

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
3	3	252.0	252.2	-17.4	-16.5	0.9
3	3	254.0	254.2	-24.3	-23.5	0.8
3	3	256.0	256.2	-25.0	-25.0	0.0
3	3	258.0	258.2	-25.0	-25.0	0.0
3	3	260.0	260.2	-25.0	-25.0	0.0
3	3	262.0	262.2	-25.0	-25.0	0.0
3	4	240.0	240.6	2.5	5.0	2.5
3	4	238.0	238.6	2.5	5.0	2.5
3	4	236.0	236.6	2.5	5.0	2.5
3	4	234.0	234.6	2.5	5.0	2.5
3	4	232.0	232.6	3.0	5.0	2.0
3	4	230.0	230.6	7.7	8.5	0.8
3	4	228.0	228.6	12.3	13.0	0.7
3	4	226.0	226.6	17.0	17.7	0.6
3	4	224.0	224.6	21.7	22.2	0.4
3	4	222.0	222.7	25.0	26.5	1.5
3	4	220.0	220.7	25.0	26.5	1.5
3	4	218.0	218.7	25.0	26.5	1.5
3	4	216.0	216.7	25.0	26.5	1.5
3	4	240.0	240.6	2.5	5.2	2.7
3	4	242.0	242.6	2.5	5.2	2.7
3	4	244.0	244.6	2.5	5.2	2.7
3	4	246.0	246.6	2.5	5.0	2.5
3	4	248.0	248.6	-2.8	-4.6	-1.7
3	4	250.0	250.5	-10.1	-11.0	-0.9
3	4	252.0	252.5	-17.7	-18.5	-0.8
3	4	254.0	254.5	-25.0	-24.5	0.5
3	4	256.0	256.5	-25.0	-24.5	0.5
3	4	258.0	258.5	-25.0	-24.5	0.5
3	4	260.0	260.5	-25.0	-24.5	0.5
3	4	262.0	262.5	-25.0	-24.5	0.5
3	5	240.0	240.6	-2.5	3.7	6.2
3	5	238.0	238.6	-2.5	3.7	6.2
3	5	236.0	236.6	-2.5	3.7	6.2
3	5	234.0	234.6	-2.5	3.7	6.2
3	5	232.0	232.6	-2.5	3.7	6.2
3	5	230.0	230.6	3.8	5.2	1.4
3	5	228.0	228.6	9.5	10.2	0.6
3	5	226.0	226.6	15.3	15.5	0.2
3	5	224.0	224.7	20.7	21.2	0.5

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
3	5	222.0	222.7	25.0	26.5	1.5
3	5	220.0	220.7	25.0	26.5	1.5
3	5	218.0	218.7	25.0	26.5	1.5
3	5	216.0	216.6	25.0	26.5	1.5
3	5	240.0	240.6	-2.5	3.7	6.2
3	5	242.0	242.6	-2.5	3.7	6.2
3	5	244.0	244.6	-2.5	3.7	6.2
3	5	246.0	246.6	-0.6	3.7	4.3
3	5	248.0	248.6	-6.9	-7.7	-0.8
3	5	250.0	250.6	-13.1	-13.5	-0.4
3	5	252.0	252.6	-19.4	-19.7	-0.3
3	5	254.0	254.5	-25.0	-24.5	0.5
3	5	256.0	256.5	-25.0	-24.5	0.5
3	5	258.0	258.5	-25.0	-24.5	0.5
3	5	260.0	260.5	-25.0	-24.5	0.5
3	5	262.0	262.5	-25.0	-24.5	0.5
3	6	240.0	240.6	**-12.5**	-18.7	-6.2
3	6	239.0	239.6	8.3	3.5	-4.8
3	6	238.0	238.6	29.2	21.7	-7.5
3	6	237.0	237.7	47.9	43.3	-4.6
3	6	236.0	236.6	50.0	51.5	1.5
3	6	235.0	235.7	50.0	51.5	1.5
3	6	234.0	234.7	50.0	51.5	1.5
3	6	233.0	233.7	50.0	51.5	1.5
3	6	232.0	232.7	50.0	51.5	1.5
3	6	231.0	231.6	50.0	51.5	1.5
3	6	240.0	240.6	-12.5	-18.2	-5.7
3	6	241.0	241.5	-31.3	-37.0	-5.7
3	6	242.0	242.4	-50.0	-49.8	0.2
3	6	243.0	243.4	-50.0	-49.8	0.2
3	6	244.0	244.4	-50.0	-49.8	0.2
3	6	245.0	245.5	-50.0	-49.8	0.2
3	6	246.0	246.5	-50.0	-49.8	0.2
3	6	247.0	247.5	-50.0	-49.8	0.2
3	7	240.0	240.6	0.0	3.7	3.7
3	7	237.0	237.6	0.0	3.7	3.7
3	7	234.0	234.6	0.0	3.7	3.7
3	7	231.0	231.6	0.0	3.5	3.5
3	7	228.0	228.6	0.0	3.5	3.5
3	7	224.0	224.6	2.5	4.8	2.3

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
3	7	220.0	220.6	5.5	7.2	1.7
3	7	216.0	216.6	8.5	9.8	1.4
3	7	212.0	212.6	11.5	12.7	1.2
3	7	208.0	208.6	12.5	14.0	1.5
3	7	240.0	240.6	0.0	3.5	3.5
3	7	243.0	243.6	0.0	3.5	3.5
3	7	246.0	246.6	0.0	3.5	3.5
3	7	249.0	249.6	0.0	3.5	3.5
3	7	252.0	252.6	-0.6	3.3	4.0
3	7	256.0	256.6	-4.8	-5.3	-0.5
3	7	260.0	260.6	-9.0	-9.0	0.0
3	7	264.0	264.6	-12.5	-12.2	0.3
3	8	240.0	240.6	0.0	3.7	3.7
3	8	238.0	238.6	0.0	3.7	3.7
3	8	236.0	236.6	0.0	3.7	3.7
3	8	234.0	234.6	0.0	3.7	3.7
3	8	232.0	232.6	0.5	3.7	3.1
3	8	230.0	230.6	5.7	6.5	0.8
3	8	228.0	228.6	10.9	11.3	0.4
3	8	226.0	226.6	16.1	16.3	0.2
3	8	224.0	224.6	21.4	21.5	0.1
3	8	222.0	222.6	25.0	26.3	1.3
3	8	220.0	220.6	25.0	26.3	1.3
3	8	218.0	218.7	25.0	26.3	1.3
3	8	216.0	216.7	25.0	26.5	1.5
3	8	240.0	240.6	0.0	3.7	3.7
3	8	242.0	242.6	0.0	3.7	3.7
3	8	244.0	244.6	0.0	3.7	3.7
3	8	246.0	246.6	0.0	3.7	3.7
3	8	248.0	248.6	-4.9	-6.0	-1.1
3	8	250.0	250.5	-11.5	-12.2	-0.7
3	8	252.0	252.5	-18.4	-19.0	-0.6
3	8	254.0	254.5	-25.0	-24.8	0.2
3	8	256.0	256.5	-25.0	-24.8	0.2
3	8	258.0	258.5	-25.0	-24.8	0.2
3	8	260.0	260.5	-25.0	-24.8	0.2
3	8	262.0	262.5	-25.0	-24.8	0.2
4	1	277.0	278.3	0.0	2.1	2.1
4	1	275.0	276.3	0.0	2.1	2.1
4	1	273.0	274.3	0.0	2.1	2.1

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
4	1	271.0	272.3	0.0	2.1	2.1
4	1	268.8	270.1	0.0	2.1	2.1
4	1	266.0	267.5	3.1	3.2	0.0
4	1	262.0	264.0	11.4	11.2	-0.2
4	1	260.0	262.3	15.5	15.4	-0.1
4	1	257.7	260.3	20.2	20.1	-0.1
4	1	255.5	258.4	24.7	24.6	-0.2
4	1	253.0	256.0	26.3	26.1	-0.2
4	1	250.5	253.5	26.3	26.3	-0.1
4	1	248.0	251.0	26.3	26.4	0.1
4	1	277.0	278.4	0.0	2.1	2.1
4	1	279.1	280.4	0.0	2.1	2.1
4	1	281.2	282.4	0.0	2.1	2.1
4	1	283.3	284.5	0.0	2.1	2.1
4	1	285.4	286.4	-3.0	-4.5	-1.4
4	1	287.5	288.1	-8.4	-9.3	-0.8
4	1	289.6	289.9	-14.1	-14.5	-0.4
4	1	291.6	291.6	-19.5	-19.6	0.0
4	1	293.7	293.4	-25.2	-25.5	-0.3
4	1	295.8	295.3	-26.3	-27.4	-1.1
4	1	297.9	297.4	-26.3	-27.1	-0.8
4	1	300.0	299.5	-26.3	-27.1	-0.8
4	2	277.0	277.7	0.0	1.4	1.4
4	2	275.0	275.7	0.0	1.4	1.4
4	2	273.0	273.7	0.0	1.4	1.4
4	2	271.0	271.7	0.0	1.3	1.3
4	2	268.8	269.5	0.0	1.3	1.3
4	2	266.0	266.9	4.5	4.7	0.2
4	2	262.0	263.3	13.1	14.0	0.8
4	2	260.0	261.4	17.6	18.7	1.0
4	2	257.7	259.3	22.6	23.3	0.6
4	2	255.5	257.3	26.3	26.6	0.2
4	2	253.0	254.8	26.3	26.6	0.2
4	2	250.5	252.3	26.3	26.5	0.2
4	2	248.0	249.8	26.3	26.5	0.2
4	2	277.0	277.8	0.0	1.4	1.4
4	2	279.1	279.8	0.0	1.4	1.4
4	2	281.2	281.9	0.0	1.5	1.5
4	2	283.3	284	0.0	1.5	1.5
4	2	285.4	286.1	-2.1	-2.2	-0.1

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
4	2	287.5	287.9	-7.8	-8.1	-0.3
4	2	289.6	289.8	-13.8	-12.7	1.1
4	2	291.6	291.6	-19.5	-19.5	0.1
4	2	293.7	293.5	-25.5	-25.8	-0.3
4	2	295.8	295.6	-26.3	-26.8	-0.5
4	2	297.9	297.6	-26.3	-27.2	-0.8
4	2	300.0	299.7	-26.3	-27.2	-0.9
4	3	277.0	276.8	0.0	1.9	1.9
4	3	275.0	274.8	0.0	2.0	2.0
4	3	273.0	272.8	0.0	2.0	2.0
4	3	271.0	270.8	0.0	1.9	1.9
4	3	268.8	268.7	0.3	2.6	2.3
4	3	266.0	266.1	6.4	7.2	0.8
4	3	262.0	262.6	14.8	16.2	1.4
4	3	260.0	260.7	19.3	20.6	1.3
4	3	257.7	258.6	24.3	25.0	0.7
4	3	255.5	256.5	26.3	26.7	0.3
4	3	253.0	254	26.3	26.7	0.3
4	3	250.5	251.5	26.3	26.7	0.3
4	3	248.0	249	26.3	26.8	0.4
4	3	277.0	276.9	0.0	2.0	2.0
4	3	279.1	278.9	0.0	2.0	2.0
4	3	281.2	281	0.0	2.0	2.0
4	3	283.3	283.1	0.0	2.1	2.1
4	3	285.4	285.1	0.0	2.1	2.1
4	3	287.5	287	-4.9	-5.2	-0.2
4	3	289.6	288.8	-10.6	-10.9	-0.2
4	3	291.6	290.7	-16.7	-15.5	1.2
4	3	293.7	292.6	-22.7	-21.9	0.8
4	3	295.8	294.5	-26.3	-26.3	0.0
4	3	297.9	296.6	-26.3	-26.4	-0.1
4	3	300.0	298.7	-26.3	-26.5	-0.2
4	4	277.0	278.4	2.5	2.9	0.4
4	4	275.0	276.4	2.5	3.0	0.5
4	4	273.0	274.5	2.5	3.0	0.5
4	4	271.0	272.5	2.5	2.9	0.4
4	4	268.8	270.3	2.5	2.8	0.3
4	4	266.0	267.7	4.9	5.4	0.5
4	4	262.0	264.2	12.4	12.0	-0.5
4	4	260.0	262.4	16.3	16.4	0.1

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
4	4	257.7	260.3	20.8	20.6	-0.3
4	4	255.5	258.4	24.9	25.0	0.1
4	4	253.0	256	26.3	26.3	-0.1
4	4	250.5	253.5	26.3	26.4	0.1
4	4	248.0	251	26.3	26.3	-0.1
4	4	277.0	278.6	2.5	3.0	0.5
4	4	279.1	280.5	2.5	3.1	0.6
4	4	281.2	282.6	2.5	2.9	0.4
4	4	283.3	284.7	2.5	3.1	0.6
4	4	285.4	286.6	-1.5	2.1	3.6
4	4	287.5	288.3	-7.4	-3.1	4.3
4	4	289.6	290	-13.3	-13.2	0.2
4	4	291.6	291.6	-18.9	-18.2	0.7
4	4	293.7	293.4	-25.1	-25.3	-0.1
4	4	295.8	295.3	-26.3	-27.0	-0.7
4	4	297.9	297.4	-26.3	-27.0	-0.7
4	4	300.0	299.5	-26.3	-27.0	-0.7
4	5	277.0	278.1	-2.5	-3.8	-1.3
4	5	275.0	276.1	-2.5	-3.8	-1.3
4	5	273.0	274.2	-2.5	-3.7	-1.2
4	5	271.0	272.2	-2.5	-3.6	-1.1
4	5	268.8	270	-2.5	-3.4	-0.9
4	5	266.0	267.4	1.2	2.0	0.8
4	5	262.0	264	10.0	10.6	0.6
4	5	260.0	262.2	14.7	13.7	-1.0
4	5	257.7	260.4	19.4	20.2	0.8
4	5	255.5	258.4	24.6	24.2	-0.4
4	5	253.0	256	26.3	26.1	-0.3
4	5	250.5	253.5	26.3	26.5	0.2
4	5	248.0	251	26.3	26.5	0.2
4	5	277.0	278.2	-2.5	-3.8	-1.3
4	5	279.1	280	-2.5	-3.8	-1.3
4	5	281.2	282.1	-2.5	-3.8	-1.3
4	5	283.3	284.4	-2.5	-3.8	-1.3
4	5	285.4	286.4	-5.2	-5.8	-0.6
4	5	287.5	288.1	-10.1	-10.3	-0.1
4	5	289.6	289.8	-15.0	-16.1	-1.1
4	5	291.6	291.6	-20.2	-20.5	-0.3
4	5	293.7	293.3	-25.0	-26.4	-1.3
4	5	295.8	295.3	-26.3	-27.2	-0.8

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
4	5	297.9	297.4	-26.3	-27.3	-0.9
4	5	300.0	299.5	-26.3	-27.5	-1.2
4	7	277.1	278.3	0.0	2.0	2.0
4	7	273.1	274.4	0.0	2.0	2.0
4	7	269.1	270.4	0.0	2.0	2.0
4	7	265.1	266.5	0.0	2.0	2.0
4	7	261.1	262.5	0.5	1.9	1.4
4	7	257.1	258.7	3.1	3.4	0.2
4	7	253.1	254.9	5.7	5.8	0.1
4	7	249.1	251.0	8.3	8.0	-0.3
4	7	245.1	247.3	10.8	10.9	0.1
4	7	241.1	243.4	13.2	13.0	-0.2
4	7	277.1	278.4	0.0	2.0	2.0
4	7	280.1	281.4	0.0	2.0	2.0
4	7	283.1	284.3	0.0	2.1	2.1
4	7	286.1	287.3	0.0	2.1	2.1
4	7	289.1	290.2	0.0	2.1	2.1
4	7	292.1	293.1	-2.0	-3.2	-1.2
4	7	295.1	295.9	-4.7	-5.3	-0.6
4	7	298.1	298.7	-7.3	-8.3	-1.0
4	7	301.1	301.6	-10.1	-10.6	-0.5
4	8	277.0	278.4	0.0	2.0	2.0
4	8	275.0	276.3	0.0	2.0	2.0
4	8	273.0	274.3	0.0	2.1	2.1
4	8	271.0	272.3	0.0	2.0	2.0
4	8	268.8	270.2	0.0	2.0	2.0
4	8	266.0	267.5	3.1	2.8	-0.4
4	8	262.0	264.0	11.4	10.3	-1.1
4	8	260.0	262.3	15.5	15.1	-0.4
4	8	257.7	260.3	20.2	19.9	-0.4
4	8	255.5	258.3	25.0	24.0	-1.0
4	8	253.0	256.0	26.3	26.2	-0.2
4	8	250.5	253.5	26.3	26.3	0.0
4	8	248.0	251.0	26.3	26.4	0.1
4	8	277.0	278.5	0.0	2.1	2.1
4	8	279.1	280.4	0.0	2.0	2.0
4	8	281.2	282.5	0.0	2.1	2.1
4	8	283.3	284.5	0.0	2.1	2.1
4	8	285.4	286.4	-3.0	-3.8	-0.8
4	8	287.5	288.2	-8.7	-9.0	-0.3

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Power Error (% Rated)
4	8	289.6	290.0	-14.4	-14.1	0.4
4	8	291.6	291.7	-19.8	-19.4	0.5
4	8	293.7	293.4	-25.2	-24.8	0.4
4	8	295.8	295.4	-26.3	-27.3	-1.0
4	8	297.9	297.4	-26.3	-27.3	-1.0
4	8	300.0	299.5	-26.3	-27.4	-1.0

Appendix C – Volt-Watt and Volt-Var Test Data

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Reactive Power Error (% Rated)	Expected Real Power (%)	Measured Real Power (%)	Real Power Error (% Rated)
1	1	120.0	120.3	0.0	-1.6	-1.6	100.0	100.0	0.0
1	1	122.1	122.4	0.0	-1.9	-1.9	100.0	100.0	0.0
1	1	123.0	123.3	0.0	-3.3	-3.3	100.0	100.0	0.0
1	1	124.7	125.0	-22.3	-31.8	-9.5	100.0	99.2	-0.8
1	1	125.6	125.9	-35.9	-39.4	-3.5	100.0	98.9	-1.1
1	1	126.5	126.8	-49.5	-53.8	-4.3	100.0	96.8	-3.2
1	1	127.3	127.6	-56.3	-57.9	-1.6	91.3	90.8	-0.4
1	1	128.2	128.4	-49.3	-51.6	-2.4	75.3	79.5	4.2
1	1	129.1	129.3	-39.9	-42.1	-2.2	57.3	64.4	7.1
1	1	130.8	131.0	-20.5	-21.7	-1.2	21.2	33.2	12.0
1	1	131.6	131.8	-15.2	-16.8	-1.6	3.1	24.5	21.4
1	1	132.5	132.6	-6.7	-7.9	-1.2	0.0	10.8	10.8
1	1	131.6	131.7	-11.7	-12.2	-0.5	6.3	18.9	12.6
1	1	130.8	130.9	-14.4	-15.8	-1.4	22.9	23.2	0.3
1	1	129.9	130.1	-22.7	-24.5	-1.7	39.6	36.7	-2.9
1	1	129.1	129.3	-30.4	-32.1	-1.7	57.3	49.1	-8.2
1	1	128.2	128.4	-38.8	-42.1	-3.4	75.3	62.5	-12.8
1	1	127.3	127.5	-47.6	-45.1	2.5	93.4	76.8	-16.5
1	1	126.5	126.8	-49.5	-55.7	-6.2	100.0	91.6	-8.4
1	1	125.6	125.9	-35.9	-48.1	-12.2	100.0	97.0	-3.0
1	1	124.7	125.0	-22.3	-39.4	-17.1	100.0	99.2	-0.8
1	1	123.9	124.2	-8.7	-25.8	-17.1	100.0	99.7	-0.3
1	1	123.0	123.3	0.0	-12.2	-12.2	100.0	100.0	0.0
1	1	122.1	122.4	0.0	-3.8	-3.8	100.0	100.0	0.0
1	1	120.0	120.3	0.0	-1.4	-1.4	100.0	100.0	0.0
1	2	120.0	120.3	0.0	-1.4	-1.4	100.0	100.0	0.0
1	2	122.1	122.4	0.0	-1.4	-1.4	100.0	100.0	0.0
1	2	123.0	123.3	0.0	-1.9	-1.9	100.0	100.0	0.0
1	2	124.7	125.0	-6.7	-10.9	-4.2	100.0	100.0	0.0
1	2	125.6	125.9	-10.8	-12.0	-1.2	100.0	99.7	-0.3
1	2	126.5	126.8	-14.9	-18.5	-3.6	100.0	97.3	-2.7
1	2	127.3	127.6	-19.0	-21.7	-2.8	91.3	91.4	0.1
1	2	128.2	128.4	-22.6	-23.6	-1.1	75.3	76.8	1.5
1	2	129.1	129.3	-26.7	-25.8	0.8	57.3	67.4	10.1
1	2	130.8	131.0	-19.0	-14.9	4.1	21.2	30.7	9.5
1	2	131.6	131.8	-15.4	-13.6	1.8	3.1	24.8	21.7

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Reactive Power Error (% Rated)	Expected Real Power (%)	Measured Real Power (%)	Real Power Error (% Rated)
1	2	132.5	132.6	-5.7	-6.8	-1.1	0.0	9.2	9.2
1	2	131.6	131.8	-12.0	-13.0	-1.0	4.2	19.4	15.2
1	2	130.8	131.0	-16.7	-17.9	-1.2	20.8	27.0	6.1
1	2	129.9	130.1	-25.9	-27.2	-1.3	39.6	41.8	2.2
1	2	129.1	129.3	-26.9	-27.2	-0.3	56.2	55.3	-1.0
1	2	128.2	128.5	-23.0	-26.4	-3.3	73.2	69.3	-4.0
1	2	127.3	127.6	-19.0	-22.3	-3.3	91.3	83.6	-7.7
1	2	126.5	126.8	-14.9	-19.3	-4.4	100.0	93.0	-7.0
1	2	125.6	125.9	-10.8	-16.3	-5.5	100.0	99.2	-0.8
1	2	124.7	125.0	-6.7	-13.6	-6.9	100.0	100.0	0.0
1	2	123.9	124.2	-2.6	-9.5	-6.9	100.0	100.0	0.0
1	2	123.0	123.3	0.0	-5.4	-5.4	100.0	100.0	0.0
1	2	122.1	122.4	0.0	-2.2	-2.2	100.0	100.0	0.0
1	2	120.0	120.3	0.0	-1.4	-1.4	100.0	100.0	0.0
4	1	277.1	278.6	0.0	-2.0	-2.0	100.0	100.5	0.5
4	1	282.0	283.5	0.0	-2.1	-2.1	100.0	100.5	0.5
4	1	284.0	285.4	0.0	-2.2	-2.2	100.0	100.0	0.0
4	1	286.0	287.1	-5.3	-6.4	-1.1	100.0	100.0	0.0
4	1	288.0	288.9	-11.0	-10.5	0.5	100.0	100.0	0.0
4	1	290.0	290.5	-16.0	-16.3	-0.2	100.0	100.0	0.0
4	1	292.0	292.1	-21.1	-22.9	-1.8	100.0	100.0	0.0
4	1	294.0	293.8	-26.3	-27.2	-0.8	99.6	100.0	0.4
4	1	296.0	295.5	-26.3	-27.6	-1.3	84.3	89.6	5.3
4	1	298.0	297.0	-26.3	-27.2	-0.8	70.7	72.6	1.9
4	1	300.0	299.6	-26.3	-26.8	-0.5	47.3	49.8	2.5
4	1	302.0	301.3	-26.3	-26.6	-0.3	31.9	34.4	2.4
4	1	304.0	302.9	-26.3	-26.5	-0.1	17.5	21.0	3.5
4	1	306.0	304.7	-26.3	-26.7	-0.3	1.3	5.4	4.1
4	1	304.0	303.0	-26.3	-26.5	-0.2	16.6	23.7	7.1
4	1	302.0	301.3	-26.3	-26.8	-0.4	31.9	39.4	7.5
4	1	300.0	299.7	-26.3	-26.9	-0.6	46.4	52.2	5.9
4	1	298.0	298.0	-26.3	-27.1	-0.8	61.7	66.2	4.5
4	1	296.0	295.4	-26.3	-27.1	-0.8	85.2	84.6	-0.6
4	1	294.0	293.8	-26.3	-27.0	-0.6	99.6	100.0	0.4
4	1	292.0	292.2	-21.4	-21.1	0.3	100.0	100.0	0.0
4	1	290.0	290.5	-16.0	-15.7	0.4	100.0	100.0	0.0
4	1	288.0	288.9	-11.0	-10.2	0.8	100.0	100.0	0.0
4	1	286.0	287.1	-5.3	-6.7	-1.4	100.0	100.0	0.0
4	1	284.0	285.4	0.0	-2.3	-2.3	100.0	100.5	0.5

Test Inverter	Test Case	Commanded Voltage (V)	Measured Voltage (V)	Expected Reactive Power (%)	Measured Reactive Power (%)	Reactive Power Error (% Rated)	Expected Real Power (%)	Measured Real Power (%)	Real Power Error (% Rated)
4	1	282.0	283.5	0.0	-2.2	-2.2	100.0	100.0	0.0
4	1	277.1	278.6	0.0	-2.2	-2.2	100.0	100.0	0.0
4	2	277.1	278.5	0.0	-2.1	-2.1	100.0	100.0	0.0
4	2	282.0	283.4	0.0	-2.1	-2.1	100.0	100.0	0.0
4	2	284.0	285.4	0.0	-2.1	-2.1	100.0	100.0	0.0
4	2	286.0	287.3	-1.8	-2.9	-1.1	100.0	100.0	0.0
4	2	288.0	289.1	-3.5	-4.3	-0.8	100.0	100.0	0.0
4	2	290.0	291.0	-5.3	-6.1	-0.8	100.0	100.0	0.0
4	2	292.0	292.2	-6.4	-7.9	-1.5	100.0	100.0	0.0
4	2	294.0	294.6	-8.7	-9.5	-0.8	92.4	93.5	1.1
4	2	296.0	296.2	-10.2	-11.0	-0.8	78.0	81.1	3.1
4	2	298.0	298.3	-12.2	-12.7	-0.5	59.0	61.2	2.2
4	2	300.0	299.9	-13.2	-14.0	-0.8	44.6	48.5	3.9
4	2	302.0	301.6	-13.2	-13.8	-0.6	29.2	34.0	4.8
4	2	304.0	303.2	-13.2	-13.6	-0.4	14.8	18.7	3.9
4	2	306.0	305.0	-13.2	-13.1	0.1	0.0	3.8	3.8
4	2	304.0	303.3	-13.2	-13.6	-0.4	13.9	18.6	4.7
4	2	302.0	301.6	-13.2	-13.7	-0.5	29.2	32.4	3.2
4	2	300.0	299.9	-13.2	-13.8	-0.6	44.6	45.4	0.9
4	2	298.0	298.4	-12.3	-12.7	-0.3	58.1	63.2	5.1
4	2	296.0	296.2	-10.2	-11.0	-0.8	78.0	81.1	3.1
4	2	294.0	294.6	-8.7	-9.3	-0.5	92.4	95.0	2.6
4	2	292.0	292.9	-7.1	-8.2	-1.1	100.0	100.0	0.0
4	2	290.0	291.0	-5.3	-6.0	-0.7	100.0	100.0	0.0
4	2	288.0	289.1	-3.5	-4.2	-0.7	100.0	100.0	0.0
4	2	286.0	287.3	-1.8	-3.0	-1.2	100.0	100.0	0.0
4	2	284.0	285.4	0.0	-2.1	-2.1	100.0	100.0	0.0
4	2	282.0	283.4	0.0	-2.1	-2.1	100.0	100.0	0.0
4	2	277.1	278.6	0.0	-2.1	-2.1	100.0	100.0	0.0

Appendix D – Real-Time Model Input Parameters

Primary – Secondary Transformer Impedance (M34): R = 0.0076 pu, L = 0.08 pu, 25 kVA, Rm = Lm = 500 pu

Primary – Secondary Transformer Impedance (K3L): R = 0.0067 pu, L = 0.0135/377 pu, 30 kVA, Rm = Lm = 500 pu

Three phase transformer (M34): R = 0.0074 pu, L = 0.0186 pu, 150 kVA, Rm = Lm = 500 pu

Three phase line impedance (K3L): R = 0.0168 pu, L = 0.000058 pu

Three phase transformer (K3L): R = 0.011 pu, L = 0.028 pu, 150 kVA, Rm = Lm = 500 pu

Three phase line impedance (K3L): R = 0.0504 pu, L = 0.00018 pu

Appendix E – Modeled Aggregate PV Inverter Ratings for PHIL Tests

All tables show PV ratings at nodes 0-7 in the feeder model, listed sequentially in each row.

PV Ratings used for VWC with FPF Tests

Inverter Ratings (kW), M34 Present (2016), No retrofit			
Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
0	0	0	0
59.8	963.0	0	0
478.3	219.0	0	0
134.9	479.6	0	0
129.7	11.1	0	0
0.0	0.0	0	0
555.6	833.5	0	0
26.9	0.0	0	0

Inverter Ratings (kW), M34 Future (2021), No retrofit			
Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
0.0	0.0	0.0	0.0
59.8	963.0	85.9	618.3
478.3	219.0	1037.5	1899.4
134.9	479.6	409.2	2459.1
129.7	11.1	263.5	1026.2
0.0	0.0	0.0	0.0
555.6	833.5	1479.0	1869.1
26.9	0.0	29.2	0.0

Inverter Ratings (kW), M34 Present (2016), 25% retrofit			
Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
0.0	0.0	0.0	0.0
44.8	722.3	14.9	240.8
358.7	164.2	119.6	54.7
101.2	359.7	33.7	119.9
97.3	8.3	32.4	2.8
0.0	0.0	0.0	0.0
416.7	625.1	138.9	208.4
20.2	0.0	6.7	0.0

Inverter Ratings (kW), M34 Future (2021), 25% retrofit			
Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
0.0	0.0	0.0	0.0
44.8	722.3	100.8	859.1
358.7	164.2	1157.0	1954.1
101.2	359.7	442.9	2579.0
97.3	8.3	295.9	1029.0
0.0	0.0	0.0	0.0
416.7	625.1	1617.9	2077.5
20.2	0.0	35.9	0.0

Inverter Ratings (kW), M34 Present (2016), 50% retrofit			
Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
0.0	0.0	0.0	0.0
29.9	481.5	29.9	481.5
239.1	109.5	239.1	109.5
67.5	239.8	67.5	239.8
64.9	5.5	64.9	5.5
0.0	0.0	0.0	0.0
277.8	416.7	277.8	416.7
13.4	0.0	13.4	0.0

Inverter Ratings (kW), M34 Future (2021), 50% retrofit			
Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
0.0	0.0	0.0	0.0
29.9	481.5	115.8	1099.8
239.1	109.5	1276.6	2008.9
67.5	239.8	476.6	2698.9
64.9	5.5	328.3	1031.7
0.0	0.0	0.0	0.0
277.8	416.7	1756.8	2285.8
13.4	0.0	42.6	0.0

Inverter Ratings (kW), K3L Present (2016), No retrofit			
Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
268.2	97.4	0	0
124.0	98.6	0	0
224.0	155.0	0	0
30.8	33.2	0	0
563.8	713.8	0	0
131.8	121.7	0	0
11.8	0.0	0	0
285.2	173.7	0	0

Inverter Ratings (kW), K3L Future (2021), No retrofit			
Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
268.2	97.4	133.5	48.5
124.0	98.6	58.9	46.8
224.0	155.0	106.3	73.6
30.8	33.2	14.6	319.7
563.8	713.8	282.1	329.3
131.8	121.7	62.5	57.8
11.8	0.0	5.6	0.0
285.2	173.7	142.0	86.5

Inverter Ratings (kW), K3L Present (2016), 25% retrofit			
Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
201.1	73.0	67.0	24.3
93.0	74.0	31.0	24.7
168.0	116.3	56.0	38.8
23.1	24.9	7.7	8.3
422.9	535.4	141.0	178.5
98.8	91.3	32.9	30.4
8.8	0.0	2.9	0.0
213.9	130.3	71.3	43.4

Inverter Ratings (kW), K3L Future (2021), 25% retrofit			
Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
201.1	73.0	200.6	72.8
93.0	74.0	89.8	71.5
168.0	116.3	162.3	112.3
23.1	24.9	22.3	328.0
422.9	535.4	423.1	507.8
98.8	91.3	95.5	88.2
8.8	0.0	8.5	0.0
213.9	130.3	213.3	129.9

Inverter Ratings (kW), K3L Present (2016), 50% retrofit			
Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
134.1	48.7	134.1	48.7
62.0	49.3	62.0	49.3
112.0	77.5	112.0	77.5
15.4	16.6	15.4	16.6
281.9	356.9	281.9	356.9
65.9	60.9	65.9	60.9
5.9	0.0	5.9	0.0
142.6	86.9	142.6	86.9

Inverter Ratings (kW), K3L Future (2021), 50% retrofit			
Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
134.1	48.7	267.6	97.2
62.0	49.3	120.8	96.1
112.0	77.5	218.3	151.1
15.4	16.6	30.0	336.3
281.9	356.9	564.1	686.2
65.9	60.9	128.4	118.6
5.9	0.0	11.5	0.0
142.6	86.9	284.6	173.4

PV Ratings used for VRT, FRT, Ramp Rate and Soft Start Tests

Inverter Ratings (kW), M34, 2016, No retrofit			
Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
0.0	0.0	0.0	0.0
14.6	22.1	45.2	940.9
419.9	69.6	58.4	149.4
74.2	49.8	60.7	429.9
89.1	6.0	40.6	5.0
0.0	0.0	0.0	0.0
425.1	188.9	130.5	644.6
19.8	0.0	7.1	0.0

Inverter Ratings (kW), K3L, 2016, No retrofit			
Legacy Enphase	Legacy Other	Advanced Enphase	Advanced Other
201.3	46.0	66.9	51.4
111.8	48.1	12.2	50.6
206.0	111.7	17.9	43.4
17.4	24.1	13.4	9.1
468.7	635.5	95.2	78.3
128.8	114.0	3.0	7.7
11.8	0.0	0.0	0.0
150.9	139.0	134.3	34.7

Appendix F – VWC with FPF Test Result Summary

Test Inverter	Test Case	V-W Curve	Power Factor	Feeder	Mode	Retrofit (%)	Present/ Future	Start Voltage 1 (pu)	End Voltage 1 (pu)	End Power 1 (pu)	Start Voltage 2 (pu)	End Voltage 2 (pu)	End Power 2 (pu)
1	1	none	1.00	K3L	snapshot	0	future	1.035	1.082	1.05	1.035	1.082	1.05
1	2	moderate	1.00	K3L	snapshot	0	future	1.035	1.072	0.38	1.035	1.072	0.38
1	3	aggressive	1.00	K3L	snapshot	0	future	1.035	1.067	0.01	1.035	1.067	0.01
1	4	none	0.98	K3L	snapshot	0	future	1.034	1.079	1.04	1.034	1.079	1.04
1	5	moderate	0.98	K3L	snapshot	0	future	1.034	1.070	0.41	1.034	1.070	0.41
1	6	aggressive	0.98	K3L	snapshot	0	future	1.034	1.065	0.03	1.034	1.065	0.03
1	7	none	0.95	K3L	snapshot	0	future	1.034	1.077	1.04	1.034	1.077	1.04
1	8	moderate	0.95	K3L	snapshot	0	future	1.034	1.069	0.43	1.034	1.069	0.43
1	9	aggressive	0.95	K3L	snapshot	0	future	1.034	1.064	0.05	1.034	1.064	0.05
1	10	none	0.90	K3L	snapshot	0	future	1.033	1.074	1.03	1.033	1.074	1.03
1	11	moderate	0.90	K3L	snapshot	0	future	1.033	1.068	0.46	1.033	1.068	0.46
1	12	aggressive	0.90	K3L	snapshot	0	future	1.033	1.063	0.07	1.033	1.063	0.07
1	13	moderate	1.00	K3L	nameplate	0	future	1.035	1.076	0.64	1.035	1.076	0.64
1	14	aggressive	1.00	K3L	nameplate	0	future	1.035	1.067	0.02	1.035	1.067	0.02
1	15	moderate	0.98	K3L	nameplate	0	future	1.034	1.074	0.70	1.034	1.074	0.70
1	16	aggressive	0.98	K3L	nameplate	0	future	1.034	1.065	0.05	1.034	1.065	0.05
1	17	moderate	0.95	K3L	nameplate	0	future	1.034	1.073	0.74	1.034	1.073	0.74
1	18	aggressive	0.95	K3L	nameplate	0	future	1.034	1.065	0.09	1.034	1.065	0.09
1	19	moderate	0.90	K3L	nameplate	0	future	1.033	1.071	0.77	1.033	1.071	0.77
1	20	aggressive	0.90	K3L	nameplate	0	future	1.033	1.064	0.13	1.033	1.064	0.13
1	21	none	1.00	M34	snapshot	0	future	1.028	1.073	1.05	1.028	1.073	1.05
1	22	moderate	1.00	M34	snapshot	0	future	1.028	1.071	0.59	1.028	1.071	0.59
1	23	aggressive	1.00	M34	snapshot	0	future	1.028	1.065	0.07	1.028	1.065	0.07
1	24	none	0.98	M34	snapshot	0	future	1.022	1.044	1.04	1.022	1.044	1.04
1	25	moderate	0.98	M34	snapshot	0	future	1.022	1.043	1.04	1.022	1.043	1.04
1	26	aggressive	0.98	M34	snapshot	0	future	1.022	1.045	0.96	1.022	1.045	0.96
1	27	none	0.95	M34	snapshot	0	future	1.018	1.026	1.03	1.018	1.026	1.03
1	28	moderate	0.95	M34	snapshot	0	future	1.018	1.026	1.03	1.018	1.026	1.03
1	29	aggressive	0.95	M34	snapshot	0	future	1.018	1.026	1.03	1.018	1.026	1.03
1	30	none	0.90	M34	snapshot	0	future	1.014	1.003	1.03	1.014	1.003	1.03
1	31	moderate	0.90	M34	snapshot	0	future	1.013	1.002	1.02	1.013	1.002	1.02
1	32	aggressive	0.90	M34	snapshot	0	future	1.013	1.002	1.02	1.013	1.002	1.02
1	33	moderate	1.00	M34	nameplate	0	future	1.027	1.071	0.81	1.027	1.071	0.81
1	34	aggressive	1.00	M34	nameplate	0	future	1.026	1.064	0.15	1.026	1.064	0.15
1	35	moderate	0.98	M34	nameplate	0	future	1.021	1.042	1.04	1.021	1.042	1.04
1	36	aggressive	0.98	M34	nameplate	0	future	1.023	1.046	0.88	1.023	1.046	0.88
1	37	moderate	0.95	M34	nameplate	0	future	1.017	1.025	1.03	1.017	1.025	1.03
1	38	aggressive	0.95	M34	nameplate	0	future	1.019	1.026	1.03	1.019	1.026	1.03
1	39	moderate	0.90	M34	nameplate	0	future	1.012	1.001	1.02	1.012	1.001	1.02
1	40	aggressive	0.90	M34	nameplate	0	future	1.014	1.003	1.02	1.014	1.003	1.02
2, 3	1	none	1.00	K3L	nameplate	0	present	1.039	1.089	0.99	1.039	1.086	1.00
2, 3	2	none	1.00	K3L	nameplate	25	present	1.039	1.088	0.99	1.039	1.086	1.00
2, 3	3	none	1.00	K3L	nameplate	50	present	1.038	1.087	0.99	1.038	1.086	1.00
2, 3	4	none	1.00	K3L	nameplate	0	future	1.039	1.089	0.99	1.038	1.086	1.00

Test Inverter	Test Case	V-W Curve	Power Factor	Feeder	Mode	Retrofit (%)	Present/ Future	Start Voltage 1 (pu)	End Voltage 1 (pu)	End Power 1 (pu)	Start Voltage 2 (pu)	End Voltage 2 (pu)	End Power 2 (pu)
2, 3	5	none	1.00	K3L	nameplate	25	future	1.039	1.089	0.99	1.039	1.087	1.00
2, 3	6	none	1.00	K3L	nameplate	50	future	1.039	1.089	0.99	1.039	1.087	1.00
2, 3	7	none	0.95	K3L	nameplate	0	present	1.037	1.077	0.94	1.037	1.077	0.96
2, 3	8	none	0.95	K3L	nameplate	25	present	1.037	1.076	0.94	1.037	1.076	0.96
2, 3	9	none	0.95	K3L	nameplate	50	present	1.036	1.074	0.94	1.037	1.075	0.96
2, 3	10	none	0.95	K3L	nameplate	0	future	1.037	1.075	0.94	1.037	1.076	0.96
2, 3	11	none	0.95	K3L	nameplate	25	future	1.036	1.074	0.94	1.036	1.074	0.96
2, 3	12	none	0.95	K3L	nameplate	50	future	1.036	1.072	0.94	1.036	1.073	0.96
2, 3	13	none	0.90	K3L	nameplate	0	present	1.036	1.071	0.89	1.036	1.073	0.91
2, 3	14	none	0.90	K3L	nameplate	25	present	1.036	1.069	0.89	1.036	1.071	0.91
2, 3	15	none	0.90	K3L	nameplate	50	present	1.035	1.067	0.89	1.036	1.070	0.91
2, 3	16	none	0.90	K3L	nameplate	0	future	1.035	1.068	0.89	1.036	1.070	0.91
2, 3	17	none	0.90	K3L	nameplate	25	future	1.035	1.066	0.89	1.035	1.068	0.91
2, 3	18	none	0.90	K3L	nameplate	50	future	1.035	1.064	0.89	1.035	1.066	0.91
2, 3	19	moderate	1.00	K3L	nameplate	0	present	1.039	1.075	0.56	1.038	1.074	0.66
2, 3	20	moderate	1.00	K3L	nameplate	25	present	1.039	1.074	0.56	1.038	1.074	0.66
2, 3	21	moderate	1.00	K3L	nameplate	50	present	1.039	1.074	0.56	1.038	1.074	0.66
2, 3	22	moderate	1.00	K3L	nameplate	0	future	1.039	1.075	0.55	1.039	1.074	0.65
2, 3	23	moderate	1.00	K3L	nameplate	25	future	1.039	1.075	0.55	1.039	1.074	0.65
2, 3	24	moderate	1.00	K3L	nameplate	50	future	1.039	1.075	0.55	1.039	1.074	0.65
2, 3	25	moderate	0.95	K3L	nameplate	0	present	1.037	1.070	0.68	1.037	1.071	0.75
2, 3	26	moderate	0.95	K3L	nameplate	25	present	1.037	1.069	0.70	1.037	1.070	0.76
2, 3	27	moderate	0.95	K3L	nameplate	50	present	1.036	1.068	0.71	1.037	1.069	0.78
2, 3	28	moderate	0.95	K3L	nameplate	0	future	1.036	1.069	0.71	1.037	1.069	0.78
2, 3	29	moderate	0.95	K3L	nameplate	25	future	1.036	1.068	0.73	1.036	1.068	0.79
2, 3	30	moderate	0.95	K3L	nameplate	50	future	1.036	1.067	0.74	1.036	1.068	0.81
2, 3	31	moderate	0.90	K3L	nameplate	0	present	1.036	1.068	0.74	1.037	1.069	0.78
2, 3	32	moderate	0.90	K3L	nameplate	25	present	1.036	1.067	0.77	1.036	1.068	0.81
2, 3	33	moderate	0.90	K3L	nameplate	50	present	1.035	1.065	0.79	1.036	1.067	0.83
2, 3	34	moderate	0.90	K3L	nameplate	0	future	1.035	1.066	0.79	1.036	1.067	0.83
2, 3	35	moderate	0.90	K3L	nameplate	25	future	1.035	1.064	0.81	1.035	1.066	0.85
2, 3	36	moderate	0.90	K3L	nameplate	50	future	1.035	1.063	0.84	1.035	1.065	0.88
2, 3	37	mild	1.00	K3L	nameplate	0	present	1.039	1.079	0.71	1.038	1.077	0.79
2, 3	38	mild	1.00	K3L	nameplate	25	present	1.039	1.079	0.71	1.038	1.077	0.79
2, 3	39	mild	1.00	K3L	nameplate	50	present	1.039	1.079	0.71	1.038	1.077	0.79
2, 3	40	mild	1.00	K3L	nameplate	0	future	1.039	1.079	0.70	1.038	1.078	0.78
2, 3	41	mild	1.00	K3L	nameplate	25	future	1.039	1.079	0.70	1.039	1.078	0.78
2, 3	42	mild	1.00	K3L	nameplate	50	future	1.039	1.079	0.70	1.039	1.078	0.78
2, 3	43	mild	0.95	K3L	nameplate	0	present	1.038	1.074	0.79	1.038	1.074	0.82
2, 3	44	mild	0.95	K3L	nameplate	25	present	1.037	1.072	0.80	1.037	1.073	0.84
2, 3	45	mild	0.95	K3L	nameplate	50	present	1.037	1.071	0.81	1.037	1.072	0.85
2, 3	46	mild	0.95	K3L	nameplate	0	future	1.037	1.071	0.81	1.037	1.072	0.85
2, 3	47	mild	0.95	K3L	nameplate	25	future	1.035	1.070	0.83	1.037	1.071	0.86
2, 3	48	mild	0.95	K3L	nameplate	50	future	1.035	1.069	0.84	1.036	1.070	0.87
2, 3	49	mild	0.90	K3L	nameplate	0	present	1.035	1.069	0.84	1.037	1.072	0.86
2, 3	50	mild	0.90	K3L	nameplate	25	present	1.035	1.068	0.86	1.036	1.071	0.88
2, 3	51	mild	0.90	K3L	nameplate	50	present	1.034	1.066	0.87	1.036	1.069	0.89
2, 3	52	mild	0.90	K3L	nameplate	0	future	1.035	1.067	0.86	1.036	1.070	0.89

Test Inverter	Test Case	V-W Curve	Power Factor	Feeder	Mode	Retrofit (%)	Present/ Future	Start Voltage 1 (pu)	End Voltage 1 (pu)	End Power 1 (pu)	Start Voltage 2 (pu)	End Voltage 2 (pu)	End Power 2 (pu)
2, 3	53	mild	0.90	K3L	nameplate	25	future	1.035	1.066	0.87	1.036	1.068	0.91
2, 3	54	mild	0.90	K3L	nameplate	50	future	1.035	1.065	0.88	1.035	1.066	0.91
2, 3	55	none	1.00	M34	nameplate	0	present	1.043	1.065	0.99	1.043	1.070	1.00
2, 3	56	none	1.00	M34	nameplate	25	present	1.043	1.064	0.94	1.043	1.070	1.00
2, 3	57	none	1.00	M34	nameplate	50	present	1.043	1.064	0.99	1.043	1.070	1.00
2, 3	58	none	1.00	M34	nameplate	0	future	1.047	1.081	0.99	1.047	1.087	1.00
2, 3	59	none	1.00	M34	nameplate	25	future	1.047	1.081	0.99	1.047	1.086	1.00
2, 3	60	none	1.00	M34	nameplate	50	future	1.047	1.081	0.99	1.047	1.086	1.00
2, 3	61	none	0.95	M34	nameplate	0	present	1.038	1.035	0.94	1.037	1.041	0.95
2, 3	62	none	0.95	M34	nameplate	25	present	1.036	1.031	0.94	1.036	1.038	0.95
2, 3	63	none	0.95	M34	nameplate	50	present	1.035	1.028	0.94	1.036	1.034	0.95
2, 3	64	none	0.95	M34	nameplate	0	future	1.036	1.023	0.94	1.036	1.029	0.95
2, 3	65	none	0.95	M34	nameplate	25	future	1.036	1.020	0.94	1.036	1.026	0.95
2, 3	66	none	0.95	M34	nameplate	50	future	1.035	1.017	0.94	1.035	1.023	0.95
2, 3	67	none	0.90	M34	nameplate	0	present	1.035	1.023	0.89	1.034	1.028	0.90
2, 3	68	none	0.90	M34	nameplate	25	present	1.034	1.018	0.89	1.033	1.024	0.90
2, 3	69	none	0.90	M34	nameplate	50	present	1.034	1.014	0.89	1.033	1.020	0.90
2, 3	70	none	0.90	M34	nameplate	0	future	1.032	0.999	0.89	1.031	1.005	0.90
2, 3	71	none	0.90	M34	nameplate	25	future	1.031	0.994	0.88	1.031	1.000	0.90
2, 3	72	none	0.90	M34	nameplate	50	future	1.030	0.989	0.88	1.029	0.996	0.90
2, 3	73	moderate	1.00	M34	nameplate	0	present	1.044	1.067	0.72	1.043	1.070	0.75
2, 3	74	moderate	1.00	M34	nameplate	25	present	1.044	1.067	0.72	1.043	1.070	0.75
2, 3	75	moderate	1.00	M34	nameplate	50	present	1.044	1.067	0.72	1.043	1.070	0.75
2, 3	76	moderate	1.00	M34	nameplate	0	future	1.048	1.086	0.31	1.047	1.089	0.37
2, 3	77	moderate	1.00	M34	nameplate	25	future	1.048	1.087	0.29	1.046	1.089	0.34
2, 3	78	moderate	1.00	M34	nameplate	50	future	1.048	1.087	0.29	1.047	1.089	0.34
2, 3	79	moderate	0.95	M34	nameplate	0	present	1.037	1.034	0.94	1.038	1.042	0.95
2, 3	80	moderate	0.95	M34	nameplate	25	present	1.035	1.030	0.94	1.037	1.038	0.95
2, 3	81	moderate	0.95	M34	nameplate	50	present	1.035	1.028	0.94	1.037	1.035	0.95
2, 3	82	moderate	0.95	M34	nameplate	0	future	1.036	1.023	0.94	1.037	1.030	0.95
2, 3	83	moderate	0.95	M34	nameplate	25	future	1.036	1.020	0.94	1.036	1.027	0.95
2, 3	84	moderate	0.95	M34	nameplate	50	future	1.035	1.017	0.94	1.036	1.024	0.95
2, 3	85	moderate	0.90	M34	nameplate	0	present	1.035	1.022	0.89	1.035	1.029	0.90
2, 3	86	moderate	0.90	M34	nameplate	25	present	1.034	1.018	0.89	1.034	1.025	0.90
2, 3	87	moderate	0.90	M34	nameplate	50	present	1.033	1.013	0.89	1.033	1.020	0.90
2, 3	88	moderate	0.90	M34	nameplate	0	future	1.032	0.999	0.89	1.032	1.006	0.90
2, 3	89	moderate	0.90	M34	nameplate	25	future	1.031	0.994	0.89	1.032	1.001	0.90
2, 3	90	moderate	0.90	M34	nameplate	50	future	1.030	0.989	0.88	1.031	0.997	0.90
2, 3	91	mild	1.00	M34	nameplate	0	present	1.044	1.066	0.86	1.043	1.070	0.86
2, 3	92	mild	1.00	M34	nameplate	25	present	1.044	1.068	0.84	1.043	1.070	0.87
2, 3	93	mild	1.00	M34	nameplate	50	present	1.045	1.068	0.84	1.043	1.070	0.87
2, 3	94	mild	1.00	M34	nameplate	0	future	1.049	1.087	0.62	1.047	1.089	0.65
2, 3	95	mild	1.00	M34	nameplate	25	future	1.049	1.087	0.62	1.047	1.089	0.66
2, 3	96	mild	1.00	M34	nameplate	50	future	1.049	1.087	0.62	1.047	1.089	0.66
2, 3	97	mild	0.95	M34	nameplate	0	present	1.040	1.037	0.94	1.037	1.041	0.95
2, 3	98	mild	0.95	M34	nameplate	25	present	1.039	1.034	0.94	1.037	1.038	0.95
2, 3	99	mild	0.95	M34	nameplate	50	present	1.038	1.030	0.94	1.036	1.035	0.95
2, 3	100	mild	0.95	M34	nameplate	0	future	1.039	1.026	0.89	1.037	1.030	0.95

Test Inverter	Test Case	V-W Curve	Power Factor	Feeder	Mode	Retrofit (%)	Present/ Future	Start Voltage 1 (pu)	End Voltage 1 (pu)	End Power 1 (pu)	Start Voltage 2 (pu)	End Voltage 2 (pu)	End Power 2 (pu)
2, 3	101	mild	0.95	M34	nameplate	25	future	1.038	1.022	0.94	1.036	1.026	0.95
2, 3	102	mild	0.95	M34	nameplate	50	future	1.038	1.019	0.94	1.035	1.023	0.95
2, 3	103	mild	0.90	M34	nameplate	0	present	1.037	1.024	0.89	1.035	1.029	0.90
2, 3	104	mild	0.90	M34	nameplate	25	present	1.036	1.020	0.89	1.034	1.025	0.90
2, 3	105	mild	0.90	M34	nameplate	50	present	1.035	1.016	0.89	1.033	1.020	0.90
2, 3	106	mild	0.90	M34	nameplate	0	future	1.034	1.000	0.88	1.032	1.006	0.90
2, 3	107	mild	0.90	M34	nameplate	25	future	1.030	0.993	0.88	1.032	1.002	0.90
2, 3	108	mild	0.90	M34	nameplate	50	future	1.029	0.988	0.88	1.031	0.997	0.90
4	1	none	1.00	K3L	nameplate	0	future	1.051	1.058	1.00			
4	2	moderate	1.00	K3L	nameplate	0	future	1.051	1.058	1.01			
4	3	aggressive	1.00	K3L	nameplate	0	future	1.051	1.055	0.52			
4	4	mild	1.00	K3L	nameplate	0	future	1.051	1.058	1.00			
4	5	none	0.95	K3L	nameplate	0	future	1.049	1.048	0.98			
4	6	moderate	0.95	K3L	nameplate	0	future	1.049	1.048	0.98			
4	7	aggressive	0.95	K3L	nameplate	0	future	1.049	1.048	0.98			
4	8	mild	0.95	K3L	nameplate	0	future	1.049	1.048	0.98			
4	9	none	0.90	K3L	nameplate	0	future	1.048	1.043	0.92			
4	10	moderate	0.90	K3L	nameplate	0	future	1.048	1.043	0.92			
4	11	aggressive	0.90	K3L	nameplate	0	future	1.048	1.043	0.92			
4	12	mild	0.90	K3L	nameplate	0	future	1.048	1.043	0.92			
4	13	none	1.00	M34	nameplate	0	future	1.064	1.094	0.77			
4	14	moderate	1.00	M34	nameplate	0	future	1.064	1.095	0.66			
4	15	aggressive	1.00	M34	nameplate	0	future	1.064	1.077	0.23			
4	16	mild	1.00	M34	nameplate	0	future	1.064	1.093	0.77			
4	17	none	0.95	M34	nameplate	0	future	1.053	1.054	0.74			
4	18	moderate	0.95	M34	nameplate	0	future	1.053	1.054	0.74			
4	19	aggressive	0.95	M34	nameplate	0	future	1.053	1.054	0.74			
4	20	mild	0.95	M34	nameplate	0	future	1.053	1.054	0.74			
4	21	none	0.90	M34	nameplate	0	future	1.048	1.035	0.72			
4	22	moderate	0.90	M34	nameplate	0	future	1.048	1.035	0.72			
4	23	aggressive	0.90	M34	nameplate	0	future	1.048	1.034	0.72			
4	24	mild	0.90	M34	nameplate	0	future	1.048	1.034	0.72			