In-Situ Measurement of Power Loss for Crystalline Silicon Modules Undergoing Thermal Cycling and Mechanical Loading Stress Testing

Preprint

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Presented at the Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes
Keystone, Colorado
July 26–29, 2015

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Conference Paper
NREL/CP-5J00-64684
September 2015

Contract No. DE-AC36-08GO28308

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***Abstract* — We analyze the degradation of multi-crystalline silicon photovoltaic modules undergoing simultaneous thermal, mechanical, and humidity-freeze stress testing to develop a dark environmental chamber in-situ measurement procedure for determining module power loss. We analyze dark I-V curves measured on modules undergoing degradation in three steps; first for shunting and recombination losses; second, series resistance and lifetime losses; and finally, other losses including short circuit current, current mismatch losses associated with a decrease in photo-current generation by removal of some cell areas due to cell fractures, and the additional series resistance losses observed under illumination. Based on the analysis, we propose an in-situ module power loss monitoring procedure that relies on dark current-voltage measurements taken during the stress test and initial and final module flash testing to determine the power degradation characteristic of the module.**

I. Introduction

Measurement of power degradation of photovoltaic (PV) modules for accelerated testing generally involves intermittently removing the module from the environmental chamber and flash testing with a solar simulator, which is a time-consuming and costly process when numerous samples are involved. However, application of statistical methods to accelerated lifetime studies of PV modules will benefit from an increased number of samples tested. Moreover, continuous monitoring of module power loss will more accurately clarify the degradation characteristic of the PV modules, and enable the application of reliability analyses and modeling. Methods are therefore sought to characterize the state of degradation of the module in-situ during environmental chamber stress testing.

In-situ characterization of crystalline silicon (c-Si) PV modules undergoing potential-induced degradation (PID) was achieved using superposition for translating in-situ-acquired dark current-voltage (I-V) curves from the first to the fourth quadrant by the module short circuit current that was determined at the beginning of testing [1]. Standard Test Conditions (STC: 1000 W/m^2, 25°C, AM1.5) power could also be well estimated from the dark *I-V* curves obtained at *elevated* stress temperature with an offset proportional to the extent of PID [2]. The PID mechanism in c-Si modules largely manifests in fill-factor loss due to increasing junction recombination (2nd diode pre-exponential, J_{02}) and decreasing shunt resistance [1]. Other degradation mechanisms lead to differing effects on the PV module *I-V* curve, so for a universal method to obtain module power in-situ in an environmental chamber, the effects of the other diode parameters such as the 1st diode pre-exponential J_{01}, series resistance (R_s), and loss of photocurrent, must be also be handled.

Modules undergoing cell breakage may undergo J_{01} increases due to increased unpassivated surface area at fracture surfaces, R_s losses due to metallization breaks, J_{02} and junction ideality factor increases, and shunt resistance decreases due to increased physical defects penetrating the junction [3]. Additionally, some fraction of the cell circuit may be removed when the cell and its metallization become electrically disconnected [4]. To study these compound degradation modes, modules underwent mechanical loading followed by thermal and humidity-freeze cycles to impart mechanical damage, during which dark *I-V* curves and flash tests were obtained to formulate a method for determining power loss in-situ during chamber stress testing.

The approach taken in this work is to analyze the diode parameters in three steps: i) effects of shunting and J_{02} recombination losses are determined by using superposition of the dark I-V curves; ii) effects of R_s and J_{01} losses are initially estimated from changes in the dark *I-V* slope at high current; and iii), the STC power estimates obtained during the course of degradation are adjusted based on module flash testing at the end of the stress test to include effects of additional series resistance losses observed with illumination, J_{01} recombination losses, and current mismatch losses. This is achieved by matching the final dark *I-V* curve-determined P_{max} to the final flash-test-determined STC P_{max}, and adjusting the intermediate power loss estimates accordingly.

II. Experiment and Module Degradation Analysis

Four new conventional 60-cell multi-crystalline silicon (mc-Si) PV modules of the same design were subjected to five rounds of stress consisting of IEC 61215 static mechanical loading, thermal cycling (TC), or humidity freeze (HF) stress tests to various extents. The initial (new) state of the modules, along with the five subsequent stages of stress applied to the modules are designated with roman numerals (I-VI), as shown in Table 1.

Table 1. Description of the experiment stages

Stage	Description
I	Four new mc-Si modules characterized at STC
II	Static mechanical loading with 2400 Pa (IEC 61215)
III	29 cycles of TC and 4 cycles of HF (IEC 61215)
IV	18 cycles of HF (IEC 61215)
V	Static mechanical loading with 2400 Pa (IEC 61215)
VI	13 cycles of HF (IEC 61215)

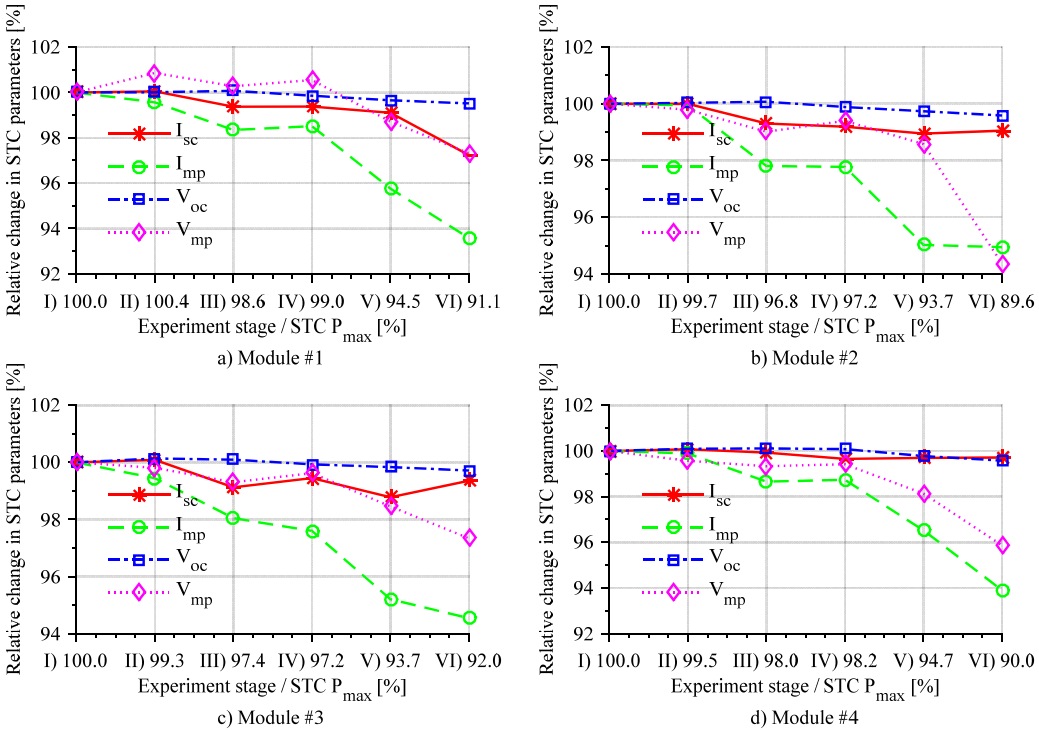

Fig. 1. Module STC P_{max} degradation and relative change in the STC parameters of the four modules during the six stages of the experiment. Stages II and V are mechanical loading; stages III, IV, and VI are IEC 61215 thermal and humidity freeze cycling of various extents.

After each stress-test stage, the modules were flash tested under STC and dark *I-V* characterized at 25°C. Fig. 1a, b, c, and d summarize the degradation of the modules STC P_{max}, STC short-circuit current (I_{sc}), open-circuit voltage (V_{oc}), maximum power point current (I_{mp}) and voltage (V_{mp}). From these plots, we can observe that I_{mp} current loss is the greatest factor associated with the power loss, which suggests current mismatch between the solar cells due to a decrease in photo-current generation by cell fracturing (confirmed by a general decrease in I_{sc}), as well as possible shunt-type losses [5]. In addition, the modules show V_{mp} voltage losses in the later stages of the experiment (V and VI). Because the V_{mp}/V_{oc} ratio decreases in these stages as well, we can deduce that these losses are caused (at least in part) by an increase in series resistance [5].

To further understand the modes of degradation associated with this type of stress, we analyze the electrical characteristics of the modules through the perspective of the solar cell diode model [6]. We fit the dark I-V curves (I_{dark}-V_{dark}) of the modules taken after each experiment stage to the two-diode model in [7] (1):

$$J = J_{01}\left\{\exp\left[\frac{q\left(V - JR_{s\_Model}\right)}{n_1 kT}\right] - 1\right\} + J_{02}\left\{\exp\left[\frac{q\left(V - JR_{sModel}\right)}{n_2 kT}\right] - 1\right\} + \frac{V - JR_{s\_Model}}{R_{sh}} \quad (1)$$

where J is the current density; V is the terminal voltage; n_1 and n_2 are the diode ideality factors; R_{s_Model} and R_{sh} are the area-specific series and shunt resistance parameters, respectively, of the solar cell; T is the cell temperature; k is the Boltzmann constant; and q is the elementary charge.

The effect of the module degradation on the solar cell model parameters is shown in Fig. 2. From these results, we can confirm a substantial increase in module series resistance (R_{s_Model}), which can be caused by corrosion [8] and metallization breaks [4]. Moreover, from Fig. 2 we can observe a significant increase in the n_2 and J_{02} diode model parameters, suggesting that solar cell junction degradation and recombination losses are occurring in the junction. Lastly, the n_1 and J_{01} diode model parameters increase, which is

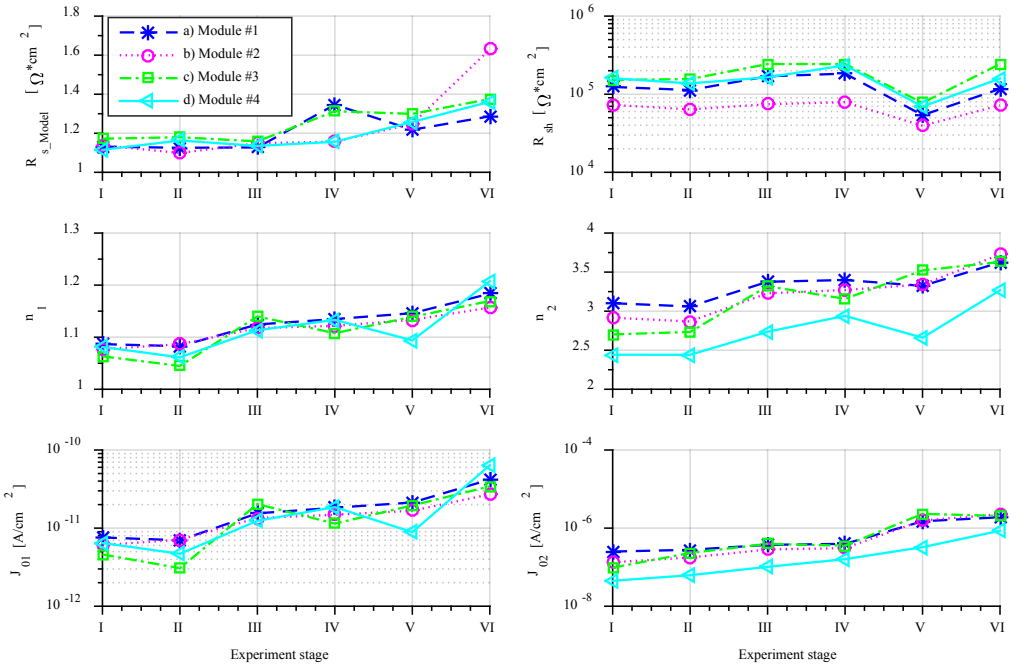

Fig. 2. Degradation of the two-diode model parameters determined by curve fitting module dark I-V measurements taken at 25°C after each experiment stage. Descriptions of experimental stages and power losses of modules (a-d) are given in the previous figure.

attributed here to increasing defects and unpassivated surfaces at the cell cracks.

In addition to these degradation modes, we must also consider the decrease in photocurrent generation when fractured cell areas are completely disconnected from the module's electrical circuit. In these cases, I_{sc} of the affected cells decreases, causing a drop in the I_{sc} of the entire module, as can be observed in the I_{sc} curves in Fig. 1.

III. In-Situ Power Loss Estimation Procedure

As was shown in the previous section, mc-Si PV modules undergoing compound thermal, mechanical, and humidity stress factors degrade by several modes. Their extent can be difficult to deconvolute from I-V measurements alone, due to the aggregated nature of the PV module, where the solar cells may degrade at different rates and by different modes. In this context, to monitor module degradation in-situ, we propose to analyze each dark I-V curve of the PV module undergoing degradation in three steps: i) shunting and J_{02} recombination losses, ii) series resistance losses, iii) other losses including J_{01} recombination losses, current mismatch losses, and a decrease in photo-current generation due to cell fracturing. We aim to estimate these failure modes' effect on module power loss separately.

The first stage, estimating the power loss due to shunting and J_{02} recombination losses, has been previously studied for crystalline silicon modules undergoing PID [1, 9]. In this case, module STC P_{max} degradation can be measured with high accuracy in-situ by superposition of the dark I-V curve with I_{sc} [1]. Some limitations of the method include modules that are severely shunted, for which the I_{sc} current starts to decrease significantly [10] and superposition using the initial I_{sc} is no longer valid.

Assuming that the dark I-V measurements are taken at 25°C, we can estimate the module STC P_{max}, accounting for the effects of shunting and J_{02} losses, by calculating the maximum power point $P_{max\_SUP}(t)$, after superposition of the dark I-V curve with I_{sc}, formulaically expressed as:

$$P_{max\_SUP}(t) = \max\left\{\left[I_{dark}(t) + I_{sc}(t_0)\right] V_{dark}(t)\right\} \quad (2)$$

where $I_{dark}(t)$-$V_{dark}(t)$ is the 25°C dark I-V curve measured at a time point t during the stress test, and $I_{sc}(t_0)$ is the initial STC I_{sc} current of the module measured on a flash tester. Note that solar cell fracturing can cause current mismatch and lead to a decrease in I_{sc}, which is compensated for in the last step of the power loss estimation procedure.

For estimation of the losses due to increases in module series resistance, we start from the empirical equations for calculating the effect of parasitic series resistance on the fill factor of solar cells [11], and rewrite them as in (3)-(4):

$$rs(R_{sx}, t) = \left[R_{sx}(t) - R_{sx}(t_0)\right] \frac{I_{mp}(t_0)}{V_{mp}(t_0)} \quad (3)$$

$$P_{max\_DIV}(R_{sx}, t) = P_{max\_SUP}(t)\left[1 - 1.1 rs(R_{sx}, t)\right] + \frac{rs(R_{sx}, t)^2}{5.4} V_{oc}(t_0) I_{sc}(t_0) \quad (4)$$

where R_{sx} is the measured series resistance of the PV module and rs is the normalized series resistance.

The P_{max_DIV} in (4) is determined from an initial (t_0) STC flash test on the module, and subsequent 25°C dark I-V measurements taken during the stress test, and will include

shunting, J_{02} recombination and R_s losses. One important issue here is the determination of the module's series resistance (R_{sx}) from dark I-V curves. This determination can be achieved by curve fitting the diode model parameters (R_{s_Model}) in (1), which requires careful parameterization of the initial conditions and does not lend itself to automatic analysis during the stress test. As an alternative solution, we propose the initial estimate for change in series resistance taken from the slope of the dark I-V curve at high current (R_{s_DIV}), as in (5), which is linearly related to the module's R_s, not including diode-internal voltage drops, which is handled subsequently [12].

$$R_{s\_DIV} = \left.\frac{dV_{dark}}{dI_{dark}}\right|_{I=\max(I_{dark})} \tag{5}$$

By substituting R_{sx} with R_{s_DIV} in (3) and (4), we can estimate the module STC P_{max} during the stress test. However, there are two limiting factors to this approach that must be considered. First, when measuring the dark I-V characteristic, the current paths through the module are more limited in area compared to the normal operation of the module when it is illuminated [13]. This situation leads to two different module R_s values, dark- and light-measured, where generally the dark-measured R_s will be smaller than the light-determined resistance. Consequently, use of the dark I-V curve-determined series resistance, such as R_{s_DIV}, will underestimate the STC P_{max} losses due to increases in R_s. Second, R_{s_DIV} does not explicitly include the effect of decreased current generation and mismatch due to cell fracturing or the increase in J_{01} recombination losses that can appear around max(I_{dark}) in the dark I-V curve and can lead to additional errors in estimating the STC P_{max}.

To address these two limiting factors we propose to adjust R_{s_DIV} such that the final P_{max} degradation, which is estimated from dark I-V measurements, matches the final STC P_{max} degradation that is measured on the flash tester. This problem can be formulated for solution as in (6), where t_0 and t_f are the initial and final 25°C dark I-V curve and STC power (P_{max_STC}) measurement points:

$$\frac{P_{max\_DIV}\left(R_{sx}, t_f\right)}{P_{max\_DIV}\left(R_{sx}, t_0\right)} = \frac{P_{max\_STC}\left(t_f\right)}{P_{max\_STC}\left(t_0\right)} \tag{6}$$

By numerically solving (6) for R_{sx}, we can determine an R_{sx}=$R_{s\_Match}(t_f)$ value, which will account for both the increase in module (light) R_s, as well as other losses, such J_{01} recombination and current mismatch losses due to cell fracturing, which occur in the module after the previous experiment stage. The R_{s_Match} is then used to adjust each intermediate $R_{s\_DIV}(t)$ with (7):

$$R_{s\_DIV\_Scaled}\left(t\right) = R_{s\_DIV}\left(t\right)\frac{R_{s\_Match}\left(t_f\right)}{R_{s\_DIV}\left(t_f\right)} \tag{7}$$

Finally $R_{s\_DIV\_Scaled}(t)$ is replaced in (3) and (4) to calculate $P_{max\_DIV\_Scaled}(t)$, which will match the final STC P_{max} degradation value and estimate the module degradation throughout the stress test more accurately.

IV. Results and Discussion

To validate the in-situ power loss estimation procedure, we first calculate P_{max_SUP} from (2), to determine the extent of power loss due to shunting and J_{02} losses. The relative change in P_{max_SUP} is shown in Fig. 3 (green) for the four modules during the six experiment stages, in comparison with the flash-tester-determined STC P_{max} degradation (red).

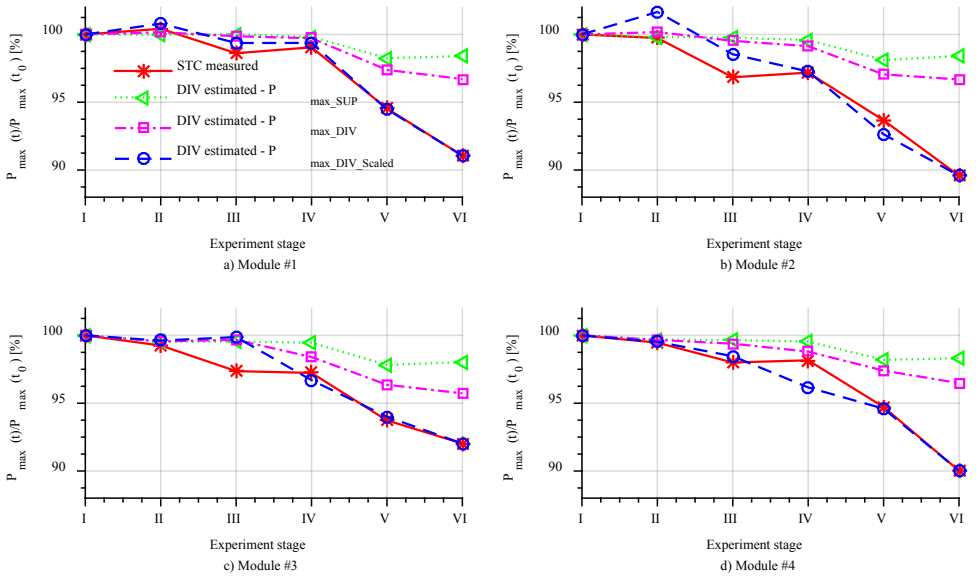

Fig. 3. Comparison of STC-measured P_{max} degradation (blue) vs. dark I-V curve (DIV)-estimated P_{max} degradation for the four modules under test (green shows P_{max_SUP} – only DIV superposition is used to estimate shunting and J_{02} losses; magenta shows P_{max_DIV} – series losses are estimated as well from the DIV curve; red shows $P_{max\_DIV\_Scaled}$ – other losses are estimated with a final STC power match).

Next, we determine the increase in R_{s_DIV} from 25°C dark I-V measurements and (5), and estimate the module P_{max} degradation, including series losses (P_{max_DIV}) from (3) and (4), shown in magenta in Fig. 3. Here we can observe that at ~5% STC P_{max} degradation (stage V), P_{max_DIV} underestimates the module degradation by ~3% (absolute error), whereas at ~10% module degradation (stage VI), the difference between the dark- vs. light-measured module power degradation can be as much as 6%-7% (absolute error). This is explained by the limited capability of R_{s_DIV} to characterize the light series resistance, as well as the impact of I_{sc} and J_{01} losses on the module STC power. Thus, monitoring only the module dark I-V curves, without final module flash testing and STC P_{max} correction, is useful only as an indicator of the module degradation during the stress test, and needs to be adjusted for accurate results.

The module power loss estimation must be improved by the final STC P_{max} adjustment, as in (6) and (7), which will compensate for most of the current mismatch, the decrease in I_{sc} and photocurrent-generation, and other losses such as J_{01} recombination losses, which are difficult to characterize from the dark I-V curve alone.

To exemplify the adjustment procedure, we used the initial and final STC flash test P_{max} to calculate the correction factor R_{s_Match} from (6), and use it to adjust the dark I-V-determined series resistance (R_{s_DIV}) as in (7), and calculate $P_{max\_DIV\_Scaled}$, shown in blue in Fig. 3. As can be observed, this approach leads to a more successful estimation of the module degradation, especially in the later stages of the experiment.

The errors between the $P_{max\_DIV\_Scaled}$ and STC P_{max} in the early stages of degradation result from the approximation that R_{s_DIV} scales linearly with the light series resistance in (6). Second, flash test and dark I-V measurement errors are compounded such that individual points in Fig. 3 may be affected. Despite these limitations, if we compare the root-mean-square error (RMSE) between the STC-measured P_{max}, and the dark I-V-estimated P_{max}, as in Table 2, we can observe the final adjustments of the series resistance based on flash testing, and reduce the total estimation error by 3-6 times.

Table 2. Comparison of RMSE between the STC-measured P_{max}, and the dark I-V-estimated P_{max} (P_{max_SUP} – only shunting and J_{02} losses are estimated; P_{max_DIV} – series losses are estimated as well; $P_{max\_DIV\_Scaled}$ – other losses are estimated with a final STC power match).

Module	*RMSE [%]*		
	P_{max_SUP}	P_{max_DIV}	$P_{max\_DIV\_Scaled}$
#1	3.42	2.65	0.37
#2	4.31	3.48	1.13
#3	3.22	2.13	1.06
#4	3.77	2.92	0.83

V. Summary and Conclusions

A method for determining module power loss in-situ in a dark environmental chamber was determined and demonstrated on four modules undergoing thermal cycling and mechanical loading stress testing. Two-diode model curve fitting was performed showing degradation of all the diode parameters. We proposed a universally applicable method for evaluating the power loss of crystalline silicon PV modules based on superposition, I-V curve slope at high current, and adjustments for 1st diode parameters made using the flash test I-V curve at the end of stress testing.

The power loss estimation method, if applied online during the stress test without final P_{max} adjustments, is useful only as an indicator of the module degradation dynamics during the stress test. However, after the experiment has been finalized, the in-situ power loss measurements are adjusted based on a final STC flash test, enabling more accurate estimates of the module STC P_{max} degradation during the stress test. These curves enable better statistics and can be used to develop module reliability and accelerated lifetime models for module degradation processes.

Acknowledgements

The authors thank Greg Perrin and Kent Terwilliger for their help performing the experiments, and Steve Rummel for module measurements. The work carried out at NREL was supported by the U.S. Department of Energy under Contract No. DE-AC36-08-GO28308 with the National Renewable Energy Laboratory.

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