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Modular Approach for Continuous Cell-level Balancing to Improve Performance of Large Battery Packs

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Abstract—Energy storage systems require battery cell balancing circuits to avoid divergence of cell state of charge (SOC). A modular approach based on distributed continuous cell-level control is presented that extends the balancing function to higher level pack performance objectives such as improving power capability and increasing pack lifetime. This is achieved by adding DC-DC converters in parallel with cells and using state estimation and control to autonomously bias individual cell SOC and SOC range, forcing healthier cells to be cycled deeper than weaker cells. The result is a pack with improved degradation characteristics and extended lifetime. The modular architecture and control concepts are developed and hardware results are demonstrated for a 91.2-Wh battery pack consisting of four series Li-ion battery cells and four dual active bridge (DAB) bypass DC-DC converters.

I. INTRODUCTION

Energy storage systems in both automotive and stationary applications require series and parallel connection of battery cells to meet voltage and power requirements. The series connection of cells creates an inherent sensitivity and limitation from mismatch of cell parameters such as capacity and series resistance. The cell mismatch is inherent in manufacturing and can range from 1% to 10% at beginning of life, depending on the quality of manufacturing and level of cell binning applied. Even more importantly, cells do not degrade evenly throughout life due to growth of the initial mismatch, temperature distribution, and other physical asymmetries across the battery pack. The result is parameter mismatch that can exceed 10% at end-of-life (EOL) for the pack [1]. The primary challenge is that the EOL is typically determined by the worst-case cell in a series connected string, and thus cell mismatch creates a significant reduction in the effective lifetime of a battery pack.

At a minimum, state-of-charge (SOC) balancing of cells must be performed periodically to avoid collapse of the available pack energy [2]. This is due in part to the set terminal voltage limits that cells are operated within, resulting in a divergence of cell SOC with repeated charge/discharge cycles. Commercial battery packs all include some form of battery cell balancing for this purpose. The most common solution is through passive balancing,

where a sequential process is performed during charging to passively dissipate the excess energy of cells that reach the maximum voltage limit first [2, 3]. This meets the basic requirement with a simple hardware structure. However, the approach still results in a pack that is energy and power limited by worst case cells throughout life and most importantly at EOL. The approach also requires wiring harnesses with bundles of wires to pass sensing of all cell voltages and temperature and passive switch control networks to a central controller [2].

Active balancing is another technique that matches cell SOC through charge redistribution among cells within the pack rather than dissipating the energy of higher SOC cells passively [3]. The clear advantages are reduced energy loss and heat dissipation. Many approaches have been demonstrated using DC-DC converters in parallel with battery cells to transfer the mismatch or differential energy through a high voltage bus [3] or shuttle energy from cell to neighboring cell using inductive, capacitive, or combined

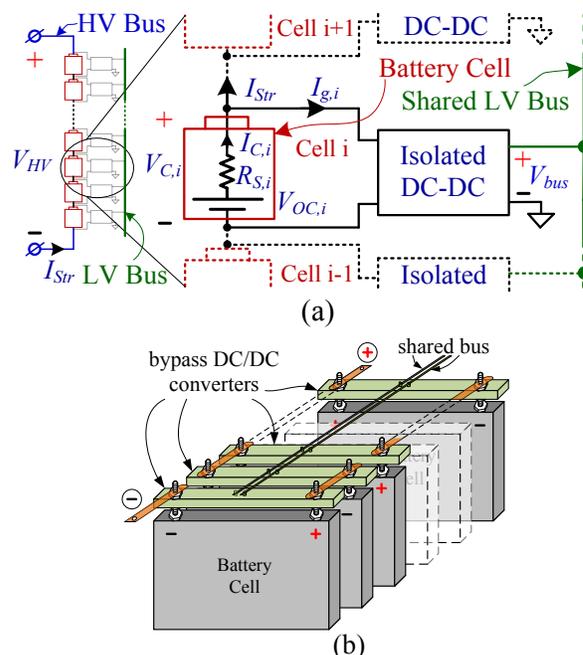


Fig. 1: (a) Schematic of the modular system architecture and (b) conceptual diagram of system implementation.

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passively [3]. The clear advantages are reduced energy loss and heat dissipation. Many approaches have been demonstrated using DC-DC converters in parallel with battery cells to transfer the mismatch or differential energy through a high voltage bus [3] or shuttle energy from cell to neighboring cell using inductive, capacitive, or combined switching [4-7]. Another approach is to use DC-DC converters cascaded with battery cells to provide full flexibility of battery processing at the cost of processing full cell power with each DC-DC [8]. The control objectives of active balancing are typically the same as for passive balancing, and commercial acceptance has been slow due to the added cost.

This paper presents an opportunity and approach to expand the benefit matrix and reduce the relative cost of active balancing systems. The approach is based on combining a modular hardware architecture [10] with distributed, continuous cell-level state estimation and control, as shown in Fig. 1. The benefit is a fully modular battery system that can be expanded to any size pack with no additional sensing, control wires or communications requirements and that self-adjusts loading of individual cells to achieve high level objectives such as maximizing energy, power capability and pack lifetime. This is accomplished by autonomously biasing individual cell SOC and SOC range such that stronger cells are cycled deeper than weaker cells. This leads to pack performance that is not limited by the weakest cells and to cell mismatch that converges over lifetime to reach a more homogeneous EOL.

The proposed modular architecture with distributed control is introduced in Section II. Details of local cell-level state estimation and lifetime prediction algorithms are given in Section III. System control objectives to improve pack performance are presented in Section IV. Bypass converter design and control details are covered in Section V. Hardware results showing balancing of a 91.2-Wh battery pack with four series Li-ion cells combined with the modular DC-DC architecture are provided in Section VI.

II. MODULAR SYSTEM ARCHITECTURE

The modular system architecture is shown in Fig. 1(a). The system includes series connected battery cells or modules, isolated DC-DC converters, and a shared low voltage (LV) bus. The battery cells are connected directly in series to the high voltage (HV) pack bus such that the high pack current is drawn directly from the cells in the series string. The isolated DC-DC converters are connected on the primary side in parallel with each battery cell and on the secondary side to the shared LV bus, as shown previously for photovoltaic (PV) application [9] cell voltage balancing [10]. The purpose of the converters is to process only a small percentage of cell mismatch power necessary to continuously enforce the offset curves in the individual cell SOC as defined in the system control objectives, e.g., for maximum power capability and pack lifetime. A key aspect of the topology and distributed control is the multi-purpose use of the isolated LV bus. (1) It provides the active balancing path to redistribute charge among cells. (2) The analog bus

voltage is used as the common reference point for all DC-DC converters and is the primary communication between converters. The converters are allowed to operate autonomously to force their objective to match the shared bus voltage. In doing so, they transfer energy from the battery cell at their input port to the shared bus at the output port, where charge is integrated to the shared bus capacitance such that the modules naturally maintain a shared reference. In a simple scenario, the objective could be the cell SOC, in which case all cells would be driven to match SOC and the shared bus voltage would be proportional to SOC. Additional control objectives and their impact on performance are detailed in Section IV. (3) The LV bus can be used as a convenient LV supply for auxiliary loads such as the 12-V load network in an electric vehicle (EV) [10]. The approach can be realized using a very simple structure, as shown in Fig. 1(b), with no requirement for wiring harnesses or high speed digital communication with a central controller. The architecture has cost advantages through the simplicity of the modular connection, removing system components such as the HV-to-LV auxiliary load DC-DC converter and central controller, and system level benefits such as increased pack power capability and extended pack lifetime. The latter benefits require the control objective to include continuous cell state estimation and life prognostic-based controls to impact cell degradation. These points are addressed in the next two sections.

III. BATTERY STATE AND LIFETIME ESTIMATION ALGORITHMS

A. SOC estimation

A number of SOC estimation methodologies are available, including coulomb counting or open-circuit-voltage V_{OC} lookup tables [11]. These approaches have limitations for continuous operation due to drifting from error integration or the requirement of no load to measure V_{OC} . Model-based approaches using a nonlinear Kalman filter provide robust SOC estimates based on data from continuous operation. Examples include the extended Kalman filter (EKF) [12] or the sigma-point Kalman filter (SPKF), which is a superset of algorithms that includes the unscented Kalman filter (UKF) [13].

Model-based estimators require a mathematical description of the system whose state is being estimated. For battery cells, (reduced-order) electrochemical models [14, 15] or equivalent-circuit models (ECM) [12, 13] could be used. For estimation of SOC as required in this work, equivalent-circuit models such as drawn in Fig. 2 are sufficient. The cell is described as having an open-circuit-voltage V_{OC} , which is a function of SOC $z(t)$, a hysteresis component, one or more resistor-capacitor networks modeling mass diffusion, and a series resistance R_θ . Nonlinear Kalman filters use this model in a predict-correct scheme: first, the internal state and output voltage are predicted using *a priori* measurements, then corrected using posteriori measurements, repeating this cycle indefinitely. Similar techniques can be used in parallel to update estimates of the model parameters, such as the series resistance [16].

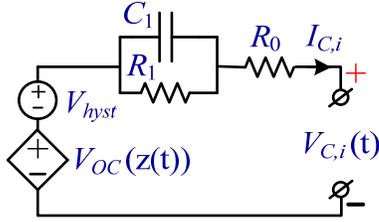


Fig. 2: Battery equivalent circuit.

To use the given approach to estimate a cell's state, we must have a "state-space" model of its dynamics:

$$\mathbf{x}_{k+1} = f(\mathbf{x}_k, \mathbf{u}_k, \mathbf{w}_k) \quad (1)$$

$$y_k = h(\mathbf{x}_k, \mathbf{u}_k, \mathbf{v}_k) \quad (2)$$

where \mathbf{x}_k is the n -component state vector at discrete-time index k , \mathbf{u}_k is the measured system input vector at time k , (perhaps including battery-pack current, temperature, etc.) and \mathbf{w}_k is unmeasured "process noise" (modeling inaccuracy of the cell model). The system output is y_k , and \mathbf{v}_k models sensor noise. The stochastic inputs \mathbf{w}_k and \mathbf{v}_k are assumed to be zero-mean white Gaussian random processes with covariance matrices Σ_w and Σ_v , respectively. Equation (1) is called the "state equation," (2) is called the "output equation," and $f(\cdot)$ and $h(\cdot)$ are (possibly nonlinear) functions, specified by the particular cell model used.

To be more specific, the system input vector equals the instantaneous cell current i_k . The system output is the cell's loaded terminal voltage. The system's state vector \mathbf{x}_k in some way represents in summary form the total effect of all past input to the system so that the present output may be predicted solely as a function of the state and present input. Values of past inputs are not required. Our method constrains the state vector to include SOC as one component, so that SOC may later be estimated using some form of Kalman filter. In particular, a sigma-point Kalman filter repeatedly executes the following steps.

SPKF step 1: State estimate time update

At each measurement interval, the time update is computed by first forming the augmented *a posteriori* state estimate vector for the previous time interval

$$\hat{\mathbf{x}}_{k-1}^{a,+} = \begin{bmatrix} (\hat{\mathbf{x}}_{k-1}^+)^T, 0, 0 \end{bmatrix}^T \quad (3)$$

and the augmented *a posteriori* covariance estimate

$$\Sigma_{\hat{\mathbf{x}},k-1}^{a,+} = \text{diag}(\Sigma_{\hat{\mathbf{x}},k-1}^+, \Sigma_w, \Sigma_v). \quad (4)$$

These are used to generate the $p+1 = 2n+1$ sigma points

$$\mathbf{X}_{k-1}^{a,+} = \left\{ \hat{\mathbf{x}}_{k-1}^{a,+}, \hat{\mathbf{x}}_{k-1}^{a,+} + \gamma \sqrt{\Sigma_{\hat{\mathbf{x}},k-1}^{a,+}}, \hat{\mathbf{x}}_{k-1}^{a,+} - \gamma \sqrt{\Sigma_{\hat{\mathbf{x}},k-1}^{a,+}} \right\} \quad (5)$$

From the augmented set, $p+1$ vectors comprising the state portion $\mathbf{X}_{k-1}^{x,+}$ and $p+1$ vectors comprising the process-noise portion $\mathbf{X}_{k-1}^{w,+}$ are extracted. The state equation is evaluated using all pairs of $\mathbf{X}_{k-1,i}^{x,+}$ and $\mathbf{X}_{k-1,i}^{w,+}$, yielding the *a priori* sigma points

$$\mathbf{X}_{k,i}^{x,-} = f(\mathbf{X}_{k-1,i}^{x,+}, \mathbf{u}_{k-1}, \mathbf{X}_{k-1,i}^{w,+}). \quad (6)$$

Finally, the *a priori* state estimate is computed as

$$\hat{\mathbf{x}}_k^- = \sum_{i=0}^p \alpha_i^{(m)} \mathbf{X}_{k,i}^{x,-} \quad (7)$$

SPKF step 2: Error covariance time update

Using the *a priori* sigma points from step 1, the *a priori* covariance estimate is computed as

$$\Sigma_{\hat{\mathbf{x}},k}^- = \sum_{i=0}^p \alpha_i^{(c)} (\mathbf{X}_{k,i}^{x,-} - \hat{\mathbf{x}}_k^-) (\mathbf{X}_{k,i}^{x,-} - \hat{\mathbf{x}}_k^-)^T \quad (8)$$

SPKF step 3: Estimate system output

The system output is estimated by evaluating the model output equation using the sigma points describing the spread in the state and noise vectors. First, we compute the points

$$\mathbf{Y}_{k,i} = h(\mathbf{X}_{k,i}^{x,-}, \mathbf{u}_k, \mathbf{X}_{k-1,i}^{w,+}, k) \quad (9)$$

The output estimate is then

$$\hat{y}_k = \sum_{i=0}^p \alpha_i^{(m)} \mathbf{Y}_{k,i} \quad (10)$$

SPKF step 4: Estimator gain matrix

To compute the estimator gain matrix, we must first compute the required covariance matrices.

$$\Sigma_{\hat{\mathbf{y}},k} = \sum_{i=0}^p \alpha_i^{(c)} (\mathbf{Y}_{k,i} - \hat{y}_k) (\mathbf{Y}_{k,i} - \hat{y}_k)^T \quad (11)$$

$$\Sigma_{\hat{\mathbf{y}},k}^- = \sum_{i=0}^p \alpha_i^{(c)} (\mathbf{X}_{k,i}^{x,-} - \hat{\mathbf{x}}_k^-) (\mathbf{Y}_{k,i} - \hat{y}_k)^T \quad (12)$$

Then, we simply compute $L_k = \Sigma_{\hat{\mathbf{y}},k}^- \Sigma_{\hat{\mathbf{y}},k}^{-1}$.

SPKF step 5: Error covariance measurement update

The final step is calculated directly from the optimal formulation:

$$\Sigma_{\hat{\mathbf{x}},k}^+ = \Sigma_{\hat{\mathbf{x}},k}^- - L_k \Sigma_{\hat{\mathbf{y}},k} L_k^T \quad (13)$$

Parameter values γ , $\alpha_0^{(m)}$, $\alpha_k^{(m)}$, $\alpha_0^{(c)}$, and $\alpha_k^{(c)}$ were chosen to fit a CDKF-style SPKF [13].

B. Lifetime prognostics

The battery life prognostic model from [17] is used to estimate the impacts of the balancing hardware and various control strategies on battery lifetime. Under storage conditions, the dominant fade mechanism is growth of a resistive film layer at the electrode surface. The resistive layer also consumes cycleable lithium from the system, reducing capacity. In the present model, resistance growth and lithium capacity loss are assumed to be proportional to the square-root of time, $t^{1/2}$, typical of diffusion-limited film growth. Under cycling-intense conditions, degradation is mainly caused by structural degradation of the electrode active sites, proportional to the number of cycles, N .

Cell resistance growth due to calendar- and cycling-driven mechanisms is assumed to be additive

$$R = a_0 + a_1 t^{1/2} + a_2 N. \quad (14)$$

Cell capacity is assumed to be controlled by either loss of cycleable Li or loss of active sites

$$Q = \min(Q_{Li}, Q_{sites}), \quad (15)$$

where

$$Q_{Li} = b_0 + b_1 t^{1/2}, \quad (16)$$

$$Q_{sites} = c_0 + c_1 N. \quad (17)$$

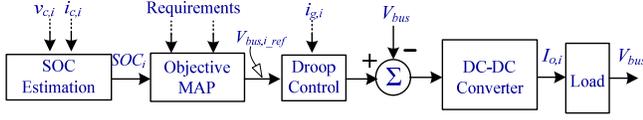


Fig. 3: Block diagram of cell balancing algorithm.

Models (14), (16), and (17) are readily fit to a resistance or capacity trajectory measured for one storage or cycling condition. With multiple storage- and cycling-condition datasets, functional dependence is built for rate constants $a_1(T, V_{OC}, \Delta DOD)$, $a_2(T, V_{OC}, \Delta DOD)$, $b_1(T, V_{OC}, \Delta DOD)$, and $c_1(T, V_{OC}, \Delta DOD)$ as described in [17]. The model (14-17) is then reformulated in state-based form to accommodate variable degradation rates. This final reformulated model thus predicts cell resistance and capacity changes with time dependent upon time-varying cell temperature, T , open-circuit voltage and charge/discharge cycling.

IV. CONTROL OBJECTIVE FOR ENERGY/POWER/LIFETIME OPTIMIZATION

The control objectives and algorithms embedded in each module can be used to bias individual cell states and impact pack performance. A diagram for the controller that is embedded in each module is shown in Fig. 3. Each module i measures the cell terminal voltage and current, $v_{c,i}$ and $i_{c,i}$ and the shared LV bus voltage, V_{bus} . The module controller then computes the estimated cell SOC, SOC_i , which is translated to a reference bus voltage, V_{bus,i_ref} , using an objective map. The reference and measured bus voltage are compared and an error signal is passed to the DC-DC converter to regulate the converter output. The SOC estimation is as described in Section III-A and the DC-DC feedback controller is a standard regulator. The question of interest is the objective map that determines the individual bus voltage reference based on the cell's SOC.

As stated earlier, this map could simply be one-to-one, which gives reference bus voltage V_{bus,i_ref} the physical meaning of the SOC for all cells (and thus proportional to the pack energy content). This control would result in continuous SOC balancing of all cells. The DC-DC converters would naturally process the mismatch power among cells with different capacity to enforce the reference bus voltage and V_{bus} to track the SOC of the pack.

As an example of a more advanced objective, consider a pack with a maximum string current requirement $\pm I_{max}$ and set voltage limits for each cell terminal voltage, V_{max} and V_{min} . If the continuous SOC balancing objective above is applied, then the SOC range for all cells must be limited to avoid exceeding V_{max} with worst case charge current at the upper end and V_{min} for worst case discharge current at the lower end, as shown in Fig. 4(a). An alternative, power optimized objective, is to offset each cell SOC_i according to its own series resistance such that each cell i maximizes its SOC range and is not limited by the worst case cell resistance, as shown in Fig. 4(b). For the same power capability, this objective achieves higher pack energy when compared to Fig. 4(a). In addition, the objective naturally

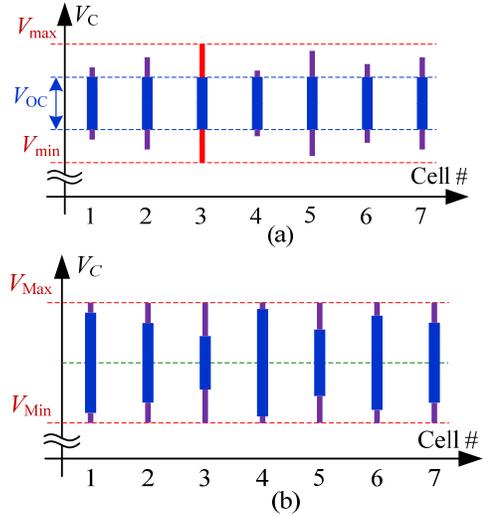


Fig. 4: Full range of battery terminal voltages with max current. Blue thick bars – Open-circuit cell voltage range; Violet & red thin bars – voltage drop due to series resistance. (a) SOC balancing with power limit, (b) power optimized balancing.

forces cells with lower series resistance to operate with a wider SOC range. This behavior, when combined with life-prognostic models [17], can be shown to force convergence of cell mismatch and leads to a more homogeneous EOL and thus a longer lifetime for the battery pack.

The power optimized objective can be realized with the architecture of Fig. 1 through an appropriate objective map and associated meaning of the shared bus. By considering Fig. 4(b), and simplifying the ECM of Fig. 2 to include only a total series cell resistance R_s , the max and min cell terminal voltages for each cell i are given by

$$\begin{aligned} V_{max} &= V_{OC,i_max} + R_{s,i} \cdot |I_{max}|, \\ V_{min} &= V_{OC,i_min} - R_{s,i} \cdot |I_{max}|, \end{aligned} \quad (18)$$

where $V_{OC,i}$ max and min are the cell open-circuit voltage limits that must be achieved within the cell model. Selection of the shared bus voltage range can be performed arbitrarily, although careful selection can give useful physical meaning. Here we match the range to the maximum cell terminal limits, V_{max} and V_{min} . Thus the individual cell limits on $V_{OC,i}$ can be mapped directly from $V_{OC,i}$ using a linear fit between the limits of (18) and the full range of V_{bus} as shown in Fig. 5. The resulting objective map equation is given by

$$V_{bus,i_ref} = \frac{V_{max}(V_{OC,i} - R_{s,i}|I_{max}|) - V_{min}(V_{OC,i} + R_{s,i}|I_{max}|)}{V_{max} - V_{min} - 2R_{s,i}|I_{max}|} \quad (19)$$

In the controller of Fig. 3, the SOC estimate, SOC_i , is mapped to the estimated open-circuit voltage $V_{OC,i}$. The shared bus voltage reference inherits the physical meaning of V_{OC} in case of SOC balancing and the average V_{OC} scaled by the nominal R_s and I_{max} as shown in Fig. 4(b).

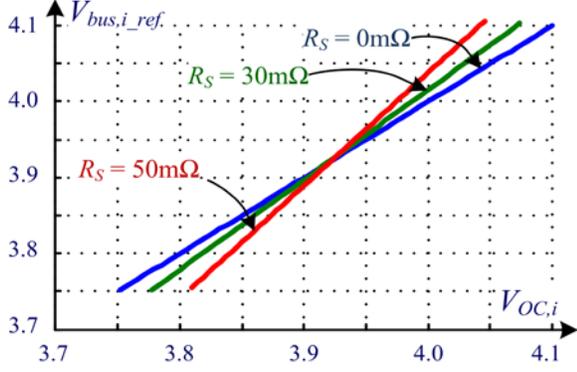


Fig. 5: Objective map for the reference battery open circuit voltage as a function of the shared bus voltage and series resistance in order to comply with power optimized balancing objective.

Due to parallel operation of bypass DC-DC converters in voltage-mode, droop control is utilized to share the load current between converters [18]. The droop control algorithm is the same for each converter, with the reference bus voltage updated as

$$V_{bus,i_ref,droop}(t) = V_{bus,i_ref}(t) - i_{g,i} R_{droop}, \quad (20)$$

where R_{droop} is droop control resistance, i_g is converter input current, and $V_{bus,i_ref}(t)$ is the reference bus voltage computed by an objective map at a given time instant.

V. BYPASS CONVERTER CONTROLLER DESIGN

The bypass converter modules of Fig. 1 can be implemented using any isolated DC-DC configuration. As an example, the system is implemented using isolated dual active bridge (DAB) converters [10]. The closed-loop converter schematic of the DAB converter under phase-shift modulation control are given in Fig. 6, where T_s is the converter switching period and t_ϕ is the phase shift, both with units in seconds. The controller uses values for reference and output voltages to generate an error signal, defined in the Laplace domain as

$$v_e(s) = H(s) (v_{bus,i_ref}(s) - v_{bus}(s)) \quad (21)$$

where $H(s)$ is the sensing gain. The error signal is then fed through compensator $G_c(s)$ to produce a control signal t_ϕ that adjusts the phase-shift of the transistor gate modulation signals.

In order to proceed with the control design of the DAB for the proposed system, the small-signal, averaged control-to-output transfer function, $G_{vo,\phi}$, is needed. In the lossless case, when switching transitions are neglected, this will be [10],

$$G_{vo,\phi} = \frac{\hat{v}_{out}}{\hat{t}_\phi} = \frac{K_{i\phi} Z_o \left(\frac{1}{n_t} + K_{iv} Z_i \right)}{1 - K_{iv}^2 Z_i Z_o} \quad (22)$$

where n_t is the transformer turns ratio, $K_{i\phi}$ and K_{iv} are scalar gains evaluated at the steady-state operating point,

$$K_{i\phi} = \frac{V_{out}}{n_t L_l T_s} (T_s - 4T_\phi) \quad (23)$$

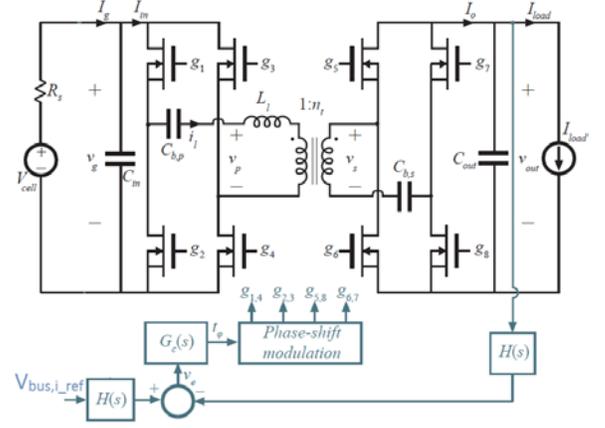


Fig. 6: Dual active bridge topology used as an isolation DC-DC converter for active balancing.

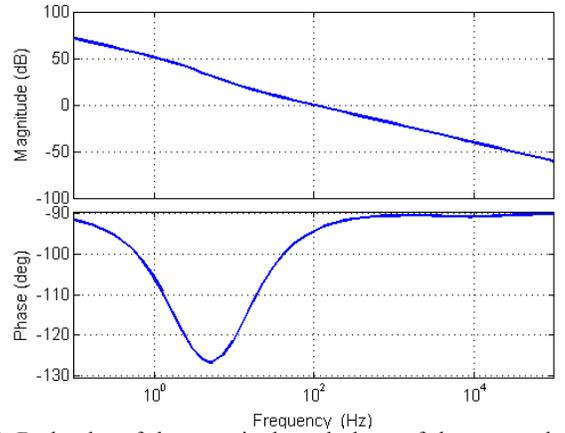


Fig. 7: Bode plot of the magnitude and phase of the system loop gain, $T(s)$, with the proposed PI compensator.

$$K_{iv} = \frac{1}{n_t L_l T_s} (T_s T_\phi - 2T_\phi^2). \quad (24)$$

The input impedance seen by the converter at the port defined by the voltage v_g is

$$Z_i = R_s || C_{in} = \frac{R_s}{1 + sR_s C_{in}}, \quad (25)$$

where R_s is the series impedance between the battery and input port, and includes cell internal resistance, connection, and wiring resistances. Similarly, the impedance seen at the output of the converter is

$$Z_o = R_{out} || C_{out} = \frac{R_{out}}{1 + sR_{out} C_{out}}, \quad (26)$$

where R_{out} is the low frequency output resistance of the converter itself, which is determined primarily by losses and ZVS transitions in the converter, both of which are neglected in this analysis [20].

The system is compensated with a standard PI compensator of the form

$$G_c = G_\infty \left(1 + \frac{\omega_z}{s} \right), \quad (27)$$

resulting system loop gain is given by

$$T(s) = G_{vo,\phi} G_c. \quad (28)$$

The compensator gain G_∞ is selected to place the crossover frequency of the system at 100 Hz with ω_z placed a decade below. For the system parameters given in Section VI, a bode plot of the resulting loop gain is plotted in Fig. 7. Analytical predictions indicate a phase margin of 85° . The compensator achieves zero steady-state error in regulating the converter output voltage to match the reference bus voltage, thus maintaining a shared bus reference and tracking the open-circuit voltage as given by the objective map. It should be noted that $V_{bus,i\ ref}$ varies as the cell V_{OC} changes but cell dynamics are much slower than converter dynamics, thus a well-compensated converter should be able to handle such change.

VI. EXPERIMENTAL RESULTS

An evaluation system consisting of four Li-ion battery cells and four DAB DC-DC bypass converters has been constructed. The converter parameters are given in Table I. Each DAB DC-DC bypass converter is rated for input currents up to $i_g = 10$ A, resulting in an output power rating of approximately 40 W. The DAB transformer turns ratio n_t is selected to match the desired ratio from battery voltage to nominal bus voltage. Waveforms are shown in Fig. 8 for operation at 250 kHz, 3.5-to-12 V, 12 W and 0 W output power. The converter achieves 91% power stage efficiency at the 12 W output power operating point.

Converter control and modulation is implemented on a Texas Instruments Piccolo DSP. The proposed controller is implemented by discretizing the continuous time PI compensator of (27) using the Tustin approximation with frequency prewarping centered on $f_c = 100$ Hz. The SPKF based SOC estimation methodology was implemented in a MATLAB script running on a PC. Each converter module communicates cell voltage and current with the PC every 1 second over RS485 communication protocol and the SOC estimates for each cell are sent back. The droop resistance was chosen to be 20 m Ω .

To verify proposed control strategies, four prototype converters are connected in series-input, parallel-output fashion as shown in Fig. 1(a). Each converter has a 6 Ah Li-ion cell at its input. The series battery string is connected to a constant current power supply and a constant current electronic load that provide charging and discharging to the full string. The parallel outputs of the converters are connected to the shared bus, V_{bus} , and for simplicity no load but converter output impedance of (26) is assumed to be present. Cell parameter mismatch is intentionally magnified to verify the difference between control strategies. The cell series resistance, R_s , is augmented by connecting wires of different length and diameter; resulting R_s values are {41, 29, 31, 25} m Ω for cell A to D respectively. The max and min cell terminal voltages are set to be $V_{max} = 4.11$ V and $V_{min} = 3.72$ V. The maximum battery string current is set to be $I_{max} = 2$ A.

TABLE I
PROTOTYPE DAB PARAMETERS

L_l [nH]	n_t	C_{out} [μ F]	C_{in} [μ F]	$C_{b,p}$ [μ F]	$C_{b,s}$ [μ F]	R_s [m Ω]	R_{out} [Ω]	f_s [kHz]
250	3.34	286	429	80	80	40	50	250

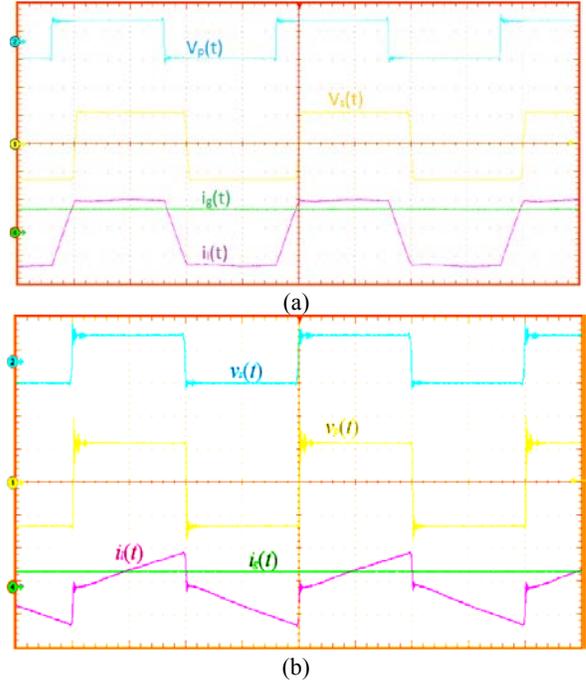


Fig. 8: Experimental operating waveforms of DAB converter corresponding to schematic given in Fig. 6 for (a) 12 W and (b) 0 W load power. Ch1: transformer primary voltage (10 V/div), Ch2: transformer secondary voltage (5 V/div), Ch3: primary side transformer current (4 A/div (a), 500 mA (b)), Ch4: converter input current (4 A/div (a), 500 mA (b)), time (1 μ s/div).

A. Balancing strategies

To demonstrate SOC and power optimized balancing, four battery cells were discharged and charged over the range of 35% to 65% SOC. Battery string current I_{string} is set to 2 A and -2 A for discharging and charging respectively. Fig. 9 shows a charging cycle for power optimized balancing. In power optimized balancing tests each converter biases its cell SOC according to the series resistance R_s (as shown in Fig. 10). As a result of biased cell SOCs, the cell terminal voltage is observed to be approximately equal at end point. In case of SOC balancing, bypass converters process the mismatch power among cells with different capacity and keep cell SOCs matched within an error band of 0.6%. It can be seen in Fig. 11 that as the battery pack discharges, the worst-case cell reaches the minimum cell terminal voltage before other cells.

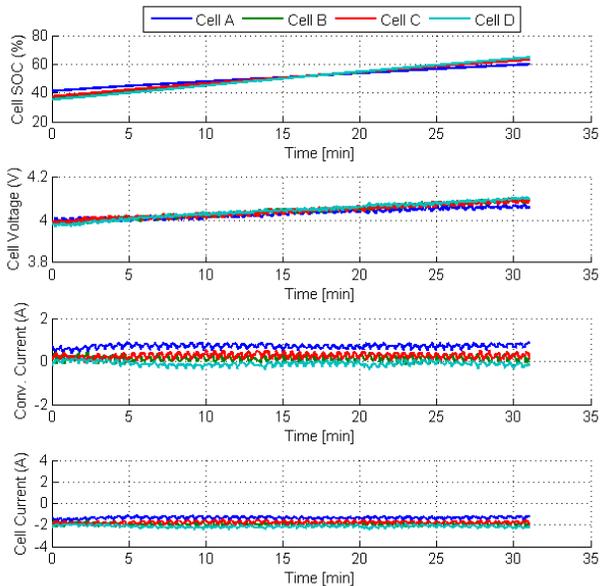


Fig. 9: Experimental charge data for a battery string with four cells and DAB converters as connected in Fig. 1. Battery cells are charged from 35% to 65% SOC with $I_{string} = -2$ A and control objective set to power optimized balancing. Results are shown for cell SOC, cell voltage, cell and converter current. R_s values are {41, 29, 31, 25} m Ω for cell A to D respectively.

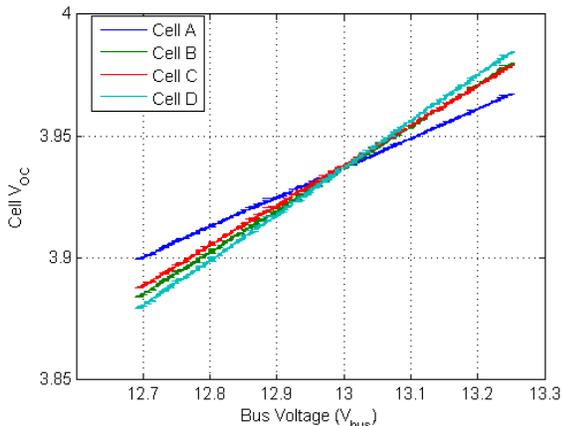


Fig. 10: Experimental charge data for the power optimized balancing test given in Fig. 13 respectively. Results show that using the shared bus reference each converter biases its cell V_{OC} according to the series resistance. R_s values are {41, 29, 31, 25} m Ω for cell A to D respectively.

B. Life prognostic simulation

As an initial analysis of lifetime benefits for automotive application, the balancing hardware and controls are implemented in NREL’s BLAST-V model (Battery Lifetime Analysis and Simulation Tool for Vehicles) for simulation of electric-drive vehicle lifetime and operating cost. Simulations presented here are for a plug-in hybrid electric vehicle with 20 mile electric range (PHEV20) operating in a Los Angeles, California climate. Drive cycles are taken from multi-day real-world datasets, for a vehicle with annual mileage of 10,000 miles/year [19].

Fig. 12 explores the impact of several power-optimized balancing strategies on cell lifetime compared to a baseline system without active balancing. Cells in the 84-cell pack are initialized at the beginning of life with $\pm 2\%$ capacity and $\pm 5\%$ resistance imbalance. Cell imbalance grows throughout life due to two factors: (1) temperature differences across cells in the pack and (2) aging process variation due to cells with slight manufacturing differences. The latter factor is simulated by applying random variation of the life model parameters for the 84 cells within $\pm 10\%$ bounds. These two factors provide reasonable levels of cell imbalance growth compared to actual observations.

In the baseline system, the pack capacity is limited by the worst cell in the pack (dashed black line). With power optimized balancing implemented during both charging and discharging of the pack, pack capacity is limited by the average of all cells’ capacities (solid magenta line), a factor that greatly extends life. For example, it takes just 5.6 years for the baseline pack to degrade to 80% remaining capacity. With power-optimized balancing implemented during both charge and discharge, it takes 6.8 years for the pack to degrade to 80% capacity, a 21% improvement in life. With power-optimized balancing implemented during discharge only, the life of the average cell further improves, however the life of the worst cell stays nearly the same. This is due to the healthy cells spending their lifetime with a lower SOC, due to a lower end-of-charge SOC for the highest capacity cells. Without balancing during charge however, the system is unable to take advantage of extra capacity in the healthy cells. Such a strategy slightly reduces available cell capacity, reducing all-electric miles achieved by the PHEV20 by some 200 of 10,000 miles in year 10. In future work, we intend to explore the impact of various control strategies on lifetime and quantify tradeoffs with performance. Preliminary results suggest that balancing control strategies have small influence on cell temperature, but larger influence on cell SOC and V_{OC} history. Controlling healthy cells to a slightly lower end of charge SOC benefits those cells and has positive impact on battery pack life.

VII. CONCLUSIONS

The function of series cell balancing circuits in large battery packs can be expanded to provide system performance improvements such as improved power capability and increased pack lifetime. The modular architecture presented extends the balancing function to higher level pack performance objectives by adding bypass DC-DC converters in parallel with cells and using state estimation and control to autonomously bias individual cell SOC and SOC range, forcing healthier cells to be cycled deeper than weaker cells. The result is a pack with improved degradation characteristics and extended lifetime. Keys to cost-effectiveness of the approach are processing only the small mismatch power between battery cells, the simplicity of the modular structure with a single isolated shared bus with no additional communications, and the ability to supply LV loads from the shared bus.

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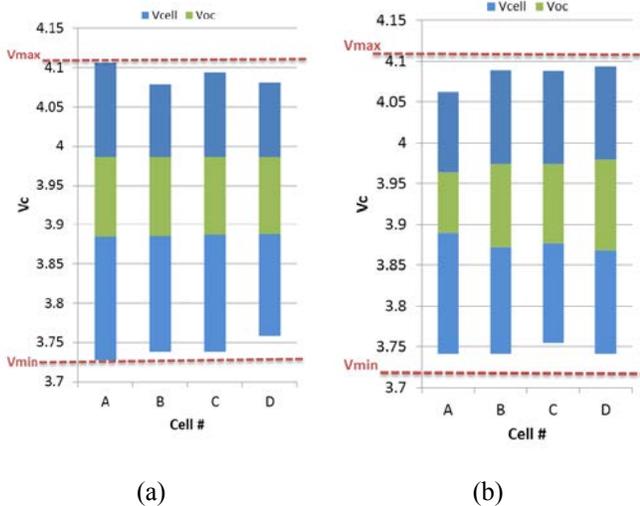


Fig. 11: Experimental charge and discharge data for SOC balancing (a) and power optimized balancing (b) tests. Results show that in case of SOC balancing each cell is limited by the worst-case cell. While in case of power optimized balancing healthier cells span a wider V_{OC} range and terminal voltage of all cells is approximately equal. R_s values are {41, 29, 31, 25} m Ω for cell A to D respectively.

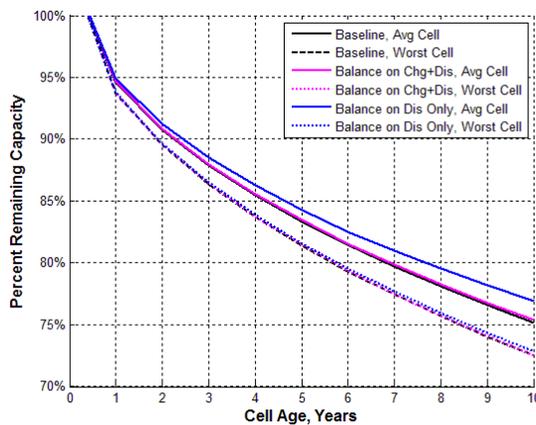


Fig. 12: Simulated lifetime of cells in 84-cell PHEV20 pack for vehicle with 10,000 annual miles. Cells are initialized with $\pm 2\%$ capacity imbalance at beginning of life.

Details are provided on the modular architecture, advanced balancing control concepts, and state and lifetime estimation. Hardware results are demonstrated with balancing of four series 6 Ah li-ion battery cells using four DAB bypass converters. Results show successful battery balancing, advanced cell-level control, and life improvement by up to 21% by enabling the system to access the extra energy in healthy cells compared to passive- or no-balancing systems in which the pack capacity is limited by the lowest capacity cell in the pack. A comparison of control strategies – utilizing balancing on both charge and discharge versus discharge-only – shows tradeoffs in lifetime and performance, to be investigated in future work.